Product Line In Vehicle Networking (PL IVN): HS-CAN transceiver datasheet update to support CAN FD up to 5 Mbit/s

Attachment to Customer Information Notification (CIN) 201605003I

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Date: June 9th 2016

1. Introduction

The third generation of NXP's PL IVN HS-CAN transceivers will receive a datasheet update, to support the new CAN FD requirements up to 5 Mbit/s.

The following products are receiving this update:

- Basic HS-CAN : TJx1051-series, TJA1057 series.
- Standby HS-CAN : TJA1042-series, TJA1044-series, TJA1049-series.
- Sleep mode HS-CAN : TJA1043-series
- Dual CAN : TJA1046TK, TJA1048-series, TJA1059TK.
- Isolated CAN : TJx1052i series,
- HS-CAN with partial networking : TJA1145 (up to 2 Mbit/s)

In addition to this, the following changes have been made to the datasheets:

- Addition of parameters and/or changes in existing parameters, in relation to the upcoming release of the ISO11898-2:2016 and SAE-J2284-4/5 specifications
- General corrections, additions and clarifications

No physical or design change whatsoever has been made to any of the above-mentioned products, their reliability and functionality is therefore not affected.

The datasheet's revision history details the changes made. The updated datasheets can be obtained from the NXP e-PCN system you're subscribed to, in the same way you obtained this document. They will be published on the NXP website 30 days after publication of this CIN.

In the sections below all changes are explained in more detail. All references to a product imply all (package) versions of that product. Unless mentioned otherwise, all datasheet changes apply to all of the above-mentioned products.

2. CAN FD requirements up to 5Mbit/s

The upcoming ISO11898-2:2016 and SAE-J2284-4/5 specifications define timing parameters, whose implementation enable reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s:

- $t_{bit(bus)}$ transmitted recessive bit width
- $t_{bit(RXD)}$ bit time on pin RXD
- Δt_{rec} receiver timing symmetry

All above-mentioned products are enabled for data rates up to 5 Mbit/s, except TJA1145 which is enabled up to 2 Mbit/s. The improved performance is achieved by applying tighter limits at final test of these products. These tighter test limits have been implemented, and hence products will comply with the updated datasheets, from datecode wk1601 onwards. This datecode is shown in the top marking of the products (see Section 5 'Traceability').

3. Other changes in relation to ISO11898-2:2016 and SAE-J2284-4/5

The upcoming ISO11898-2:2016 specification consolidates ISO11898-2:2003, ISO11898-5:2007 and ISO11898-6:2013. Apart from the above-mentioned 5 Mbit/s, many more changes have been made to this specification. New requirements/parameters have been defined and/or conditions/limits for existing parameters have changed.

For ease of use a parameter cross-reference list has been added as appendix to all the datasheets, explaining where applicable the difference in parameter symbol and name between the ISO11898 specification and the NXP datasheets. This table is shown in Appendix 2 on page 5. Below, primary reference is made to the datasheet symbol, with the corresponding ISO symbol between brackets.

The following changes/additions have been made to the datasheets:

- **$V_{(CANH-CANL)}$ (V_{Diff})**: limiting value for the voltage between pin CANH and pin CANL
  - +/-40V for TJA1145 (already in previous datasheet revision)
  - +/-20V for TJA1043
  - +/-27V for all other products
- **$V_{O(dom)}$ (V_{CAN_H}, V_{CAN_L})**: add load condition R_L = 50-65 Ω
- **V_{TXsym} (V_{SYM})**: add parameter and associated test circuit for measuring diagram
- **$V_{O(dif)}$ (V_{Diff})**: add load conditions (45-70 Ω and 2240 Ω), add condition for standby/sleep mode
- **$V_{rec(RX)}$, $V_{dom(RX)}$ (V_{Diff})**: additional parameters
- **$I_{O(sc)dom}$ (I_{CAN_H}, I_{CAN_L})**: extended conditions for V_{CANH} and V_{CANL}
- The 'CAN transceiver timing' and 'Loop delay symmetry timing' diagrams have been updated

4. General corrections, additions and clarifications

The following additional changes have been made to the datasheets:

4.1 Parameter name and symbol alignment

Various parameters had slightly different names and symbols across the product datasheets. To enable a single parameter cross-reference between the datasheets and the ISO specification, the parameter names and symbols have been made consistent across all the datasheets:

- $V_{O(dif)bus}$ bus differential output voltage ➔ $V_{O(dif)}$ differential output voltage
- $I_{O(dom)}$ dominant output current ➔ $I_{O(sc)dom}$ dominant short-circuit output current
- $I_{O(rec)}$ recessive output current ➔ $I_{O(sc)rec}$ recessive short-circuit output current
- I_{IL} input leakage current ➔ I_L leakage current
- $R_{i\ (cm)}$ common-mode input resistance ➔ R_i input resistance

4.2 Clarifications

The following clarifications have been made in all the datasheets:

- In the pin description table the footnote explaining how to connect the exposed diepad, for the HVSON package variant of the product, has been rewritten.
- In the limiting values table two changes have been made:
  - A footnote on the definition of the Absolute Maximum Rating (AMR) for the voltage on pins has been added
  - The format for V_{trt}, the transient voltage, and its associated footnote have been made more clear
- The application diagrams have been updated to show the advised capacitor components.

4.3 Wake-up

To improve the description of how products wake-up from sleep/standby mode and align this across all datasheets the following changes have been made (note:these changes do not apply to the Basic HS-CAN products TJx1051 and TJA1057):

- A ‘Wake-up timing’ diagram has either been added or adapted.
- A section ‘Remote wake-up (via the CAN bus)’ has been added for products TJA1043, TJA1048 and TJA1059
- Parameter $t_{fltr(wake)bus}$ bus wake-up filter time has been added for products TJA1044, TJA1046, TJx1052i and TJA1145. This is not a change in functionality of those products, the parameter addition merely more appropriately describes the functionality as it has always been.
- The description of the parameter $t_{fltr(wake)bus}$ has been improved for product TJA1059.
- The section ‘Bus dominant time-out function’ and parameter $t_{to(dom)bus}$, bus dominant time-out time, have been removed from the datasheet of products TJA1044, TJA1046 and TJA1049, as they are redundant. This is explained in more detail in Appendix 1 on page 4. This change does not in any way change the functionality of the products TJA1044, TJA1046 and TJA1049. Of all the products mentioned in Section 1, only TJA1042 and TJA1043 continue to have the parameter $t_{to(dom)bus}$ defined in the datasheet, for all other products it is not applicable.

4.4 VIO

Various products have a VIO functionality or option, allowing direct interfacing to microcontrollers with supply voltages from 3 V to 5 V (TJA1042, TJA1043, TJA1049, TJx1051, TJA1057 and TJA1145). In the conditions of various parameters reference is made to the voltage VIO. Throughout the datasheets of these products clarifying comments have been added to describe the case where the non-VIO product is used or when $V_{IO}=V_{CC}$. There is no change in functionality of these products.

4.5 Changes to specific datasheets

There are a few very specific changes, which only apply to individual products:

- **TJA1043**:
  - The maximum specification for parameters $t_{wake(busdom)}$ / $t_{wake(busrec)}$ has improved from 5 to 3 μs
  - The minimum specification for parameters $t_{to(dom)TXD}$ / $t_{to(dom)bus}$ has improved from 0.3 to 0.4 μs
- **TJx1051**: the minimum possible bit rate has improved from 40 kbit/s to 20 kbit/s
- **TJx1052i**:
  - Throughout the datasheet incorrect references to V_{CC} have been replaced with $V_{DD1/2}$. This does not in any way influence the functionality of the product.
  - The I_{DD2}, supply current 2, specification was incorrect, not taking into account the voltage on pin STB (V_{STB}). This has been corrected, leading to an overall improvement of the specification.
- **TJA1145**:
  - A ‘Quick reference data’ section has been added
  - Parameter $V_{th(sw)hys}$, switching threshold voltage hysteresis, has been added to the SPI description
  - The SPI timing diagram, which was incorrectly removed from the previous revision datasheet, has been re-introduced.

5. Traceability

There are no changes in NXP product (version) names, orderable part numbers, 12NC ordering codes or product identification in the first line of the product's top-side marking. The compliance to the CAN FD requirements is fully traceable by datecode marked on the products. The datecode is shown in the 3rd line of the product marking, either with 3 (yww) or 4 (yyww) digits. In the example in Figure 1 below, the datecode is '430' (y=4➔14, ww=30, wk 30, 2014). The compliance to the CAN FD requirements is applicable to products marked with datecode 1601 onwards.

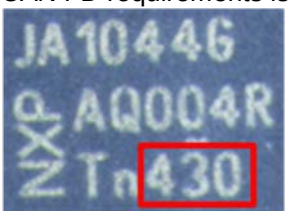

Figure 1: example product marking

6. Summary

Table 2 in Appendix 3 on page 6 summarizes all the changes described in Sections 3 and 4.

Appendix 1: Redundancy of $t_{to(dom)bus}$ for products with WUP

TJA1044, TJA1046 and TJA1049 are devices that wake-up through a 3-pulse dominant-recessive-dominant Wake-Up Pattern (WUP) on the bus, as defined in ISO11898 and shown in Figure 2 below. For the 3-pulse WUP to be valid, the dominant/recessive pulses need to be longer than $t_{wake(busdom)}$/$t_{wake(busrec)}$ and the pattern needs to be received within $t_{to(wake)bus}$.

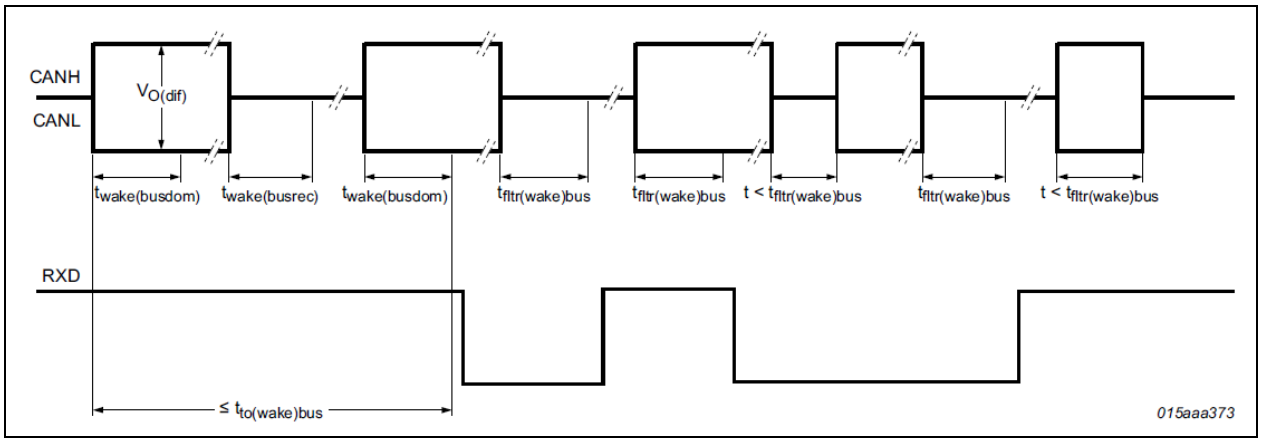

Figure 2: Wake-up timing diagram for devices that wake-up through a 3-pulse WUP

That the parameter $t_{to(dom)bus}$, bus dominant time-out time, is redundant for these products can be understood as follows:

- The bus dominant time-out function only works in standby mode of the device, and is disabled as soon as a valid WUP is detected (see below extract from the previous revision TJA1044 datasheet).

> **7.3.2 Bus dominant time-out function**
>
> In Standby mode a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than $t_{to(dom)bus}$, the RXD pin is reset to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state. The bus dominant time out function is disabled as soon as a valid wake-up pattern is detected.

- This is also confirmed by the definition of parameter $t_{to(dom)bus}$ (see below extract from the current TJA1044 datasheet).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{to(dom)bus}$	bus dominant time-out time	Standby mode	0.8	3	6.5	ms

- For a device without WUP in standby mode:
  - If a bus dominant pulse is longer than $t_{wake(busdom)}$, RXD goes low.
  - After the bus dominant time-out time $t_{to(dom)bus}$ has passed, RXD goes high again.
- For a device with WUP in standby mode:
  - RXD will only go low after a valid 3-pulse WUP (see Figure 2 above)
  - Once a valid WUP has been received, the device will go in normal mode and the bus dominant time-out function is no longer active.
- In conclusion, a bus dominant time-out time $t_{to(dom)bus}$ is a redundant parameter for devices that wakes up through a 3-pulse WUP, like TJA1044, TJA1046 and TJA1049.

Appendix 2: ISO11898-2:2016 parameter cross-reference list

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V_{SYM}	V_{TXsym}	transmitter voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)dom}$	dominant short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
Optional HS-PMA transmit dominant timeout			
Transmit dominant timeout, long	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time
Transmit dominant timeout, short			
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R_{Diff}	$R_{i(dif)}$	differential input resistance
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	R_i	input resistance
Matching of internal resistance	MR	ΔR_i	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(bus)}$	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RXD)}$	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt_{Rec}	Δt_{rec}	receiver timing symmetry

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating V_{Diff}	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating VCAN_H and VCAN_L			
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
HS-PMA bus biasing control timings			
CAN activity filter time, long	t_{Filter}	$t_{wake(busdom)}$[1]	bus dominant wake-up time
CAN activity filter time, short		$t_{wake(busrec)}$[1]	bus recessive wake-up time
Wake-up timeout, short	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up timeout, long			
Timeout for bus inactivity	$t_{Silence}$	$t_{to(silence)}$	bus silence time-out time
Bus Bias reaction time	t_{Bias}	$t_{d(busact-bias)}$	delay time from bus active to bias

[1] $t_{flt(wake)bus}$ - bus wake-up filter time, in devices with basic wake-up functionality

Table 1: ISO11898-2:2016 to NXP datasheet parameter conversion

Appendix 3: Summary of all changes

Topic	Type of CAN transceiver =>	Basic HS-CAN		Standby HS-CAN			Sleep mode HS-CAN	Dual CAN			Isolated CAN	HS-CAN with partial networking
	Product =>	TJA1051 TJF1051	TJA1057	TJA1042	TJA1044	TJA1049	TJA1043	TJA1046	TJA1048	TJA1059	TJA1052i TJF1052i	TJA1145
ISO11898-2:2016 (sections 2 and 3)	CAN FD requirements met up to	5 Mbit/s	5 Mbit/s	5 Mbit/s	5 Mbit/s	5 Mbit/s	5 Mbit/s	5 Mbit/s	5 Mbit/s	5 Mbit/s	5 Mbit/s	2 Mbit/s
	Parameter $V_{(CANH-CANL)}$ added with voltage range	+/-27V	+/-27V	+/-27V	+/-27V	+/-27V	+/-20V	+/-27V	+/-27V	+/-27V	+/-27V	+/-40V [1]
	Add load condition R_L = 50-65 Ω to $V_{O(dom)}$	X	X	X	X	X	X	X	X	X	X	X
	Add parameter V_{TXsym} and associated test circuit for measuring diagram	X	X	X	X	X	X	X	X	X	X	X [2]
	Add load conditions and condition for standby/sleep mode to $V_{O(dif)}$	X	X	X	X	X	X	X	X	X	X	X
	Add parameters $V_{rec(RX)}$ and $V_{dom(RX)}$	X	X	X	X	X	X	X	X	X	X	X
	Extended condition for V_{CANH} and V_{CANL} for parameter $I_{O(sc)dom}$	X	X	X	X	X	X	X	X	X	X	X
	Update 'CAN transceiver timing' and 'Loop delay symmetry timing' diagrams	X	X	X	X	X	X	X	X	X	X	X
parameter name and symbol alignment (section 4.1) [3]	$V_{O(dif)bus}$ => $V_{O(dif)}$	X	X	X	X	X	X	X	X	X	X	X
	$I_{O(dom)}$ => $I_{O(sc)dom}$		X		X							X
	$I_{O(rec)}$ => $I_{O(sc)rec}$		X		X							X
	I_{IL} => I_L						X					X
	$R_{i(cm)}$ => R_i											X
Clarifications (section 4.2) [3]	Pin description table footnote HVSON package	X	X	X	X	X	X	X	X	X	N/A [4]	X
	Added footnote on definition AMR to 'Limiting values' table	X	X	X	X	X	X	X	X	X	X	X
	More clear format V_{trt} in 'Limiting values' table	X		X		X	X		X	X	X	X
	Updated application diagram	X		X		X	X		X	X	X	X
Wake-up (section 4.3) [5]	Wake-up timing' diagram added or adapted	N/A		X	X	X	X	X	X	X	X	X
	Added section 'Remote wake-up (via the CAN bus)'						X		X	X		
	Parameter $t_{filtr(wake)bus}$ added				X			X			X	X
	Improved description parameter $t_{filtr(wake)bus}$									X		
	Section 'Bus dominant time-out function' and parameter $t_{to(dom)bus}$ removed				X	X		X				
VIO (section 4.4)	Clarification non-VIO product and/or V_{IO}=V_{CC} [6]	X	X	X		X	X					X
Changes to specific datasheets (section 4.5) [7]		X					X				X	X

Table 2: Summary of all datasheet changes
[1] For TJA1145 the parameter $V_{(CANH-CANL)}$ was already defined in the datasheet with voltage range +/-40V
[2] For TJA1145 the parameter V_{TXsym} and the associated test circuit for measuring diagram were already available in the datasheet.
[3] 'X' indicates the change has been made for that specific product. No 'X' indicates it was already OK in the current datasheet and therefore does not require changing.
[4] The footnote is not applicable to TJx1052i, as it does not have a leadless HVSON package version.
[5] 'X' indicates the change has been made for that specific product. No 'X' indicates the change is either not applicable, or it was already OK in the current datasheet and therefore does not require changing.
[6] The products marked with 'X' are the only ones that have a VIO pin or option, and therefore the change is only relevant for them.
[7] Only the products marked with 'X' have specific datasheet changes, as described in Section 4.5.