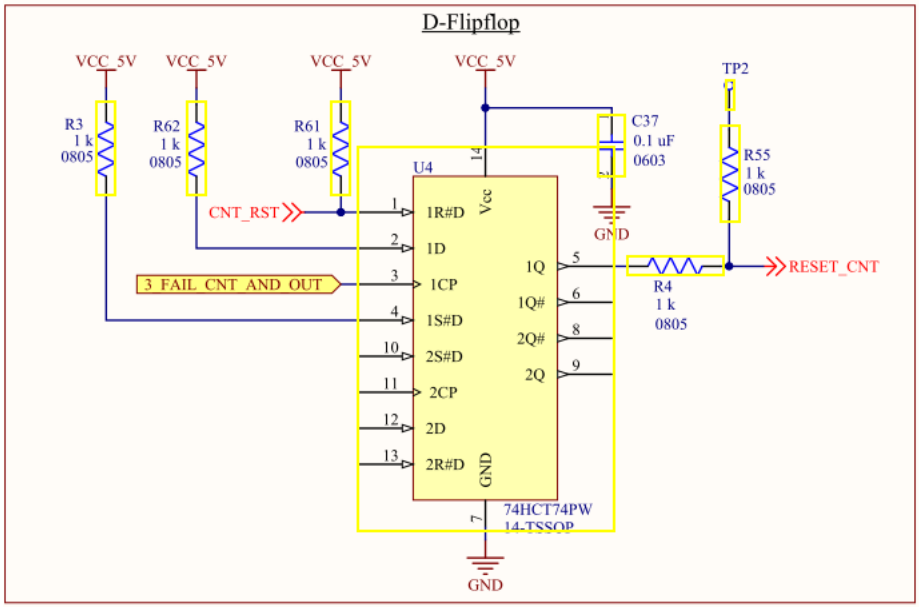
I have used following part in one of my design.

Part #: 74HCT74PW
Function: D-type flip-flop
Description: Dual D-type flip-flop with set and reset; positive-edge trigger; TTL-enabled

Circuit diagram:



The Net 'CNT_RST' is connected to GPO of microcontroller to clear the flip-flop. The Net 'RESET_CNT' is connected to GPI of microcontroller to get the status.

I'm referring the your datasheet "Rev. 5" Dated: 3 December 2015 and I'm unable to get the following from datasheet,

Input				Output (Present state)	
1SD#	**1RD#**	**1CP**	**1D**	**1Q**	**1Q#**
H	H	X	X	?	?
H	H	L	H	?	?

Initially after power ON, 'CNT_RST' GPO (Pin 1, 1R#D) is in HIGH state, pin-4 (1S#D) is in HIGH state (pulled-up) and pin-3 (1CP) is in LOW state.
With this configuration, I got output pin-5 (1Q) as HIGH.

I have considered the following,

Table 4. Function table[1]

Input				Output	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ_{n+1}	$n\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH transition; Q_{n+1} = state after the next LOW-to-HIGH CP transition; X = don't care.

Clarification required:

My expected output will be HIGH, only when the SD=HIGH, RD=HIGH and also CP is in positive rising edge. But, I'm getting output pin-5 (1Q) as HIGH, when the CP is in low state.

Request you to clarify the understanding is correct or not.