8.1.2 Control registers overview

Table 7. Control and function registers overview

Bit positions labeled as - are not implemented. After reset, all registers are set according to Table 62 on page 59.

Address	Register name	Bit								Reference
		7	6	5	4	3	2	1	0	
Offset register										
24h	Offset	OFFSET[7:0]								Section 8.8
Control registers										
25h	Oscillator	CLKIV	OFFM	12_24	LOWJ	OSCD[1:0]		CL[1:0]		Section 8.10
26h	Battery_switch	-	-	-	BSOFF	BSRR	BSM[1:0]		BSTH	Section 8.11
27h	Pin_IO	CLKPM	TSPULL	TSL	TSIM	TSPM[1:0]		INTAPM[1:0]		Section 8.12
28h	Function	100TH	PI[1:0]		RTCM	STOPM	COF[2:0]			Section 8.13
29h	INTA_enable	ILPA	PIEA	OIEA	A1IEA	A2IEA	TSRIEA	BSIEA	WDIEA	Section 8.9
2Ah	INTB_enable	ILPB	PIEB	OIEB	A1IEB	A2IEB	TSRIEB	BSIEB	WDIEB	Section 8.9
2Bh	Flags	PIF	A2F	A1F	WDF	BSF	TSR3F	TSR2F	TSR1F	Section 8.14
RAM byte										
2Ch	RAM_byte	B[7:0]								Section 8.6
WatchDog registers										
2Dh	WatchDog	WDM	WDR[4:0]					WDS[1:0]		Section 8.5
Stop										
2Eh	Stop_enable	-	-	-	-	-	-	-	STOP	Section 8.16
Reset										
2Fh	Resets	CPR	0	1	0	SR	1	0	CTS	Section 8.15