1. I²C bus interface and register settings

The **NXQ1TXH5** supports the 400 kHz I2C-bus microcontroller interface mode standard. The I²C-bus is used to control the **NXQ1TXH5** and to transmit and receive data.

The **NXQ1TXH5** can operate only in I²C slave mode, as a slave receiver or as a slave transmitter.

1.1 NXQ1TXH5 address

The **NXQ1TXH5** is accessed via an 8-bit code. Bits 1 to 7 contain the device address. Bit 0 (R/W) indicates whether a read (1) or a write (0) operation has been requested.

ADDRESS	
0110 1000	For write mode
0110 1001	For read mode

Table 1. Address selection via address selection bits

1.2 I²C-bus write cycle

The sequence of events that needs to be followed when writing data to the **NXQ1TXH5**'s I²C-bus registers is detailed in Table 2. One byte is transmitted at a time. Each register stores two bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The write cycle sequence using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller transmits the 7-bit device address of the **NXQ1TXH5**, followed by the R/W bit set to 0.
3. The **NXQ1TXH5** asserts an acknowledge (A).
4. The microcontroller transmits the 8-bit **NXQ1TXH5** register address to which the first data byte will be written.
5. The **NXQ1TXH5** asserts an acknowledge.
6. The microcontroller transmits the first byte (the most significant byte).
7. The **NXQ1TXH5** asserts an acknowledge.
8. The microcontroller transmits the second byte (the least significant byte).
9. The **NXQ1TXH5** asserts an acknowledge.
10. The microcontroller can either assert the stop condition (P) or continue transmitting data by sending another pair of data bytes, repeating the sequence from step 6. In the latter case, the targeted register address will have been auto-incremented by the **NXQ1TXH5**.

Table 2. **I²C-bus write cycle NXQ1TXH5**

Start	NXQ1TXH5 address	R/W		First register address		MSB		LSB		More data...	Stop
S	0110100	0	A	ADDR	A	MS1	A	LS1	A	<....>	P

1.3 I²C-bus read cycle description

The sequence of events that needs to be followed when reading data from the **NXQ1TXH5**'s I²C-bus registers is detailed in Table 3. One byte is transmitted at a time. Each of the registers stores two bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The read cycle sequence using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller transmits the 7-bit device address of the **NXQ1TXH5**, followed by the R/W bit set to 0.
3. The **NXQ1TXH5** asserts an acknowledge (A).
4. The microcontroller transmits the 8-bit **NXQ1TXH5** register address from which the first data byte will be read.
5. The **NXQ1TXH5** asserts an acknowledge.
6. The microcontroller asserts a repeated start (Sr).
7. The microcontroller re-transmits the device address followed by the R/W bit set to 1.
8. The **NXQ1TXH5** asserts an acknowledge.
9. The **NXQ1TXH5** transmits the first byte (the MSB).
10. The microcontroller asserts an acknowledge.
11. The **NXQ1TXH5** transmits the second byte (the LSB).
12. The microcontroller asserts either an acknowledge or a negative acknowledge (NA).
    - If the microcontroller asserts an acknowledge, the target register address is auto-increased by the **NXQ1TXH5** and steps 9 to 12 are repeated.
    - If the microcontroller asserts a negative acknowledge, the **NXQ1TXH5** frees the I²C-bus and the microcontroller generates a stop condition (P).

Table 3. **I²C-bus read cycle NXQ1TXH5**

Start	NXQ1TXH5 address	R/W		First register address			NXQ1TXH5 address	R/W		MSB		LSB		More data...		Stop
S	0110100	0	A	ADDR	A	Sr	0110100	1	A	MS1	A	LS1	A	<...>	NA	P

1.4 On/off

To enable on/off control via I2C the device can be set into Off mode via I2C in register 10 bit 0, All other bits in register 10 need to remain 0.

Table 4. **I²C On/Off control**

Bit $10[0] powerdown	function
0000000000000000	Normal operation (default value)
0000000000000001	Device is in OFF mode

1.5 Read register map

1.5.1 Manager Status register

In register 00h the Manager status of the **NXQ1TXH5** can be read, bits 14:10 gives the status of operation and in bit 0 the supply status can be read. Status “10000” means that the device is in charge mode and the DSP is having control in the device. So if a phone is put on the charger and the receiver has been recognized the **NXQ1TXH5** will go into this state. Be aware that also without a phone the **NXQ1TXH5** will do a DIGITAL PING each 4.5 secs and will be in this state “10000” for about 70msec. So to read if the device is in real charging mode, this register should be true for at least more than 70 msec, Or should be read for example every sec.

Table 5. System status register (address 00h)

Bit	*Value*	*Description*
15	reserved	
14:10	**10000**	**status report: status "10000" means DSP is operational, device is in CHARGE mode**
9	reserved	
8	reserved	
7	reserved	
6	reserved	
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	reserved	
0	**1**	**digital supply (V_{DDD}) voltage level is ok**
	0	**digital supply (V_{DDD}) voltage level is < 1.2 V**

1.5.2 Supply Status register

In register 02h the Supply status of the **NXQ1TXH5** can be read. On bits 9:0 the Supply Voltage can be linearly read in 1023 steps, where FFh means that the Supply is 6V

Table 6. Supply status register (address 02h)

Bit	*Value*	*Description*
15:10	reserved	
9:00	**xxx**	**supply level sensor value; 0V to 6V in 1023 steps**

1.5.3 Temperature Status register

In register 03h the Temperature status of the **NXQ1TXH5** can be read. On bits 8:0 the Temperature can be linearly read in 511 steps, in two complements code, where 8Fh means that the Temperature 255 degrees C.

Table 7. Temperature status register (address 03h)

Bit	*Value*	*Description*
15:09	reserved	
8:00	**xxx**	**temperature level sensor**

1.5.4 NTC Status register

In register 07h the NTC pin input Voltage status of the **NXQ1TXH5** can be read. On bits 9:0 the NTC pin input voltage can be linearly read in 1023 steps where FFh means that the input Voltage is 1.5V

Table 8. NTC status register (address 07h)

Bit	*Value*	*Description*
15:09	reserved	
8:00	**xxx**	**NTC pin input voltage**