


MPC5675KEVB473 Evaluation Board

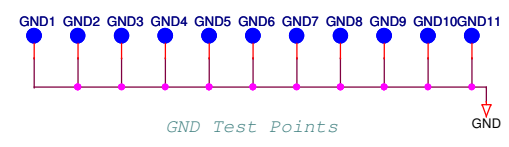
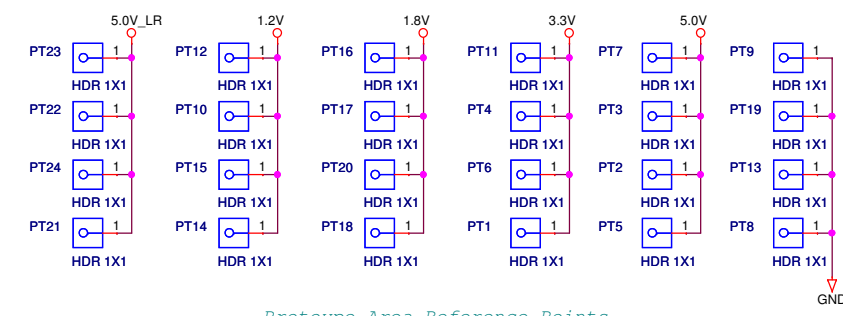
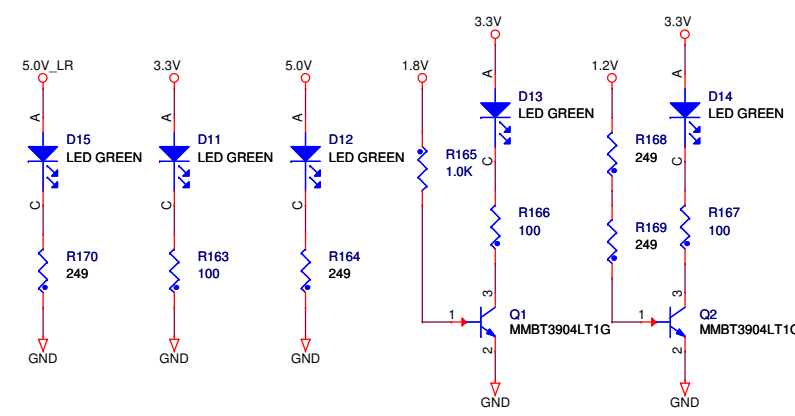
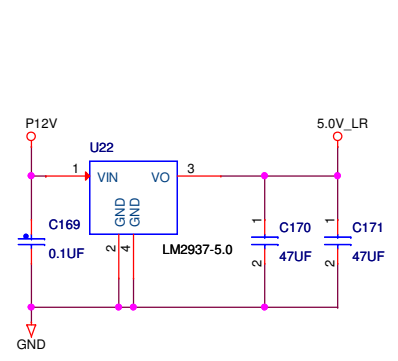
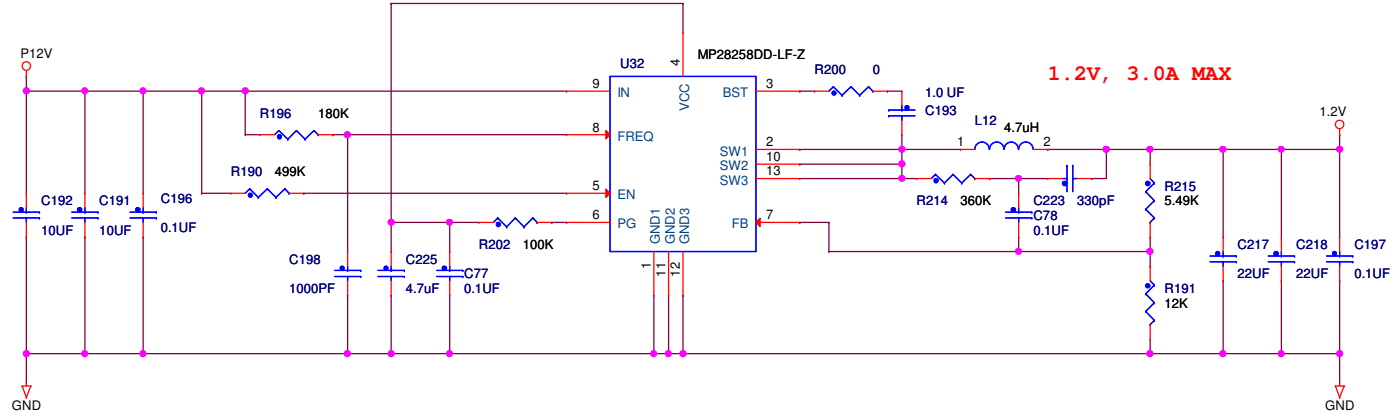
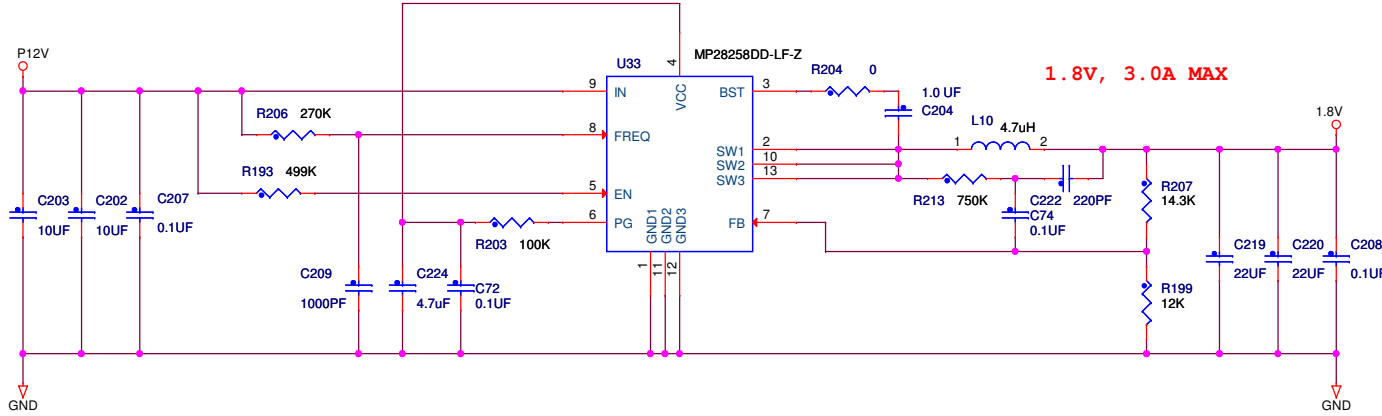
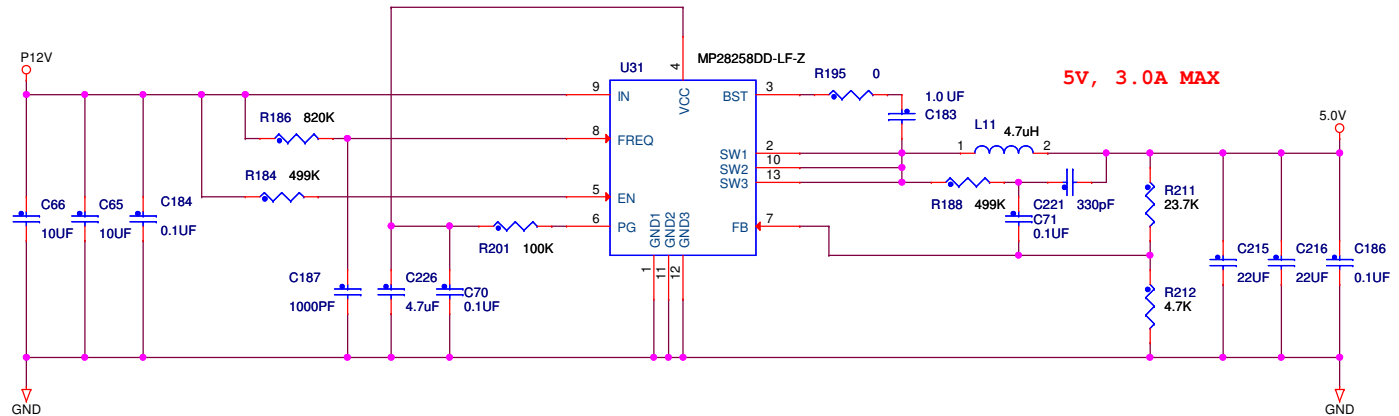
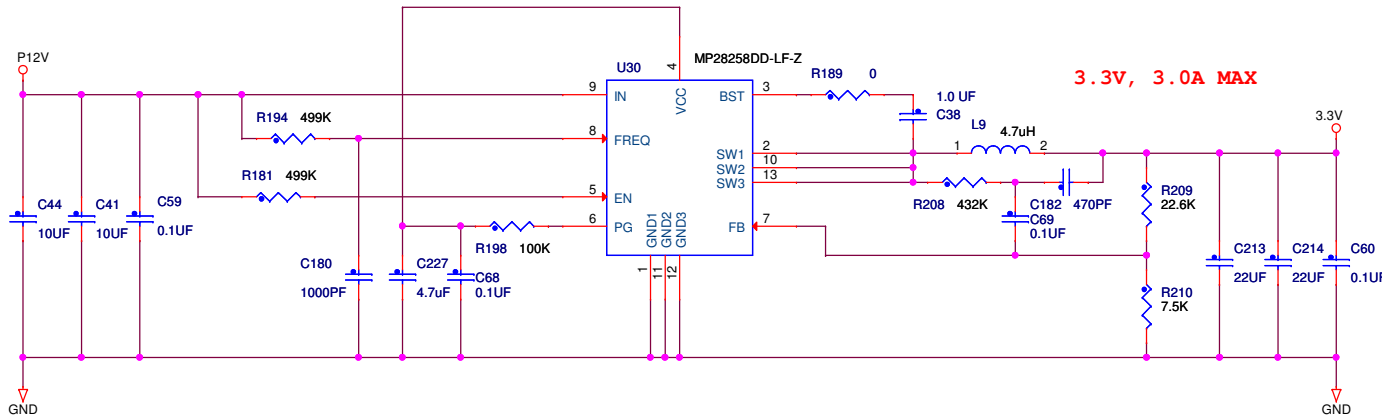
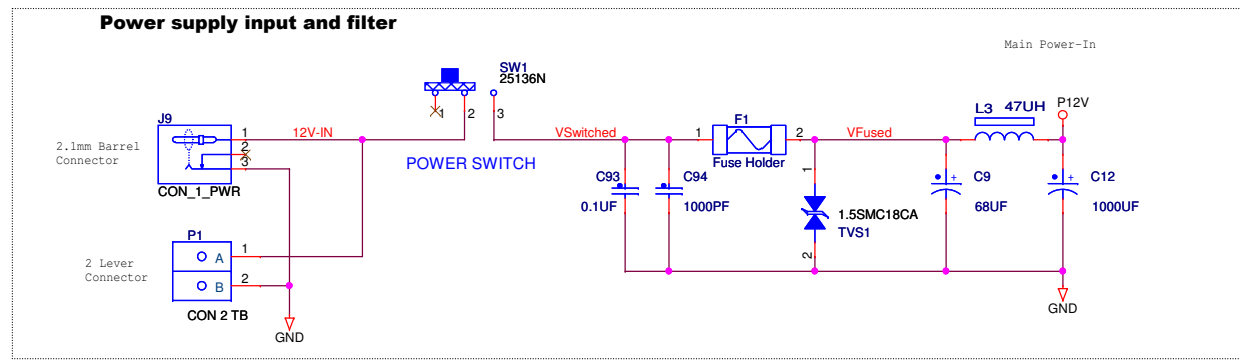
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Revisions

Rev	Description	Date	Designer
X1	Draft	January 22, 2010	Qiao Jun
X2	Draft 2	January 29, 2010	Robertson Andrew & Qiao Jun
X3	Draft 3	February 2, 2010	Robertson Andrew & Qiao Jun
X4	Draft 4	February 6 2010	Robertson Andrew & Qiao Jun
X5	Draft 5	February 9 2010	Robertson Andrew & Qiao Jun
X6	Split ONLY for MPC5675K 473BGA	February 10 2010	Robertson Andrew & Qiao Jun
X7	reset circuitry update	February 11 2010	Robertson Andrew & Qiao Jun
X8	Various updates on pages	February 15 2010	Robertson Andrew
X9	Back annotate	February 23 2010	Qiao Jun
A	Release	February 26 2010	Qiao Jun
A1	Revise	June 20 2010	Robertson Andrew & Qiao Jun
A2	Revise	June 22 2010	Robertson Andrew & Qiao Jun
A3	Revise	June 24 2010	Robertson Andrew & Qiao Jun
B	Release	July 8 2010	Qiao Jun
B1	Revise	December 15 2010	Qiao Jun
C	Release	December 17 2010	Qiao Jun
C1	Remove socket, add mDDR	May 11 2011	Qiao Jun
C2	Revise power regulation	July 15 2011	Qiao Jun
D	Release	July 29 2011	Qiao Jun

		Microcontroller Solutions Group	
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Designer: R60321 & B23443		ICAP Classification: FCP: FIUC: X PUBI:	
Drawing Title: MPC5675KEVB473			
Drawn by: Qiao Jun		Page Title: TITLE PAGE	
Approved: Robertson Andrew	Size C	Document Number SCH-26488 PDF: SPF-26488	Rev D
Date: Tuesday, August 02, 2011		Sheet 1 of 16	



ICAP Classification: FCP: FIUO: X PUBL:

Drawing Title: **MPC5675KEVB473**

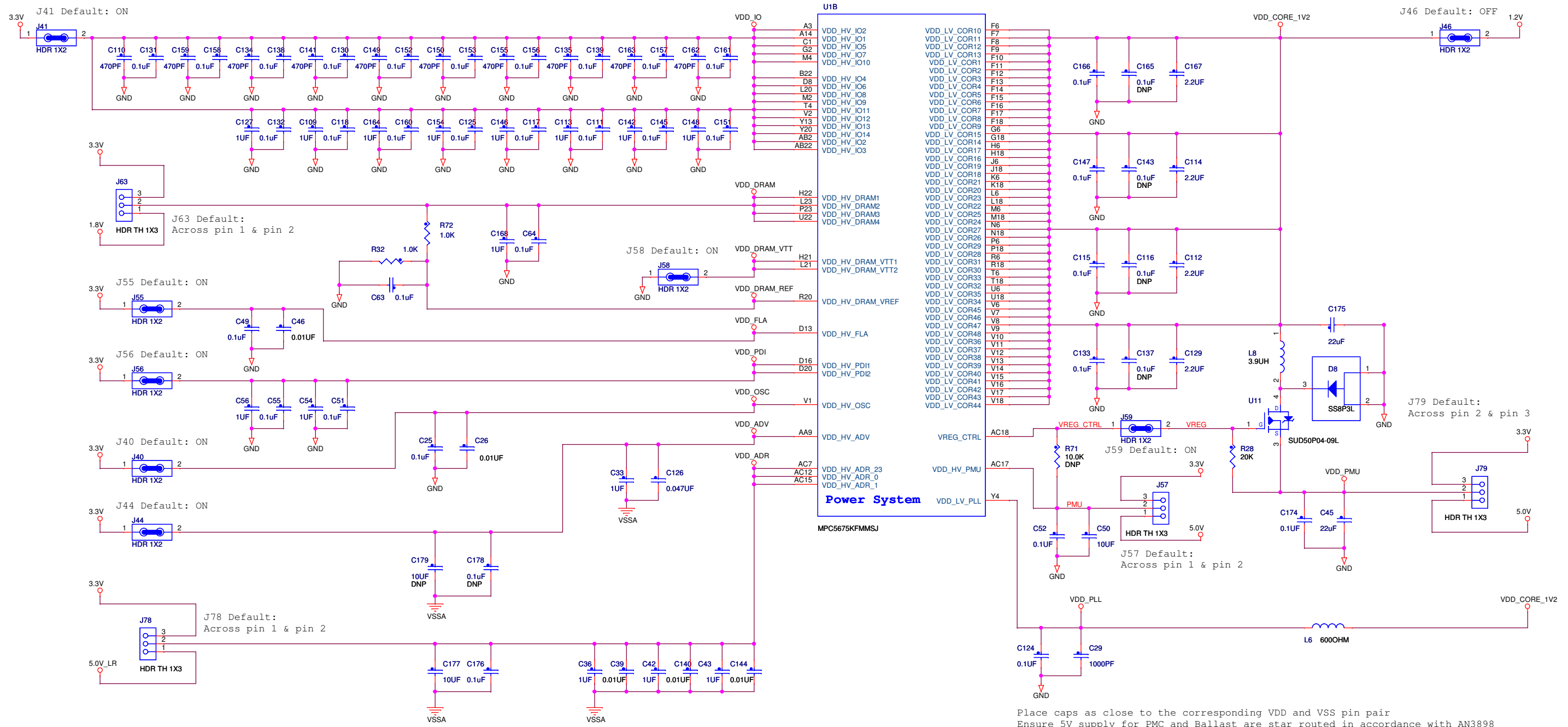
Page Title: **Power Input and Regulation**

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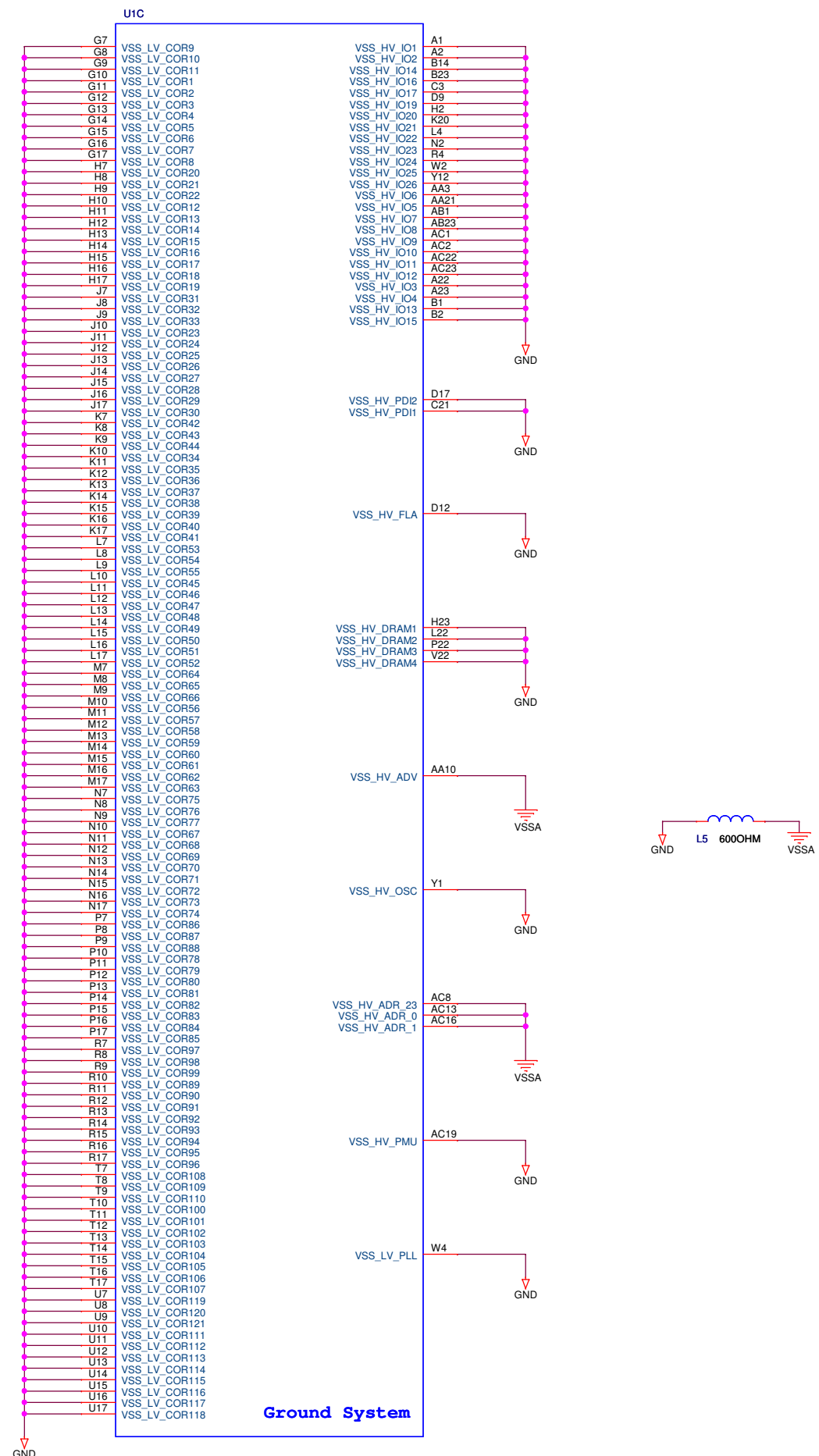
Place all caps below as close as possible to the corresponding VDD and VSS pin pair

Put as close as possible between VDD_LV_COR and VSS_LV_COR,
Ideal placement at bottom side of PCB between center ball matrix and IO ring,
Place circuitry 4 times at the centre.



Place caps as close to the corresponding VDD and VSS pin pair
Ensure 5V supply for PMC and Ballast are star routed in accordance with AN3898

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MPC5675KEVB473		
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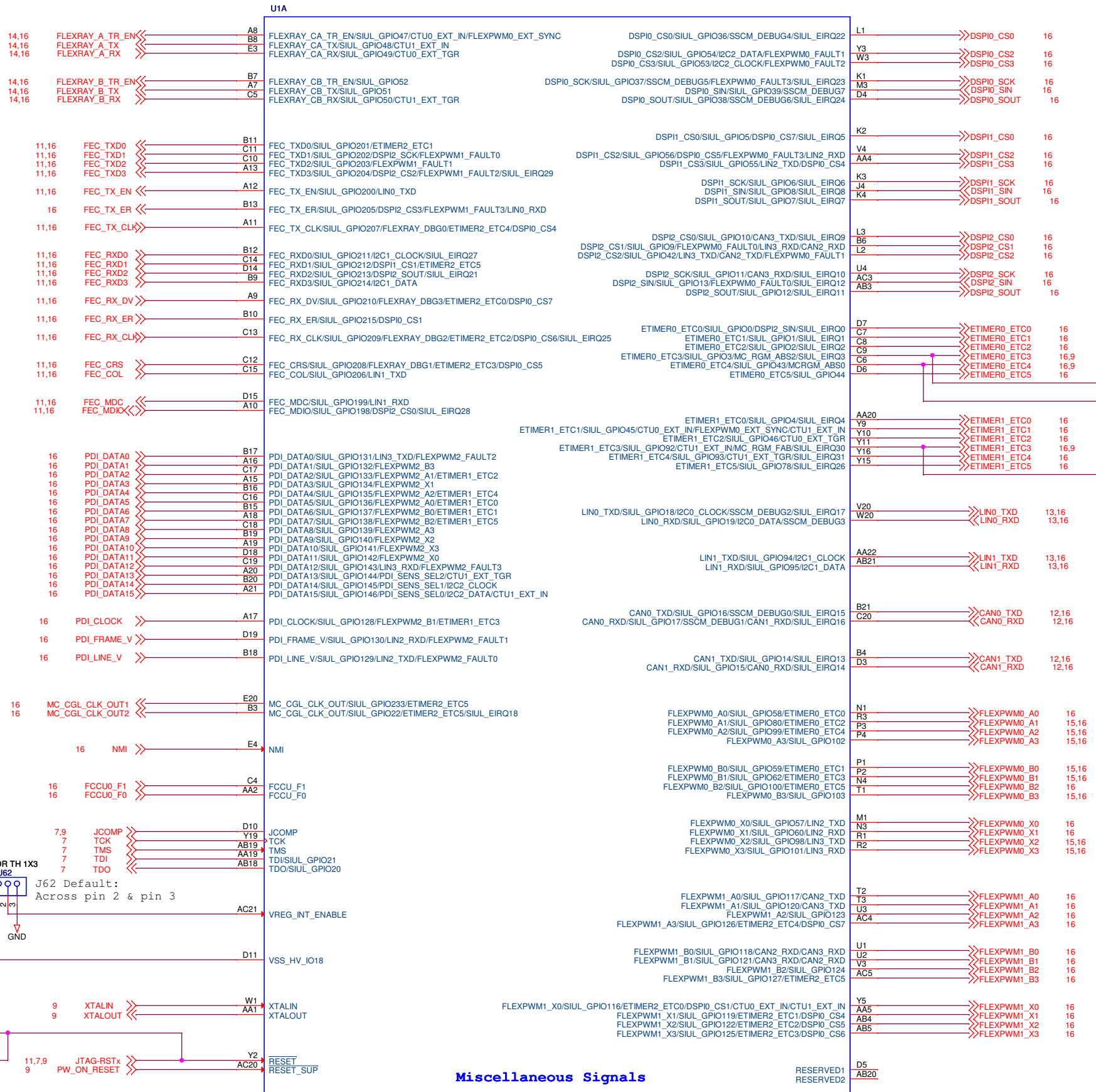


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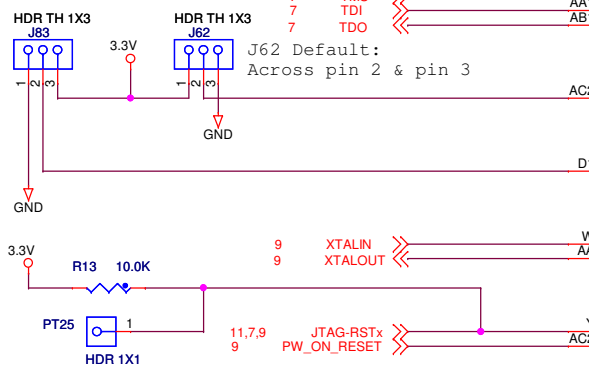
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MPC5675K GND Pin

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J83 Default:
Across pin 1 & pin 2



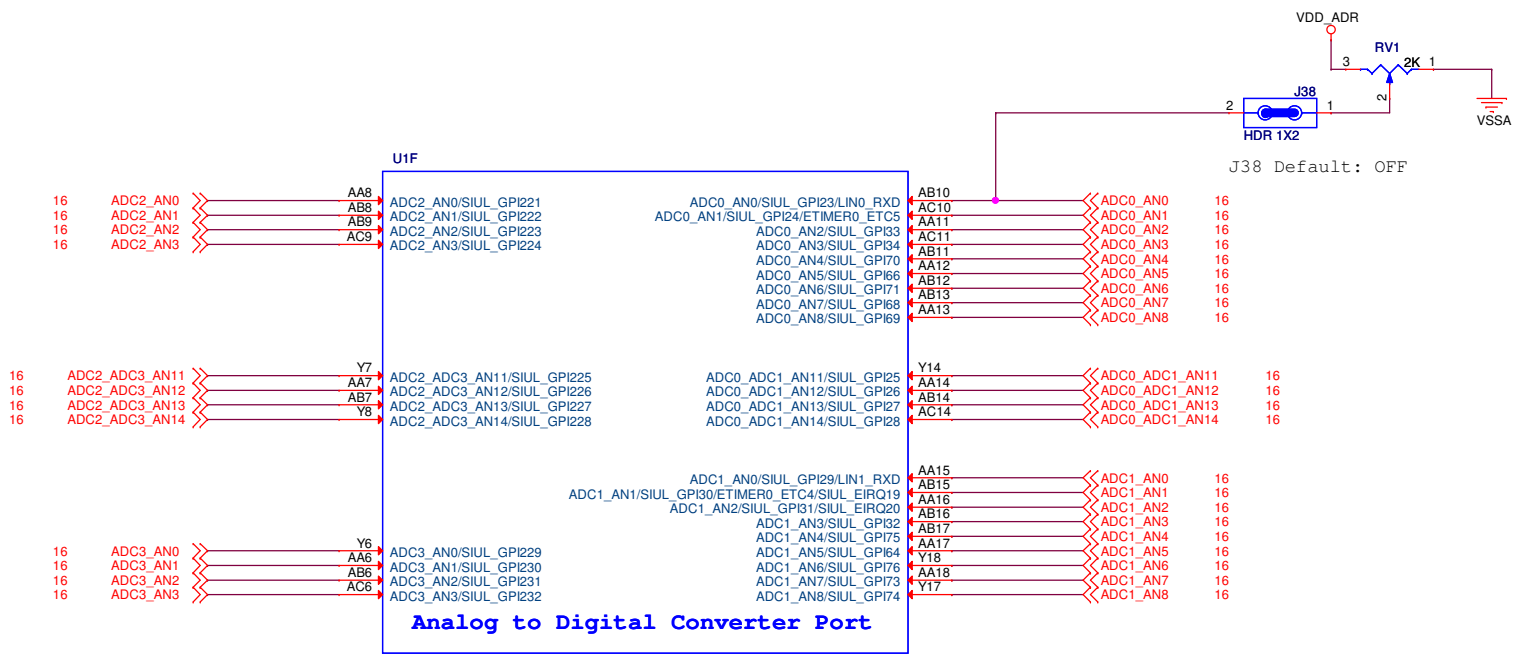
Miscellaneous Signals

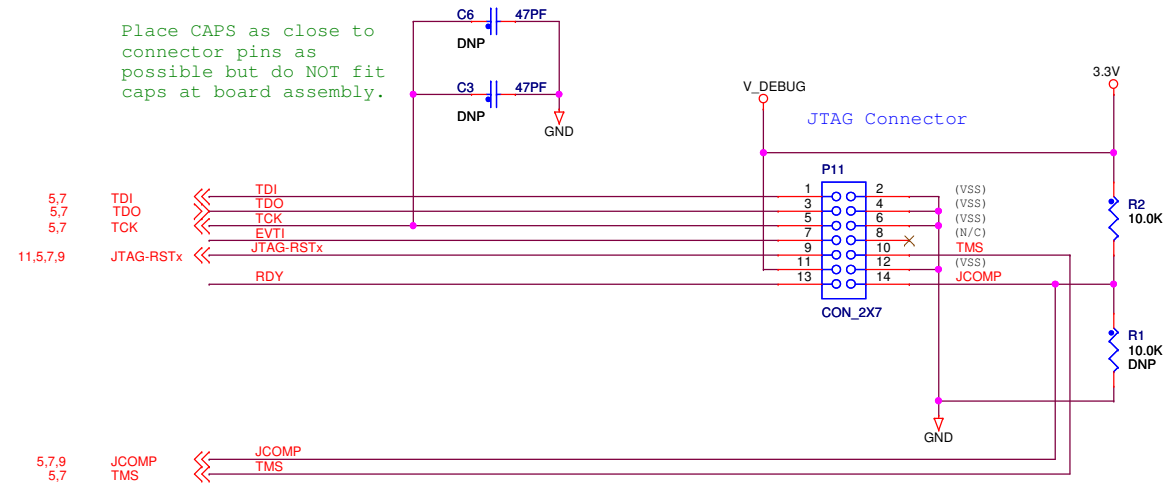
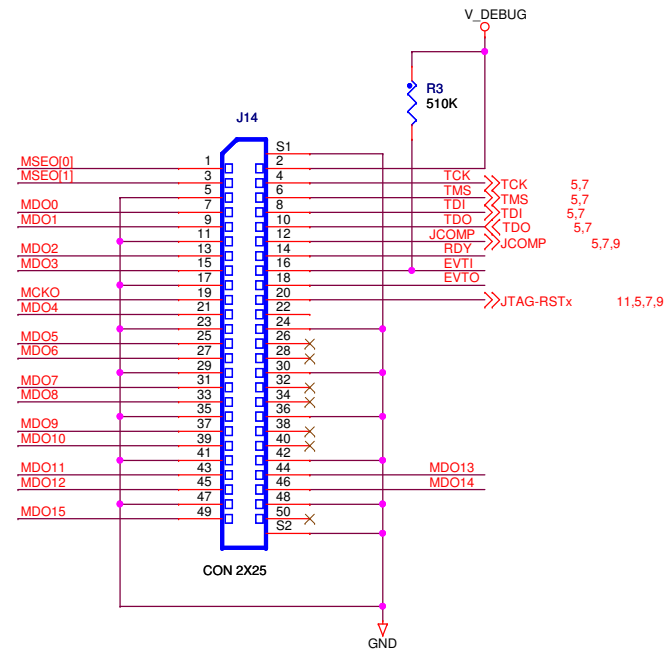
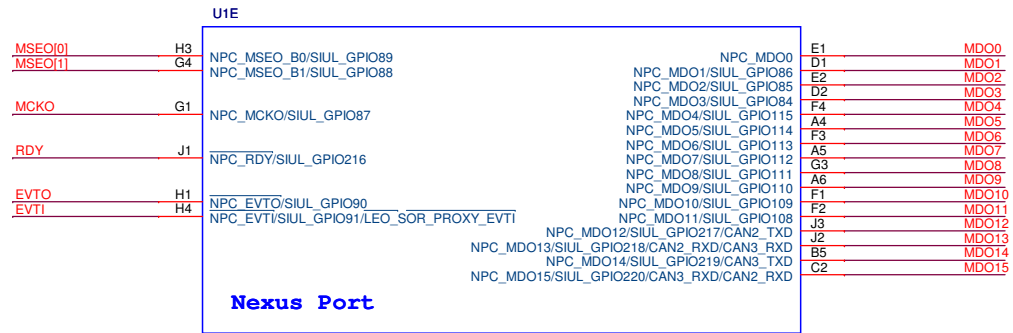
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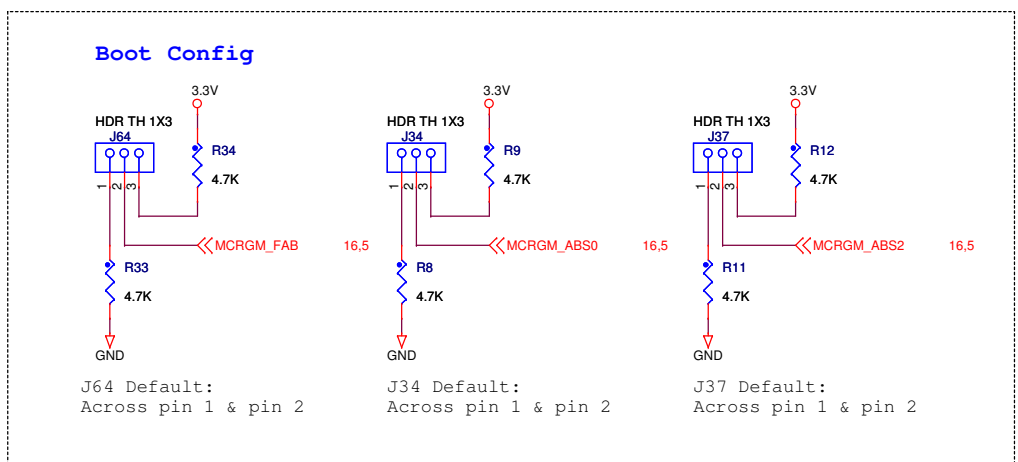
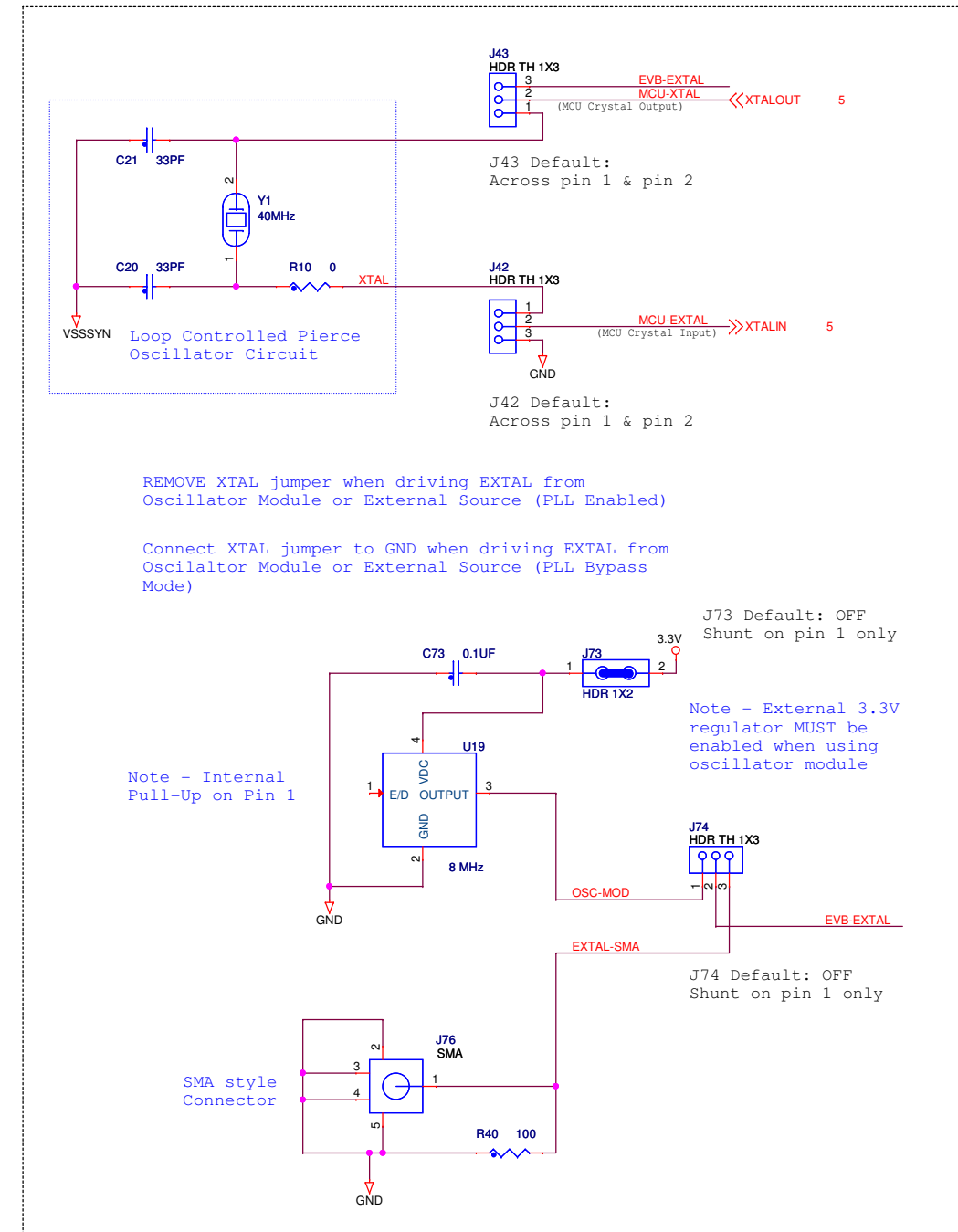
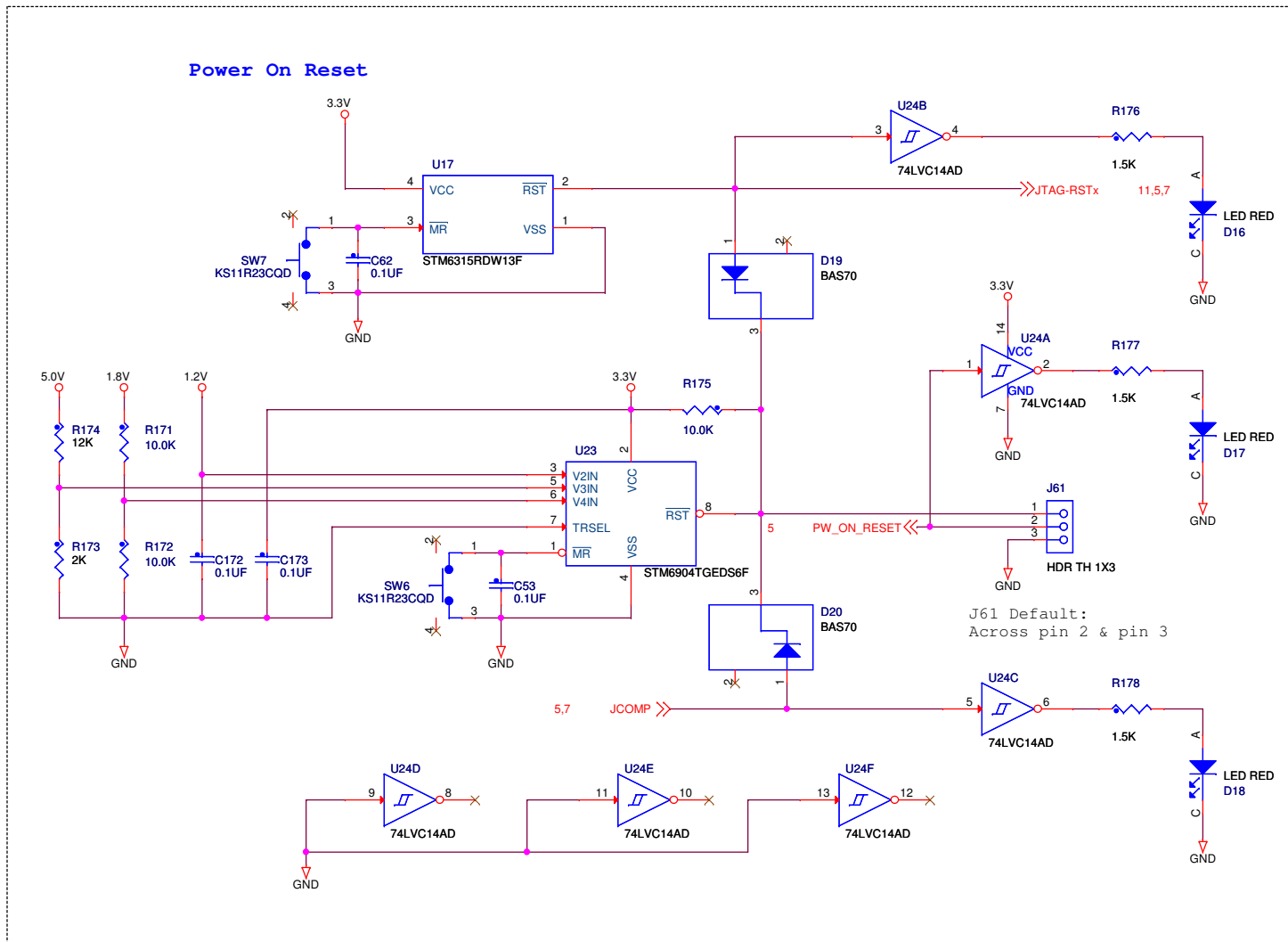
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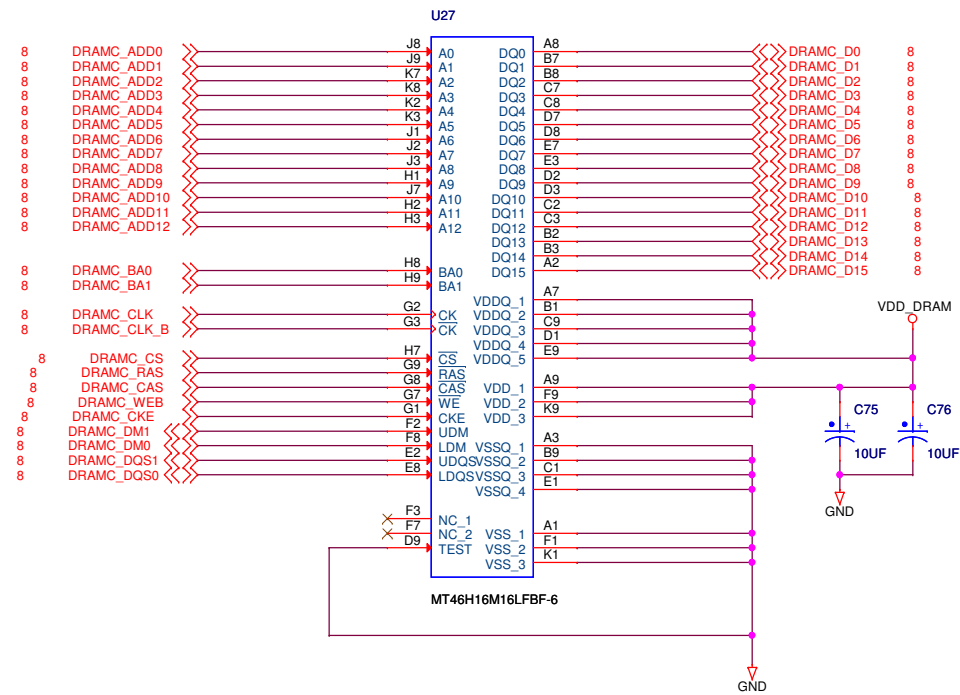
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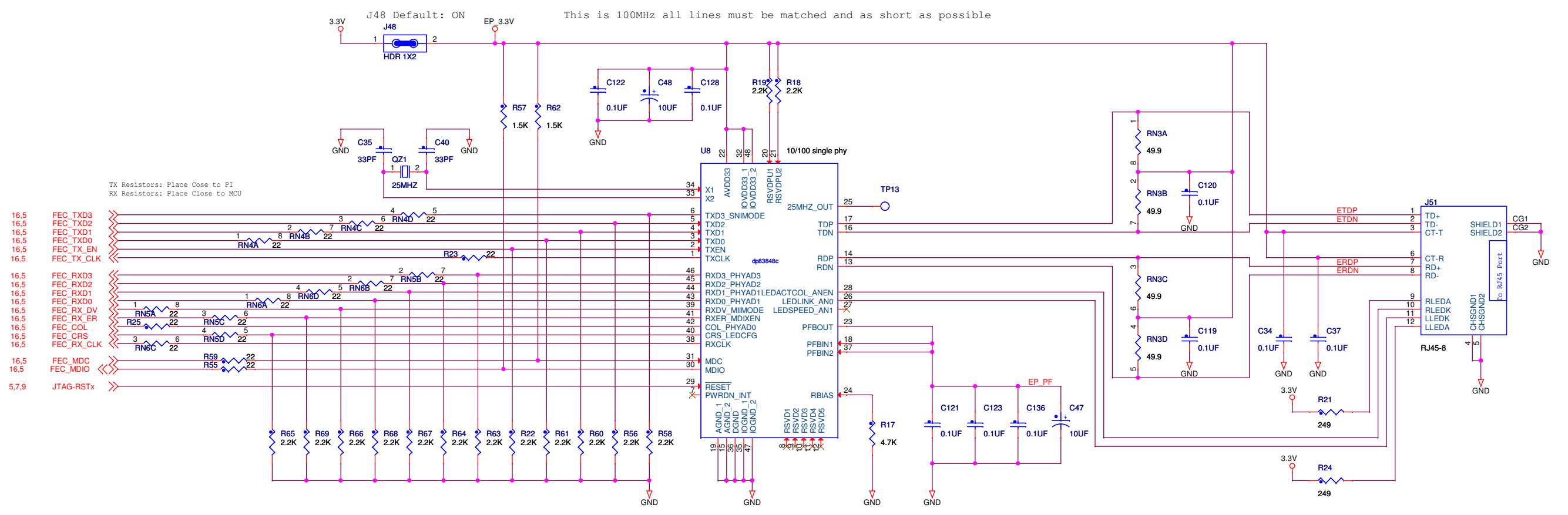
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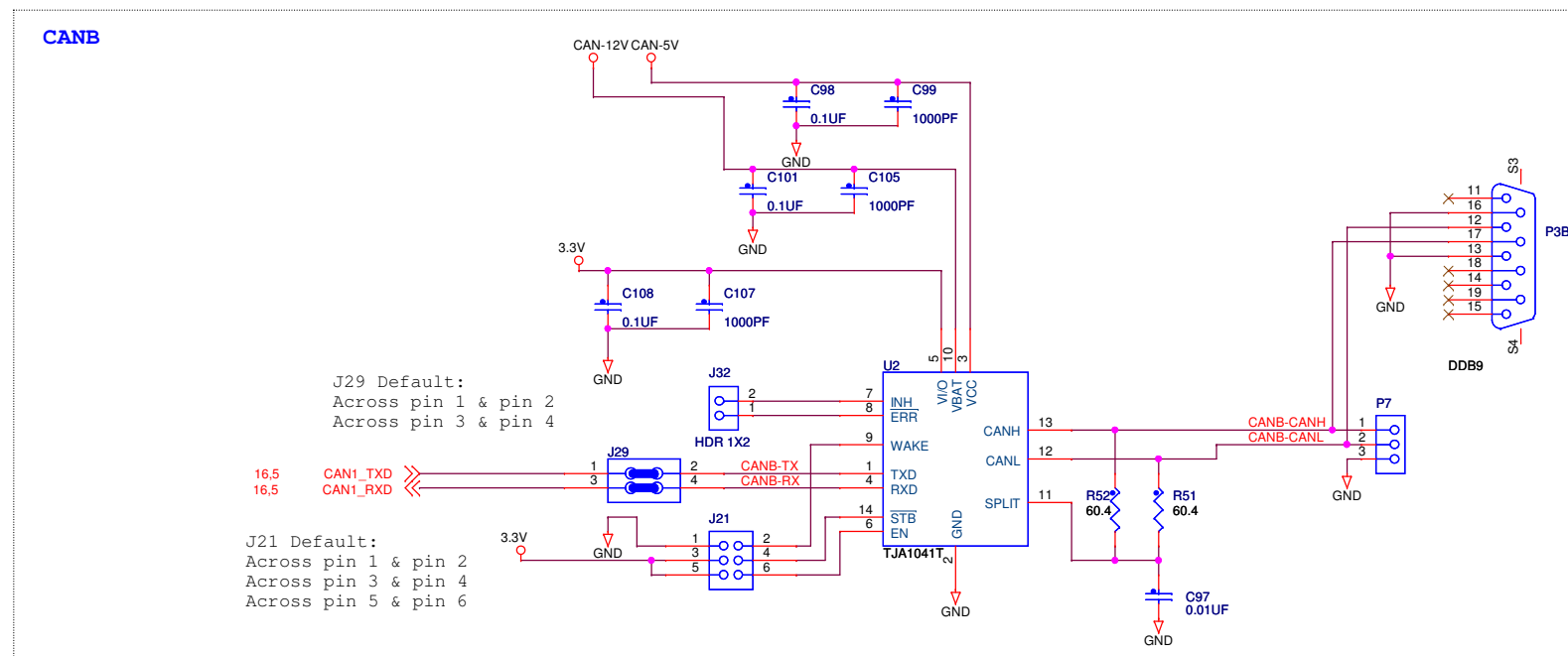
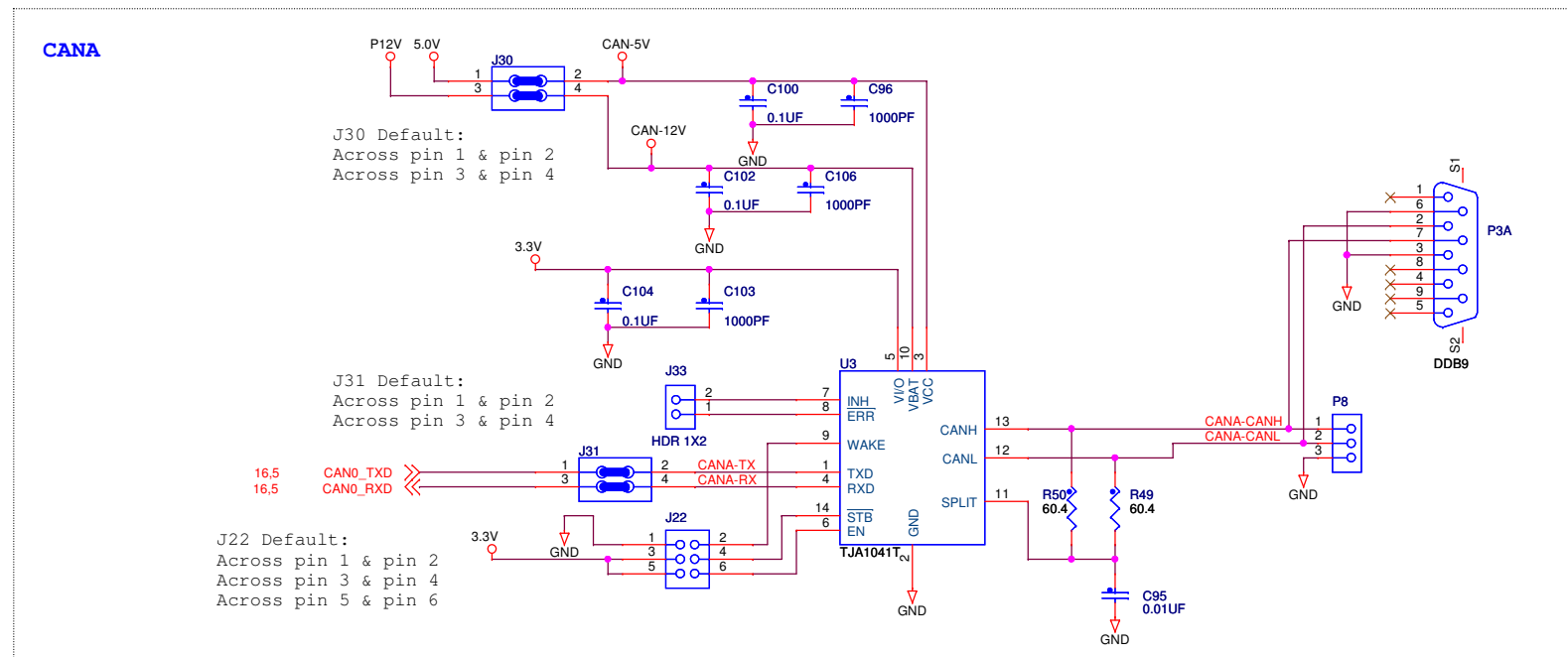






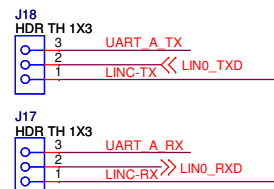




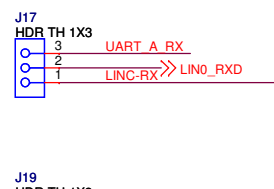


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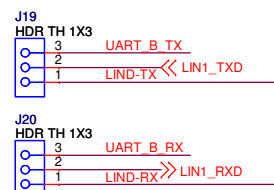
J18 Default:
Across pin 2 & pin 3



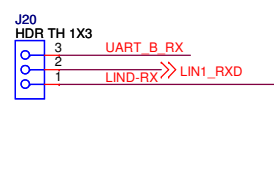
J17 Default:
Across pin 2 & pin 3



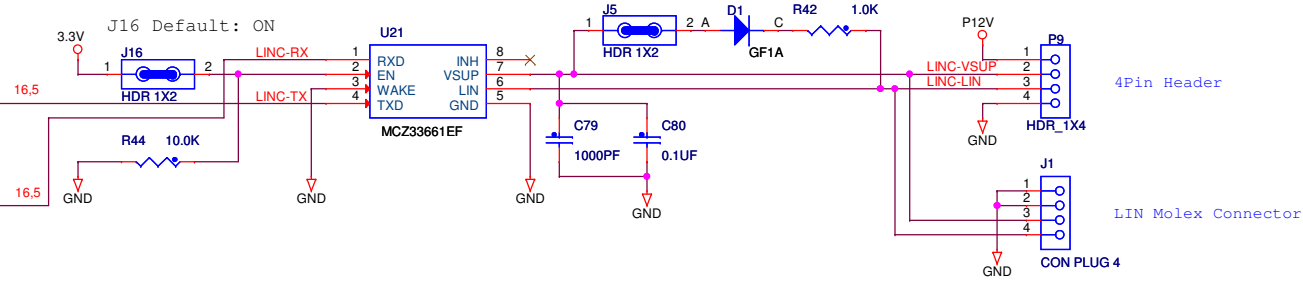
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Across pin 2 & pin 3



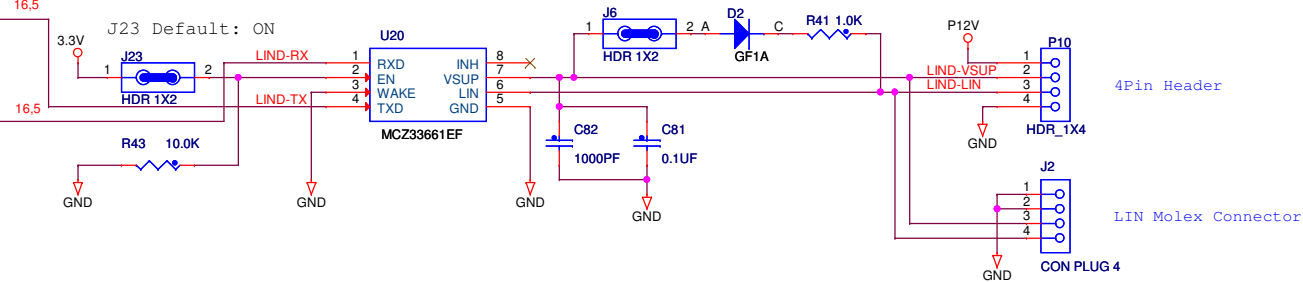
J20 Default:
Across pin 2 & pin 3



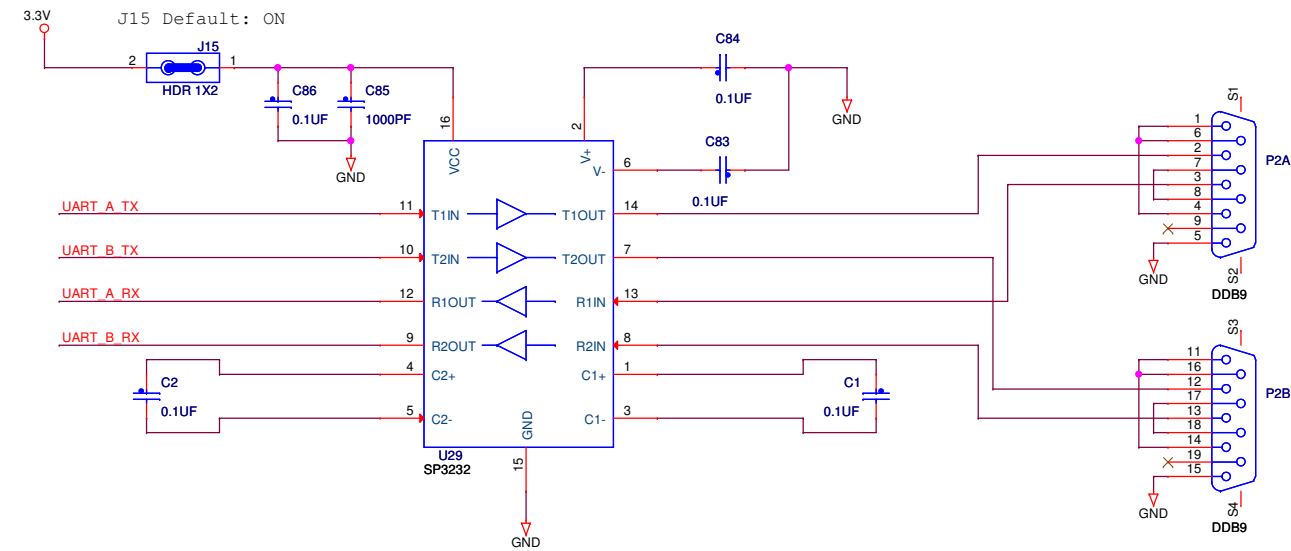
J5 Default: ON Master Mode Pullup Enable

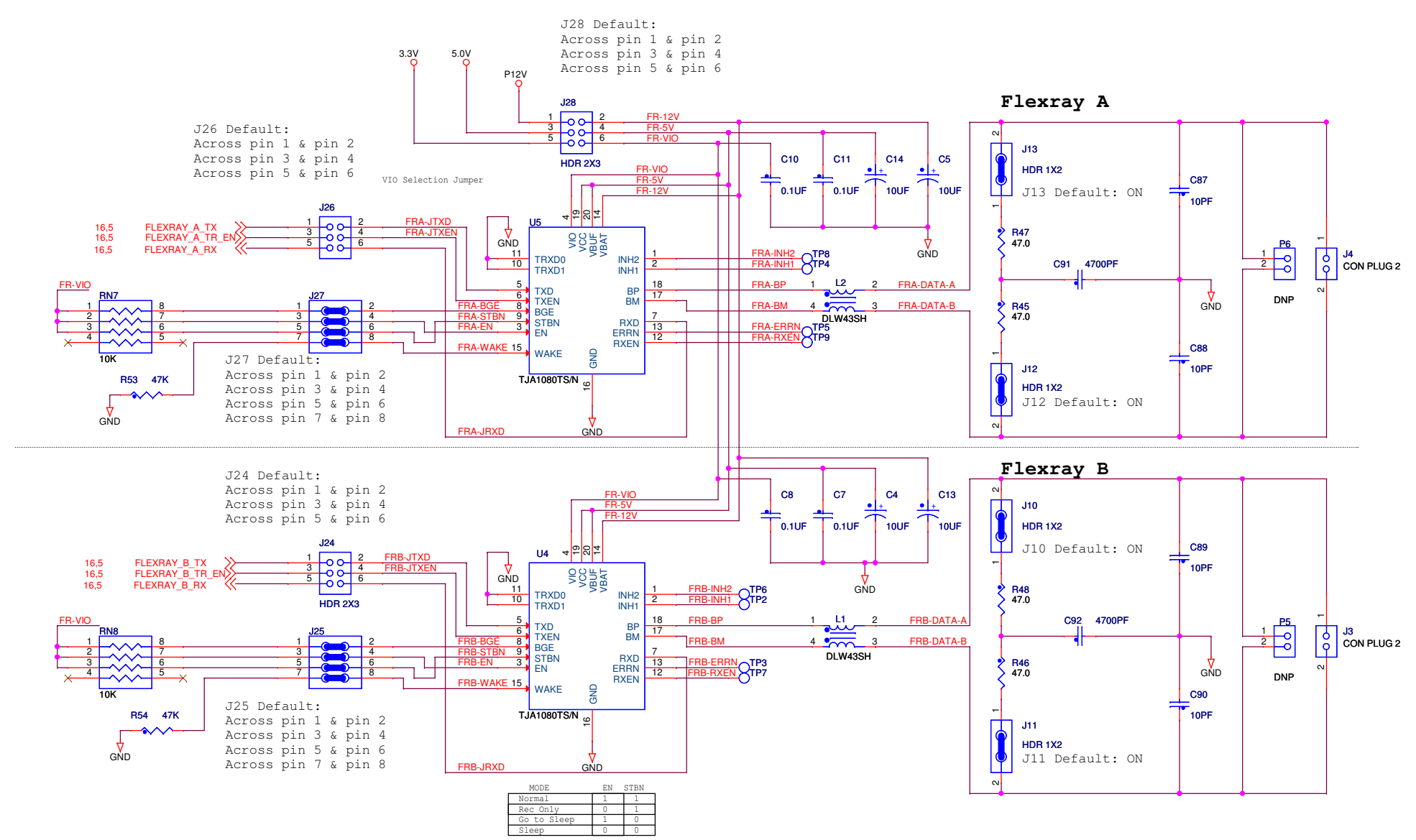


J6 Default: ON Master Mode Pullup Enable

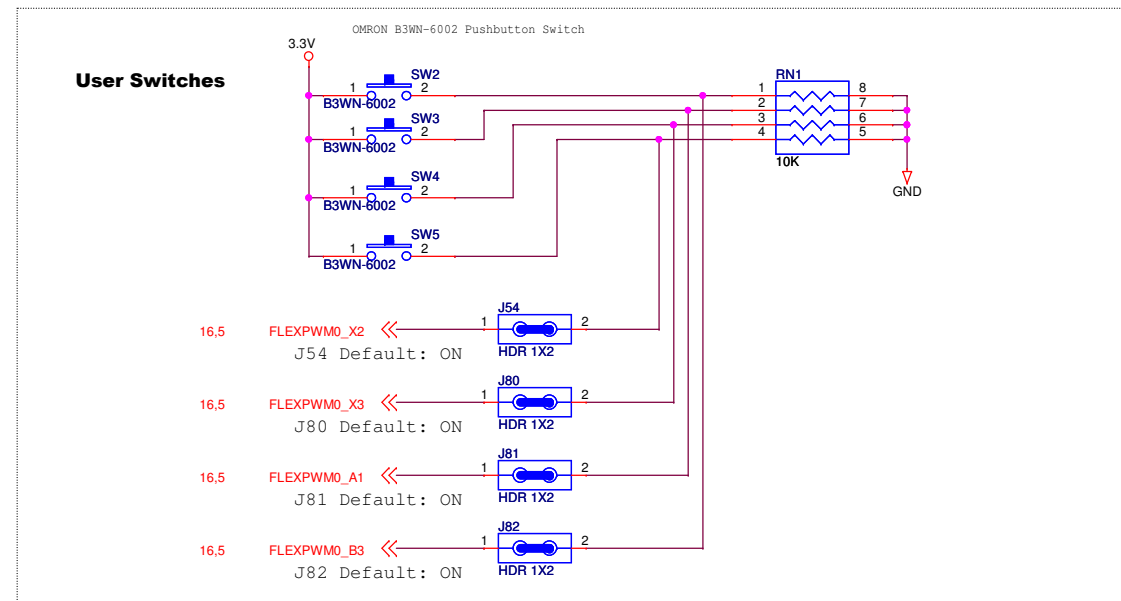
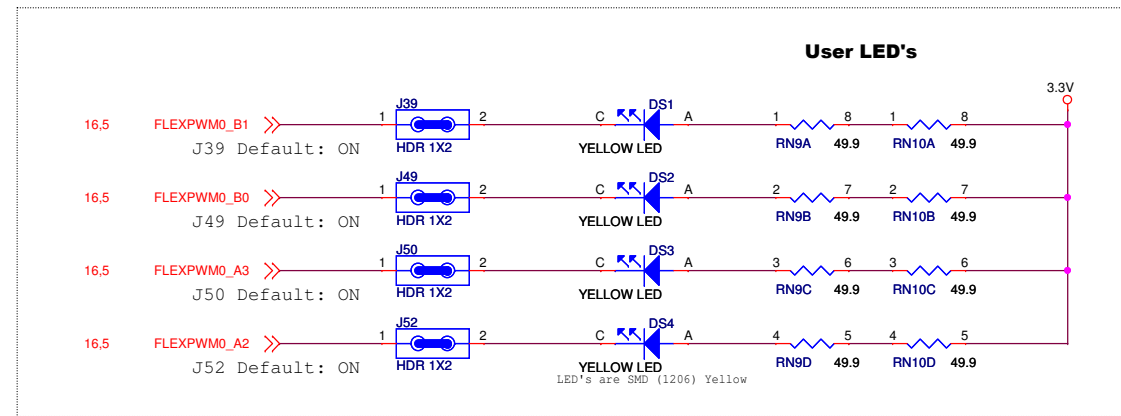


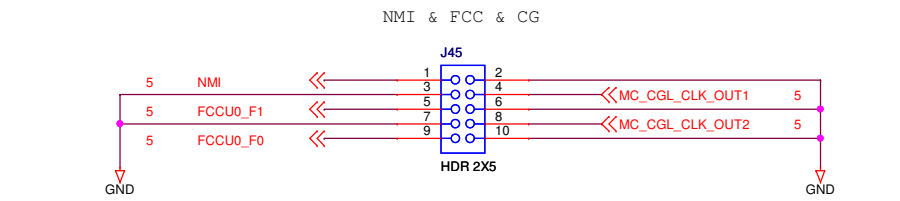
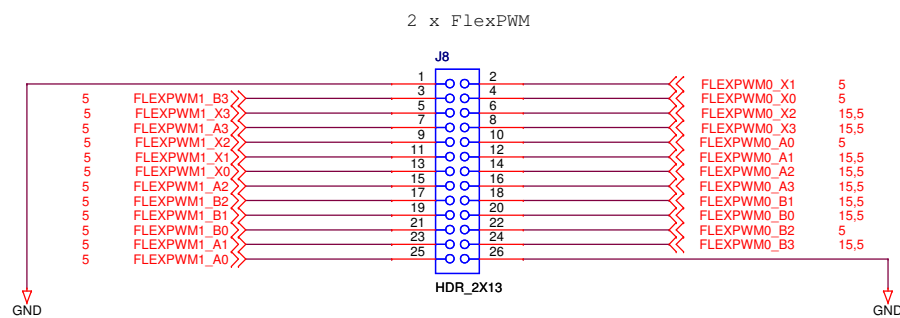
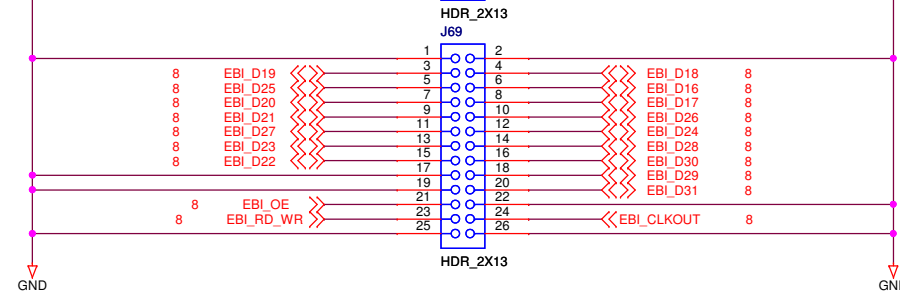
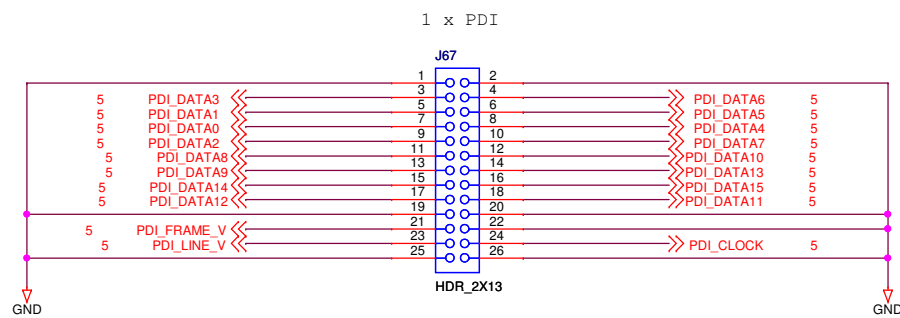
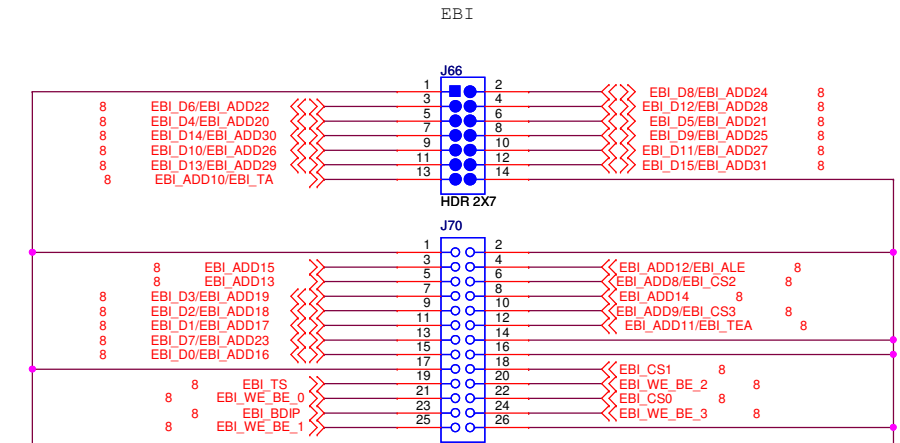
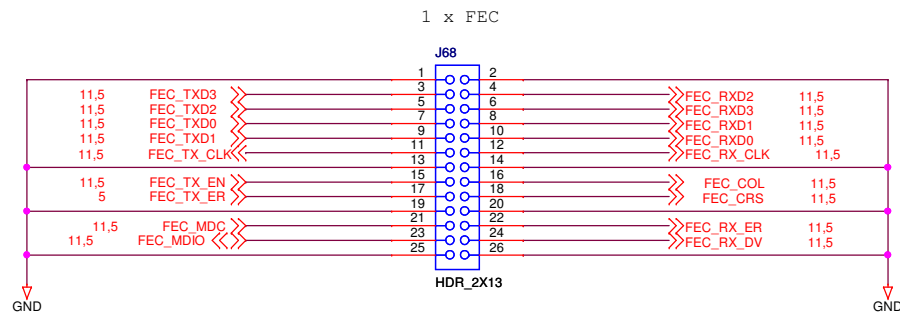
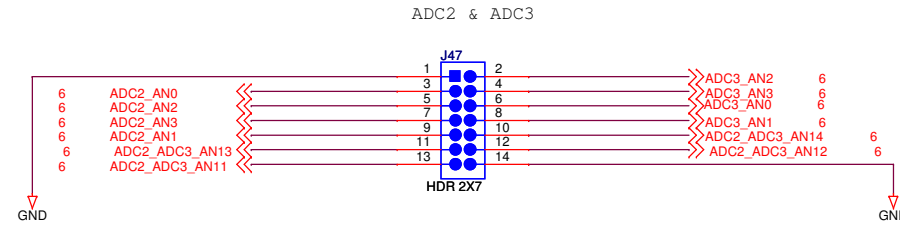
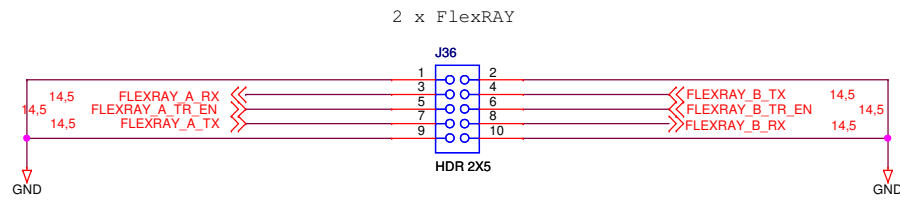
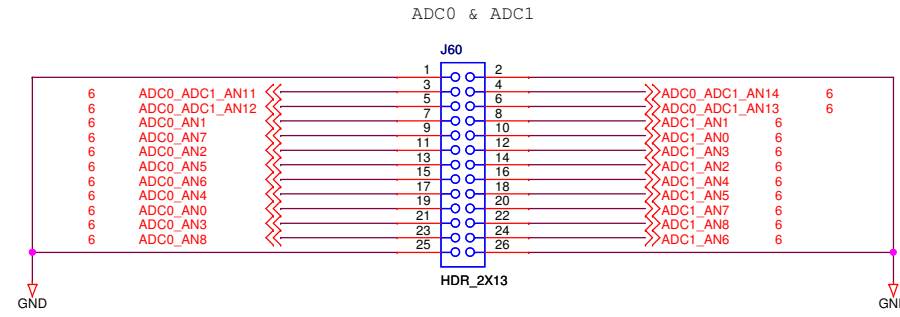
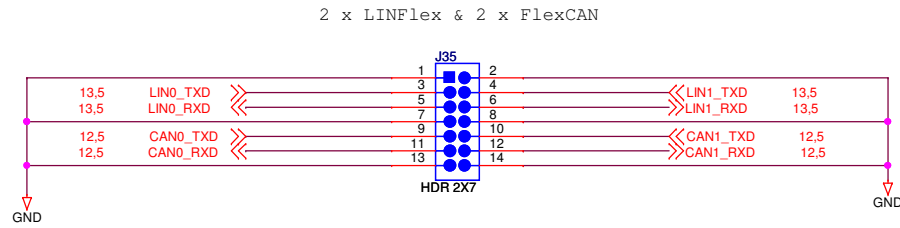
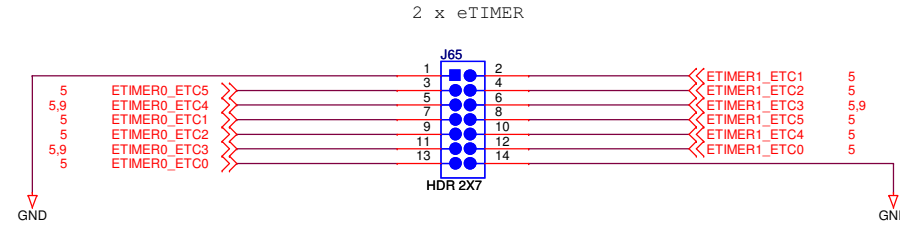
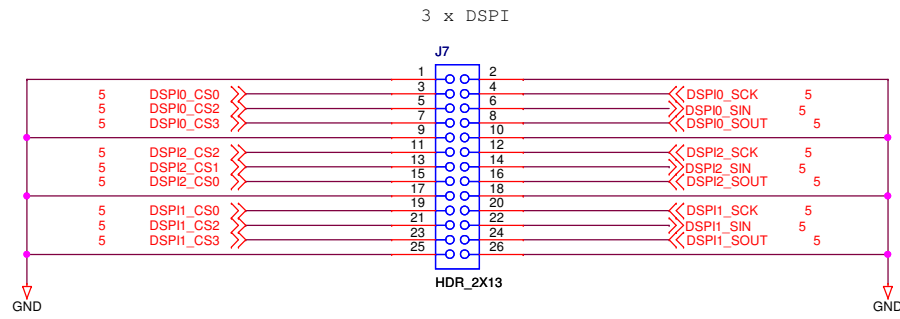
SCI





MODE	EN	STBN
Normal	1	1
Rec Only	0	1
Go to Sleep	1	0
Sleep	0	0





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