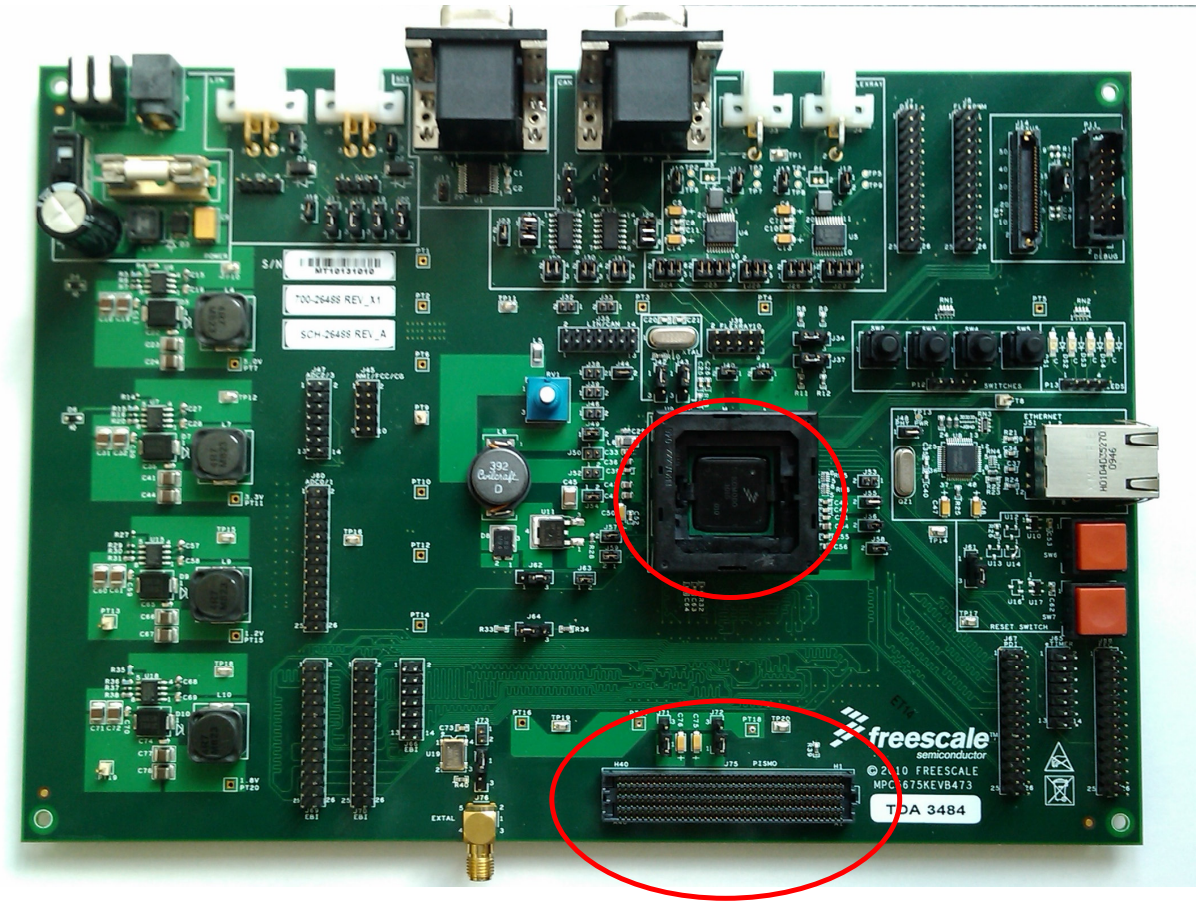
User's Attention Sheet

The DRAMC interface on the MPC5675K EVB may have some timing restrictions. The DRAM modules are connected via a PISMO connector to the MCU situated in the BGA socket. Both connectors have parasitic inductance and capacitance that when high speed signal pass through them, can potentially inducing volatility of the impedance of DDR traces which may increase reflection and noise.

Due to this configuration, the timing of the DDR modules may need adjusting to compensate for the potential timing restrictions. All reasonable precautions have been taken to ensure this feature functions correctly, but cannot be guaranteed."

This problem is removed when the MCU and DRAM is solder directly on to the PCB.



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