Document Number: SGTL5000ER
Rev. 2.0, 6/2013

SGTL5000 Silicon Errata

Introduction

Device Revision Identification

This errata document applies to the following devices:

Table 1. Silicon Revision

Part Number	Package	Silicon Revision
SGTL5000XNLA3	20QFN 3x3	ALL
SGTL5000XNAA3	32QFN 5x5	ALL
SGTL5000XNLA3R2	20QFN 3x3	ALL
SGTL5000XNAA3R2	32QFN 5x5	ALL

General Description

This errata document applies to SGTL5000 series.

Table 2. Definitions of Errata Severity

Errata Level	Meaning
High	Failure mode that severely inhibits the use of the device for all or a majority of intended applications.
Medium	Failure mode that might restrict or limit the use of the device for all or a majority of intended applications.
Low	Unexpected behavior that does not cause significant problems for the intended applications of the device.
Enhancement	Improvement made to the device due to previously found issues on the design.

Table 3. Errata for the SGTL5000

Errata No.	Erratum	System Impact	Description
Medium Severity			
ER1	Internal V_{DDD} regulator does not start up	Cannot communicate with IC.	**Issue:** On some very rare combinations of parts and application boards, and on a very small percentage of those rare part/board combinations, sometimes the V_{DDD} internal regulator does not start up after IC power-up. This can occur at any V_{DDIO} and V_{DDA} voltage level, and on either the QFN20 or QFN32 part. The failure is a function of board design and the slew rates of the power supplies, V_{DDIO} and V_{DDA}. The failure does not occur if an external regulator is used to supply V_{DDD}. **Result:** The most noticeable symptom is that no IC communication/control occurs, and that the I^2C bus lines are held in a low state. Power must be cycled to attempt another power-up, and to attempt to regain IC communication. Note that the same applies for SPI communication. **Workarounds:** New Designs Use an external supply in the system or a separate regulator to supply V_{DDD}. This V_{DDD} supply must be between 1.1 V and 2.0 V, and must source at least 11 mA of current. A 0.1 μF cap should also be added from V_{DDD} to ground when V_{DDD} is supplied externally. In order to save power, the LINREG_D_POWERUP, LINREG_SIMPLE_POWERUP, and STARTUP_POWERUP bits in register 0x0030/CHIP_ANA_POWER should be cleared after IC power-up, and after the application of the external V_{DDD} voltage. If power savings is not a concern, this software change is not required. The preferred supply sequencing is V_{DDIO}/V_{DDA} (it does not matter which comes first) and then V_{DDD}. Existing Designs For existing designs, if you have not experienced the issue to date, you likely will not. As stated previously, the issue requires the right combination of application board and part, and the right combination is very rare. If you are not planning a new board design, you can decrease the likelihood of seeing the issue by ramping both V_{DDIO} and V_{DDA} up in less than 1.0 ms. If V_{DDIO} and V_{DDA} are separate supplies, ramp V_{DDIO} up first. Any “soft-start” supply mechanisms for V_{DDIO}/V_{DDA} should be disabled, and any large caps on V_{DDIO}/V_{DDA} that are not absolutely necessary should be removed, as long as there is no adverse effect on product performance. If a new board pass is planned, follow the steps in the “New Designs” section and use an external V_{DDD}, as the external V_{DDD} fix is the only solution that is guaranteed to solve the issue 100% of the time. Note that the potential failure rate of an existing design in the field cannot be determined. **Fix Plan/Status:** No fix scheduled.

Revision History

Revision	Date	Description
1.0	10/2012	• Initial release
2.0	6/2013	• Better clarified the erratum ER1

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