Design Guideline

PTN36502 USB Type-C USB3.1 Gen 1 and DisplayPort v1.2 Combo Re-driver Design Guideline

Rev. 0.1 – August 10, 2017

Document information

Info	Content
Keywords	PTN36502, PTN5150A, PTN5110, NX5P3090, USB Type-C, CC Logic, Orientation Detection, USB3.1 Gen1, SuperSpeed, DisplayPort, Redriver
Abstract	This user manual presents demonstration / application board capability of interfacing an USB3.0 xHCI controller to USB Type-C port. The application board is intended for use as an evaluation and customer demonstration tool, as well as a reference design.

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Revision history

Rev	Date	Description
0.1	05/01/2017	Initial release

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1. Introduction

PTN36502 is a Type-C USB3.0/ DP1.2 combo re-driver that is optimized for USB3 and DisplayPort applications on either the Downstream Facing Port (DFP) or Upstream Facing Port (UFP) by following the 4 high speed differential data flow to extend the signal reach.

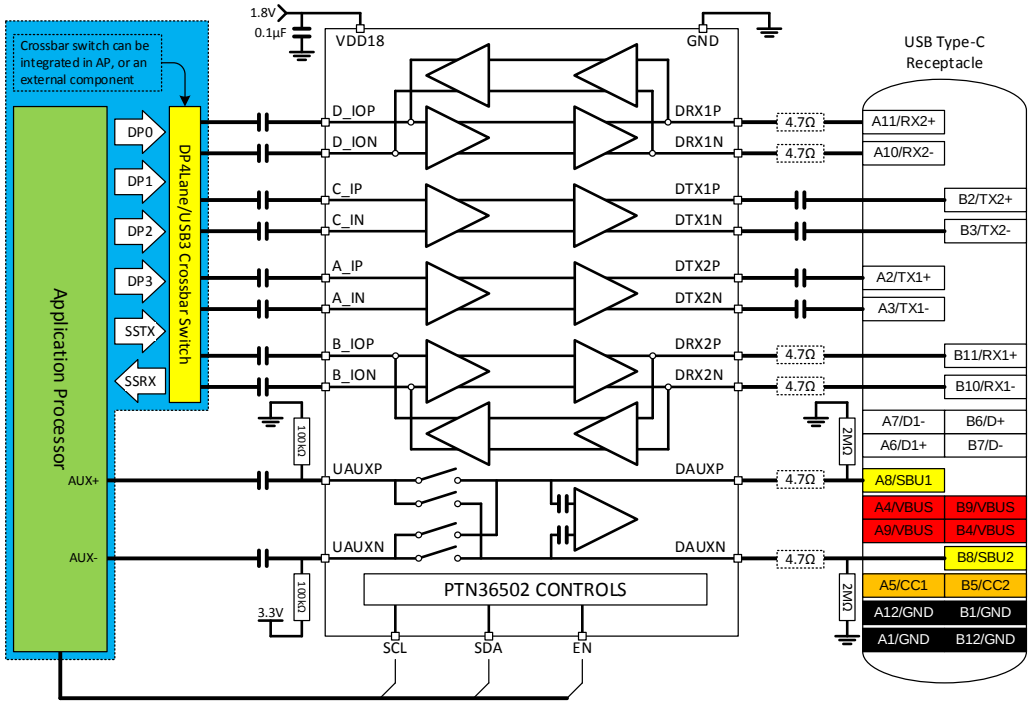
PTN36502 can be used in different system configurations (DFP, UFP or Dongle), and can be configured through I^2C or GPIO mode. This document discusses in details how each design can be achieved, in terms of schematics and layout.

2. Different Configurations (DFP/UFP/Dongle)

PTN36502 can be used in a DFP, UFP, or Dongle system. In each configuration, each pin has its specific connection in the system.

2.1. DFP (Down Facing Port) System

A DFP system usually consists of a USB3 xHCI controller and/or a DisplayPort signal source such as a GPU. PTN36502 should be placed between the xHCI controller/GPU and the Type-C connector.



2.1.1 High Speed Switches

PTN36502 itself does not have any built-in switch to select USB3 or DisplayPort signals. In the system diagram above, assuming USB3 and DisplayPort signals are multiplexed properly by high-speed switches, either internally in the chipset, or thru external components on the PCB. The switches can be configured for standard Type-C signal definition with orientation flipping. If the application processor and/or GPU don't have multiplexer integrated, NXP has the following high speed switches available for selection

- Simple 2:1 switch: CBTU02043, CBTL01023, CBTL02043, CBTL04083
- Integrated Type-C switch: CBTL08GP053

2.1.2 AC Capacitor Location

Due to the fact that the TX or RX common mode voltage of PTN36502 might be different from the chipset's or device's voltage, AC caps should be placed on all high speed lanes on the left side of PTN36502 (A_IN, B_IO, C_IN, and D_IO pins). The right side of the PTN36502 are connected to Type-C connector, and the AC caps are placed according to the Type-C standard guidelines.

2.1.3 Connection to Chipset

As indicated in the datasheet, left side of PTN36502 is connected to the chipset or application processor, with specific function assigned to each pin. The designer should match the function of each pin.

PTN36502 pins		**Application processor signal names**					
Symbol	**Pin name**	**USB3**		**USB3 & DP2Lane**		**DP4Lane**	
		Normal	**Reversed**	**Normal**	**Reversed**	**Normal**	**Reversed**
23	D_ION		SSRX-	ML0-	SSRX-	ML0-	ML3-
24	D_IOP		SSRX+	ML0+	SSRX+	ML0+	ML3+
3	C_INP		SSTX+	ML1+	SSTX+	ML1+	ML2+
4	C_INN		SSTX-	ML1-	SSTX-	ML1-	ML2-
5	A_INP	SSTX+		SSTX+	ML1+	ML2+	ML1+
6	A_INN	SSTX-		SSTX-	ML1-	ML2-	ML1-
9	B_IOP	SSRX+		SSRX+	ML0+	ML3+	ML0+
10	B_ION	SSRX-		SSRX-	ML0-	ML3-	ML0-
7	UAUXP			AUX+	AUX+	AUX+	AUX+
8	UAUXN			AUX-	AUX-	AUX-	AUX-

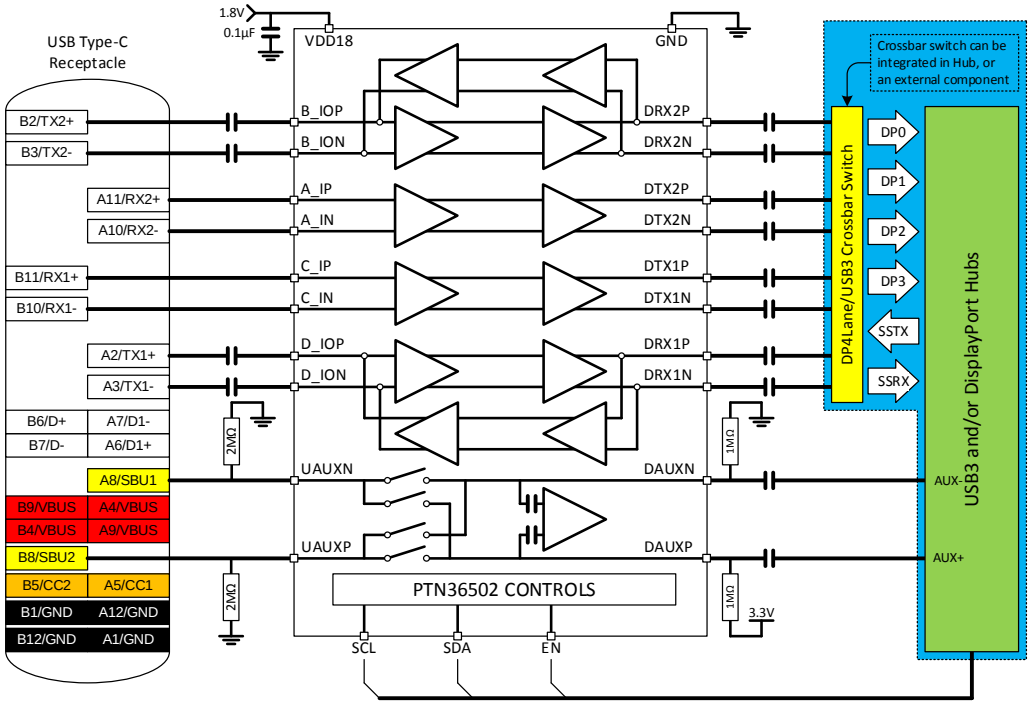
2.1.4 Connection to Type-C

As indicated in the datasheet, right side of PTN36502 is connected to the Type-C connector with specific pin assignment. Also, the AC caps are placed on the TX1 and TX2 pins per Type-C standard guidelines.

PTN36502 pins		USB Type-C receptacle pins	
Symbol	**Pin name**	**Symbol**	**Pin name**
22	DRX1P	A11	RX2+
21	DRX1N	A10	RX2-
18	DTX1N	B3	TX2-
17	DTX1P	B2	TX2+
16	DTX2P	A2	TX1+
15	DTX2N	A3	TX1-
12	DRX2N	B10	RX1-
11	DRX2P	B11	RX1+
14	DAUXP	A8	SBU1
13	DAUXN	B8	SBU2

2.2. UFP (Up Facing Port) System

A UFP system usually consists of a USB3 hub and/or a DisplayPort sink. PTN36502 should be placed between the Type-C connector and the USB3 Hub/DisplayPort sink.



2.2.1 High Speed Switches

PTN36502 itself does not have any built-in switch to select USB3 or DisplayPort signals. In the system diagram above, assuming USB3 and DisplayPort signals are multiplexed properly by high-speed switches, either internally in the chipset, or thru external components on the PCB. The switches can be configured to route USB3 and DisplayPort signals to the proper locations, based on Type-C signal definition with orientation flipping. If the USB3 hub and/or DisplayPort GPU don't have multiplexer integrated, NXP has the following high speed switches available for selection

- Simple 2:1 switch: CBTU02043, CBTL01023, CBTL02043, CBTL04083
- Integrated Type-C switch: CBTL08GP053

2.2.2 AC Capacitor Location

Due to the fact that the TX or RX common mode voltage of PTN36502 might be different from the chipset's or device's voltage, AC caps should be placed on all high speed lanes on the right side of PTN36502 (DTX1, DTX2, DRX1, DRX2 pins). The left side of the PTN36502 are connected to Type-C connector, and the AC caps are placed according to the Type-C standard guidelines.

2.2.3 Connection to USB3 Hub/ DisplayPort Sink

As indicated in the datasheet, right side of PTN36502 is connected to the chipset or application processor, with specific function assigned to each pin. The designer should match the function of each pin.

PTN36502 pins		Signal names					
Symbol	Pin name	USB3		USB3 & DP2Lane		DP4Lane	
		Normal	Reversed	Normal	Reversed	Normal	Reversed
22	DRX1P	SSTX+		SSTX+	ML0+	ML3+	ML0+
21	DRX1N	SSTX-		SSTX-	ML0-	ML3-	ML0-
18	DTX1N	SSRX-		SSRX-	ML1-	ML2-	ML1-
17	DTX1P	SSRX+		SSRX+	ML1+	ML2+	ML1+
16	DTX2P		SSRX+	ML1+	SSRX+	ML1+	ML2+
15	DTX2N		SSRX-	ML1-	SSRX-	ML1-	ML2-
12	DRX2N		SSTX-	ML0-	SSTX-	ML0-	ML3-
11	DRX2P		SSTX+	ML0+	SSTX+	ML0+	ML3+
14	DAUXP			AUX+	AUX+	AUX+	AUX+
13	DAUXN			AUX-	AUX-	AUX-	AUX-

2.2.4 Connection to Type-C

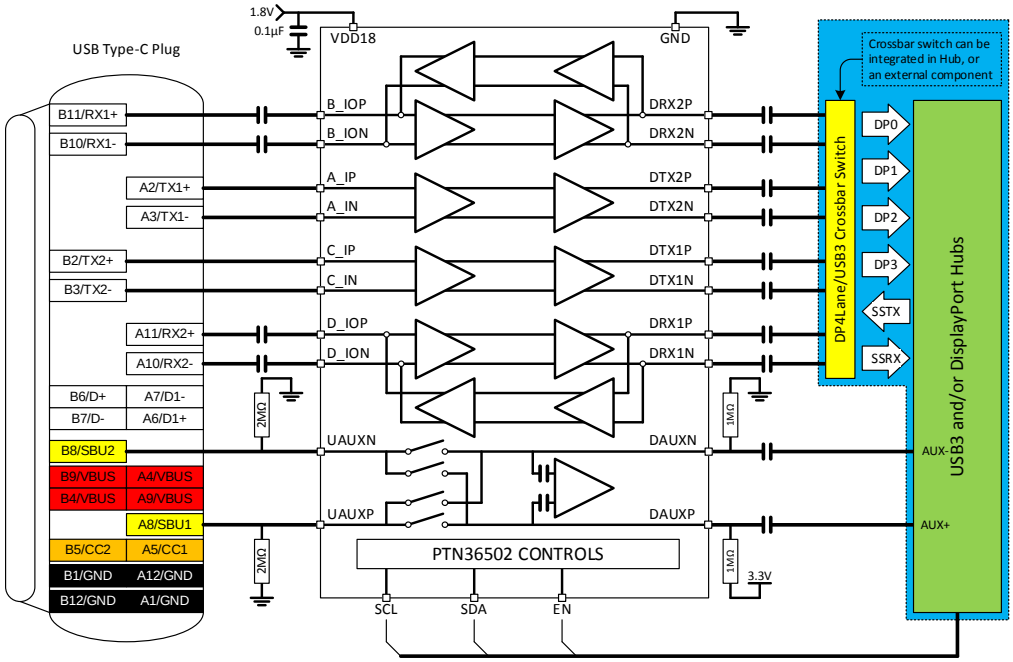
As indicated in the datasheet, left side of PTN36502 is connected to the Type-C connector with specific pin assignment. Also, the AC caps are placed on the TX1 and TX2 pins per Type-C standard guidelines.

PTN36502 pins		USB Type-C receptacle pins	
Symbol	Pin name	Symbol	Pin name
23	D_ION	A3	TX1-
24	D_IOP	A2	TX1+
3	C_INP	B11	RX1+
4	C_INN	B10	RX1-
5	A_INP	A11	RX2+
6	A_INN	A10	RX2-
9	B_IOP	B2	TX2+
10	B_ION	B3	TX2-

7	UAUXP	B8	SBU2
8	UAUXN	A8	SBU1

2.3. Dongle System

A dongle system is very similar to UFP system, except the Type-C connector is a plug configuration instead of a receptacle configuration. A dongle usually consists of a USB3 hub and/or a DisplayPort sink. PTN36502 should be placed between the Type-C connector and the USB3 Hub/DisplayPort sink.



2.3.1 High Speed Switches

PTN36502 itself does not have any built-in switch to select USB3 or DisplayPort signals. In the system diagram above, assuming USB3 and DisplayPort signals are multiplexed properly by high-speed switches, either internally in the chipset, or thru external components on the PCB. The switches can be configured to route USB3 and DisplayPort signals to the proper locations, based on Type-C signal definition with orientation flipping. If the USB3 hub and/or DisplayPort GPU don't have multiplexer integrated, NXP has the following high speed switches available for selection

- Simple 2:1 switch: CBTU02043, CBTL01023, CBTL02043, CBTL04083
- Integrated Type-C switch: CBTL08GP053

2.3.2 AC Capacitor Location

Due to the fact that the TX or RX common mode voltage of PTN36502 might be different from the chipset's or device's voltage, AC caps should be placed on all high speed lanes on the right side of PTN36502 (DTX1, DTX2, DRX1, DRX2 pins). The left side of the PTN36502 are connected to Type-C connector, and the AC caps are placed according to the Type-C standard guidelines.

2.3.3 Connection to USB3 Hub/ DisplayPort Sink

As indicated in the datasheet, right side of PTN36502 is connected to the chipset or application processor, with specific function assigned to each pin. The designer should match the function of each pin.

PTN36502 pins		Signal names					
Symbol	Pin name	USB3		USB3 & DP2Lane		DP4Lane	
		Normal	Reversed	Normal	Reversed	Normal	Reversed
22	DRX1P		SSTX+	ML0+	SSTX+	ML0+	ML3+
21	DRX1N		SSTX-	ML0-	SSTX-	ML0-	ML3-
18	DTX1N		SSRX-	ML1-	SSRX-	ML1-	ML2-
17	DTX1P		SSRX+	ML1+	SSRX+	ML1+	ML2+
16	DTX2P	SSRX+		SSRX+	ML1+	ML2+	ML1+
15	DTX2N	SSRX-		SSRX-	ML1-	ML2-	ML1-
12	DRX2N	SSTX-		SSTX-	ML0-	ML3-	ML0-
11	DRX2P	SSTX+		SSTX+	ML0+	ML3+	ML0+
14	DAUXP			AUX+	AUX+	AUX+	AUX+
13	DAUXN			AUX-	AUX-	AUX-	AUX-

2.3.4 Connection to Type-C

As indicated in the datasheet, left side of PTN36502 is connected to the Type-C connector with specific pin assignment. Also, the AC caps are placed on the TX1 and TX2 pins per Type-C standard guidelines.

PTN36502 pins		USB Type-C receptacle pins	
Symbol	Pin name	Symbol	Pin name
23	D_ION	A10	RX2-
24	D_IOP	A11	RX2+
3	C_INP	B2	TX2+
4	C_INN	B3	TX2-

5	A_INP	A2	TX1+
6	A_INN	A3	TX1-
9	B_IOP	B11	RX1+
10	B_ION	B10	RX1-
7	UAUXP	A8	SBU1
8	UAUXN	B8	SBU2

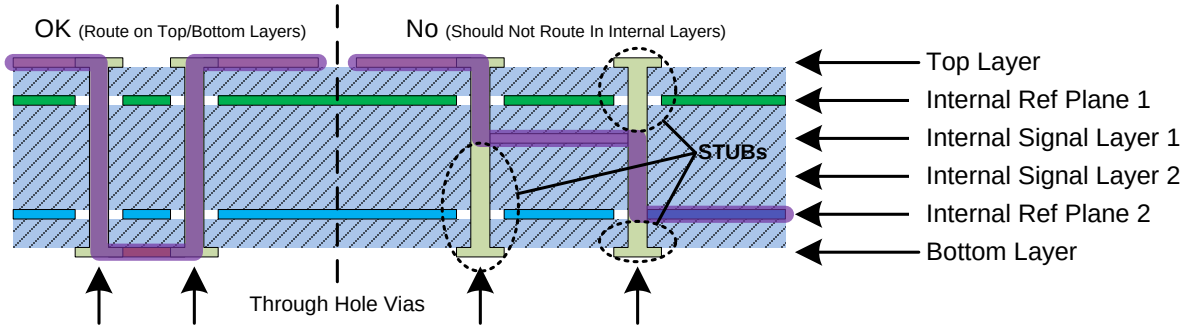
3. Layout Guidelines

3.1. General Differential Layout Guideline

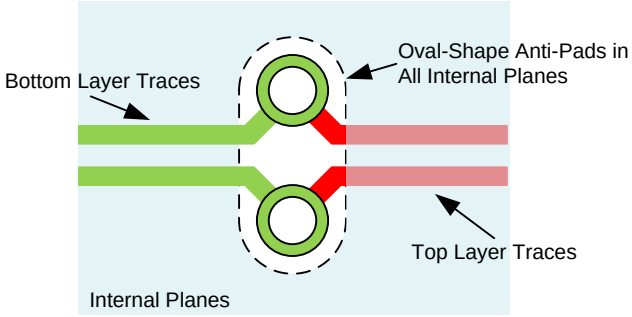
Please refer to AN10798 for general differential layout guidelines.

High speed transmission lines need to be designed with impedance matching in mind. For USB3 and DisplayPort signals, the traces should be designed with 90Ω differential impedance. Signal trace length within the same differential pair should be equal. If it is difficult to achieve exact same length within the same differential pair, the mismatch in length should be minimized to no more than 3 mils.

High speed signals should be routed over the top or bottom layer of a multi-layer PCB because signals travel faster on the buried microstrips than striplines. These signals should also not to be routed on the internal power/ground layers, or in the internal signal layers to avoid stubs created by the vias.



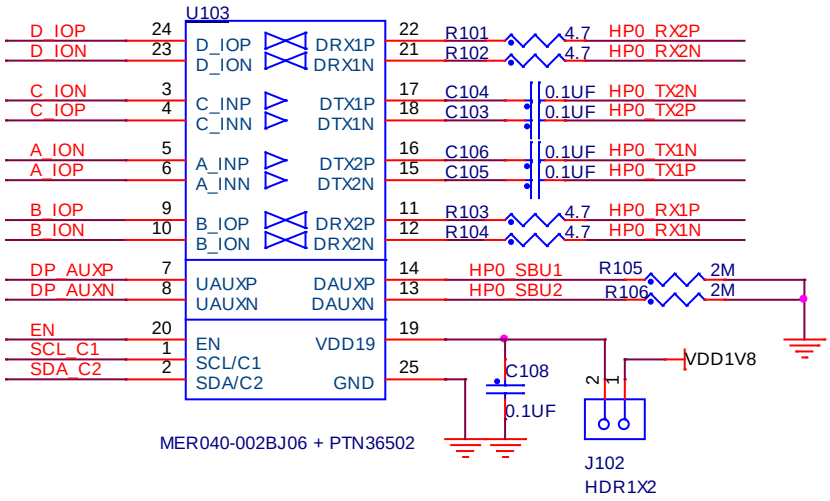
Solid internal reference ground planes should be designed immediately underneath or above the high-speed transmission lines. The distance between the two differential traces should be kept equal as long as possible. Try to avoid vias in the transmission lines themselves. If it is required to use a via, make sure the trace branches to the vias are symmetrical, and oval-shape anti-pads should be used on all internal planes for transitional vias as show in Figure 7 below.



3.2. High Speed P and N Signal Assignment

PTN36502's high speed lanes are agnostic to the polarity of the signal, and it is okay to swap the P and N signal to achieve better layout result. However, when the polarity the left side is inverted, the polarity of the corresponding signal pair on the right side should be inverted at the same time.

For example, in the schematics below, polarity assignment of pin 16 (DTX2P) and pin 15 (DTX2N) was modified to connect to net HP0_TX1N and HP0_TX1P, which is the inverted polarity assignment from the pin name. The corresponding signal pair on the left side are pin 5 (A_INP) and pin 6 (A_INN), and the polarity assignment of the signal should be inverted as well.



3.3. AUX P and N Signal Assignment

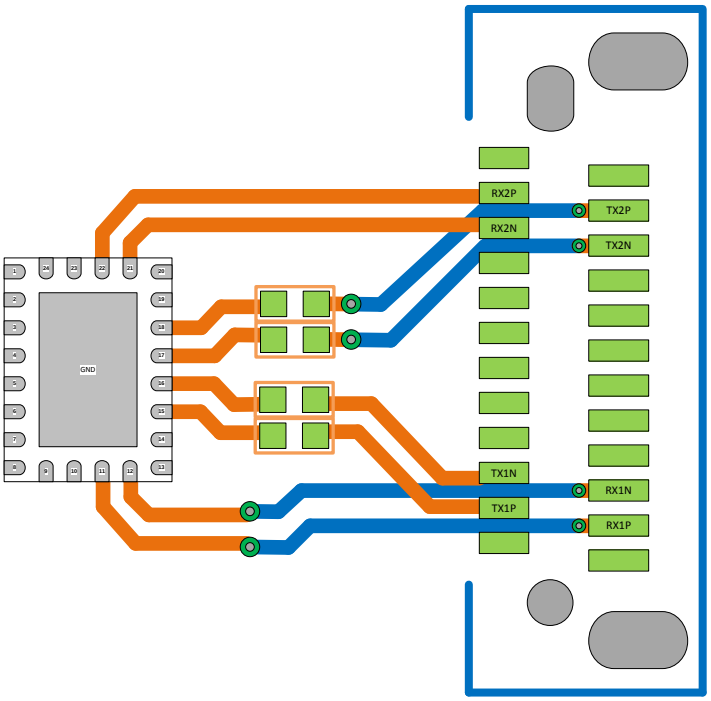
PTN36502's AUX P and N assignments (either on the upstream side or downstream side) should not be inverted. The polarity assignment should follow the signal connection suggestion in the previous section. The AUX snooping logic inside PTN36502 will decode AUX traffic based on current orientation assignment of the signal, and thus the polarity is not agnostic.

3.4. High Speed Signal Routing

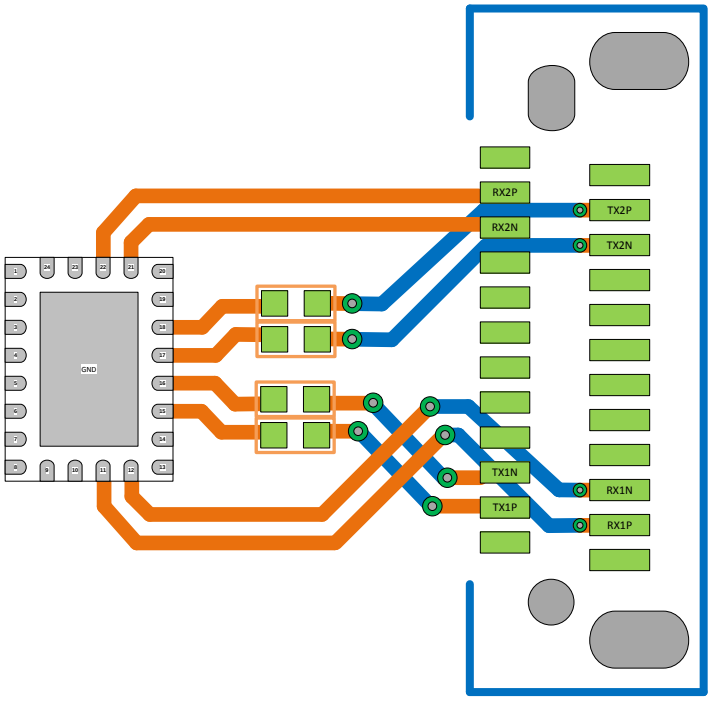
PTN36502 pin assignments are defined in such a way that connection to Type-C connector can be minimized. High speed traces should be routed between PTN36502 and Type-C connector with minimum layer transition. Whenever possible, route signals on the same layer.

In the layout example below, orange color traces are on the top layer, and blue traces are on the bottom layer. The AC caps can be placed on the same side as PTN36502, close to the chip. For traces connecting to RX2 and TX1 on the Type-C connector, the trace can be routed all on the top layer. For traces connecting to TX2 and RX1 on the Type-C connectors, because it is very difficult to fan out these signals only on the top layer, and vias are usually required. Try to minimized the

total number of vias used on the traces. Usually two vias for each trace should be enough to complete the routing.



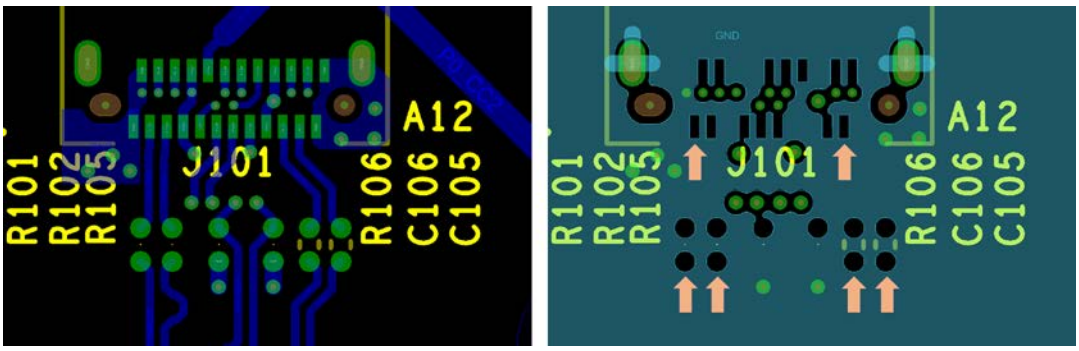
In the next layout example below, even the RX1 signal pairs are routed with minimum number of vias, but the vias are not placed at the optimum position. This layout causes TX1 signal traces to have 2 extra vias that will impact the signal integrity. This should be avoided.



3.5. Impedance Matching across the AC Capacitors

When these AC-Coupling capacitors are placed on the high-speed signals, impedance of the trace changes across these AC-Coupling capacitors. To minimize the impedance change, a void in the adjacent reference ground plane is required. The size of the void should be the same size of the capacitor's pad size.

In the below figure, the picture on the left side illustrates the top layer routing, with component pads showing in green color. The picture on the right side illustrates the inner ground layer. Directly under the component pads that are connected to high speed signals, a void with same shape and same size of the pad are created in the inner ground layer. This void can also be applied under connector pads, or PTN36502's high speed signal pin pads.



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