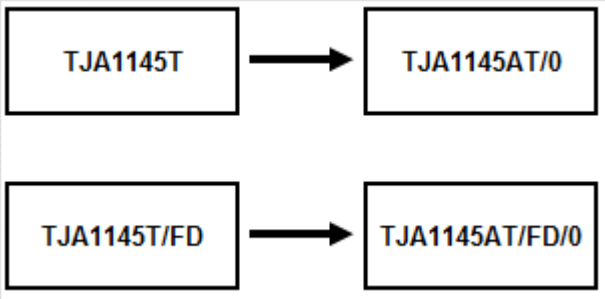
# Product Line In-Vehicle Networking (PL IVN):
# Transition from SO package product TJA1145T(/FD) to successor CAN FD drop-in replacement product TJA1145AT(/FD)

Attachment to PCN 202002034F01




Changes:

- Minor design updates in the CAN transmitter and receiver to enable additional CAN FD specifications (5 Mbit/s timing, extended bus wake-up time-out time and short Wake-Up Pattern (WUP) wake-up time)
- Minor design changes to fix four issues that could potentially affect your application (as previously communicated by NXP PL IVN CIN 201909013I from December 6 2019), and to increase robustness
- Introduction of Dual Source, waferfab Vanguard International Semiconductor Corporation (VIS) in Hsinchu, Taiwan, next to the already released wafer fab SSMC, Singapore, and the addition of a Moisture Barrier Bag (MBB) around the reel inside the 'pizza' box



Han Gerritsen
Quality Manager PL IVN
NXP Semiconductors

Building FD3.040
Gerstweg 2
6534 AE Nijmegen
The Netherlands

E-mail: ivn.customer.service@nxp.com

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## 1. Introduction

NXP Product Line In Vehicle Networking (PL IVN) informed you in December 2019 via Customer Information Notification (CIN) 201909013I of four design-related issues affecting product TJA1145. These could potentially affect your application using product TJA1145, and cause failures or customer returns.

This PCN announces the transition of the SO package product TJA1145T(/FD) to its drop-in replacement CAN FD successor product TJA1145AT(/FD), fulfilling additional CAN FD specifications as required by certain OEMs (5 Mbit/s timing, short Wake Up Pattern (WUP) wake-up time and extended bus wake-up time-out time according latest ISO 11898-2:2016 standard). In this TJA1145AT(/FD) product before-mentioned four issues have been fixed through minor design changes.

Note that in February of this year the PCN 202001016F01 for the transition of the leadless HVSON package TJA1145TK(/FD)➔TJA1145ATK(/FD) has been sent.

Three months after this PCN for the SO package product TJA1145AT(/FD), a separate formal Discontinuation Notification (DN) for the 'old' TJA1145 (both SO and leadless HVSON package product versions) will be sent, with a 1-year Last Time Buy (LTB) period, followed by a 1-year Last Time Shipment (LTS) period. This implies that you are required to act on this PCN, as you no longer can order the current TJA1145 product after this period.

## 2. Why do you get this change notification?

You get this change notification because you have bought or are still buying one or more of the NXP SO package product versions of TJA1145, i.e. TJA1145T or TJA1145T/FD.

## 3. Summary of the change

Product TJA1145T(/FD) in the SO package will be replaced by its drop-in replacement CAN FD successor TJA1145AT(/FD). The differences between the two products are:

- Minor design updates in the CAN transmitter and receiver to enable additional CAN FD specifications (5 Mbit/s timing, extended bus wake-up time-out time and short Wake-Up Pattern (WUP) wake-up time according latest ISO 11898-2:2016 standard)
- Minor design changes to fix four issues that could potentially affect your application (as previously communicated by NXP PL IVN CIN 201909013I from December 6 2019), and to increase robustness
- Introduction of Dual Source, waferfab Vanguard International Semiconductor Corporation (VIS) in Hsinchu, Taiwan, next to wafer fab SSMC, Singapore (different than for HVSON TJA1145ATK(/FD), see Appendix 4)
- Addition of a Moisture Barrier Bag (MBB) around the reel inside the ‘pizza’ box

For the successor CAN FD product TJA1145AT the following is available:

- A new datasheet, with improved/expanded/additional CAN FD specifications (attached to this PCN)
- An AEC-Q100 Qualification results report (attached to this PCN)
- On request a PPAP for TJA1145AT(/FD) with a.o. new:
    - EMC reports for both ‘classic’ CAN and CAN FD
    - ESD report
    - Electrical Distribution (ED) report
    - C&S CAN Conformance Test report
    - Application Hints

For the transition TJA1145T(/FD)➔TJA1145AT(/FD) there are no other changes than the 4 items in the boxed text above:

- No change in package outline or dimension ➔ no change in PCB footprint
- No change in leadframe ➔ no change in solderability
- No change in Bill of Material (BoM)
- Single change in manufacturing site, addition of VIS, Taiwan wafer fab next to SSMC, Singapore wafer fab
- No change in manufacturing flow:
    - No change in diffusion process
    - No change in assembly site and process
    - No change in wafer- or final test site, process or program, with the single exception of tests to verify compliance to the improved/expanded/additional CAN FD specifications
- No change in packing, shipping, labeling, other than the addition of a MBB (Moisture Barrier Bag)
- The above-mentioned minor design updates/changes are made with:
    - No change in die size (or thickness)
    - No change in product floorplan➔no change in location of I/O cells, functional IP blocks, ESD protections, etc.
    - No change in design rules
    - No addition of, and no removal of IP blocks
    - Only minor design changes in CAN transmitter, receiver, and ISR IP blocks, and digital circuitry

The previous page gives a high-level summary of the transition TJA1145T(/FD)➔TJA1145AT(/FD) that this PCN is about. In the rest of this document more detailed information is provided. You are not required to read all this detailed information, it is provided to enable you to find the answer to specific questions you might have. To facilitate the search for specific information, please check the table of contents of this document at the top of the next page.

The main part of the remainder of this document is dedicated to the design issues and fixes for it, which are both explained in detail. This is done for three reasons:

- To explain in appropriate detail the underlying design root causes and the minor analogue or digital fixes for them
- To show that these issues are eliminated for TJA1145AT(/FD)
- To show that the total changes between TJA1145T(/FD) and TJA1145AT(/FD) are very small, which should enable you to use the provided appropriate AEC-Q100 qualification results to make a smooth and low-effort change-over to TJA1145AT(/FD)

Please check in any case Section 11 ‘Migration guide TJA1145➔TJA1145A’, explaining step-by-step all aspects of the switch to TJA1145A.

The qualification results for this change TJA1145T(/FD)➔TJA1145AT(/FD) are described in the reliability report that is attached to this PCN. You can obtain this report in the same way as you obtained this document. TJA1145AT(/FD) samples can be obtained via your NXP sales contact. TJA1145AT(/FD) production orders can be placed, using the new NXP 12NC ordering codes described in this document.

You are required to act on this PCN and replace product TJA1145T(/FD) with its CAN FD successor drop-in replacement product TJA1145AT(/FD), as product TJA1145T(/FD) will be discontinued after Q4 2020 (details described in the remainder of this document).

## 4. What information is in the rest of this document?

Information on various aspects of this change, the transition from the SO package TJA1145T(/FD) to its successor CAN FD drop-in replacement TJA1145AT(/FD), can be found in the following sections:



## 5. List of TJA1145 products involved in this announcement

In Table 1 a detailed overview is given of the TJA1145 products and their successor CAN FD drop-in replacement product TJA1145A. This PCN is about the transition TJA1145T(/FD)➔TJA1145AT(/FD) for the SO package products.

| Product | Package | Current released TJA1145 products [1] | | | Successor CAN FD drop-in replacement TJA1145A | | |
|---|---|---|---|---|---|---|---|
| | | Product Type Name | Orderable part number | Ordering code (12NC) | Product Type Name | Orderable part number | Ordering code (12NC) |
| TJA1145 | SO14 | TJA1145T | TJA1145T,118 | 9352 962 07118 | TJA1145AT/0 | TJA1145AT/0Z | 9353 984 49431 |
| | | TJA1145T/FD | TJA1145T/FDJ | 9353 002 86118 | TJA1145AT/FD/0 | TJA1145AT/FD/0Z | 9353 984 54431 |

[1] See Appendix 1 for details on the definitions for Product Type Name, Orderable part number and 12NC ordering code.

**Table 1**: Overview of the TJA1145 product versions involved in this announcement, with explicit reference to the NXP Product Type Names, Orderable part numbers and 12NC ordering codes for the current products and their successor CAN FD drop-in replacement products.

The PCN 202001016F01 for the transition of the leadless HVSON package TJA1145TK(/FD) to its drop-in replacement CAN FD successor product TJA1145ATK(/FD) has been sent in February 2020.

## 6. Design changes TJA1145➔TJA1145A

Products TJA1145T(/FD) and its successor CAN FD drop-in replacement TJA1145AT(/FD) have the exact same die floorplan. There is no change in location of I/O cells, functional IP blocks, ESD protections, etc.

The products also have the same base design with only very minor changes:

- Minor design updates in the CAN transmitter and receiver to enable additional CAN FD specifications (5 Mbit/s timing and short Wake-Up Pattern (WUP) wake-up time according to the latest ISO 11898-2:2016 standard)
- Minor design changes to fix four issues that could potentially affect your application (as previously communicated by NXP PL IVN CIN 201909013I from December 6 2019), and to increase robustness

In Figure 1 below the TJA1145A die is shown. The colored blocks indicate the IP/functional blocks that contain the above-mentioned minor design updates/changes.

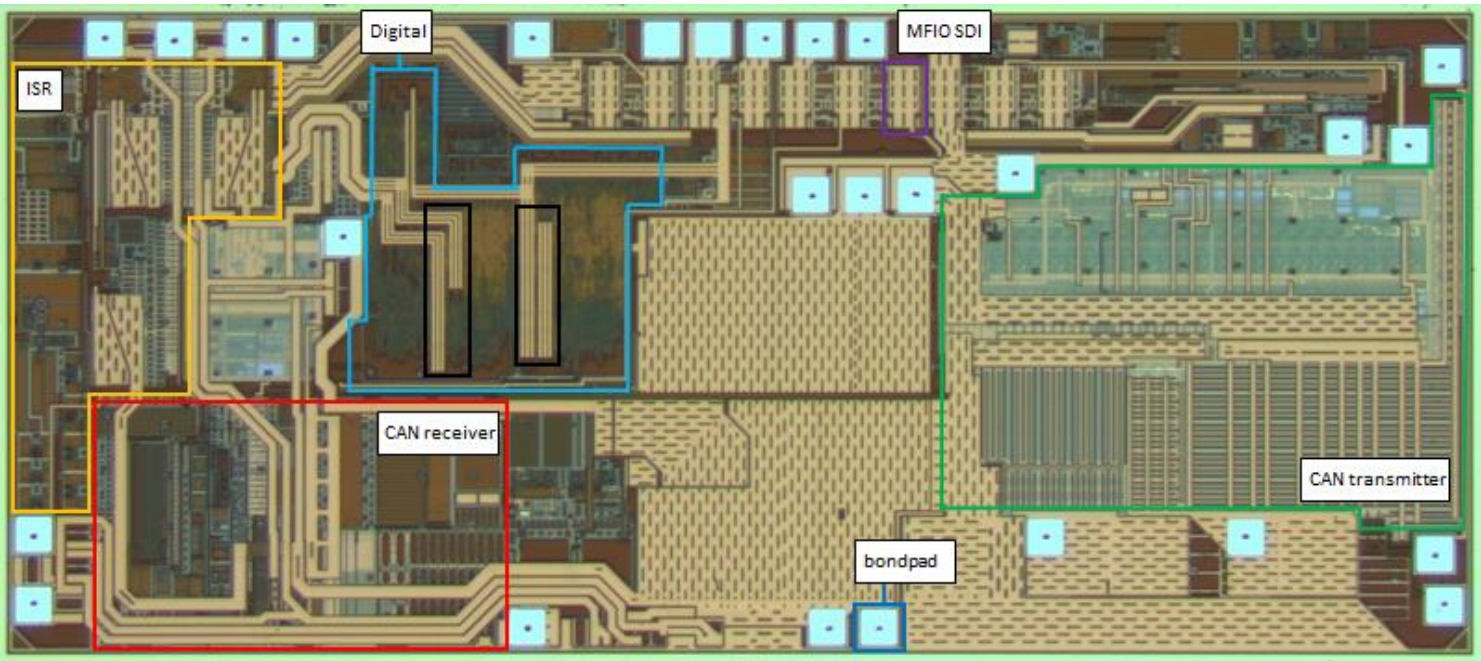



**Figure 1**: Die view of TJA1145A, with various design blocks identified:

- Red: CAN receiver
- Green: CAN transmitter
- Blue: Digital circuitry
- Orange: Internal Supply Reference (ISR)
- Black: Power routing to digital circuitry
- Dark blue: Bondpad (of SDI pin)
- Purple: Multi-Functional IO cell (MFIO), for pin SDI

## 6.1 CAN FD design updates

The three CAN FD datasheet parameters that require a minor design change in the CAN transmitter and receiver, to comply with the 5 Mbit/s timing, are $t_{bit(bus)}$, $t_{bit(RXD)}$ and $\Delta t_{rec}$ (see Table 2 below, copied from TJA1145A datasheet, Table 35, page 42). 5Mbit/s CAN FD requires a tighter timing tolerance / less spread on bit timing parameters to support higher bus speeds. So the change is about 'higher timing precision' which even improves the system performance, if lower bus speeds are used. So, only positive effect also for old applications.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{bit(bus)}$ | transmitted recessive bit width | $t_{bit(TXD)}$ = 500 ns [3] | 435 | - | 530 | ns |
| | | $t_{bit(TXD)}$ = 200 ns [3] | 155 | - | 210 | ns |
| $t_{bit(RXD)}$ | bit time on pin RXD | $t_{bit(TXD)}$ = 500 ns [3] | 400 | - | 550 | ns |
| | | $t_{bit(TXD)}$ = 200 ns [3] | 120 | - | 220 | ns |
| $\Delta t_{rec}$ | receiver timing symmetry | $t_{bit(TXD)}$ = 500 ns | −65 | - | +40 | ns |
| | | $t_{bit(TXD)}$ = 200 ns | −45 | - | +15 | ns |

**Table 2**: TJA1145A datasheet CAN FD parameters related to the minor design updates in the CAN transmitter and receiver for 5 Mbit/s ($t_{bit(TXD)}$ = 200 ns)

There are only two minor design updates needed to comply with the CAN FD 5 Mbit/s timing requirement for these three parameters (see Figures 2 and 3):

- One in the CAN receiver (red IP block in Figure 1) to shorten $t_{bit(RXD)}$, the bit time on pin RXD
- One in the CAN transmitter (green IP block in Figure 1) to shorten $t_{bit(bus)}$, the transmitted recessive bit width

**CAN receiver $t_{bit(RXD)}$**: Figure 2 shows a small part of the design between the bus (CANH/CANL, on the left, Vin) and pin RXD (on the right, Vout). The incoming pulse (e.g. dominant-recessive-dominant, or dom-rec-dom) controls the switch for the top current source 2I, which can deliver twice as much current as the bottom current source I. Through an inverter Vout is then pulled either HIGH or LOW, to create a pulse of equal width and inverse polarity. For TJA1145A a second path using these current sources is added, which has slower flanks due to the added capacitor. The NAND gate then delivers on Vout effectively a narrower pulse.

**CAN transmitter $t_{bit(bus)}$**: Figure 3 shows a small part of the design between pin TXD (on the left, Vin) and the bus (CANH/CANL, on the right, Vout). The only design change here is the addition of a resistor inside the inverter, and a capacitor (indicated in red). This results in a narrower pulse on Vout.

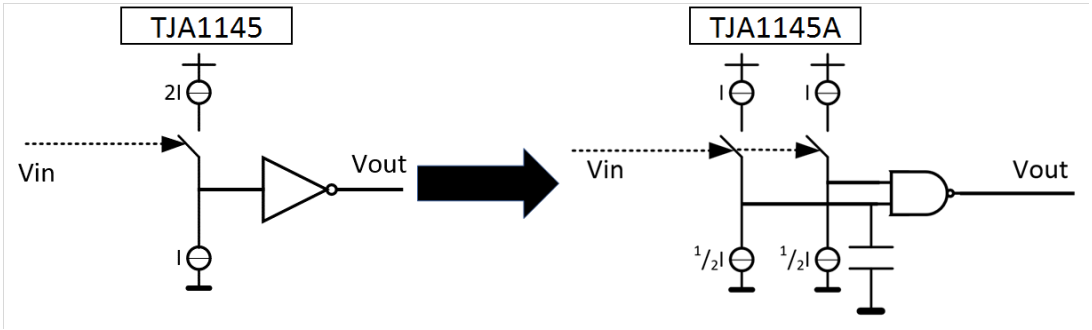



**Figure 2**: Minor design change in the CAN receiver to shorten $t_{bit(RXD)}$.

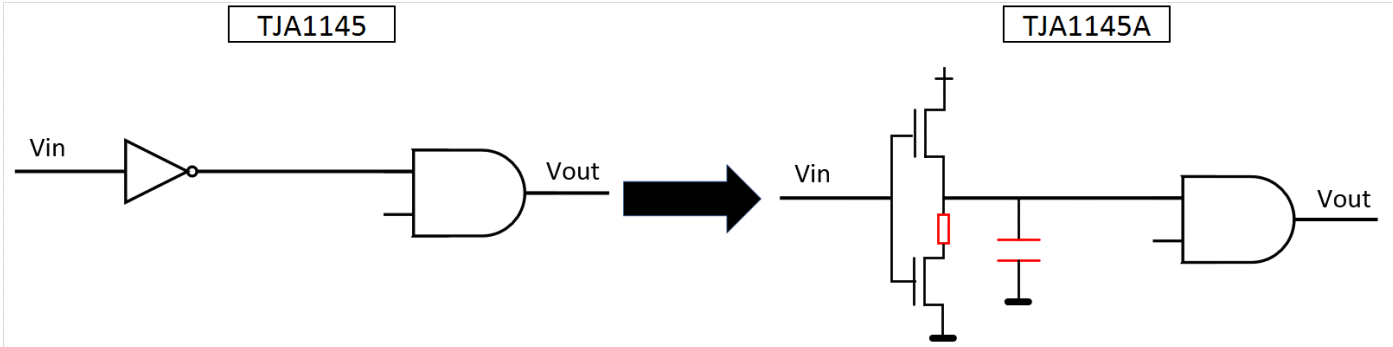



**Figure 3**: Minor design change in the CAN transmitter to shorten $t_{bit(bus)}$.

To achieve the short Wake-Up Pattern (WUP) wake-up time to comply with the latest ISO 11898-2:2016 standard (i.e. $t_{wake(busdom)}$ and $t_{wake(busrec)}$ 0.5/-/3.0 ➔ 0.5/-/1.8 µs, see Table 3) only a minor digital design change is required. Pin RXD is sampled for a WUP, consisting of a dominant-recessive-dominant pulse, and the shorter wake-up time is achieved by adjusting the digital filter time. Source code or a schematic picture of this will not be shown, as it would disclose NXP-proprietary information.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{wake(busdom)}$ | bus dominant wake-up time | first pulse (after first recessive) for wake-up on pins CANH and CANL; CAN Offline mode | 0.5 | - | 1.8 | µs |
| | | second pulse for wake-up on pins CANH and CANL | 0.5 | - | 1.8 | µs |
| $t_{wake(busrec)}$ | bus recessive wake-up time | first pulse for wake-up on pins CANH and CANL; CAN Offline mode | 0.5 | - | 1.8 | µs |
| | | second pulse (after first dominant) for wake-up on pins CANH and CANL | 0.5 | - | 1.8 | µs |

**Table 3**: TJA1145A datasheet CAN FD parameters related to the minor design update in the digital circuitry for a short Wake-Up Pattern(WUP) wake-up time: $t_{wake(busdom)}$ and $t_{wake(busrec)}$ (TJA1145 specification was 0.5/-/3.0 µs)

Product TJA1145 has an EMC immunity fail. To eliminate this immunity fail a minor analogue design change in the low-power CAN receiver (within the red block in Figure 1) is required. This change is shown in Figure 4.

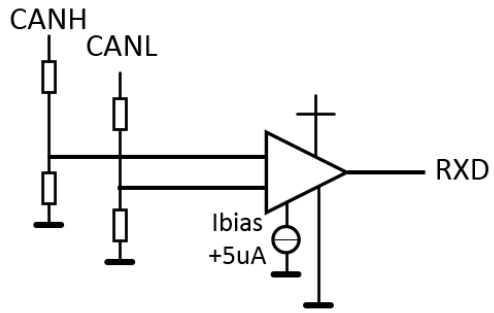



**Figure 4**: Minor design change in the low-power CAN receiver to improve immunity

The change is to improve the robustness of the comparator (immunity) by slightly increasing its bias current by 5μA. The immediate and inevitable side-effect of this is the quiescent current increase with this 5μA in the datasheet (see Section 9). The proof of effectiveness of this change is in the new IBEE EMC report for the leadless HVSON product TJA1145ATK(/FD), which indeed no longer shows an immunity fail but now a pass. For the SO package TJA1145AT(/FD) that *this* PCN is about, there is a full pass with choke, without choke no pass but an improvement.

Note that this information is provided to explain/show the minor design changes made in the CAN receiver and transmitter, enabling customer to judge the extent of the changes and facilitating an easy migration from TJA1145 to TJA1145A. We will not provide further specifics, as this is NXP-proprietary information. NXP guarantees that product TJA1145A complies with its datasheet specifications, on request a PPAP is available with a.o. a C&S CAN Conformance Test report and EMC reports.

## 6.2 Design fixes for four issues

The root cause explanation for the four issues as provided in the Customer Information Notification (CIN) 201909013I from December 6 2019 is not repeated here. In this document and these sections only the design fixes for these four issues described in this CIN are discussed.

### 6.2.1 TeEn (Testmode Enable)

To enter TeEn (testmode) a specific 13-bit 'unlock' code has to be applied to SDI/SCK 'reversed' within the first 20ms after a Power On Reset (POR). To make TeEn more robust against accidental and unintended customer access an extra condition to enter TeEn is added, namely that $V_{BAT}$>30V. The minor digital design fix is shown in Figure 5 below (left is TJA1145, right is TJA1145A, OVD30V is the digital flag that signals $V_{BAT}$>30V). Note that this OVD30V flag was already present in product TJA1145 and being used for another purpose. The only change therefore is to use this existing flag now as an an extra condition to enter testmode.

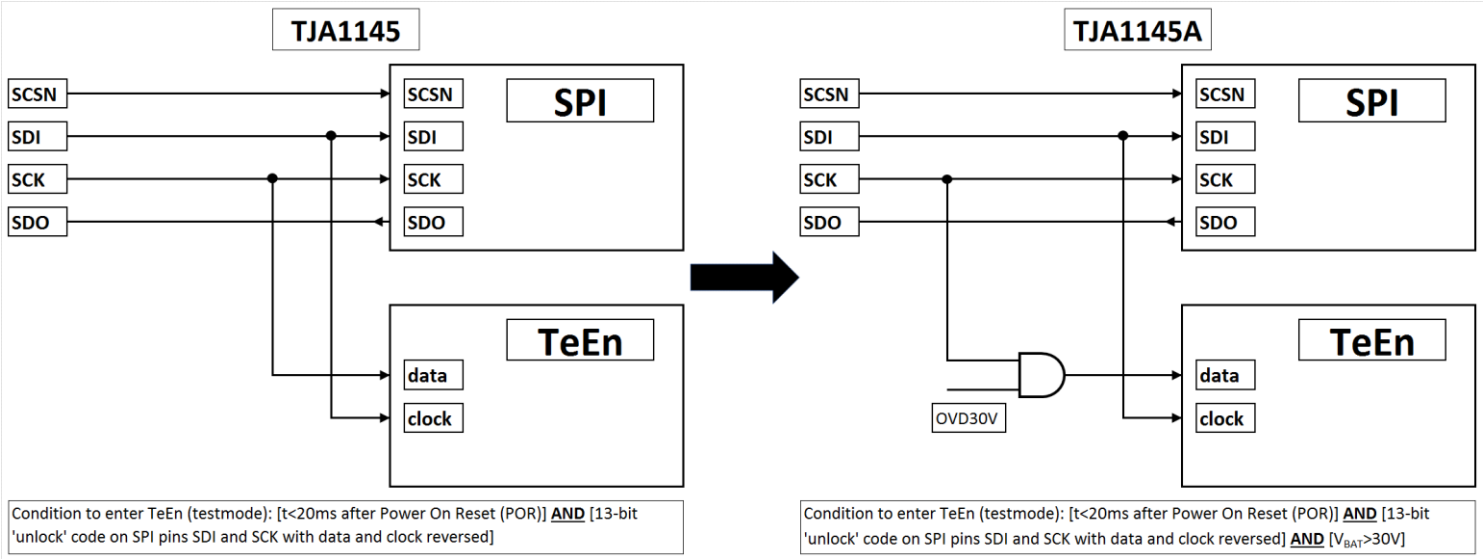


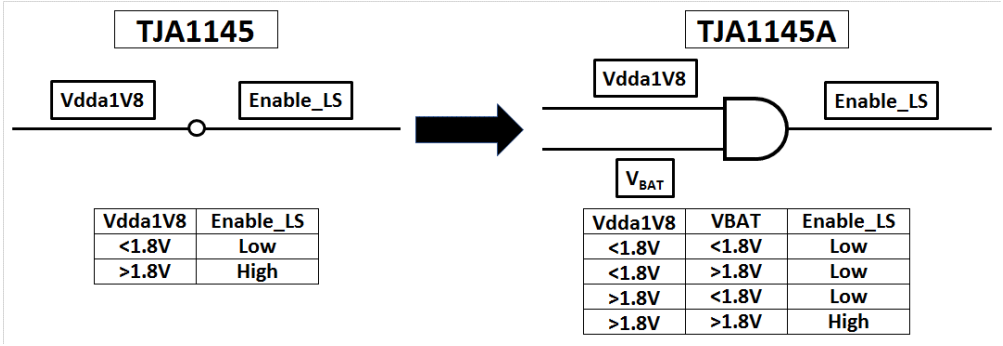

**Figure 5**: Minor design fix for the TeEn issue inside the digital circuitry (blue box in Figure 1): additional condition to enter TeEn $V_{BAT}$>30V (designated by the digital flag OVD30V).

The AND function between SCK (used as data for TeEn) and OVD30V ensures that testmode can only be entered if $V_{BAT}$>30V, which is outside the datasheet allowed operating range.

### 6.2.2 MTP soft write

The fail observed in a single customer application using TJA1145 was loss of INH pin functionality (INH permanently off) after Power On Reset (POR)/boot. This is the result of the product entering fail-safe-off because the MTP (Multi Time Programmable memory in the product) read gave an ECC error. This in turn comes from corrupted product configuration MTP content through accidental and unintended low $V_{BAT}$ (~1V, significantly below the normal operating voltage $V_{BAT}$≥4.5V) writing to the MTP (hence the term 'MTP soft write'). In the CIN 201909013I it has been explained that the root cause is related to an analogue flag Enable_LS, which was not properly reset in case $V_{BAT}$ was decreasing but not reaching 0V, but instead hanging at ~1V.

The minor analogue design fix made in the Internal Supply Reference (ISR) is shown in Figure 6.




| Vdda1V8 | Enable_LS |
|---|---|
| <1.8V | Low |
| >1.8V | High |

| Vdda1V8 | VBAT | Enable_LS |
|---|---|---|
| <1.8V | <1.8V | Low |
| <1.8V | >1.8V | Low |
| >1.8V | <1.8V | Low |
| >1.8V | >1.8V | High |

**Figure 6**: Minor analogue design fix made in the ISR (orange box in Figure 1): additional condition to read from/write to the MTP only when $V_{BAT}$>1.8V

The additional AND function with the condition $V_{BAT}$>1.8V ensures that Enable_LS is reset when the customer application is switched off but $V_{BAT}$ incorrectly does not go to 0V, e.g. due to module cabling effects, acting as antennas keeping the module internal BAT supply permanently around 1V.

### 6.2.3 Lock-up at cold temperature

The lock-up at cold temperature is caused by a sequence of two events/issues, see Figure 7:

- A slight unbalance in a current mirror used in a comparator inside the Internal Supply reference (ISR) creates glitches (~100ps) on the Enable_LS signal in a sub-ppm part of the products. To make this very clear:
  - All products, except a sub-ppm part of them, never show any glitches and therefore never have a lock-up
  - It is <u>not</u> the case that an individual product has a sub-ppm chance of showing lock-up:
    - If a product is <u>not</u> in above-mentioned sub-ppm part of all products, there is <u>zero</u> chance of lock-up
    - If a product *is* in above-mentioned sub-ppm part of all products, there is a <u>high</u> chance of lock-up at a device-specific small temperature window of a few degrees Celcius below room
- When present these glitches progress through the circuitry and impact the intended state transitions of the flipflops in the 1:8 clock divider Linear Feedback Shift Register (LFSR). The glitch disturbs the symmetry between 0➔1 and 1➔0 flipflop state transitions, leading over time to an LFSR state of '1111', which is functionally inaccessible and from which the LFSR can't recover (lock-up). With the LFSR in lock-up the 125KHz clock signal is no longer there and the device locks-up

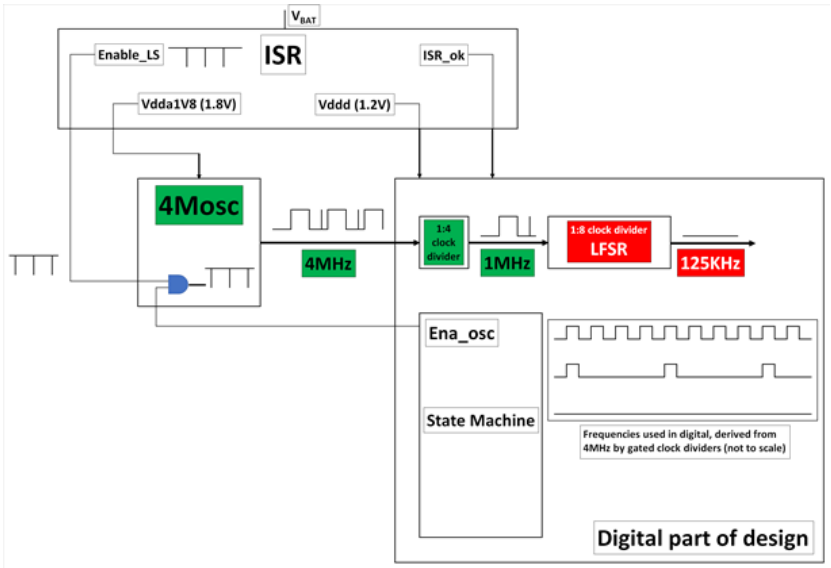



**Figure 7**: Product TJA1145 in lock-up (picture copied from CIN 201909013I from December 6 2019)

To solve this lock-up issue two minor design fixes are needed, one in the analogue ISR circuitry to prevent glitches, and one in the digital circuitry to prevent the LFSR lock-up (state '1111').

### 6.2.3.1 ISR design fix to prevent glitches

After Power On Reset (POR) the analogue supply voltage Vdda1V8 inside the ISR (see Figure 7) increases until 1.8V and then remains at that value during device operation. The Enable_LS flag is intended to have:

- Vdda1V8 < Vref ➔ Enable_LS=LOW
- Vdda1V8 > Vref ➔ Enable_LS=HIGH

The analogue circuit for Enable_LS, shown in Figure 8, shall work for all datasheet-allowed (supply) voltages and temperatures, and has to take into account normal process variation. Vref is therefore a normal distribution, and the Enable_LS flag is only set reliably outside the 6σ limits of this distribution. An individual device has a certain fixed Vref within this normal distribution. In case Vref>1.8V, Enable_LS would never become high, the 4MHz oscillator would not start (see Figure 7), and the TJA1145 device would not start-up.

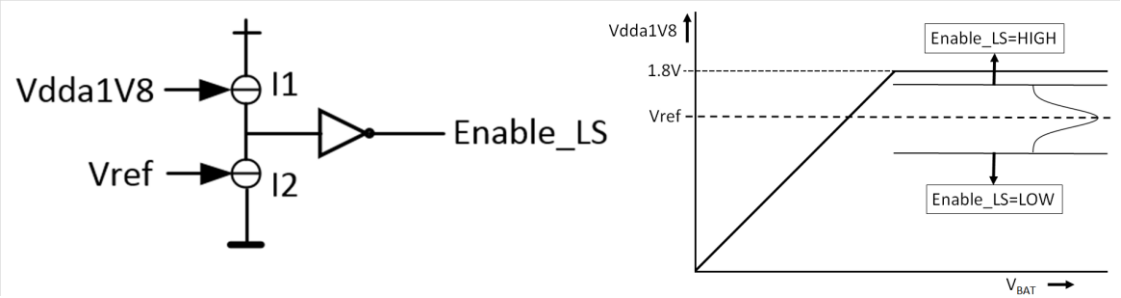



**Figure 8**: Simplified schematic of the Enable_LS flag inside the ISR, and the intended behavior of Vdda1V8

A current mirror, consisting of two opposing current sources I1 and I2 driven by Vdda1V8 and Vref, determines if the flag Enable_LS is pulled HIGH or LOW. This whole circuitry is operated at sub-Vt (i.e. transistor sub-threshold), necessary to reduce power consumption, needed to meet the required quiescent current specification in the datasheet.

The best sub-Vt simulation tools and models available at the time of the original non-A TJA1145 product showed the Vref 6σ limits to be below 1.8V (black curve in Figure 9). However, a new simulation of TJA1145, using the latest sub-Vt simulation tools and models available, shows a shifted and wider distribution with a tail exceeding 1.8V (blue curve in Figure 9). As explained above, the devices having a Vref that is always exceeding 1.8V (green circle in Figure 9) do not start-up, are screened out by NXP final test, and therefore will never reach the customer.

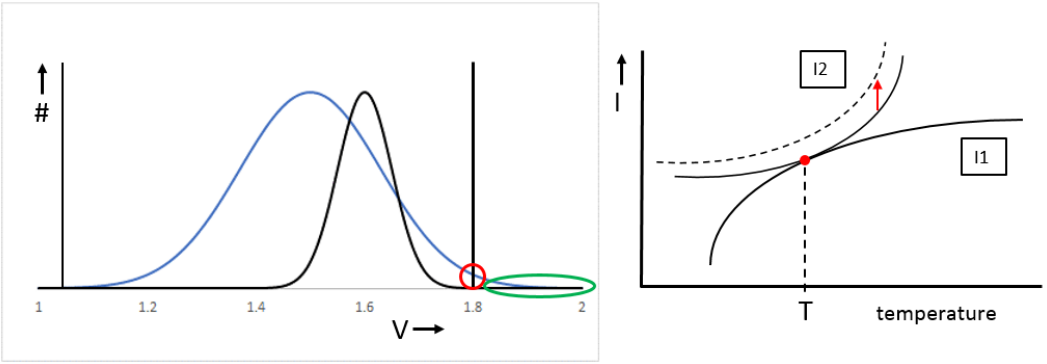



**Figure 9**: Left: Vref normal distribution, not to scale, Right: temperature dependence of I1 and I2

A sub-ppm part of the devices has Vref=1.8V exactly (red circle in Figure 9, which is not to scale). These devices will start-up but will have jitter on Enable_LS, i.e. the ~100ps glitches which are the root cause for the lock-up. Note that Vref is not a measurable/testable/screenable parameter, but a physical property of an individual device. The right side of Figure 9 shows the temperature dependence of current sources I1 and I2 from Figure 8. The above-mentioned devices where Vref=1.8V exactly, have I1=I2 exactly at a certain temperature, specific for each of these devices. The condition I1=I2 is only true for a very narrow window around this temperature. In the few complaint devices we found this temperature window to be typically +/-5$^0$C. A device in the red circle will only show potential lock-up in this specific temperature window, irrespective of the conditions applied.

The wider Vref distribution is the consequence of a slight unbalance in the current mirror in Figure 8. The solution is to re-balance this current mirror by making the Vref/I2 current source slightly stronger. This is done by replacing a single transistor within the current mirror, one with a 2/10 width-length ratio, by one with a 2.5/10 ratio (see Figure 10). The consequence is that I2 shifts and no longer has a touchpoint with I1 (indicated by the dashed I2 curve in the right side of Figure 9).

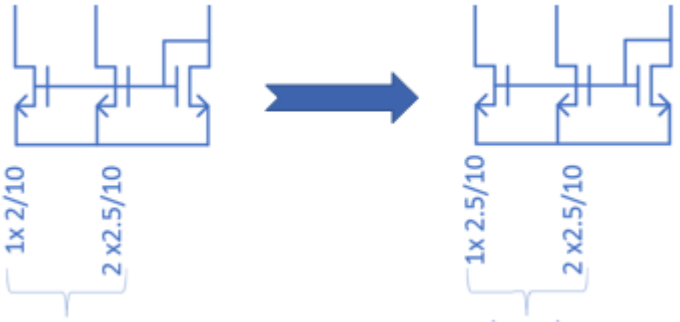



**Figure 10**: Change in current mirror from TJA1145 (left) to TJA1145A (right).

The simulations of product TJA1145A show that this change results in a narrower distribution, moving Vref away from 1.8V and completely eliminating the sub-ppm glitch (returning to the black curve in the left of Figure 9). In other words, there are no TJA1145A products (not even at sub-ppm level) that will have Vref=1.8V or even above, the 6σ limit of the Vref distribution for TJA1145A is below 1.8V.

### 6.2.3.2 Digital design fix to prevent LFSR lock-up

The 1:8 clock divider circuitry in digital, used to gate the 1MHz clock down to 125KHz by passing through only every 8th clock pulse, contains a standard 4-bit Linear Feedback Shift Register (LFSR, see Figure 11). With only a clock input (CLK) and starting from 0 (4 bits LFSR[3:0]=0000), its output runs through a fixed sequence of numbers and returns to 0 in 16 steps. The pseudo-random sequence of the counter (deterministic and repetitive, so not random, but not linear/sequential) is fixed and determined by the LFSR's 4-flipflop design with feedback loops as shown in Figure 11.

In the LFSR implementation in product TJA1145, requiring a count till 8, the LFSR RESET input is used to reset to 0 at count 6 (LFSR[3:0]=0110, see Table 4). This is achieved with a single statement in the source code for the digital circuitry: 'WHEN LFSR[3:0]=0110 THEN RESET'. Therefore the steps 8 till 15 are not used and have become inaccessible. Should any of these steps 8-15 be entered through a defect mechanism, e.g. the above-mentioned Enable_LS glitches, Table 4 shows that the LFSR will automatically recover by stepping on each clock cycle towards step 15 and then reset.

For this standard 4-bit LFSR, the state LFSR[3:0]=1111 is impossible to access functionally from any of the available steps 0-15. However, the Enable_LS glitches disturb the symmetry between 0➔1 and 1➔0 transitions of the 4 flipflops in the LFSR. From simulation statistics it is seen that the glitches, which are only present in a sub-ppm part of all products, decrease the chance that an intended transition 1➔0 is made correctly. Over time this inevitably leads to the LFSR ending up in the state LFSR[3:0]=1111, from which it can never escape/reset, irrespective of the amount of clock cycles. This is the LFSR lock-up, leading to the loss of the 125KHz internal clock, in turn inevitably leading to loss of functionality of the TJA1145 device, i.e. lock-up. From the few complaint return devices we've seen that the time from Power On reset (POR) to lock-up varies from seconds to hours, but is specific and fixed for each of these devices.

The digital design fix to prevent this LFSR lock-up is the addition of a single statement in the source code for the digital circuitry: 'WHEN LFSR[3:0]=1111 THEN RESET'.

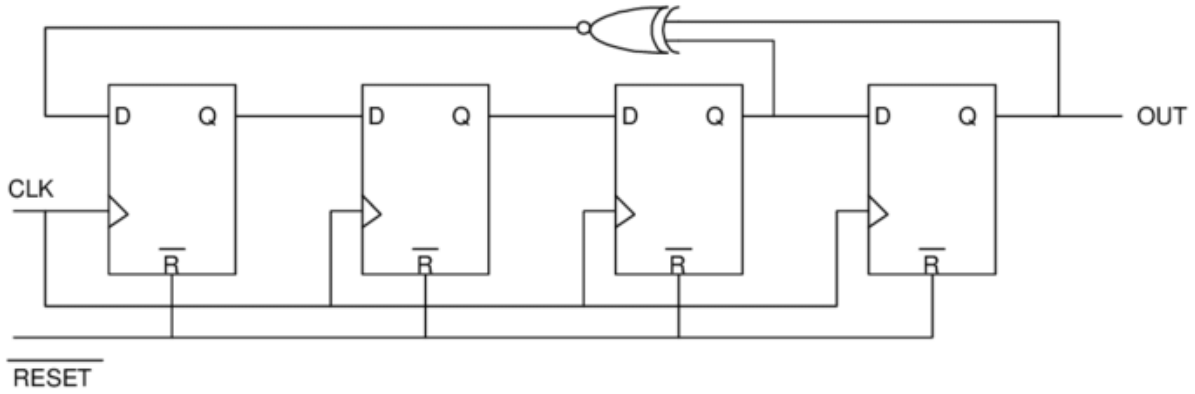



**Figure 11**: Standard 4-bit Linear Feedback Shift Register (LFSR), consisting of flipflops #3-0 (left to right)

| step | fliflop #3 | fliflop #2 | fliflop #1 | fliflop #0 | Counter | Comment |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Start |
| 1 | 0 | 0 | 0 | 1 | 1 | |
| 2 | 0 | 0 | 1 | 1 | 3 | |
| 3 | 0 | 1 | 1 | 1 | 7 | |
| 4 | 1 | 1 | 1 | 0 | 14 | |
| 5 | 1 | 1 | 0 | 1 | 13 | |
| 6 | 1 | 0 | 1 | 1 | 11 | |
| 7 | 0 | 1 | 1 | 0 | 6 | End |
| 8 | 1 | 1 | 0 | 0 | 12 | Unused |
| 9 | 1 | 0 | 0 | 1 | 9 | |
| 10 | 0 | 0 | 1 | 0 | 2 | |
| 11 | 0 | 1 | 0 | 1 | 5 | |
| 12 | 1 | 0 | 1 | 0 | 10 | |
| 13 | 0 | 1 | 0 | 0 | 4 | |
| 14 | 1 | 0 | 0 | 0 | 8 | |
| 15 | 0 | 0 | 0 | 0 | 0 | |
| | 1 | 1 | 1 | 1 | 15 | Functionally not accessible state |

**Table 4**: Standard 4-bit LFSR step sequence, with only step 0-7 from available 0-15 being used in the TJA1145(A) implementation. Count 15 (LFSR[3:0]=1111) is functionally not accessible.

In summary:

- The digital LFSR fix prevents LFSR lock-up in case it ends up in the ‘forbidden’ state ‘1111’, through a reset
- The analogue ISR fix prevents the Enable_LS glitches, thereby preventing the LFSR from getting in the ‘forbidden’ state ‘1111’ in the first place

The combination of both these simple analogue and digital design fixes makes the TJA1145A product 100% robust against the lock-up issue.

### 6.2.4 FSMS/PNFDE bits

The TJA1145 FSMS bit should only be cleared (1➔0) at power-on or at next entering of the Sleep mode (caused by a regular SPI request without VCC/VIO undervoltage). Incorrectly the FSMS bit is also cleared in the transition from Forced Sleep to Standby by local/remote wake-up. This is corrected by the addition of a single statement in the source code for the digital circuitry.

In case product TJA1145 is forced into Sleep Mode due to an undervoltage on VCC or VIO, all pending events shall get cleared in order to properly switch the device into Sleep Mode. Bit PNFDE (Partial Networking Frame Detection Error) has been found not to be cleared when entering forced Sleep Mode. The PNFDE bit is set to 0, but a clock-request to clock this data in was missing. In Sleep mode the clock is switched off to save power, and if bits need to be changed a clock request is needed. This has been solved by the addition of a single statement in the source code for the digital circuitry.

Source code or a schematic picture for these two fixes will not be shown, as it would disclose NXP-proprietary information.

## 6.3 Summary of the design updates for CAN FD and fixes for four issues

As shown, the updates in either analogue IP blocks or the digital circuitry, for CAN FD (Section 6.1) and to fix the four issues (Section 6.2), are all very small/minor design changes on the level of individual transistors/flipflops. The area size of the changes is tiny in comparison to the size of the IP block the change is made in. The digital design changes have been made in the source code for digital, and the digital circuitry has been re-synthesized with:

- No change in design rules
- No change in location, shape/form or size of the digital circuitry
- Change just in visual appearance as a result of the re-synthesis

## 6.4 Layout/design changes for robustness

Various layout/design fixes for robustness have been made:

- **Tiling**: The waferfab continuously produces a mix of products within the same diffusion process. For diffusion processing of metal layers it's favorable to reduce the variation of metal density in the layout from product to product. An industry-standard methodology to achieve this is the use of tiling. In the last step from transforming a design layout to photomasks, needed to pattern the product on the wafer in the diffusion process, dummy metal tiles are added to the empty spaces in the metal layers. These tiles are not connected to each other or to any part of the design, and have no relation with or influence on any of the product's (electrical) characteristics. The tiling algorithm used for product TJA1145 simply fills the empty spaces without a link to the design context. The opportunity of the introduction of the new TJA1145A product has been used to implement an improved tiling algorithm, which does take into account the design context. This means e.g. that if a certain matched transistor pair appears multiple times in the layout, the new tiling algorithm will make sure they get tiled exactly the same, whereas the old algorithm did not. This is a general robustness improvement, there is no problem in TJA1145 to be solved. This tiling difference between TJA1145 and TJA1145A is not a design or layout change, but it does influence the visual appearance of the die, as can be seen in Figure 12.

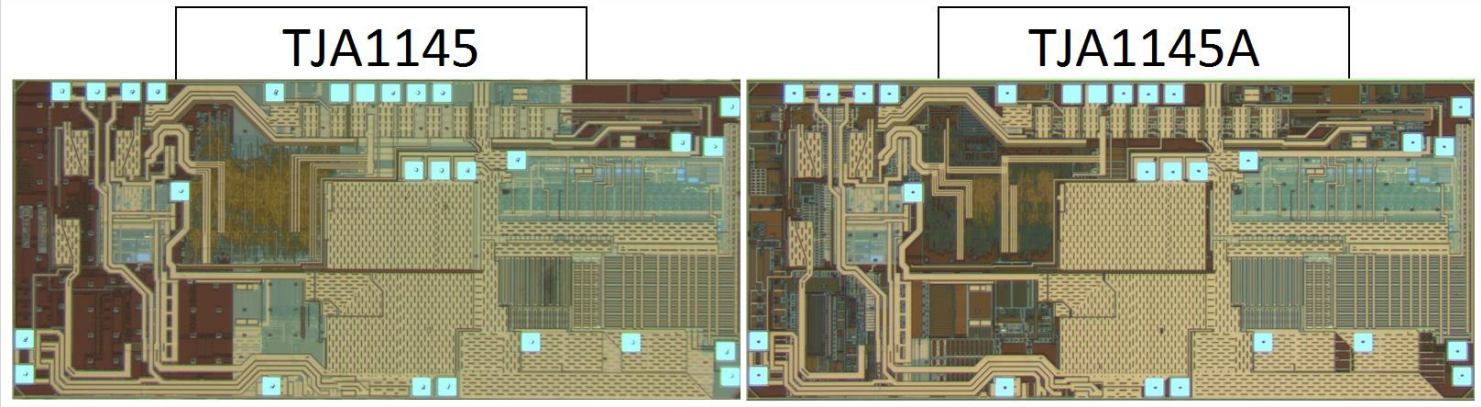



**Figure 12**: Visual appearance difference between TJA1145 and TJA1145A due to tiling and re-synthesis of digital

- **Pull-down/pull-up resistance on pin SDI**: Product TJA1145A has internal pull-down/pull-up resistors for pin SDI, likely enabling the removal of external resistors that your application might be using with product TJA1145. See Section 9 and Appendix 2 for more information. To make the change from TJA1145 to TJA1145A there is no design change, but merely a configuration change in digital for the configurable Multi-Functional IO cell (MFIO) for pin SDI (see Figure 1). In other words, the internal resistors have always been physically there in the MFIO design, but in TJA1145 are not used and are now used in TJA1145A.

  On a side-note, in TJA1145 these internal resistors weren't used because previous generation microprocessors kept their ports active in low-power mode. Using internal resistors was not needed and in cases of many devices connected to the SPI bus not even desirable. Likely for power consumption reduction, newer generation microprocessors no longer keep their ports active in low-power mode. TJA1145A facilitates their use, by providing internal resistors, clearly specified in the new datasheet.
- **Power routing to digital**: The layout of the voltage supply lines to the digital circuitry (power routing) has changed from TJA1145 to TJA1145A, see Figure 13 below. This is not a design (rule) change, and there's no change in the voltage supplied to, or power consumed by, the digital circuitry. The routing change merely enables a more evenly distributed power supply to digital.

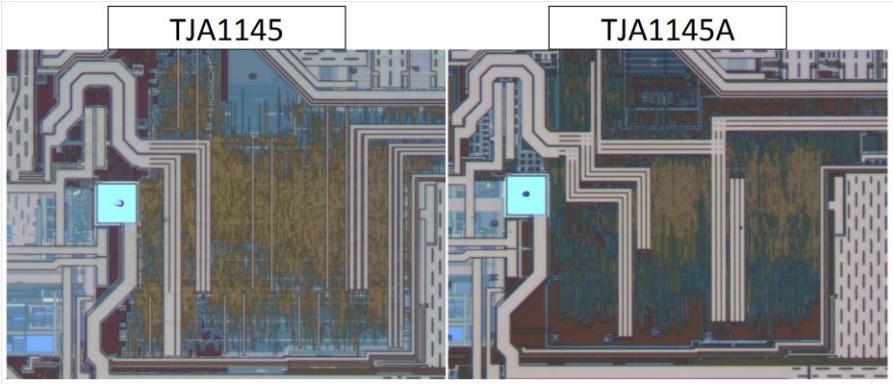



**Figure 13**: Comparison of power routing to digital between TJA1145 and TJA1145A

- **<u>Preparation for potential future transition to Cu bondwire</u>**: The SO package product TJA1145AT(/FD) continues to use AuPd bondwire instead of changing to Cu bondwire, like for TJA1145ATK(/FD) as announced by NXP PCN 202001016F01 from February this year. Both product versions use the exact same silicon die, which is updated to accommodate Cu wire bonding (see Appendix 4 for details). The changes are:
    - <u>Bondpad</u>: To accommodate the transition to Cu bonding the sub-top-metal (i.e. ME4) square mesh has changed to a smaller grid size. The contacts to and from this ME4 layer (i.e. VIA3 and VIA4) have changed accordingly. The top metal (ME5) and all other layers have not changed. Note that there is no active design area underneath the bondpads. The size and the locations of the bondpad have not changed (see Figure 14, which is without ME5).

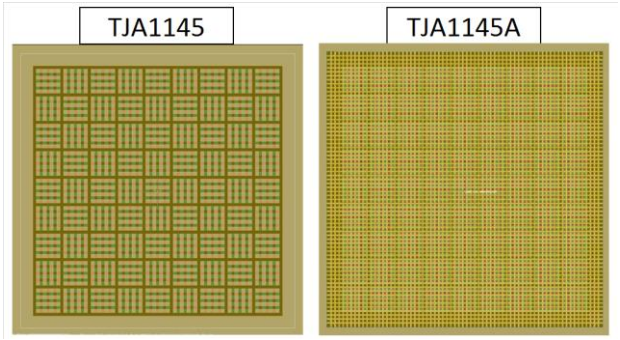



**Figure 14**: Change in bondpad's ME4 square mesh to smaller grid size for Cu bonding

    - <u>Wafercoat opening</u>: Products TJA1145(A) have a wafercoat overlayer, protecting the die and minimizing die-package stress. A Cu bondball is lower in height than the Au bondball. To facilitate access for the chisel to do ball shear measurements on a Cu bondball, the wafercoat opening around various bondpads has been enlarged. This can be seen in Figure 15. Note that there is no change in wafercoat material, thickness or processing. This is not a die design change, but a layout change in the wafercoat layer overlaying the die.
- **<u>50µm wafercoat pull-back</u>**: The opportunity of the introduction of the new TJA1145A product has been used to introduce a 50µm pull-back of the wafercoat edge from the die edge (shown in Figure 15). Figure 16 shows a side-by-side comparison of the wafercoat layout for the same location in design for TJA1145 and TJA1145A. The purpose of this wafercoat pull-back is to eliminate the possibility of creep of die sawing residues along the wafercoat edge to the bondpads. This is a general industrial robustness improvement, there have been no such issues on product TJA1145. Note that there is no change in wafercoat material, thickness or processing. This is not a die design change, but a layout change in the wafercoat layer overlaying the die.

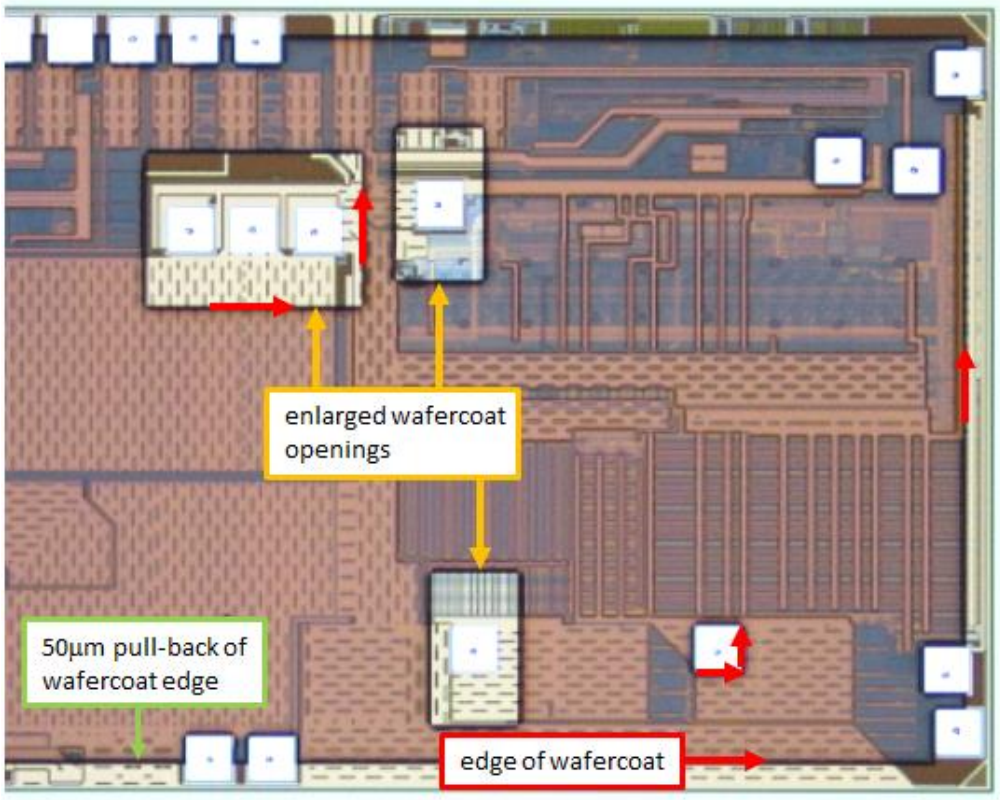



**Figure 15**: Right-hand die view of TJA1145A with wafercoat on top (compare to Figure 1)

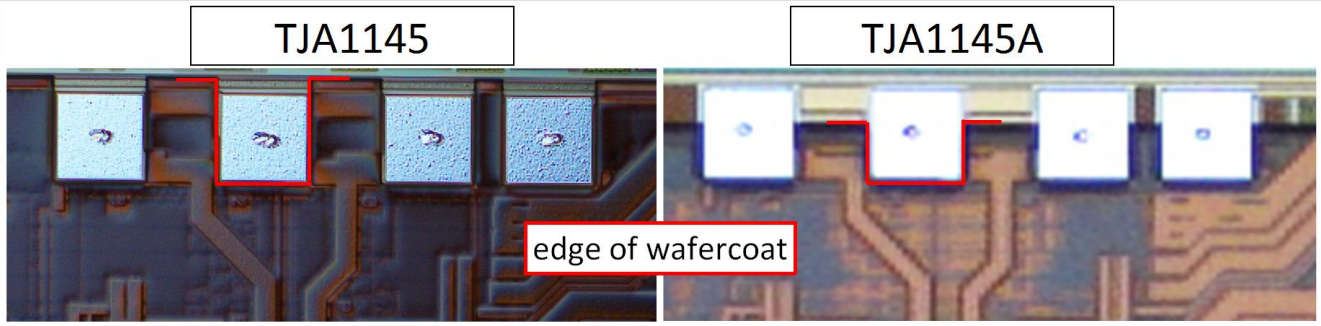



**Figure 16**: Difference in wafercoat layout for the same location in design between TJA1145 and TJA1145A.

## 7. How is it proven that the four issues have been resolved in TJA1145A?

### 7.1 TeEn (Testmode Entry)

The TeEn fix as shown in Figure 5 has been proven by standard design (code) review and functional simulation, and by measurements on actual TJA1145A devices. Note that in the standard production final test program, product TJA1145A has to be put in testmode to enable certain measurements. This can only be done by using the additional requirement to enter testmode as explained in Section 6.2.1. The effectiveness of the fix is 100%.

### 7.2 MTP soft write

The MTP soft write fix as shown in Figure 6 has been proven by standard design review and functional simulation. As the fail has only ever been seen in a single customer application, and can not be provoked on a standalone TJA1145(A) product, a separate validation on silicon can not be made. Given the trivial design change, this is however also not needed to guarantee a 100% effectiveness of the fix.

### 7.3 Lock-up at cold temperature

On the few complaint devices that have been returned to NXP we observed the following:

- Each complaint device only locks within a +/-5$^0$C window around a specific low temperature, and this is different for each returned device (a.o. -35$^0$C, -20$^0$C +10$^0$C)
- Each complaint device only locks after a specific time after Power On Reset (POR) of the device, and this is different for each returned device (from 30 seconds to 6hrs)

The two-stage root cause for the lock-up has been proven in the following way, using these few complaint return devices:

- We've proven the LFSR to be in lock-up (LFSR[3:0]=1111)
- We've proven on a decapped complaint device that by restoring the current mirror balance, the lock-up can be prevented

Through simulation we have proven that:

- For a sub-ppm part of all TJA1145 products, the Enable_LS signal in the ISR has ~100ps glitches
- The glitches cause the LFSR to end up in the lock-up state (LFSR[3:0]=1111)
- With the minor design change (Figure 10) there are no glitches at all (i.e. the 6$\sigma$ limits of the Vref distribution are below 1.8V)

All this information and evidence gives confidence that the two-step fix (analogue fix to prevent the glitches, digital fix to prevent the LFSR from locking-up) fully eliminates the lock-up issue for product TJA1145A.

### 7.4 FSMS/PNFDE bits

The fixes for the FSMS and PNFDE bit have been proven by standard design review and functional simulation, as well as by bench-testing on actual TJA1145 and TJA1145A devices. The effectiveness of the fixes is 100%.

## 8. Qualification of the change TJA1145T(/FD)➔TJA1145AT(/FD)

### 8.1 Qualification plan

The qualification results report can be downloaded from the NXP e-PCN system, on the same tab 'Files' you obtained this document from. The AEC-Q100 qualification tests performed are shown in Table 5.

| Item# | Abbr. | Test | Not applicable to this change | To be considered for this change | | Not applicable to TJA1145A at all | Comment |
|---|---|---|---|---|---|---|---|
| | | | | Not applicable | Applicable | | |
| **Accelerated Environment Stress Tests (AEC-Q100-REV-G)** | | | | | | | |
| A1 | PC | Preconditioning | | | X | | Tests are performed |
| A2 | HAST | Highly Accelerated Stress Test | | | X | | |
| A3 | UHAST | Unbiased HAST | X | | | X | UHAST failure modes are fully covered by HAST |
| A4 | TC | Temperature Cycling | | | X | | Tests are performed |
| A5 | PTC | Power Temperature Cycling | | | X | | |
| A6 | HTSL | High Temperature Storage Life | | | X | | |
| **Accelerated Lifetime Simulation Tests (AEC-Q100-REV-G)** | | | | | | | |
| B1 | HTOL | High Temperature Operating Life | | | X | | Tests are performed |
| B2 | ELFR | Early Life Failure Rate | | | X | | |
| B3 | EDR | Endurance, Data Retention | X | | | X | TJA1145A doesn't contain EPROM or EEPROM, the MTP data retention has been validated over the automotive mission profile during the diffusion process release. During production all devices are submitted to a data retention bake, and subsequently tested for data retention perfomance. |
| **Package Assembly Integrity Tests (AEC-Q100-REV-G)** | | | | | | | |
| C1 | WBS | Wire Bond Shear | | | X | | Tests are performed |
| C2 | WBP | Wire Bond Pull | | | X | | |
| C3 | SD | Solderability | X | | | | No change in leadframe |
| C4 | PD | Physical Dimensions | X | | | | No change in package outline or dimensions |
| C5 | SBS | Solder Ball Shear | | | | X | TJA1145A is an SMD device, has no solder balls |
| C6 | LI | Lead Integrity | | | | X | Only applicable for though-hole devices, TJA1145A is an SMD device |
| **Die Fabrication Reliability Tests (AEC-Q100-REV-G)** | | | | | | | |
| D1 | EM | Electromigration | | | X | | No change in the diffusion process, already released in the current waferfab SSMC, Singapore. These tests are performed for the release of this diffusion process in the 2nd waferfab VIS, Hsinchu, Taiwan. |
| D2 | TDDB | Time Dependent Dielectric Breakdown | | | X | | |
| D3 | HCI | Hot Carrier Injection | | | X | | |
| D4 | NBTI | Negative Bias Temperature Instability | | | X | | |
| D5 | SM | Stress Migration | | | X | | |
| **Electrical Verification Tests (AEC-Q100-REV-G)** | | | | | | | |
| E2 | HBM/MM | ESD Human Body Model/Machine Model | | | X | | Tests are performed |
| E3 | CDM | ESD Charged Device Model | | | X | | |
| E4 | LU | Latch-up | | | X | | |
| E5 | ED | Electrical Distribution | | | X | | Updated ED report is available |
| E7 | CHAR | Characterization | X | | | | Wafer- and Final Test programs and the limits therein for TJA1145A are the same as those for TJA1145, with only additional tests for CAN FD. |
| E8 | GL | Gate Leakage | X | | | | No change in waferfab diffusion process |
| E9 | EMC | Electromagnetic Compatibility | | | X | | Updated EMC report is available |
| E10 | SC | Short Circuit Characterization | | | | X | Only applicable to smart power devices, which TJA1145A is not |
| E11 | SER | Soft Error Rate | X | | | X | Only applicable to devices with >1Mbit SRAM or DRAM, which TJA1145A does not have at all |

**Table 5**: AEC-Q100 qualification plan for the release of successor CAN FD drop-in replacement product TJA1145AT(/FD)

Legend for Table 5:

- The first three columns ('Item#', 'Abbr' and 'Test') give the AEC-Q100 test number, abbreviation/acronym and description
- In the column 'Not applicable to this change', 'X' marks those tests that do not apply to this change. All the tests not marked with 'X' in this column should be considered. Of those, various tests are not required given the specific change that is being made, and others are. This is marked with 'X' in the 5th and 6th column under the heading 'To be considered for this change'.
- Various tests never apply to product TJA1145A, irrespective of the change made. This is marked in the 7th column.
- In the 'Comment' column an explanation is given where applicable
- The rows are color-coded to guide the eye:
  - Dark grey: all tests that are not applicable, either for this change or not to TJA1145 at all
  - Light grey: tests to be considered for the change, but not applicable (argument in column 'Comment')
  - White: tests performed for this change

## 8.2 ZVEI Delta Qualification Matrix (DeQuMa)

The corresponding ZVEI DeQuMa ID numbers for the changes in this PCN are SEM-DS-01—03 (datasheet changes), SEM-DE-01—02 (design changes), SEM-PW-13 (introduction 2nd wafer fab) and SEM-PS-01 (addition of the Moisture Barrier Bag or MBB). The ZVEI DeQuMa is attached to this PCN for reference, both in zipped excel and pdf format. It can be obtained from the NXP e-PCN system you're subscribed to, in the same way you obtained this document.
The original release of TJA1145 has been done with AEC-Q100 revision G, including ESD MM specification in the datasheet. It's successor TJA1145A, still with ESD MM specification in the datasheet, is therefore also qualified according to revision G.

## 9. Datasheet changes TJA1145➔TJA1145A

Product TJA1145AT(/FD) has a new, separate datasheet from the current TJA1145T(/FD) product. Differences are:

- The new/additional CAN FD requirements that TJA1145AT(/FD) fulfills:
  - Compliance to final ISO 11898-2:2016 and SAE J2284-1 till SAE J2284-5
  - 5 Mbit/s i.s.o. 2 Mbit/s timing compliance:
    - $V_{TXsym}$ (page 39): condition $f_{TXD}$=2.5MHz added
    - Additional specifications/conditions for parameters on page 42:
      - $t_{bit(bus)}$ : transmitted recessive bit width
      - $t_{bit(RXD)}$ : bit time on pin RXD
      - $\Delta$trec : receiver timing symmetry
    - Improved Figures 11 (page 43) and 12 (page 44)
    - Short WUP wake-up time, $t_{wake(busdom)}$ and $t_{wake(busrec)}$ (page 42): 0.5/-/3.0 µs ➔ 0.5/-/1.8 µs
  - Extended specification for $t_{to(wake)bus}$ (bus wake-up time-out time, page 42): 0.57/-/1.2 ms ➔ 0.8/-/10 ms
- TJA1145AT(/FD) has a design fix for improved EMC immunity performance, that it shares with the leadless HVSON package TJA1145ATK(/FD) using the exact same silicon die. The inevitable consequence of the minor design change made to achieve this (see Section 6.1 Figure 4) is a slight increase in the $I_{BAT}$ quiescent current (pages 3 and 37):
  - $I_{BAT}$ in Sleep mode : -/40/59 µA ➔ -/48/64 µA
  - $I_{BAT}$ in Standby mode: -/44/68 µA ➔ -/56/73 µA
  - $V_{hys(RX)dif}$ (page 40): specification improvement 50/200/400 mV ➔ 1/30/60 mV

  The design change is shown in Section 6.1 Figure 2.
- Data mask register: response for DLC>8 has changed to resolve a previous ISO16845-2 CAN Conformance violation:
  - Frame control register (page 20, Table 12): description for the 4-bit DLC>8 (1001 to 1111) changed (text ‘DM0 ignored’ has been removed)
  - Figure 8 ‘Data mask register usage for different values of DLC’, page 21: for DLC>8 ‘00h’➔’DM0’
- Following a general microcontroller trend to turn off ports completely during lower-power mode, the TJA1145A has been upgraded. For pin 11 SDI, parameter $I_{LI(SDI)}$ (input leakage current on pin SDI) has been replaced by parameters $R_{pd(SDI)}$ and $R_{pu(SDI)}$ (page 38, pull-down/pull-up resistance on pin SDI). Underlying this datasheet specification change is a minor product configuration change (in the digital circuitry) that switches on internal pull-down/pull-up resistors, thereby enabling the removal of external pull-down/pull-up resistors that you might be using in your application. For more detailed information, please see Appendix 2.
- New/additional parameters, missing for TJA1145 and now added for TJA1145A (no design change involved):
  - $V_{th(sw)hys}$: switching threshold voltage hysteresis (page 38)
  - $t_{d(SDI-SDO)}$: SDI to SDO delay time (page 41)
- Editorial and other changes:
  - Product TJA1145AT(/FD) in the SO-package will be released separately in Q4 2020 ➔ Specific SO-package information is removed from the new TJA1145A datasheet (e.g. pinning in Figure 2, Package outline in Figure 17). After the release of TJA1145AT(/FD) the datasheet will be (re)-updated with this SO-package specific information, and you will be properly informed of this change.
  - The HBM ESD specification text has been re-formatted with more appropriate footnotes (page 35, Table 32). There is no HBM ESD specification change.
  - Improved Figures 13 (SPI timing diagram), 15 (Timing test circuit for CAN transceiver) and 16 (Test circuit for measuring transceiver driver symmetry)
  - Parameter $t_{fltr(wake)bus}$ has been removed from the datasheet, as it is not applicable for both TJA1145 and TJA1145A. There is no $t_{fltr(wake)bus}$ visible on pin RXD after valid CAN wake-up pattern detection (page 13), since pin RXD is continuously driven LOW after wake-up detection in CAN Offline mode (see Figure 5 ‘CAN wake-up timing’ on page 14). There is no change in functionality of either TJA1145 or TJA1145A, this is a correction of a mistake in the datasheet. As TJA1145 will be discontinued, no changes to that datasheet will be made anymore.
  - The specifications for parameter $t_{d(uvd-sleep)}$ have changed: 200/-/400 ms ➔ 180/-/440 ms. There is no underlying change and there is no difference between TJA1145 and TJA1145A, the new specification appropriately represents the performance of TJA1145(A) as it has always been.

Before-mentioned NXP PL IVN CIN 201909013I informed you that for product TJA1145 the bits FSMS (Forced Sleep Mode Status) and PNFDE (Partial Networking Frame Detection Error) under specific conditions function slightly different than described in the datasheet (see Appendix 3 for more details). Minor digital design fixes in product TJA1145A have corrected these deviations (see also Sections 6.2.4. and 7.4). There is no datasheet change associated with this, and product TJA1145A fully complies with the description of the functionality of these FSMS and PNFDE bits in the TJA1145A datasheet.

Conclusions:

- All datasheet changes in the transition TJA1145➔TJA1145A are improvements (tightening) and/or additions, with the single exception of the inevitable slight increase of quiescent current $I_{BAT}$ for Sleep and Standby mode.
- The design implementation of pull-down/pull-up resistances for pin SDI allows the removal of external components that you might be using in your application (please check the detailed information in Appendix 2).
- The FSMS/PNFDE bit functionality deviation from datasheet for TJA1145 has been resolved for TJA1145A.

## 10. Product marking TJA1145T(/FD)➔TJA1145AT(/FD)

The change in product marking for the transition TJA1145T(/FD)➔TJA1145AT(/FD) is shown in Figure 17 below.

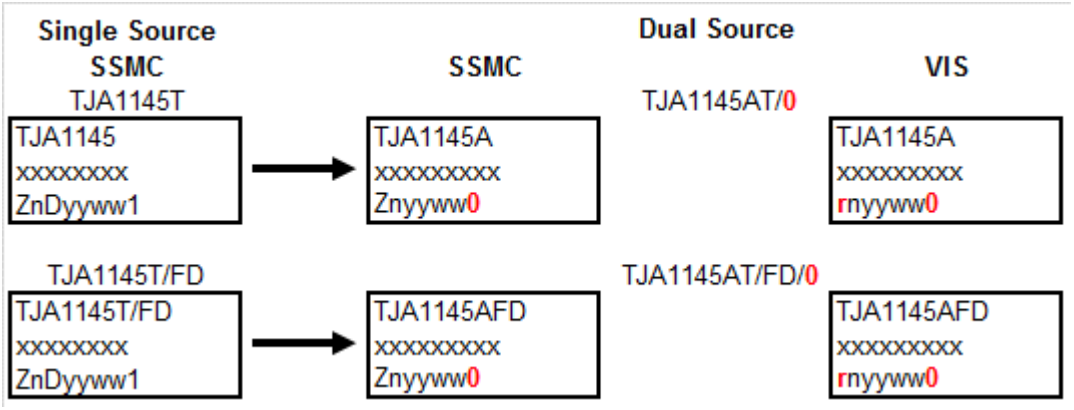



**Figure 17**: Product marking change TJA1145T(/FD)➔TJA1145AT(/FD)

The following applies:

- The 2nd marking line contains NXP-internal traceability information on diffusion and assembly batch
- The 3rd line marking:
  - Z: diffusion waferfab SSMC Singapore, r: diffusion waferfab VIS Hsinchu, Taiwan.
  - n: assembly and test site ATBK, Bangkok, Thailand, no change
  - D: redundant identifier for dark green mold compound removed.
  - yyww: product datecode, year and week number

NXP can not judge if this marking change has impact on potential PCB AOI (Automatic Optical Inspection) done by customer.

## 11. Migration guide TJA1145➔TJA1145A

This PCN on the transition TJA1145T(/FD)➔TJA1145AT(/FD) and the subsequent discontinuation of product TJA1145T(/FD) implies that your application(s) will have to switch from TJA1145T(/FD) to TJA1145AT(/FD).

The successor CAN FD product TJA1145AT(/FD) is a true drop-in replacement for TJA1145T(/FD). This section explains the migration from TJA1145T(/FD) to TJA1145AT(/FD) step-by-step. Together with the reliability qualification results (report attached to this PCN) this should enable a change-over with little or no (qualification) effort on your behalf.

For the transition TJA1145➔TJA1145A the following holds:

- Form : Only change is Cu wire, and associated change of mold compound
- Fit : No change, TJA1145AT is a drop-in replacement for TJA1145T
- Function : Improved through fulfillment of additional datasheet CAN FD specifications
- Performance : No change
- Reliability : No change, product TJA1145AT(/FD) is fully AEC-Q100 qualified and released
- Quality : Improved through minor design changes to fix before-mentioned four issues

Step-by-step migration from TJA1145T(/FD) to TJA1145AT(/FD):

- Packing: There is no change in the product's MSL level 1. The additional Moisture Barrier Bag (MBB plastic bag) around the reel in the 'pizza' box is put in to be more robust against poor customer storage conditions, which in specific cases we have become aware of.
- Package outline or dimension: No change, the product TJA1145AT(/FD) fits to the exact same package outline and dimensions as TJA1145T(/FD). The package outline drawing in the datasheet (Figure 17 on page 47) is unchanged. Therefore no change in PCB footprint is needed.
- Solderability: No change in leadframe dimensions or material composition, therefore no change in solderability.
- PCB population: Should your application have external pull-up/pull-down resistors on pins SDI/SDO, these likely no longer need to be populated, enabling a cost-saving (see Section 8 and Appendix 2).
- Product marking: Please check if the marking change (see Section 10) impacts PCB AOI (Automatic Optical Inspection), in case you're using that for your application.
- Software: Product TJA1145(A) doesn't come with software. No change in module/car software is needed, as the product's functionality, modes and (configuration) registers haven't changed. Just for completeness we would like to point you to a hypothetical case. For TJA1145 CAN partial networking, the data mask 0 configuration was ignored for the 4-bit DLC>8, leading to an ISO16845-2 CAN Conformance violation. TJA1145A fully conforms to ISO16845-2 CAN, the data mask 0 configuration now also works for DLC>8. In the very unlikely case that your TJA1145 module/car software somehow inappropriately exploited that the data mask configuration 0 for DLC>8 was ignored (i.e. you were using DLC 1001 to 1111 for something else), this will need to be changed.

- Datasheet functionality and specification:
    - The additional/improved/enhanced specifications for CAN FD up to 5 Mbit/s to comply with ISO11898-2:2016 and SAE J2284-1 till SAE J2282-5 are backwards compatible with classic CAN.
        - Short Wake-Up Pattern (WUP) wake-up time: as the new specification is a subset of the previous, there's no impact in switching to TJA1145A.
        - Extended specification for bus wake-up time-out time $t_{to(wake)bus}$ (0.57/-/1.2 ms ➔ 0.8/-/10 ms): no impact in switching to TJA1145A, there's been no customer requirement for the range 0.57-0.8 ms. TJA1145A fully complies with ISO 11898-2:2016.
    - The slight increase in quiescent current $I_{BAT}$ has no functional impact, and is the inevitable side-effect of the minor design change made to improve EMC immunity for the leadless HVSON package TJA1145ATK(/FD) which uses the exact same die design.
    - $t_{d(uvd-sleep)}$: there's no change in the product, only the datasheet is updated to appropriately represent the behavior/functionality/performance of TJA1145 and TJA1145A as it has always been.

Conclusion: The differences between TJA1145T(/FD) and TJA1145AT(/FD) are minor and should enable you to migrate to TJA1145AT(/FD) with little or no effort.

## Appendix 1: Details on TJA1145(A) product names

This PCN is about the transition from the TJA1145T product family to the TJA1145AT product family. Each product family consists of two functional variants ('normal' and /FD) and two package variants (T is SO-package, TK is leadless HVSON package). Last but not least there could be multiple packing variants (e.g. tube, reel).

Each product, with specific functionality, package and packing is uniquely identified by the NXP 12-digit 12NC ordering code. The first 9 digits (9NC) have a one-to-one link with the product's functional and package variant, The so-called Product Type Name. The last 3 digits (3NC) have a one-to-one link with the product's packing.

| | | Current released TJA1145 products [1] | | | Successor CAN FD drop-in replacement TJA1145A | | |
|---|---|---|---|---|---|---|---|
| Product | Package | Product Type Name | Orderable part number | Ordering code (12NC) | Product Type Name | Orderable part number | Ordering code (12NC) |
| TJA1145 | SO14 | TJA1145T | TJA1145T,118 | 9352 962 07118 | TJA1145AT/0 | TJA1145AT/0Z | 9353 984 49431 |
| | | TJA1145T/FD | TJA1145T/FDJ | 9353 002 86118 | TJA1145AT/FD/0 | TJA1145AT/FD/0Z | 9353 984 54431 |

[1] See Appendix 1 for details on the definitions for Product Type Name, Orderable part number and 12NC ordering code.

**Repeat of Table 1**: Overview of the TJA1145 product versions involved in this announcement, with explicit reference to the NXP Product Type Names, Orderable part numbers and 12NC ordering codes for the current products and their successor CAN FD drop-in replacement products.

The datasheet for all non-A TJA1145 product variants is TJA1145 and includes Product Types:

- TJA1145T in SO-package➔T
- TJA1145T/FD (FD variant of the product, explained in the datasheet, in SO package➔T)
- TJA1145TK in leadless HVSON package➔TK
- TJA1145TK/FD (FD variant of the product, explained in the datasheet, in leadless HVSON package➔TK)

All these product variants are only available in reel packing (3NC=118 ending). The datasheet does not refer to Orderable part number and 12NC, as this is logistic information that could change over time, and has nothing to do with the functional behavior of the product as described in the datasheet.

The Orderable part number is the Product Type Name + suffix for 3NC packing ending, see Table 6 for examples.

| Packing variant | 3NC | Suffix | Comment |
|---|---|---|---|
| Tube | 112 | U | Not applicable for TJA1145 |
| Reel | 118 | ,118 or J | |
| Dry-pack reel | 518 | Y | Not applicable for TJA1145 |
| Reel in MBB | 431 | J | |

**Table 6**: Examples of 3NC packing endings and their Product Type Name suffix

The NXP label on the reel's 'pizzabox' shows the Product Type Name and 12NC, e.g. TJA1145T/FD and 9353 014 17118.

The datasheet for the new TJA1145A product variants is TJA1145A and includes Product Types:

- TJA1145AT/0 in SO package➔T
- TJA1145AT/FD/0 (FD variant of the product, explained in the datasheet, in SO package➔T)
- TJA1145ATK/0 in leadless HVSON package➔TK
- TJA1145TAK/FD/0 (FD variant of the product, explained in the datasheet, in leadless HVSON package➔TK)

The /0 indicates the first revision for these products. Should in future a new-12NC be required for these products, the /0 will be increased to /1. In the datasheet the product names without this revision number /0 are documented. Also see the explanation on the product marking in Section 10. Note that due to space restrictions the Product Type Name on the 1st line of marking will have to be truncated.

All these TJA1145A product variants are only available in reel packing with a Moisture Barrier Bag (MBB, 3NC=431 ending).

## Appendix 2: SDI pin input behavior

The non-A TJA1145 has a high-impedance (floating) input pin SDI. When Standby mode (or Sleep mode with VIO supplied) was used as low-power mode for the application, and if the MCU pin connected to the SDI signal was floating as well, an external pull-up or pull-down resistor had to be added.

Following a general microcontroller trend to turn off ports completely during lower-power mode, the TJA1145A has been upgraded. With the new TJA1145A such external resistor is no longer needed, because there is an internal, automatic pull-up/down resistor at the SDI pin. The internal resistor polarity follows the signal applied to the pin:

- While a high level is applied, the internal pull-up is activated.
- While a low level is applied, the internal pull-down is activated. When the applied level changes, the resistor configuration changes as well.

This means that any external pull-up or pull-down resistor on the PCB does not have to be populated anymore. Or, if a pull-up or -down source in the MCU was used, that one can now be turned off.

If there is an external pull-up or pull-down resistor, it could build a voltage divider together with the internal resistor, while both are pulling to opposite directions. Such situation has been illustrated in the upper part of Figure 18. To avoid permanent cross current created by such condition, the resulting level at pin SDI should be above / below the switching threshold voltage $V_{th(sw),}$ when the external resistor is pulling high / low, respectively. Then the internal resistor direction will automatically adapt to the external resistor configuration, like illustrated in the lower part of Figure 18. For the example of an external pull-down resistor $R_{ext}$, the corresponding condition is:

$$R_{ext} / (R_{ext} + R_{pu(SDI),min}) \times V_{VIO} < V_{th(SW),min}$$

With $V_{th(SW),min} = 0.25 \times V_{VIO}$, the condition for $R_{ext}$ can be calculated as:

$$R_{ext} < 0.25 \times (R_{ext} + R_{pu(SDI),min})$$

$$0.75 \times R_{ext} < 0.25 \times R_{pu(SDI),min}$$

$$R_{ext} < 1/3 \times R_{pu(SDI),min} = 1/3 \times 40\ k\Omega = 13.3\ k\Omega$$

Due to the symmetric specifications of $V_{th(SW)}$ min/max values and identical min values for $R_{pu(SDI)}$ and $R_{pd(SDI)}$, the very same result can be calculated for the case of an external pull-up resistor $R_{ext}$.

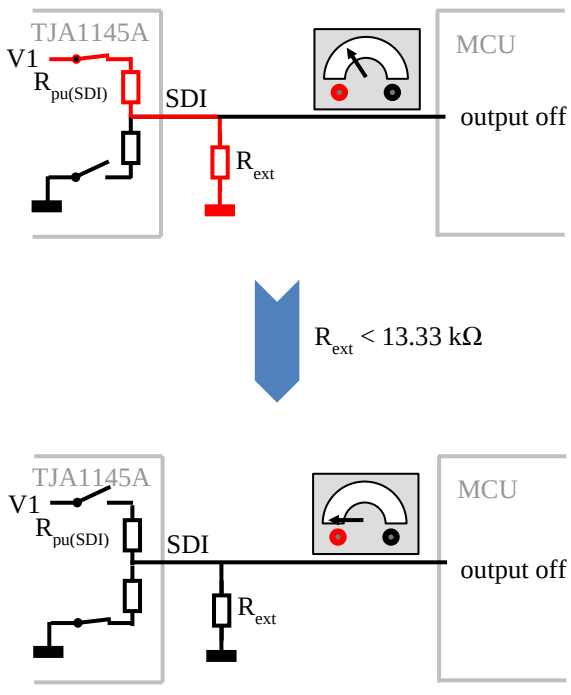



**Figure 18**: Example of an application with an external pull-down resistor Rext.

In other words: when there is an external pull-up or pull-down resistor with lower resistance than 13.33 kΩ, there is no conflict between that one and the internal automatic resistor. The automatic resistor will simply pull to the same direction. Then it does not matter if the external resistor is kept or omitted.

However, when that external resistor has higher impedance than 13.33 kΩ, the external resistor should be omitted. Otherwise a situation could occur where internal resistor and external resistor are pulling into opposite directions, i.e. the quiescent current would increase. The same applies, when instead of an external resistor component an MCU-internal pull-up or pull-down resistor with more than 13.33 kΩ was activated.

Figure 19 illustrates which application circuitry at the SDI signal is recommended, and which is not. For simplification, only examples with external pull-down resistor are shown. Equivalent rules would apply for a pull-up resistor.

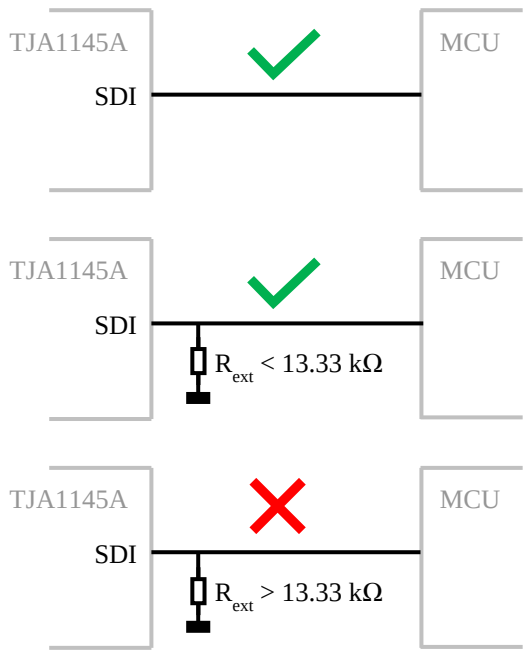



**Figure 19**: Examples for recommended (✓) and not recommended (x) application circuitry at SDI signal. Note that the non-recommendation (x) only applies, when Standby mode is used as low-power mode, i.e. when the MCU supply stays on.

## Appendix 3: FSMS/PNFDE bits in the TJA1145 datasheet

For product TJA1145 (not for the new product TJA1145A) the bits FSMS (Forced Sleep Mode Status) and PNFDE (Partial Networking Frame Detection Error) under specific conditions function slightly different than described in the datasheet. The datasheets for both TJA1145 and TJA1145A are the same w.r.t. the FSMS and PNFDE bits, and both describe the intended and correct behavior of these bits. Through minor digital design fixes product TJA1145A fully complies to the datasheet. Below information makes explicit what product TJA1145 (non-A) does w.r.t. the FSMS and PNFDE bits. References are to the TJA1145 datasheet (italic text is copied from the datasheet), and the yellow highlights indicate deviations from it for non-A product TJA1145 only.

**TJA1145 FSMS**

Section 7.1.1.3 Sleep mode:
*Status bit FSMS in the Main status register (Table 6) indicates whether a transition to Sleep mode was selected via an SPI command (FSMS = 0) or was forced by an undervoltage event on VCC or VIO (FSMS = 1). This bit can be read after the TJA1145 wakes up from Sleep mode to allow the settings of CWE, WPFE, WPRE and CPNC to be re-adjusted if an undervoltage event forced the transition to Sleep mode (FSMS = 1).*

Real TJA1145 behavior is that FSMS=1 only in case there is no local/remote wake-up.

Section 7.11 $V_{CC}$/$V_{IO}$ undervoltage protection:
*Status bit FSMS is set to 1 when a transition to Sleep mode is forced by an undervoltage event (see Table 6). This bit can be sampled after the TJA1145 wakes up from Sleep mode to allow the settings of CWE, WPFE, WPRE and CPNC to be re-adjusted if an undervoltage event forced the transition to Sleep mode (FSMS = 1).*

Like above, real TJA1145 behavior is that FSMS=1 only in case there is no local/remote wake-up.

**Table 31. Register bit settings in TJA1145 operating modes**

| Symbol | Off (reset values) | Standby | Normal | Sleep | Overtemp | Forced Sleep (uv) |
|---|---|---|---|---|---|---|
| FSMS | 0 | no change | no change | 0 | no change | 1 |

In Table 31 on page 33 'no change' for Standby mode is not correct, actual TJA1145 behavior for bit FSMS is:

- Forced sleep ➔ Standby by SPI mode change request : FSMS=1 ➔ FSMS=1 (correct behavior)
- Forced sleep ➔ Standby by local/remote wake-up : FSMS=1 ➔ FSMS=0 (incorrect behavior)
- Any other change to Standby ➔ no change : FSMS=0➔0 or FSMS=1➔1 (all correct behavior)

**TJA1145 PNFDE**

Section 7.1.1.3 Sleep mode:
*The TJA1145 will also be forced to switch to Sleep mode if a $V_{CC}$ of $V_{IO}$ undervoltage event is detected ($V_{CC}$/$V_{IO}$ < $V_{UVD(VCC)}$/$V_{UVD(VIO)}$ for longer than $t_{det(uv)(VCC)}$/$t_{det(uv)(VIO)}$). In this event, all pending wake-up events will be cleared. CAN wake-up (CWE = 1) and local wake-up via the WAKE pin (WPFE = WPRE = 1) are enabled in order to avoid a system deadlock (see Section 7.11) and selective wake-up is disabled (CPNC = 0).*

Real TJA1145 behavior is that bit PNFDE is not cleared.

Section 7.11 $V_{CC}$/$V_{IO}$ undervoltage protection (1st bullet point):
*All previously captured events (address range 0x61 to 0x64) are cleared before the TJA1145 switches to Sleep Mode to avoid repeated attempts to wake up while an undervoltage is present.*

Like above, real TJA1145 behavior is that bit PNFDE is not cleared.

**Table 31. Register bit settings in TJA1145 operating modes**

| Symbol | Off (reset values) | Standby | Normal | Sleep | Overtemp | Forced Sleep (uv) |
|---|---|---|---|---|---|---|
| PNFDE | 0 | no change | no change | no change | no change | 0 |

In Table 31 on page 33 '0' for Forced Sleep (uv) is not correct. The real TJA1145 behavior is not that bit FSMS is set to '0', but that bit FSMS is not changed (0➔0, 1➔1, incorrect behavior).

Since product TJA1145 will be discontinued, no changes will be made anymore to its datasheet.

## Appendix 4: Differences between SO package TJA1145AT(/FD) and leadless HVSON package TJA1145ATK(/FD)

In February of this year PCN 202001016F01 for the transition of the leadless HVSON package product TJA1145T**K**(/FD)➔ TJA1145AT**K**(/FD) was sent. This PCN 202002034F01 is for the transition of the SO package product TJA1145T(/FD)➔ TJA1145AT(/FD). The exact same die design is used in TJA1145T(/FD) and TJA1145T**K**(/FD). Likewise, the exact same die design is used in TJA1145AT(/FD) and TJA1145AT**K**(/FD).The design changes from the non-A- to the A-version silicon die are described in Chapter 6.

For practical NXP manufacturing (capacity) reasons TJA1145AT and TJA1145AT**K** do not have the same Bill-of-Material (BoM) and sourcing changes:

- TJA1145AT**K**(/FD) has transitioned from AuPd to Cu bondwire, but is still SSMC waferfab Single Source
- TJA1145AT(/FD) continues to use AuPd bondwire, but has transitioned to SSMC/VIS waferfab Dual Source

The consequence of the SO package TJA1145AT(/FD) using the exact same A-version silicon die as the leadless HVSON package TJA1145AT**K**(/FD) is that the bondpad and wafercoat openings on the A-version silicon die have been adapted to the Cu wire bonding of the leadless HVSON package TJA1145AT**K**(/FD). This has no impact on the AuPd wire bonding of TJA1145AT(/FD).

Table 7 below shows an overview of this.

| Topic | | TJA1145T(K)(/FD) | TJA1145AT(K)(/FD) | |
|---|---|---|---|---|
| CAN FD timing | | Up to 2 Mbit/s | Up to 5 Mbit/s, through a minor re-design of transmitter/receiver | |
| Short Wake-Up Pattern (WUP) wake-up time | | Not applicable | Applicable, through a minor digital design change | |
| Extended bus wake-up time-out time | | | | |
| Datasheet | | TJA1145 | TJA1145A:<br>- New/additional CAN FD specifications<br>- Compliance to ISO 11898-2:2016 and SAE J2284-1 till SAE J2284-5 | |
| Four design-related issues (see NXP CIN 201909013I) | | Applicable | Fully resolved, through minor design fixes | |
| | | | **TJA1145ATK(/FD)** | **TJA1145AT(/FD)** |
| Bill of Material (BoM) | | 25 µm AuPd bondwire<br>GE7470 Nold Compound | 25 µm bare Cu bondwire<br>EME-G700 Mold Compound | 25 µm AuPd bondwire<br>GE7470 Mold Compound |
| Diffusion waferfab sourcing | | Single Source SSMC | Single Source SSMC, Singapore | Dual Source SSMC-VIS (Vanguard International Semiconductor) |
| Classic HS-CAN IBEE EMC report | | Immunity RF fail | Pass, through a minor design change in the low-power receiver | Full pass with choke; without choke no pass but improvement through minor design change in low-power receiver |
| CAN FD IBEE EMC report | | N/A | Available, only CAN FD 2Mbit/s RF immunity pass | |
| CAN FD Phoenix EMC report | | N/A | Available, full pass of CAN FD 2Mbit/s | |
| Packing | | Reel in 'pizzabox', without Moisture Barrier Bag (MBB) | Reel in Moisture Barrier Bag (MBB), in 'pizzabox' | |
| Layout/design changes for robustness | Updated tiling algorithm | Not applicable | Applicable | |
| | Internal SDI pull-up/down resistors | | | |
| | Updated power routing to digital | | | |
| | Bondpad configuration optimized | For Au(Pd) bondwire | For Cu bondwire [1] | |
| | 50µm pull-back and enlarged wafercoat openings | Not applicable | Applicable [1] | |
| [1] TJA1145ATK (leadless HVSON package) and TJA1145AT (SO package) use the exact same die design. This implies that TJA1145AT with 25µm AuPd bondwire, although not strictly needed, uses the bondpad configuration further optimized for Cu bondwire and has the large wafercoat openings. | | | | |

**Table 7**: Overview of changes from TJA1145T(K)(/FD) to leadless HVSON package TJA1145AT**K**(/FD) and SO package TJA1145AT(/FD)