AH1014

Application Hints - Standalone high speed CAN transceiver TJA1042 / TJA1043 / TJA1048 / TJA1051

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Summary

The TJA1042, TJA1043, TJA1048, TJA1051 and their variants form the next generation of standalone high speed CAN transceivers from NXP Semiconductors.

The intention of this application hints document is to provide the necessary information for hardware and software designers for creation of automotive applications using the new high speed CAN transceiver generation products. It further on describes the advantages in terms of characteristics and functions offered to a system and how the system design can be simplified by replacing the 2nd by the 3rd generation HS-CAN transceivers from NXP.

Revision history

Rev	Date	Description
01.00	2010-04-30	Initial version
01.10	2010-12-01	Fig 26 Block diagram and pinning of the TJA1048 : new block diagram added with separate mode control Table 14 Average VCC supply current (assuming 500kbit/s) : TJA1048 also supports 10% VCC tolerance, re-calculation of buffer capacitance Chapter 10.3 added: Available CAN Simulation Models
1.20	2010-12-03	List of References updated – data sheets of TJA1042, TJA1043, TJA1048, TJA1051 and SBCs UJA107x changed to UJA107xA
1.30	2014-04-04	Chapter 6.9; Software flow (TJA1043): Figure 41 adapted Chapter 10.2.3; Upgrading Hints TJA1041A – TJA1043: new checkpoint inserted on transition from Low Power Mode to Normal Mode operation
1.40	2015-04-27	Chapter 6.6, Software flow (TJA1043) extended with alternative bus failure detection strategy

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Contents

1. Introduction 6
1.1 Standalone high speed CAN transceiver products 8
1.1.1 TJA1051 – Basic high speed CAN transceiver 8
1.1.2 TJA1042 – High speed CAN transceiver with Standby Mode 9
1.1.3 TJA1048 – Dual high speed CAN transceiver with Standby Mode 9
1.1.4 TJA1043 – High speed CAN transceiver with Sleep Mode and diagnostics 10
1.2 Integrated high speed CAN transceiver products 11
1.2.1 UJA107xA – Core System Basis Chip with integrated high speed CAN 11
1.2.2 UJA106x – Fail-safe System Basis Chip with integrated high speed CAN 11
2. Basics of high speed CAN applications 13
2.1 Example of a high speed CAN application 13
2.2 Power management depended high speed CAN transceiver selection 16
3. The TJA1051 – Basic high speed CAN transceiver 18
3.1 Main features 18
3.2 Operation modes 20
3.2.1 Normal Mode 20
3.2.2 Silent Mode 21
3.2.3 OFF Mode 21
3.3 System fail-safe features 22
3.3.1 TXD dominant clamping detection in Normal Mode 22
3.3.2 Bus dominant clamping prevention at entering Normal Mode 22
3.3.3 Undervoltage detection & recovery 23
3.4 Hardware application 23
4. The TJA1042 – High speed CAN transceiver with Standby Mode 26
4.1 Main features 26
4.2 Operation modes 28
4.2.1 Normal Mode 28
4.2.2 Standby Mode 29
4.2.3 OFF Mode 29
4.3 System fail-safe features 30
4.3.1 TXD dominant clamping detection in Normal Mode 30
4.3.2 Bus dominant clamping prevention at entering Normal Mode 30
4.3.3 Bus dominant clamping detection in Standby Mode 30
4.3.4 Undervoltage detection & recovery 32
4.4 Hardware application 32
5. The TJA1048 – Dual high speed CAN transceiver with Standby Mode 35
5.1 Main features 35
5.2 Operating modes 36
5.2.1 Normal Mode 36
5.2.2 Standby Mode 37
5.2.3 OFF Mode 37
5.3 Remote Wake-up (via CAN bus) 38
5.4 System fail-safe features 39
5.4.1 TXD dominant clamping detection in Normal Mode 39
5.4.2 Bus dominant clamping prevention at entering Normal Mode 39
5.4.3 Undervoltage detection & recovery 40
5.5 Hardware application 41

continued >>

6. The TJA1043 – High speed CAN transceiver with Sleep Mode & diagnostics 42
6.1 Main features 42
6.2 Operating modes 44
6.2.1 Normal Mode 45
6.2.2 Listen-only Mode 45
6.2.3 Standby Mode 46
6.2.4 Sleep Mode 46
6.2.5 Go-to-Sleep Mode 47
6.3 Hardware application 49
6.4 Wakeup detection 51
6.5 Flag signaling 53
6.6 Bus failure diagnosis 55
6.7 Local failure diagnosis 59
6.8 Undervoltage detection & recovery 62
6.9 Software 65
7. Hardware application of common pins 72
7.1 Power Supply Pins 72
7.1.1 V_{CC} pin 72
7.1.2 Thermal load consideration for the V_{CC} voltage regulator 72
7.1.3 Dimensioning the bypass capacitor of the voltage regulator 73
7.1.4 V_{IO} pin 74
7.2 Interface Pins 75
7.2.1 TXD pin 75
7.2.2 RXD pin 75
7.3 Mode control pins EN / STBN / STB / S 75
7.4 Bus Pins CANH / CANL 75
8. EMC aspects of high speed CAN 77
8.1 Common mode choke 77
8.2 Capacitors 78
8.3 ESD protection diodes 78
8.4 Power supply buffering 79
8.5 Split termination concept 79
8.6 Summary of EMC improvements 80
8.7 Common mode stabilization via SPLIT pin 80
8.8 GND offset and Common mode range 81
8.9 PCB layout rules (check list) 84
9. Bus network aspects of high speed CAN 85
9.1 Maximum number of nodes 85
9.2 Maximum bus line length 87
9.3 Topology 88
10. Appendix 90
10.1 Pin FMEA 90
10.1.1 TJA1051 90
10.1.2 TJA1042 93
10.1.3 TJA1048 95
10.1.4 TJA1043 98
10.2 Upgrading hints 101
10.2.1 TJA1050 – TJA1051 101
10.2.2 TJA1040 – TJA1042 105

continued >>

10.2.3 TJA1041A – TJA1043 108
10.3 Simulation models 116
11. Abbreviations 117
12. References 118
13. Legal information 120
13.1 Definitions 120
13.2 Disclaimers 120

continued >>

1. Introduction

The TJA1042, TJA1043, TJA1048 and TJA1051 and their variants TJA1042/3, TJA1051/3 and TJA1051/E are the next step up from the NXP Semiconductors high speed CAN transceivers TJA1040, TJA1041A and TJA1050 (see Fig 1).

All transceivers provide the physical link between the protocol controller and the physical transmission medium according to the ISO11898 ([18], [19]) and SAE J2284 [20]. This ensures full interoperability with other ISO11898 compliant transceiver products.

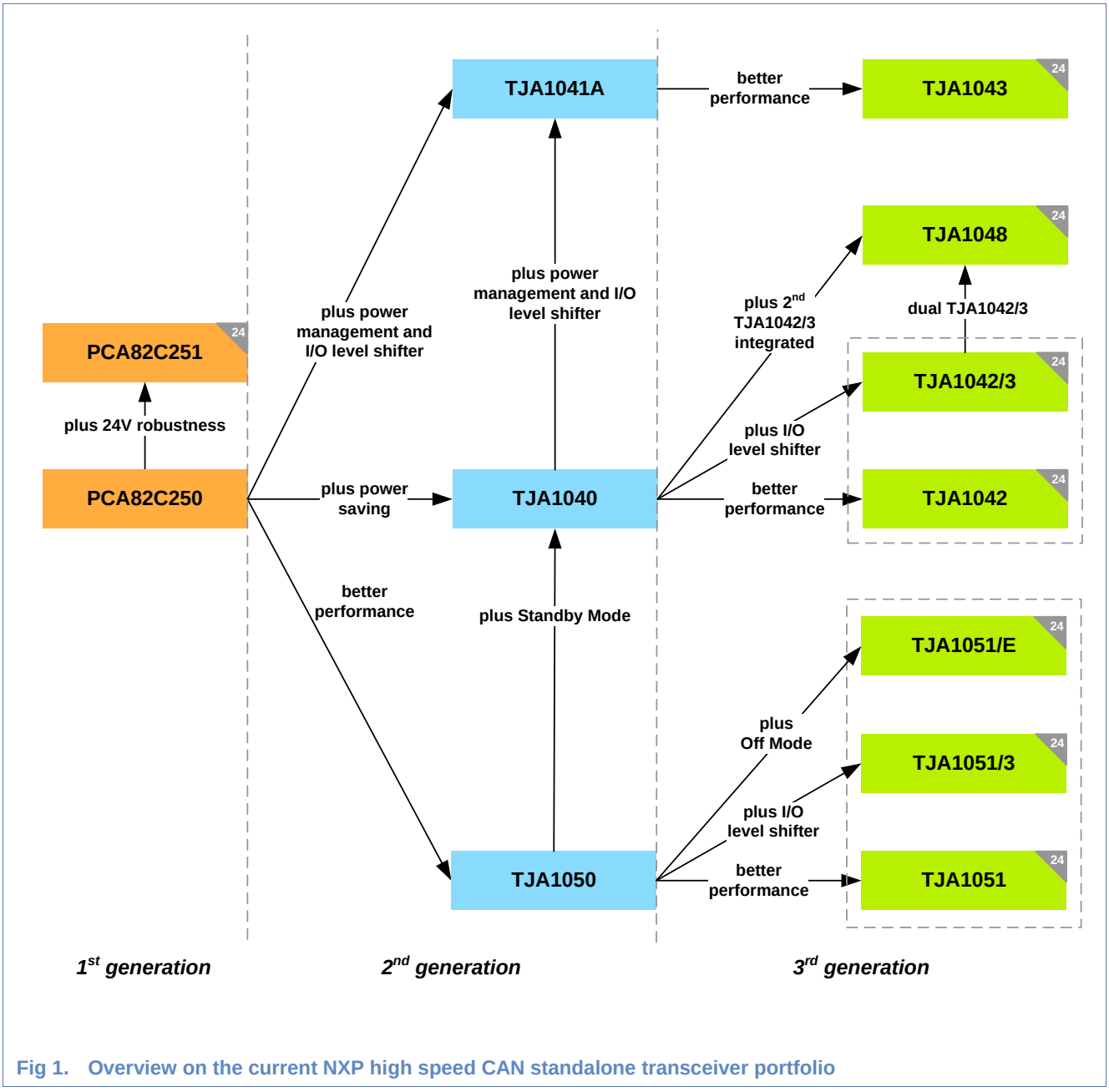


Fig 1. Overview on the current NXP high speed CAN standalone transceiver portfolio

Beside three versions offering a 100% drop-in replacement (TJA1042, TJA1043 and TJA1051) to their predecessor (TJA1040, TJA1041(A) and TJA1050) three new versions are introduced in the 3rd generation. The new TJA1042/3 and TJA1051/3 allow interfacing to 3V microcontrollers via a new introduced V_{IO} pin. The new TJA1051/E offers a dedicated Off Mode to completely disable the transceiver. The TJA1048 offers two integrated TJA1042/3 blocks and thus is the new dual high speed CAN standalone transceiver solution from NXP Semiconductors.

Compared to their functional predecessors the 3rd generation high speed CAN transceivers from NXP Semiconductors offer

- a significantly improved ESD robustness,
- a further reduction in electromagnetic emission (EME)
- beside an improved electromagnetic immunity (EMI),
- a higher voltage robustness in order to full support 24V applications
- and a predictable undervoltage behavior at all supply conditions

With the extended portfolio of high speed CAN transceivers NXP Semiconductors enables ECU designers to find the best application fitting standalone transceiver product in order to cover all main application specific requirements.

For full coverage NXP Semiconductors offers integrated high speed CAN transceivers in their System Basis Chip Families UJA106x and UJA107x.

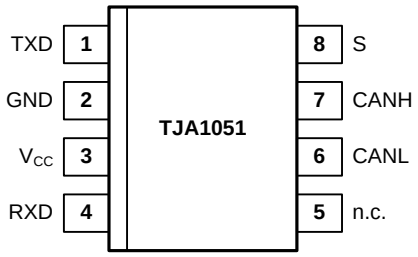
			Modes					Fail-safe features						Wake-up			
HSCAN device	No. of pins	No. of CAN channels	Normal	Listen-only	Standby	Sleep	Off	TXD dominant timer	Bus dominant timer	Undervoltage detection	Short circuit protection	Temperature protection	Error detection	Remote via CAN	Local via WAKE	Host Interface	SPLIT pin
TJA1051	8	1	√	√				√		√	√	√				5V	
TJA1051/3	8	1	√	√				√		√	√	√				3-5V	
TJA1051/E	8	1	√	√			√	√		√	√	√				5V	
TJA1042	8	1	√		√			√	√	√	√	√		√		5V	√
TJA1042/3	8	1	√		√			√	√	√	√	√		√		3-5V	
TJA1048	14	2	√		√			√		√	√	√		√		3-5V	
TJA1043	14	1	√	√	√	√		√		√	√	√	√	√	√	3-5V	√

Fig 2. Feature overview of 3rd generation high speed CAN standalone transceiver portfolio

1.1 Standalone high speed CAN transceiver products

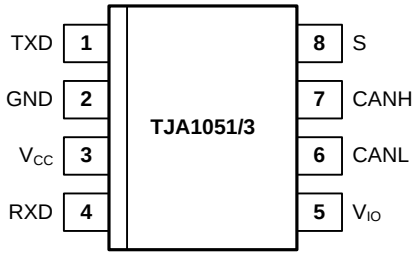
1.1.1 TJA1051 – Basic high speed CAN transceiver

TJA1051 – Basic high speed CAN transceiver *(page 18 ff.)*



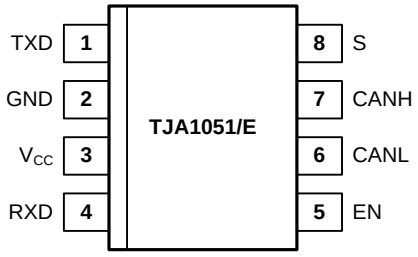
- Successor of the TJA1050 basic high speed CAN transceiver
- Normal Mode (transmit / receive CAN data)
- Silent Mode (receiving CAN data only)
- Undervoltage detection on pin V_{CC}

TJA1051/3 – Basic high speed CAN transceiver with 3V microcontroller interface *(page 18 ff.)*



- Variant of the TJA1051 basic high speed CAN transceiver including:
- Direct interfacing to microcontrollers with 3V to 5V supply voltage
- Undervoltage detection on pin V_{IO}

TJA1051/E – Basic high speed CAN transceiver with Off Mode *(page 18 ff.)*

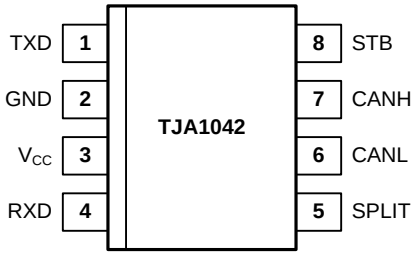


- Variant of the TJA1051 basic high speed CAN transceiver including:
- Off Mode (disabled transceiver with zero bus load)

Fig 3. Pin configuration and short functional description of the TJA1051, TJA1051/3 and TJA1051/E

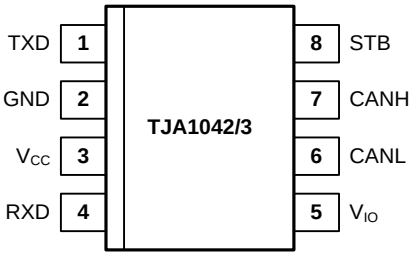
1.1.2 TJA1042 – High speed CAN transceiver with Standby Mode

TJA1042 – High speed CAN transceiver with Standby Mode *(page 26 ff.)*



- Successor of the TJA1040 high speed CAN transceiver
- Normal Mode (transmit / receive CAN data)
- Standby Mode (low power mode with CAN wake-up capability)
- SPLIT pin for recessive bus level stabilization
- Bus dominant time-out function in Standby Mode
- Undervoltage detection on pin V_{CC}

TJA1042/3 – High speed CAN transceiver with Standby Mode and 3V microcontroller interface *(page 26 ff.)*



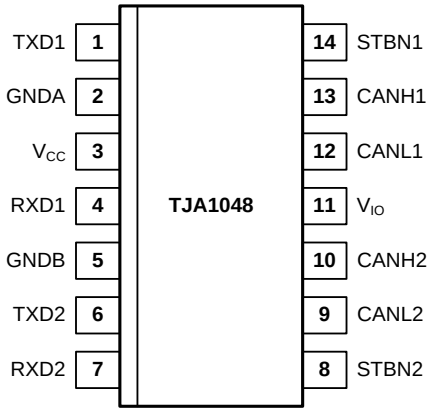
- Variant of the TJA1042 high speed CAN transceiver including:

- Direct interfacing to microcontrollers with 3V to 5V supply voltage
- Low power receiver supply in Standby Mode by V_{IO} only
- Undervoltage detection on pin V_{IO}
- No SPLIT pin for recessive bus level stabilization

Fig 4. Pin configuration and short functional description of the TJA1042 and TJA1042/3

1.1.3 TJA1048 – Dual high speed CAN transceiver with Standby Mode

TJA1048 – Dual high speed CAN transceiver with Standby Mode *(page 34 ff.)*

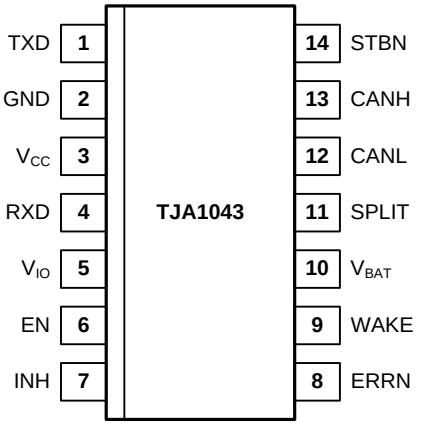


- Dual CAN transceiver based on TJA1042/3
- Normal Mode (transmit / receive CAN data)
- Standby Mode (low power mode with CAN wake-up capability)
- Channel independent mode control
- Direct interfacing to microcontrollers with 3V to 5V supply voltage
- Low power receiver supply in Standby Mode by V_{IO} only
- Undervoltage detection on pins V_{CC} and V_{IO}
- Enhanced CAN wake-up pattern

Fig 5. Pin configuration and short functional description of the TJA1048

1.1.4 TJA1043 – High speed CAN transceiver with Sleep Mode and diagnostics

TJA1043 – High speed CAN transceiver with Sleep Mode and diagnostics *(page 42 ff.)*



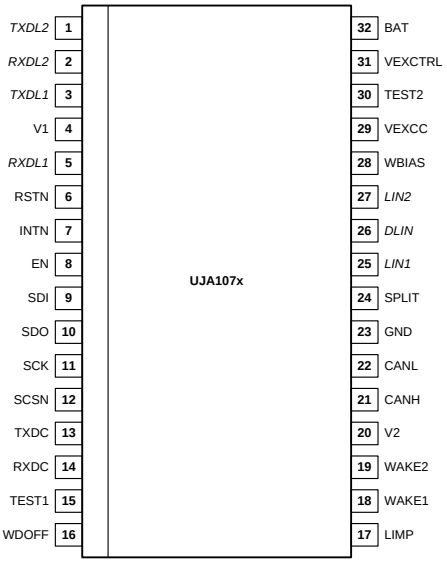
- Successor of the TJA1041A high speed CAN transceiver
- Normal Mode (transmit / receive CAN data)
- Listen-only Mode (receiving CAN data only)
- Standby Mode (first-level low power mode – INH on)
- Sleep Mode (second-level low power mode – INH off)
- Local and remote wake-up with wake-up source recognition
- Direct interfacing to microcontrollers with 3V to 5V supply voltage
- SPLIT pin for recessive bus level stabilization
- Undervoltage detection on pins V_{BAT}, V_{CC} and V_{IO}
- Several protection and diagnostic functions

Fig 6. Pin configuration and short functional description of the TJA1043

1.2 Integrated high speed CAN transceiver products

1.2.1 UJA107xA – Core System Basis Chip with integrated high speed CAN

UJA107xA – Core System Basis Chip with integrated high speed CAN transceiver



The core System Basis Chip (SBC) family replaces basis discrete components commonly found in ECUs:

- Advanced independent watchdog
- 250mA voltage regulator (150mA internal, scalable with PNP)
- Integrated voltage regulator for CAN
- Serial peripheral interface (SPI)
- 2 local wake-up input ports
- Limp home output port
- Advanced low-power concept
- Safe and controlled system start-up behavior
- Detailed status reporting on system and sub-system levels

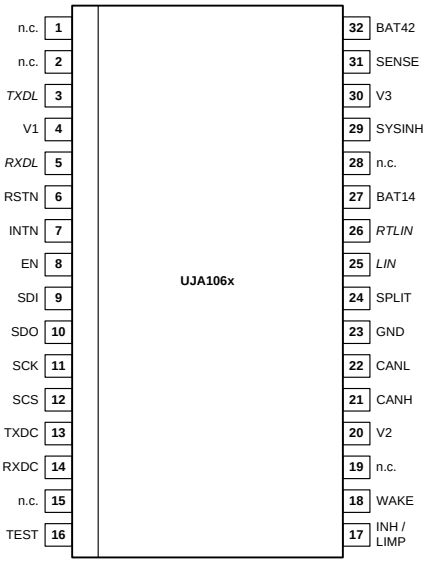
High speed CAN variants:

- UJA1075A / High speed CAN / LIN core SBC [15]
- UJA1076A / High speed CAN core SBC [16]
- UJA1078A / High speed CAN / dual LIN core SBC [17]

Fig 7. Pin configuration and short functional description of the UJA107xA

1.2.2 UJA106x – Fail-safe System Basis Chip with integrated high speed CAN

UJA106x – Fail-safe System Basis Chip with integrated high speed CAN transceiver



The fail-safe System Basis Chip (SBC) family replaces basis discrete components commonly found in ECUs:

- Advanced independent watchdog
- Voltage regulators for microcontroller and CAN transceiver
- Serial peripheral interface (SPI)
- Local wake-up input port
- Inhibit/Limp home output port
- Advanced low-power concept
- Safe and controlled system start-up behavior
- Advanced fail-safe system behavior that prevents any deadlock
- Detailed status reporting on system and sub-system levels

High speed CAN variants:

- UJA1065 / High speed CAN / LIN fail-safe SBC [13]
- UJA1066 / High speed CAN fail-safe SBC [14]

Fig 8. Pin configuration and short functional description of the UJA106x

2. Basics of high speed CAN applications

2.1 Example of a high speed CAN application

Fig 9 illustrates an example of a high speed CAN application. Several ECUs (Electronic Control Units) are connected via stubs to a linear bus topology. Each bus end is terminated with 120Ω (R_T), resulting in the nominal 60Ω bus load according to ISO11898. The figure shows the split termination concept, which is helpful when improving the EMC of high speed CAN bus systems. The former single 120Ω termination resistor is split into two resistors of half value ($R_T/2$) with the center tap connected to ground via the capacitor C_{spl}.

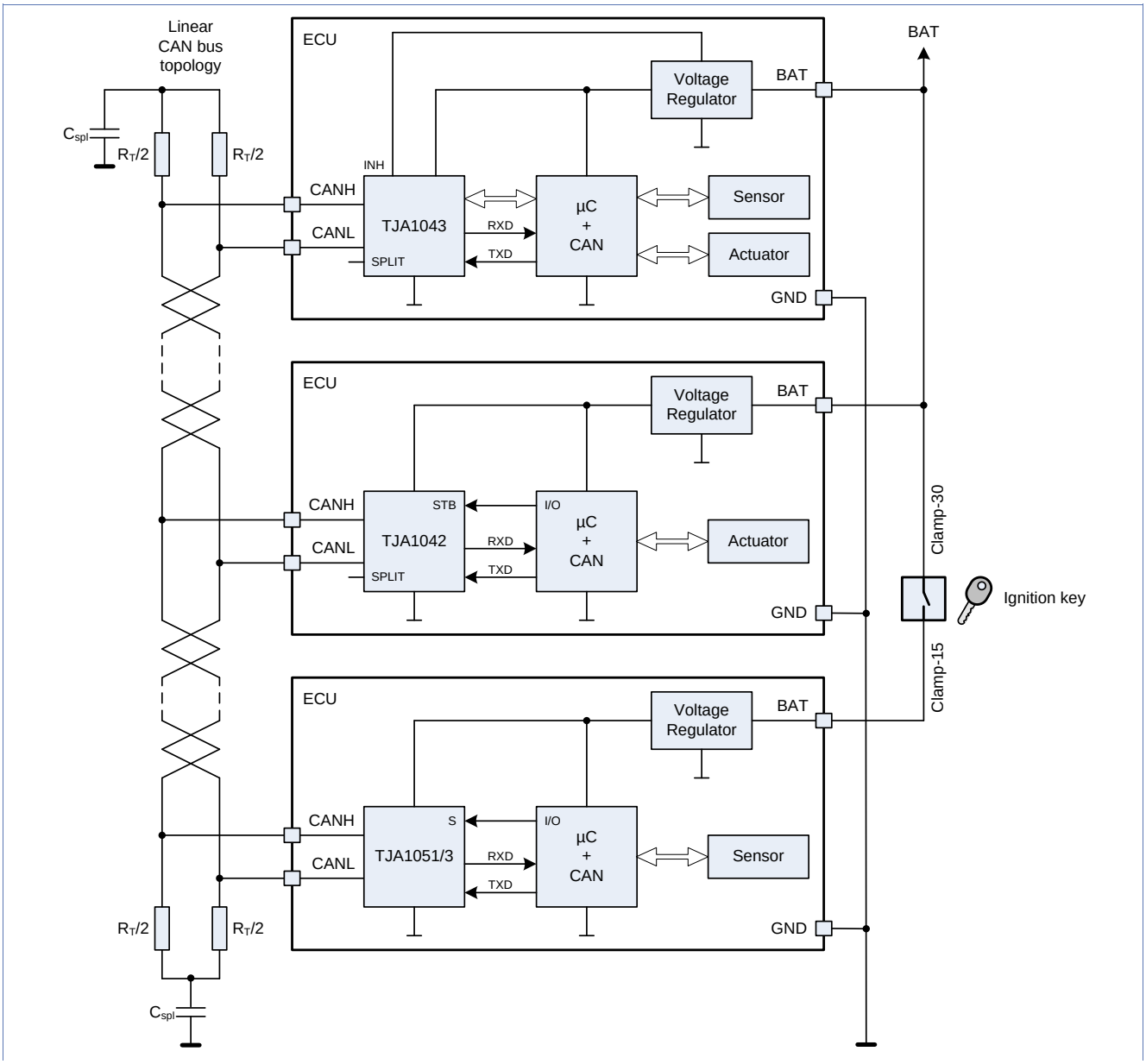


Fig 9. High speed CAN application example

The block diagram in Fig 9 describes the internal structure of an ECU. Typically, an ECU consists of a standalone transceiver (here the TJA1042, TJA1043 and TJA1051/E) and a host microcontroller with integrated CAN-controller, which are supplied by one or more voltage regulators. While the high speed CAN transceiver needs a +5 V supply to support the ISO11898 bus levels, new microcontroller products are increasingly using lower supply voltages like 3,3 V. In this case a dedicated 3,3 V voltage regulator is necessary for the microcontroller. The protocol controller is connected to the transceiver via a serial data output line (TXD) and a serial data input line (RXD). The transceiver is attached to the bus lines via its two bus terminals CANH and CANL, which provide differential receive and transmit capability.

Depending on the selected transceiver different mode control pins (e.g. STB, S, EN) are connected to I/O pins of the host microcontroller for operation mode control. The split termination approach can be further improved using the pin SPLIT of the TJA1042 or TJA1043 for DC stabilization of the common mode voltage (see Section 7.1).

In the case of the TJA1043 there is an additional INH signal line (indicated in Fig 9) controlling the voltage regulator. Leaving control over the voltage regulator(s) for V_{CC} and µC supply voltage to the TJA1043 allows for an extremely low ECU quiescent current as required in Clamp-30 applications (see Section 1.1).

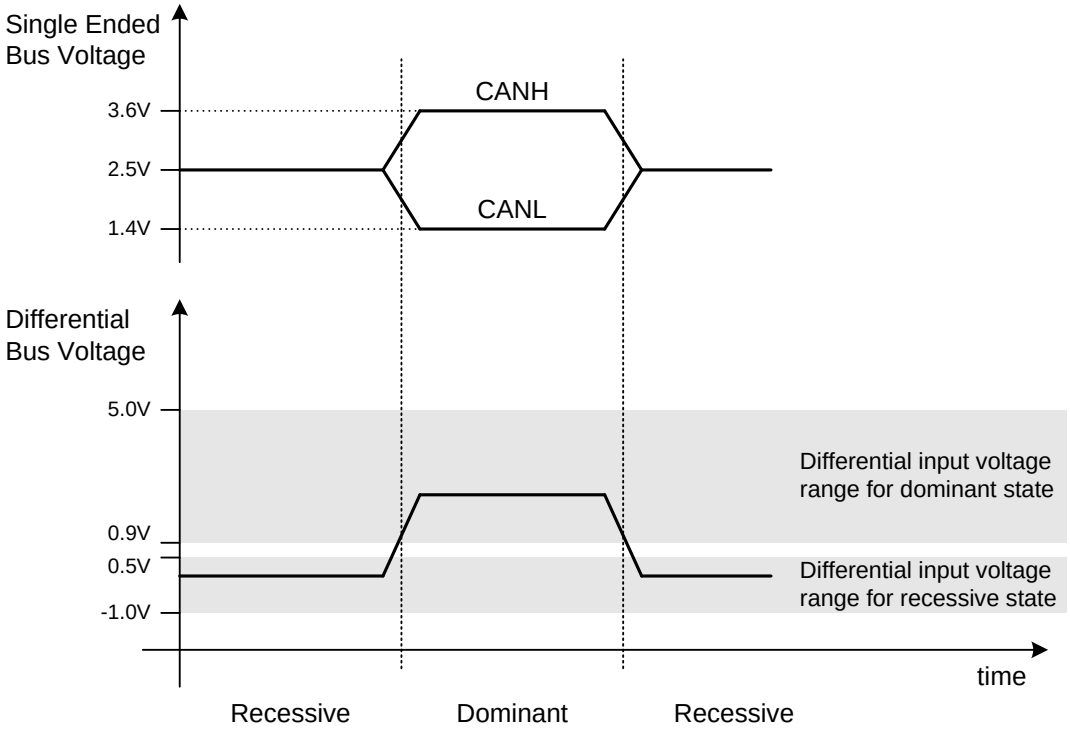


Fig 10. Nominal bus levels according to ISO11898

The protocol controller outputs a serial transmit data stream to the TXD input of the transceiver. An internal pull-up function within each NXP high speed CAN transceiver sets the TXD input to logic HIGH, which means that the bus output driver stays recessive in the case of a TXD open circuit condition. In the recessive state (Fig 10) the CANH and CANL pins are biased to a voltage level of $V_{CC}/2$. If a logic LOW level is applied to TXD, the output stage is activated, generating a dominant state on the bus line (Fig 10). The output driver CANH provides a source output from V_{CC} and the output driver CANL a sink output towards GND. This is illustrated in Fig 11 showing the high speed CAN driver block diagram.

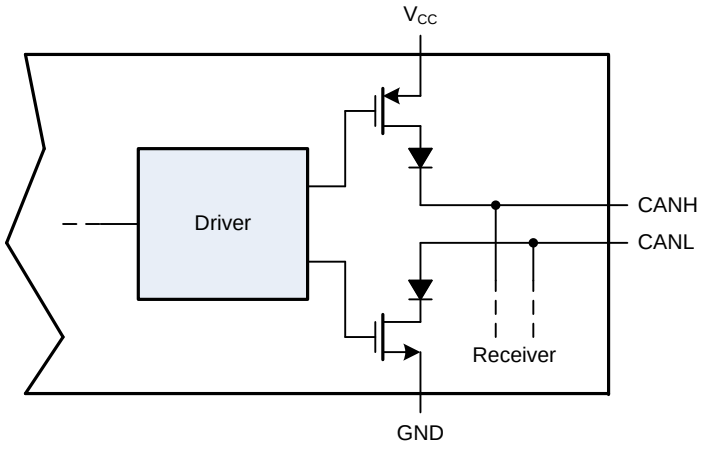


Fig 11. High speed CAN driver block diagram

If no bus node transmits a dominant bit, the bus stays in recessive state. If one or multiple bus nodes transmit a dominant bit, then the bus lines enter the dominant state overriding the recessive state (wired-AND characteristic).

The receiver converts the differential bus signal to a logic level signal, which is output at RXD. The serial receive data stream is provided to the bus protocol controller for decoding. The internal receiver comparator is always active. It monitors the bus while the bus node is transmitting a message. This is required to support the non-destructive bit-by-bit arbitration scheme of CAN.

2.2 Power management depended high speed CAN transceiver selection

In-vehicle high speed CAN networks come with different requirements, depending on the implemented application. First of all, high speed CAN is the ideal choice for all applications which require a high data throughput (up to 1 Mbit/s).

From the ECU power management point of view four different application areas can be distinguished.

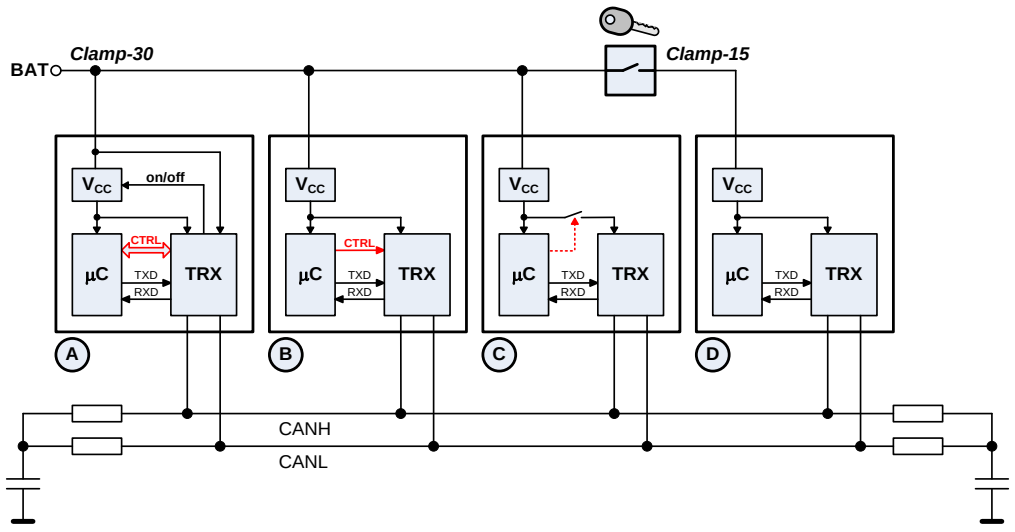


Fig 12. Target applications for HSCAN transceivers

Type A – Available all time - Applications, which have to be available all time, even when the car is parked and ignition-key is off, are permanently supplied from a permanent battery supply line, often called “Clamp-30”. However, those nodes need the possibility to reduce the current consumption for power saving by control of the local ECU supply (V_{CC}). These type A applications allow switching off the entire supply system of the ECU including the microcontroller supply while keeping the wake-up capability via CAN possible.

The TJA1043 is the first choice for these applications. It can be put into its Sleep Mode (all V_{CC} and V_{IO} supplies off), which allows reducing the total current consumption of the entire ECU down to typically 20uA, while keeping the capability to receive wake-up events from the bus and to restart the application.

Type B – Always active microcontroller - Those applications, which need an always-active microcontroller, are permanently supplied from the battery supply line “Clamp-30” using a continuously active V_{CC} supply. In order to reduce the ECU power consumption, the transceiver needs to be set into a mode with reduced supply current while its supply stays active.

Here the Standby Mode of the TJA1042, TJA1042/3 and TJA1048 offers the best choice. During Standby Mode the device reduces the transceiver supply current (via VCC and VIO) to a minimum, while still monitoring the CAN bus lines for bus traffic.

If monitoring the bus traffic is not required the TJA1051/E is the best selection. The TJA1051/E can be switched into Off Mode. During Off Mode the device reduces the transceiver supply current (as in Standby Mode of the TJA1042) and additionally disengages from the bus (zero load).

Type C – Always active microcontroller & controlled transceiver supply - Dedicated applications, which need an always-active microcontroller and therefore are permanently supplied from the “Clamp-30” line, additionally come with a microcontroller controlled transceiver voltage supply. In contrast to type B applications, further current can be saved, because the transceiver becomes completely un-powered by microcontroller control. These applications require absolute passive bus behavior of the transceiver, while its voltage supply is inactive. This is important in order not to affect the remaining bus system, which might continue communication.

Most suitable for such kind of applications are the TJA1042 variants, the TJA1051 variants as well as the TJA1048. All named HSCAN transceiver types disengage from the bus, if unpowered and thus behave absolutely passive.

Type D – Only active at ignition-key switched on - Applications, which do not need to be available with ignition-key off, are simply switched off and become totally un-powered during ignition-key off. They are supplied from a switched battery supply line, often called “Clamp-15”. This supply line is only switched on with ignition-key on. Depending on system requirements, e.g. partial communication of the still supplied nodes during ignition-key off, these un-powered nodes need to behave passively towards the remaining bus, similar to type C applications.

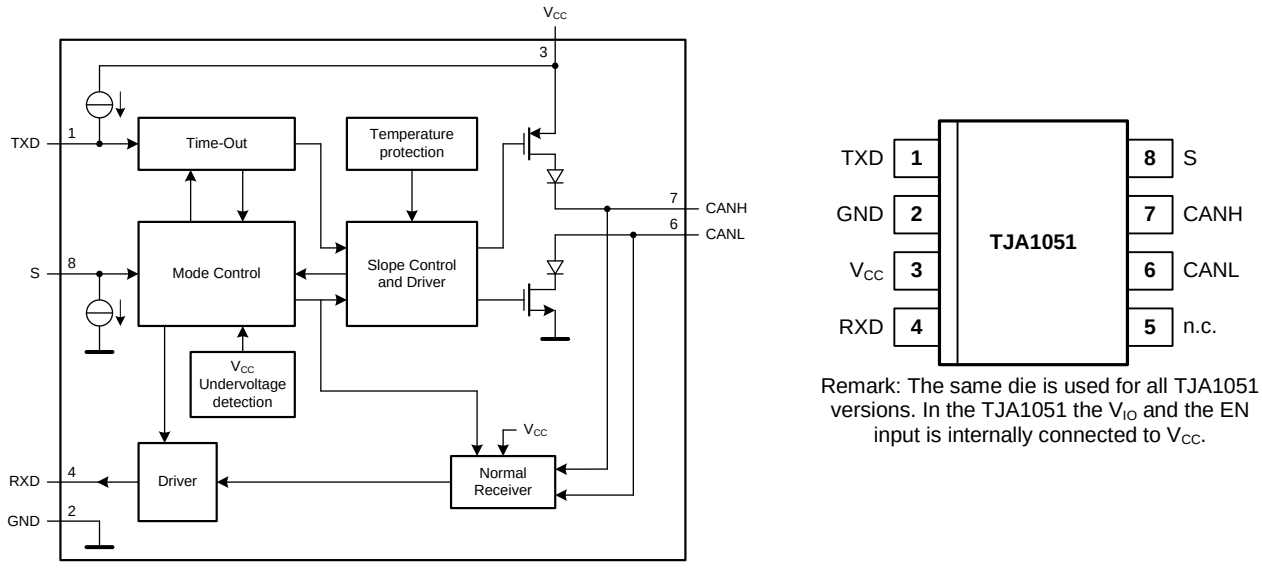
As for type C applications, it is recommended to use the TJA1042 variants, the TJA1051 variants as well as the TJA1048 due to their absolutely passive behavior to the bus when becoming unpowered.

3. The TJA1051 – Basic high speed CAN transceiver

3.1 Main features

The TJA1051 is the basic high speed CAN transceiver is being delivered in three versions, distinguished only by the function of pin 5:

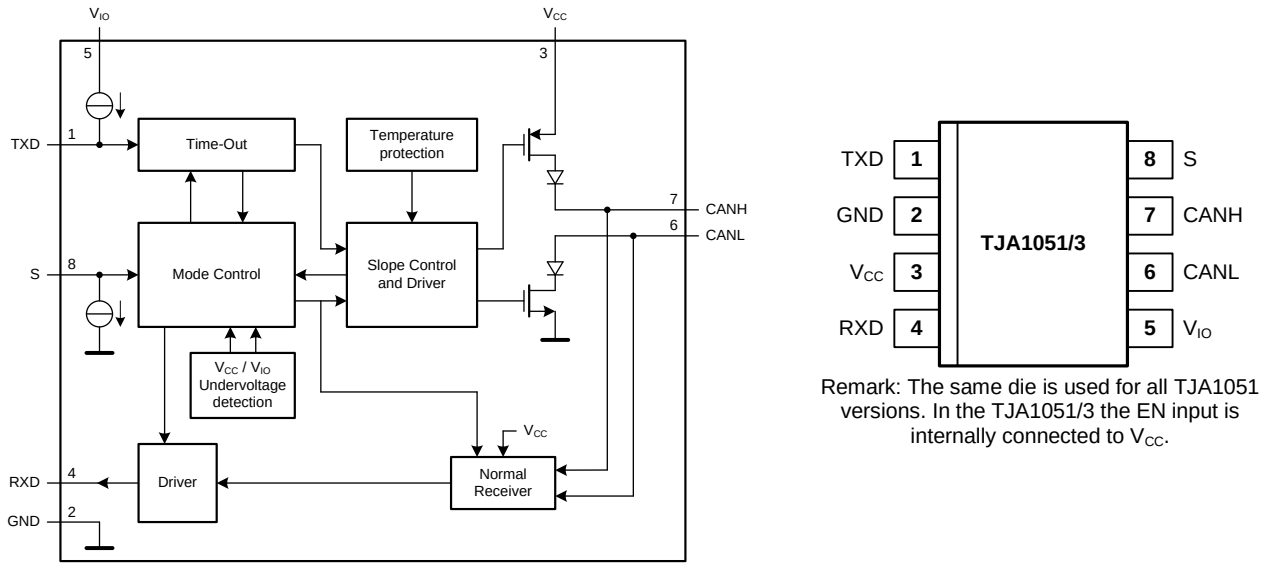
- TJA1051 – the version with pin 5 open (n.c.) is 100% backwards compatible with the TJA1050:



Remark: The same die is used for all TJA1051 versions. In the TJA1051 the V_{IO} and the EN input is internally connected to V_{CC}.

Fig 13. Block diagram and pinning of the TJA1051

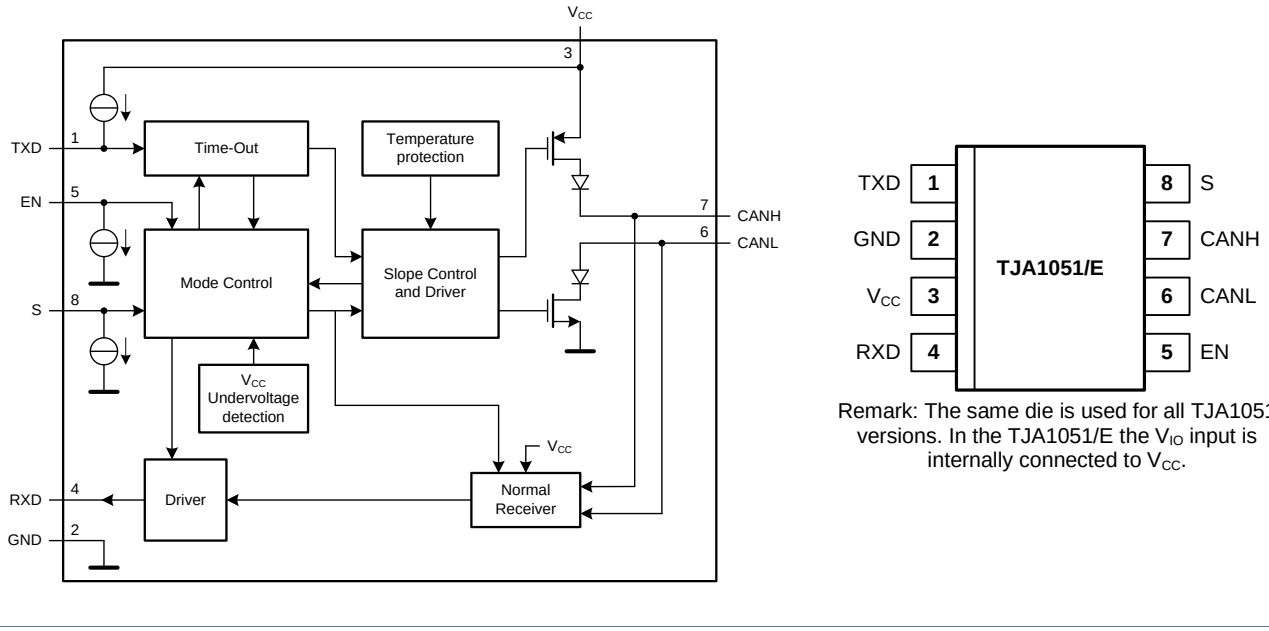
- TJA1051/3 – the version with a V_{IO} pin allows for direct interfacing to microcontrollers with supply voltages down to 3V:



Remark: The same die is used for all TJA1051 versions. In the TJA1051/3 the EN input is internally connected to V_{CC}.

Fig 14. Block diagram and pinning of the TJA1051/3

- TJA1051/E – the version with a EN pin allows disabling the transceivers requiring lowest quiescent current with disengaging from the bus (zero load):

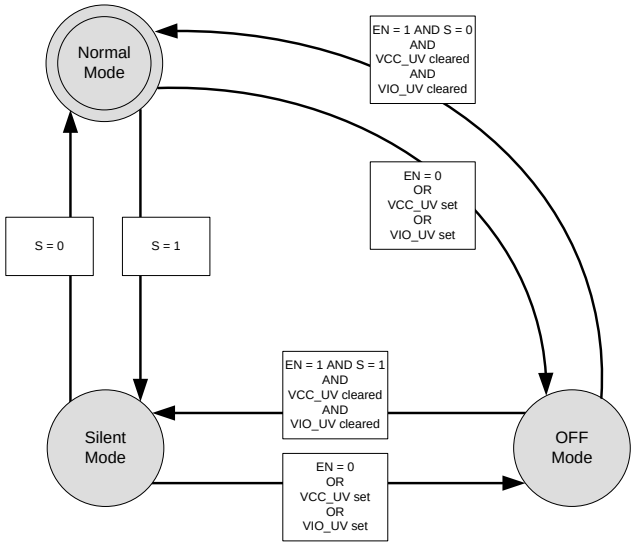


Remark: The same die is used for all TJA1051 versions. In the TJA1051/E the V_{IO} input is internally connected to V_{CC}.

Fig 15. Block diagram and pinning of the TJA1051/E

3.2 Operation modes

The TJA1051 offers 2 different power modes, Normal Mode and Silent Mode which are directly selectable. Taking into account the TJA1051/E with its EN input pin and the undervoltage detection a third power mode is available, the so-called OFF Mode. Fig 16 shows how the different operation modes can be entered. Every mode provides a certain behavior and terminates the CAN channel to a certain value. The following sub-chapters give a short overview of those features.



Remark: The same die is used for all TJA1051 versions.

- In the TJA1051 the V_{IO} and the EN input is internally connected to V_{CC}.
- In the TJA1051/3 the EN input is internally connected to V_{CC}.
- In the TJA1051/E the V_{IO} input is internally connected to V_{CC}.

Fig 16. State diagram TJA1051, TJA1051/3 and TJA1051/E

3.2.1 Normal Mode

In Normal Mode the CAN communication is enabled. The digital bit stream input at TXD is transferred into corresponding analog bus signals. Simultaneously, the transceiver monitors the bus, converting the analog bus signals into the corresponding digital bit stream output at RXD. The bus lines are biased to $V_{CC}/2$ in recessive state and the transmitter is enabled. The Normal Mode is entered setting pin S to LOW. Due to an internal pull-down function it is the default mode if pin S is unconnected.

In Normal Mode the transceiver provides following functions:

- The CAN transmitter is active.
- The CAN receiver is active.
- CANH and CANL are biased to $V_{CC}/2$.
- V_{CC} and V_{IO} undervoltage detectors are active for undervoltage detection.

3.2.2 Silent Mode

The Silent Mode is used to disable the transmitter of the TJA1051 regardless of the TXD input signal. In Silent Mode the TJA1051 is not capable of transmitting CAN messages, but all other functions, including the receiver, continue to operate. The Silent Mode is entered setting pin S to HIGH.

Babbling idiot protection

The Silent Mode allows a node to be set to a state, in which it is absolutely passive to the bus. It becomes necessary when a CAN-controller gets out of control and unintentionally sends messages (“Babbling idiot”), that block the bus. Activating the Silent Mode by the microcontroller allows the bus to be released even when there is no direct access from the microcontroller to the CAN-controller. The Silent Mode is very useful for achieving high system reliability required by today’s electronic applications.

Listen-only function

In Silent Mode RXD monitors the bus lines as usual. Thus, the Silent Mode provides a Listen-Only Mode for diagnostic features. It ensures that a node does not influence the bus with dominant bits.

In Silent Mode the transceiver provides following functions:

- The CAN transmitter is off.
- The CAN receiver is active.
- CANH and CANL are biased to $V_{CC}/2$.
- V_{CC} and V_{IO} undervoltage detectors are active for undervoltage detection.

3.2.3 OFF Mode

The non-operation OFF Mode is introduced offering total passive behaviour to the CAN bus system. The OFF Mode is entered by undervoltage detection on V_{CC} or V_{IO} (TJA1051/3 only) or by setting pin EN to LOW (TJA1051/E only). In OFF Mode the TJA1051 requires very low current for operation.

In OFF Mode the transceiver provides following functions:

- The CAN transmitter is off.
- The CAN receiver is off.
- CANH and CANL are floating (lowest leakage current on bus pins).
- V_{CC} and V_{IO} undervoltage detectors are active for undervoltage recovery.

Table 1. Characteristics of the different modes

Operating mode	S pin	EN pin	V_{CC} or V_{IO} undervolt.	RXD pin		Bus bias	TXD pin	CAN driver
				Low	High			
Normal	0	1	no	Bus dominant	Bus recessive	$V_{CC}/2$	0	dominant [1]
							1	recessive
Silent	1	1	no	Bus dominant	Bus recessive	$V_{CC}/2$	X	off
OFF	X	0	X	-	-	float	X	off
	X	X	yes					

[1] $t < t_{to(dom)TXD}$, afterwards the TXD dominant clamping detection disables the transmitter.

3.3 System fail-safe features

3.3.1 TXD dominant clamping detection in Normal Mode

The TXD dominant clamping detection prevents an erroneous CAN-controller from clamping the bus to dominant level by a continuously dominant TXD signal.

After a maximum allowable TXD dominant time $t_{to(dom)TXD}$ the transmitter is disabled. According to the CAN protocol only a maximum of eleven successive dominant bits are allowed on TXD (worst case of five successive dominant bits followed immediately by an error frame). Along with the minimum allowable TXD dominant time, this limits the minimum bit rate to 40 kbit/s.

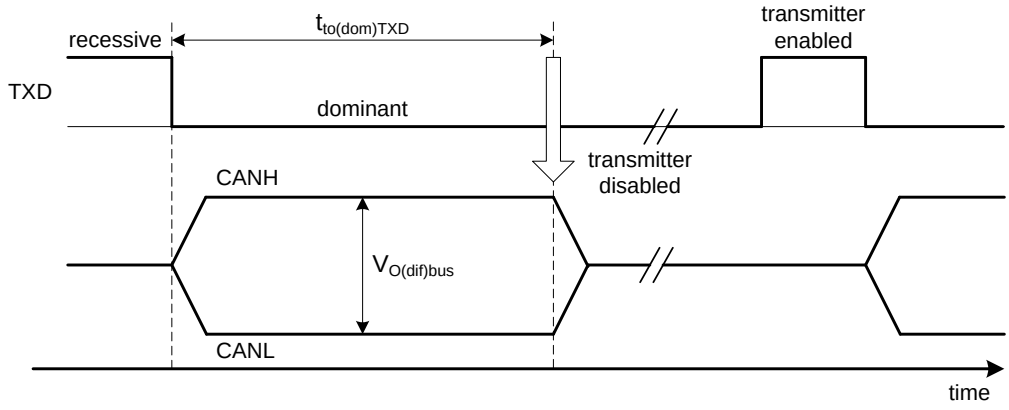


Fig 17. TXD dominant clamping in Normal Mode

3.3.2 Bus dominant clamping prevention at entering Normal Mode

Before transmitting the first dominant bit to the bus in Normal Mode the TXD pin once needs to be set HIGH in order to prevent a transceiver initially clamping the entire bus when starting up with not well defined TXD port setting of the microcontroller.

3.3.3 Undervoltage detection & recovery

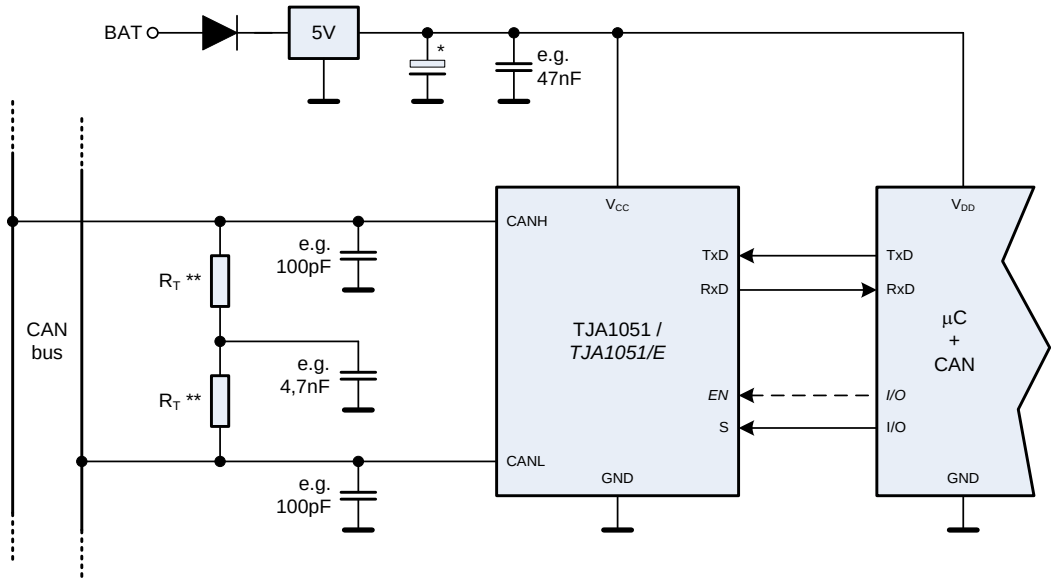
Compared to their predecessor TJA1050, the TJA1051 versions take advantage of high precision integrated undervoltage detection on their supply pins (see Table 2). Without this function undervoltage conditions might result in unwanted system behaviour, if the supply leaves the specified range. (e.g. the bus pins might bias to GND).

Table 2. Mode control at undervoltage conditions

Undervoltage condition		HS-CAN with Silent Mode		
V_{CC}	V_{IO}	TJA1051	TJA1051/3	TJA1051/E
no	no	Normal or Silent	Normal or Silent	Normal, Silent or Off
yes	no	Off	Off	Off
no	yes	not applicable	Off	not applicable
yes	yes	Off	Off	Off

3.4 Hardware application

Fig 18 and Fig 19 show how to integrate the TJA1051 and its variants within a typical application. The application examples assume either a 5V or a 3V supplied host microcontroller. In each example there is a dedicated 5V regulator supplying the TJA1051 transceiver on its VCC supply pin (necessary for proper CAN transmit capability).

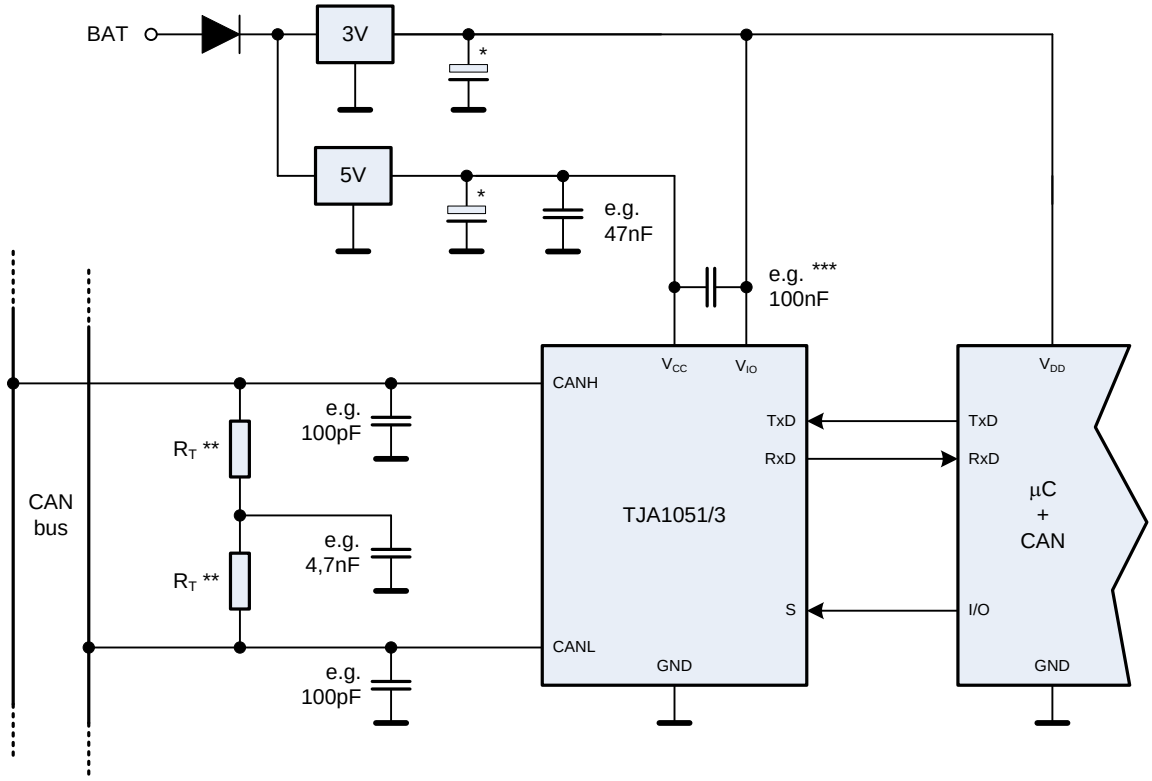


* Size of capacitor depends on regulator.

** For bus line end nodes RT = 60Ohm in order to support the „Split termination concept“
For stub nodes an optional "weak" termination of e.g. RT = 1,3kOhm can be foreseen, if required by the OEM.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 18. Typical application with TJA1051 or TJA1051/E and a 5V microcontroller



* Size of capacitor depends on regulator.

** For bus line end nodes R_T = 60Ohm in order to support the „Split termination concept“.
For stub nodes an optional "weak" termination of e.g. R_T = 1,3kOhm can be foreseen, if required by the OEM.

*** Decoupling V_{IO} to V_{CC} (instead GND) with a capacitor close to the pins achieves a high-frequent short of the supplies and thus improves the electromagnetic immunity for the TJA1051/3 by enabling the same HF-conditions like existing with V_{CC} connected directly to V_{IO} in 5V-only environments.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 19. Typical application with TJA1051/3 and a 3V microcontroller

Note: For detailed hardware application guidance please refer to chapter 7 explaining how the pins of the TJA1051 are properly connected in an application environment.

4. The TJA1042 – High speed CAN transceiver with Standby Mode

4.1 Main features

The TJA1042 is the high speed CAN transceiver providing a low power mode (called Standby Mode) beside a Normal Mode. It is being delivered in two versions, distinguished only by the function of pin 5:

- TJA1042 – the version with a SPLIT output is 100% backwards compatible with the TJA1040:

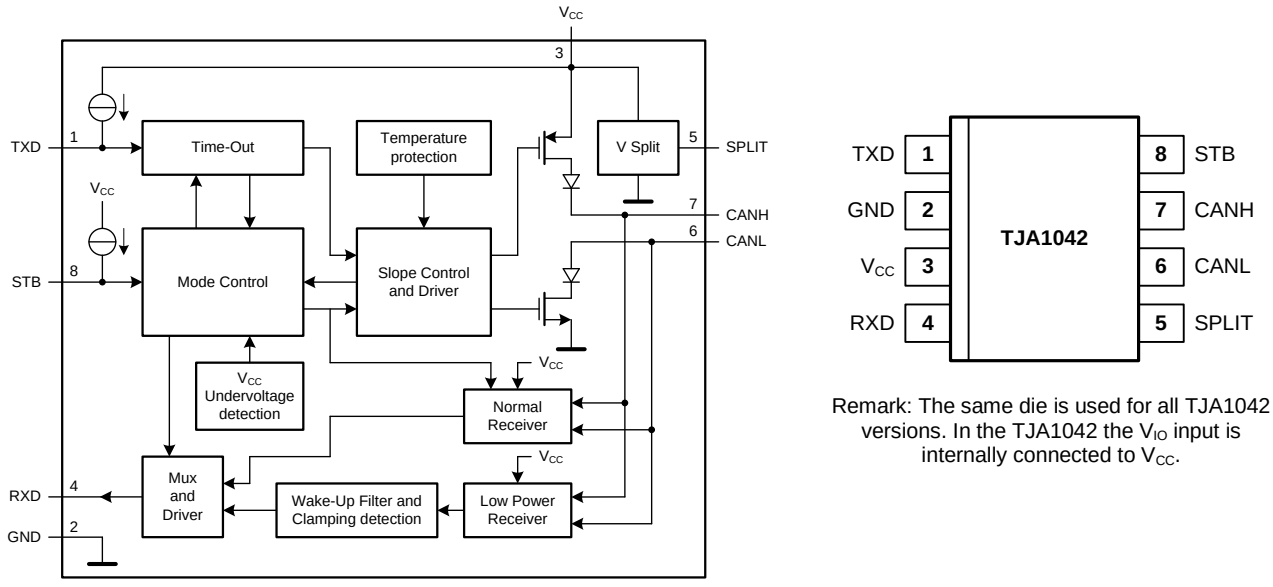
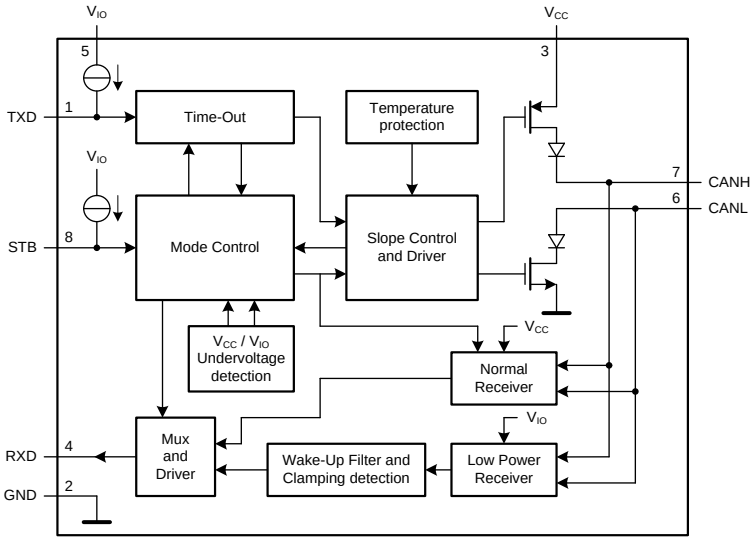
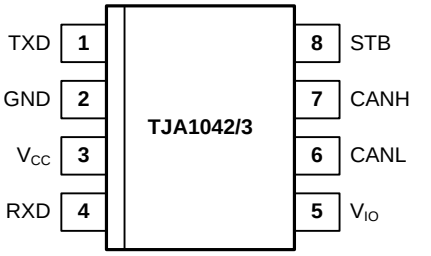


Fig 20. Block diagram and pinning of the TJA1042

- TJA1042/3 – the version with a V_{IO} pin allows for direct interfacing to microcontrollers with supply voltages down to 3V:



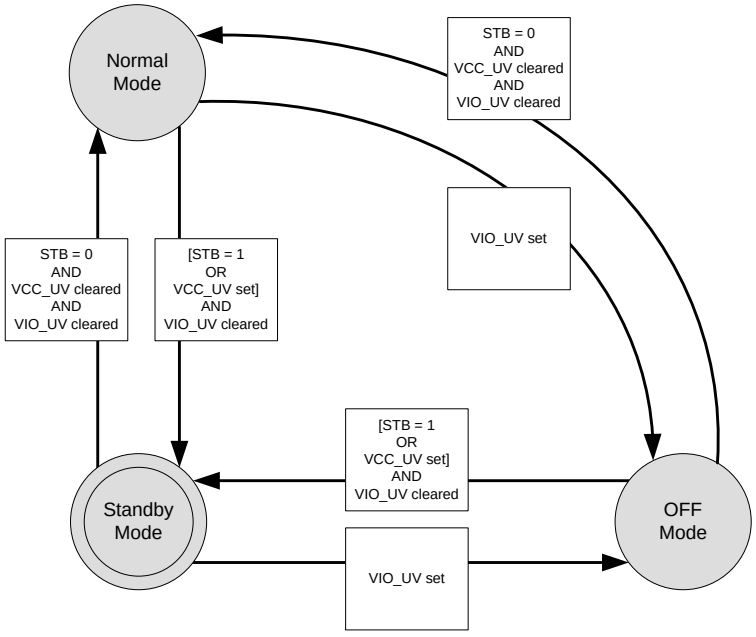


Remark: The same die is used for all TJA1042 versions. In the TJA1042/3 the SPLIT output is internally left open.

Fig 21. Block diagram and pinning of the TJA1042/3

4.2 Operation modes

The TJA1042 offers 2 different power modes, Normal Mode and Standby Mode which are directly selectable. Taking into account the undervoltage detection a third power mode is available, the so-called OFF Mode. Fig 22 shows how the different operation modes can be entered. Every mode provides a certain behavior and terminates the CAN channel to a certain value. The following sub-chapters give a short overview of those features.



Remark: The same die is used for all TJA1042 versions.

- In the TJA1042 the V_{IO} input is internally connected to V_{CC}.
- In the TJA1042/3 the SPLIT output is internally left open.

Fig 22. State diagram TJA1042 and TJA1042/3

4.2.1 Normal Mode

In Normal Mode the CAN communication is enabled. The digital bit stream input at TXD is transferred into corresponding analog bus signals. Simultaneously, the transceiver monitors the bus, converting the analog bus signals into the corresponding digital bit stream output at RXD. The bus lines are biased to $V_{CC}/2$ in recessive state and the transmitter is enabled. The Normal Mode is entered setting pin STB to LOW.

In Normal Mode the transceiver provides following functions:

- The CAN transmitter is active.
- The normal CAN receiver is active.
- The low power CAN receiver is active.
- CANH and CANL are biased to $V_{CC}/2$.

- Pin RXD reflects the normal CAN Receiver.
- SPLIT is biased to $V_{CC}/2$ (TJA1042 only).
- V_{CC} and V_{IO} undervoltage detectors are active for undervoltage detection.

4.2.2 Standby Mode

The Standby Mode is used to reduce the power consumption of the TJA1042 significantly. In Standby Mode the TJA1042 is not capable of transmitting and receiving regular CAN messages, but it monitors the bus for CAN messages.

Only a low power CAN receiver is active, monitoring the bus lines for activity. The bus wake-up filter ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on the RXD pin. The low-power receiver is supplied by the V_{IO} pin, thus even with a switched off V_{CC} supply the TJA1042/3 offers full support of detecting a remote wake-up via the bus with lowest supply current. This allows 3V microcontroller designs to entirely disable all 5V supplies in the system while staying wake able via the CAN bus lines.

To reduce the current consumption as far as possible the bus is terminated to GND rather than biased to $V_{CC}/2$ as in Normal Mode. The Standby Mode is selected setting pin STB to HIGH or by undervoltage detection on V_{CC}. Due to an internal pull-up function on the STB pin it is the default mode if pin STB is unconnected.

In Standby Mode the transceiver provides following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The low power CAN receiver is active.
- CANH and CANL are biased to GND.
- SPLIT is floating (TJA1042 only) (lowest leakage current on SPLIT pin).
- Pin RXD reflects the low-power CAN Receiver.
- V_{CC} undervoltage detector is active for undervoltage detection / recovery.
- V_{IO} undervoltage detector is active for undervoltage detection.

4.2.3 OFF Mode

The non-operation OFF Mode is introduced offering total passive behaviour to the CAN bus system. The OFF Mode is entered by undervoltage detection on V_{IO}.

In OFF Mode the transceiver provides following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The low power CAN receiver is off.
- CANH and CANL are floating (lowest leakage current on bus pins).
- SPLIT is floating (TJA1042 only) (lowest leakage current on SPLIT pin).
- V_{CC} and V_{IO} undervoltage detectors are active for undervoltage recovery.

Table 3. Characteristics of the different modes

Operating mode	STB pin	V_{CC} underv.	V_{IO} underv.	RXD pin		Bus bias	SPLIT pin	TXD pin	CAN driver
				Low	High				
Normal	0	no	no	Bus dominant	Bus recessive	$V_{CC}/2$	$V_{CC}/2$	0	dominant [1]
								1	recessive
Standby	1	X	no	Wake-up request detected	No wake-up request detected	GND	float	X	off
	X	yes	no						
OFF	X	X	Yes	-	-	float	float	X	off

[1] $t < t_{to(dom)TXD}$, afterwards the TXD dominant clamping detection disables the transmitter.

4.3 System fail-safe features

4.3.1 TXD dominant clamping detection in Normal Mode

As the TJA1051 the TJA1042 provides TXD dominant clamping detection in Normal Mode. Please refer to chapter 3.3.1 for more details.

4.3.2 Bus dominant clamping prevention at entering Normal Mode

As the TJA1051 the TJA1042 provides bus dominant clamping prevention at entering Normal Mode. Please refer to chapter 3.3.2 for more details.

4.3.3 Bus dominant clamping detection in Standby Mode

For system safety reasons a new bus dominant timeout function in Standby Mode is introduced in the TJA1042. At any bus dominant condition in Standby Mode the RXD pin gets switched LOW. If the dominant condition holds for longer than the timeout $t_{to(dom)bus}$, the RXD pin gets set HIGH again in order to prevent generating a permanent wake-up request at a bus failure condition. Consequently a system can now enter the Standby Mode even with a permanently dominant clamped bus.

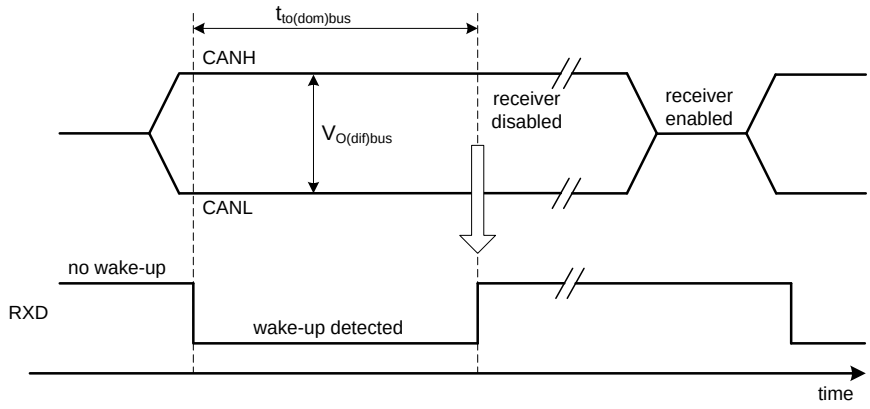


Fig 23. Bus dominant clamping in Standby Mode

4.3.4 Undervoltage detection & recovery

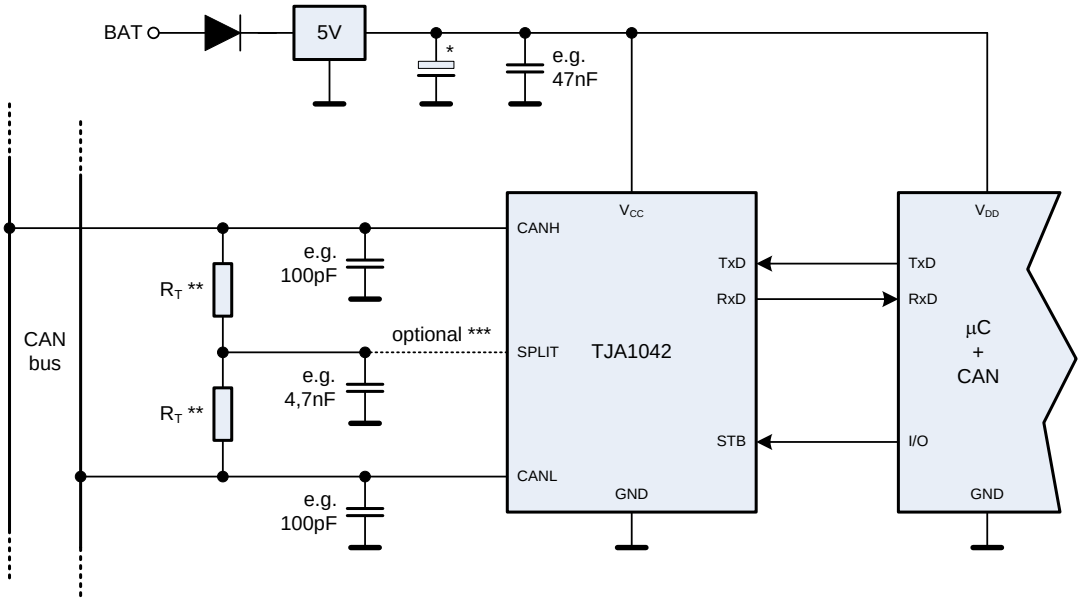
Compared to their predecessor TJA1040, the TJA1042 versions take advantage of high precision integrated undervoltage detection on their supply pins (see Table 4). Without this function undervoltage conditions might result in unwanted system behavior, if the supply leaves the specified range. (e.g. the bus pins might bias to GND).

Table 4. TJA1042 and TJA1042/3 mode control at undervoltage conditions

Undervoltage condition		HS-CAN with Standby Mode	
V_{CC}	V_{IO}	TJA1042	TJA1042/3
no	no	Normal or Standby	Normal or Standby
yes	no	Standby	Standby
no	yes	not applicable	OFF
yes	yes	OFF	OFF

4.4 Hardware application

Fig 24 and Fig 25 show how to integrate the TJA1042 and the TJA1042/3 within a typical application. The application examples assume either a 5V or a 3V supplied host microcontroller. In each example there is a dedicated 5V regulator supplying the TJA1042 transceiver on its V_{CC} supply pin (necessary for proper CAN transmit capability).



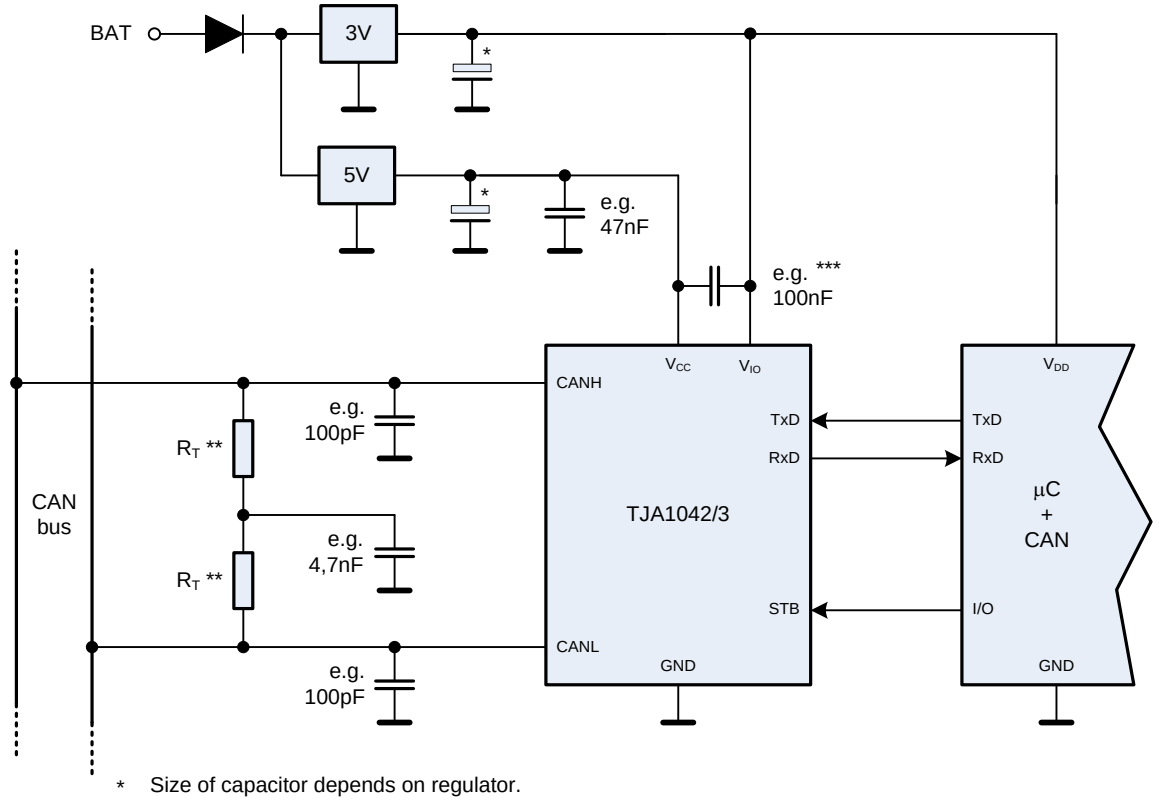
* Size of capacitor depends on regulator.

** For bus line end nodes RT = 60Ohm in order to support the „Split termination concept“
For stub nodes an optional "weak" termination of e.g. RT = 1,3kOhm can be foreseen, if required by the OEM.

*** Optional common mode stabilization by a voltage source of $V_{CC}/2$ at the pin SPLIT.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 24. Typical application with TJA1042 and a 5V microcontroller



* Size of capacitor depends on regulator.

** For bus line end nodes R_T = 60Ohm in order to support the „Split termination concept“.
For stub nodes an optional "weak" termination of e.g. R_T = 1,3kOhm can be foreseen, if required by the OEM.

*** Decoupling V_{IO} to V_{CC} (instead GND) with a capacitor close to the pins achieves a high-frequent short of the supplies and thus improves the electromagnetic immunity for the TJA1042/3 by enabling the same HF-conditions like existing with V_{CC} connected directly to V_{IO} in 5V-only environments.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 25. Typical application with TJA1042/3 and a 3V microcontroller

Note: For detailed hardware application guidance please refer to chapter 7 explaining how the pins of the TJA1042 are properly connected in an application environment.

5. The TJA1048 – Dual high speed CAN transceiver with Standby Mode

5.1 Main features

The TJA1048 is the first dual high-speed CAN transceiver from NXP Semiconductors providing two independent CAN channels with a low power mode (called Standby Mode) besides a Normal Mode. The TJA1048 can be interfaced directly to microcontrollers with supply voltages from 3V to 5V.

The TJA1048 is the excellent choice for all types of HS-CAN networks containing more than one HS-CAN interface that require a low-power mode with wake-up capability via the CAN bus, especially for Body Control and Gateway units.

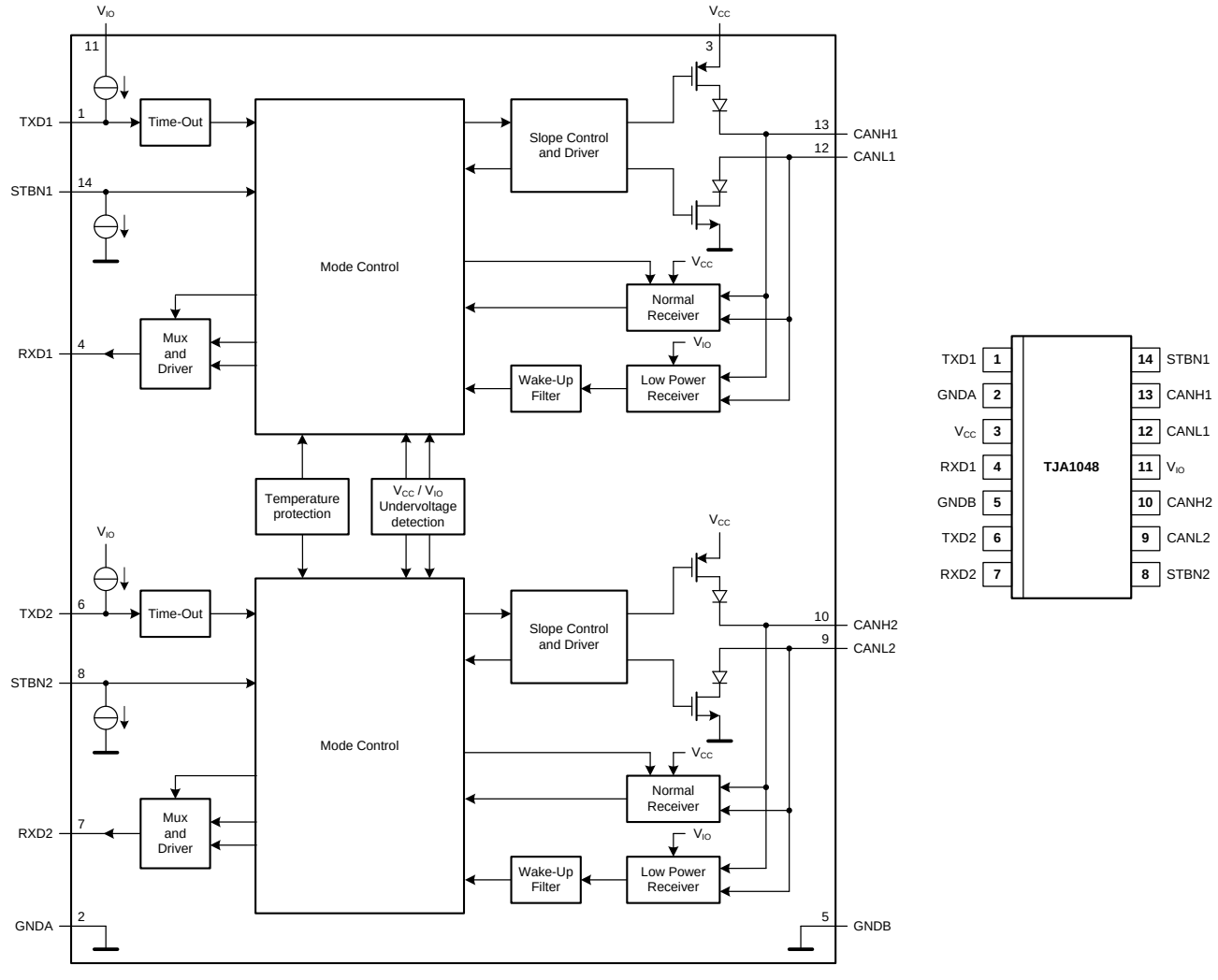


Fig 26. Block diagram and pinning of the TJA1048

5.2 Operating modes

The TJA1048 offers 2 different power modes, Normal Mode and Standby Mode which are directly selectable for each CAN channel. Taking into account the V_{IO} undervoltage condition a third power mode can be entered, the so-called OFF Mode, selected generally for both CAN channels. Fig 27 shows how the different operation modes can be entered. Every mode provides a certain behavior and terminates the CAN channel to a certain value. The following sub-chapters give a short overview of those features.

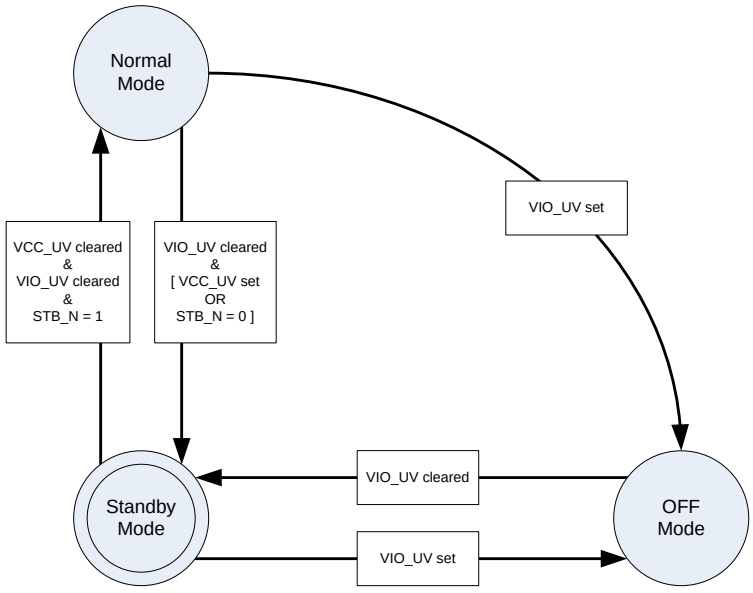


Fig 27. State diagram TJA1048

5.2.1 Normal Mode

In Normal Mode the CAN communication is enabled. The digital bit stream input at TXD is transferred into corresponding analog bus signals. Simultaneously, the transceiver monitors the bus, converting the analog bus signals into the corresponding digital bit stream output at RXD. The bus lines are biased to $V_{CC}/2$ in recessive state and the transmitter is enabled. The Normal Mode is entered setting STBN1 or STBN2 to HIGH. Switching into Normal Mode is CAN channel independently.

In Normal Mode the transceiver provides the following functions:

- The CAN transmitter is active.
- The normal CAN receiver is active.
- The low power CAN receiver is active.
- CANH and CANL are biased to $V_{CC}/2$.
- Pin RXD reflects the normal CAN Receiver.
- V_{CC} and V_{IO} undervoltage detectors are active for undervoltage detection.

5.2.2 Standby Mode

The Standby Mode is used to reduce the power consumption of the TJA1048 significantly. In Standby Mode the specific CAN channel is not capable of transmitting and receiving regular CAN messages, but it monitors the bus for CAN messages. After passing the wake-up filter the bus signal is transferred to RXD with an additional time delay $t_{fltr(wake)bus}$. To reduce the current consumption as far as possible the bus is terminated to GND rather than biased to $V_{CC}/2$ as in Normal Mode. The Standby Mode is selected setting STBN1 or STBN2 to LOW channel independently or by undervoltage detection on V_{CC} for both channels at the same time. Due to an internal pull-down function on the pins STBN1 and STBN2 it is the default mode if the pins are unconnected.

In Standby Mode the transceiver provides the following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The low power CAN receiver is active.
- CANH and CANL are biaed to GND.
- Pin RXD reflects the low power CAN receiver .
- V_{IO} undervoltage detector is active for undervoltage detection.
- V_{CC} undervoltage detector may be disabled

5.2.3 OFF Mode

The non-operation Off Mode is introduced offering total passive behaviour to bus system. The OFF Mode is entered by undervoltage detection on V_{IO}. Entering and leaving OFF Mode is done for both channels at the same time, thus not independently. In OFF Mode the transceiver provides the following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The low power CAN receiver is off.
- CANH and CANL are floating (lowest leakage current on bus pins).
- V_{IO} undervoltage detector is active for u ndervoltage detection.
- V_{CC} undervoltage detector may be disabled

Table 5. Characteristics of the different modes

Ch1 Op. mode	Ch2 Op. mode	STBN1 pin	STBN2 pin	V_{CC} underv.	V_{IO} underv.	RXD1 pin		Bus1 bias	RXD2 pin		Bus2 bias
						Low	High		Low	High	
Normal	Normal	1	1	no	no	Bus dom.	Bus rec.	$V_{CC}/2$	Bus dom.	Bus rec.	$V_{CC}/2$
Standby	Normal	0	1	no	no	Wake-up detected	No wake-up detected	GND	Bus dom.	Bus rec.	$V_{CC}/2$
Normal	Standby	1	0	no	no	Bus dom.	Bus rec.	$V_{CC}/2$	Wake-up detected	No wake-up detected	GND
Standby	Standby	0	0	no	no	Wake-up detected	No wake-up detected	GND	Wake-up detected	No wake-up detected	GND
Standby	Standby	X	X	yes	no	Wake-up detected	No wake-up detected	GND	Wake-up detected	No wake-up detected	GND
OFF	OFF	X	X	X	yes	-	-	float	-	-	float

5.3 Remote Wake-up (via CAN bus)

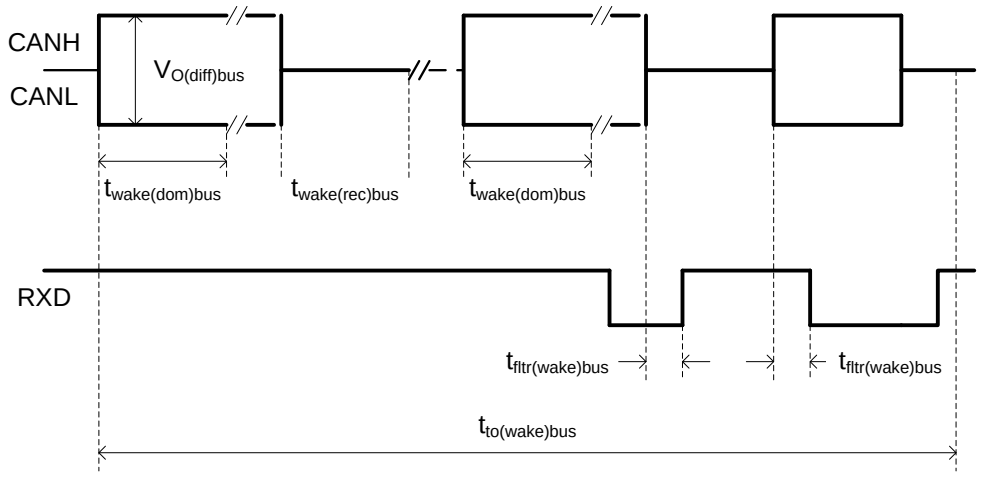
In comparison to the TJA1042 the TJA1048 offers a slightly enhanced remote wake-up procedure. The TJA1042 in Standby Mode transfers the bus signal to RXD with an additional time delay $t_{fltr(wake)bus}$ in oder to filter noise and spikes.

A dedicated wake-up sequence (specified in ISO11898-5) must be received to wake-up the TJA1048 from Standby Mode. This filtering improves the robustness against spurious wake-up events due to a dominant clamped CAN bus or dominant phases caused by noise or spikes on the bus.

The wake-up pattern consists of:

- A dominant phase of at least $t_{wake(busdom)}$ followed by
- A recessive phase of at least $t_{wake(busrec)}$ followed by
- A dominant phase of at least $t_{wake(busdom)}$

The complete dominant-recessive-dominant pattern must be completed within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Fig 28). Otherwise the internal wake-up logic gets reset and the complete wake-up pattern needs to be re-applied to the low power receiver of CAN1 or CAN2 before generating a proper remote wake-up. Pins RXD1 and RXD2 will remain recessive until the wake-up event has been triggered.



$t_{to(wake)bus}$ = 0.5ms to 12ms

$t_{fltr(wake)bus}$ = 0.5µs to 5µs

$t_{wake(dom)bus}$ = $t_{wake(rec)bus}$ = 0.5µs to 5µs

Fig 28. Wake-up timings and behaviour

After the wake-up sequence has been detected, the TJA1048 behaves equal to the TJA1042 and will remain in Standby Mode with the bus signals reflected on RXD1/RXD2. Note that dominant or recessive phases less than $t_{fltr(wake)bus}$ will not be detected by the low power differential receiver and will not be reflected on RXD1/RXD2 in Standby Mode.

A wake-up event will not be registered if any of the following events occurs while a wake-up sequence is being received:

- The TJA1048 switches to Normal Mode
- The complete wake-up pattern was not received within $t_{to(wake)bus}$
- A V_{IO} undervoltage was detected ($V_{IO} < V_{uvd(VIO)}$)

If any of these events occurs while a wake-up sequence is being received, the internal wake-up logic will be reset and the complete wake-up sequence will have to be re-transmitted to trigger a wake-up event.

5.4 System fail-safe features

5.4.1 TXD dominant clamping detection in Normal Mode

As the TJA1051, TJA1042 the TJA1048 provides TXD dominant clamping detection in Normal Mode for each CAN channel. Please refer to chapter 3.3.1 for more details.

5.4.2 Bus dominant clamping prevention at entering Normal Mode

As the TJA1051, TJA1042 the TJA1048 provides bus dominant clamping prevention at entering Normal Mode. Please refer to chapter 0 for more details.

5.4.3 Undervoltage detection & recovery

The TJA1048 provides two supply pins, V_{CC} and V_{IO}. The V_{CC} voltage is needed for the CAN physical interface. V_{CC} provides the current needed for the CAN transmitter and receiver in Normal Mode. Pin V_{IO} should be connected to the microcontroller supply voltage. This will adjust the signal levels of pins TXD1, TXD2, RXD1, RXD2, STBN1 and STBN2 to the I/O levels of the microcontroller. Pin V_{IO} also provides the internal supply voltage for the low power differential receiver of each integrated transceivers. For applications running in low power, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin V_{CC}.

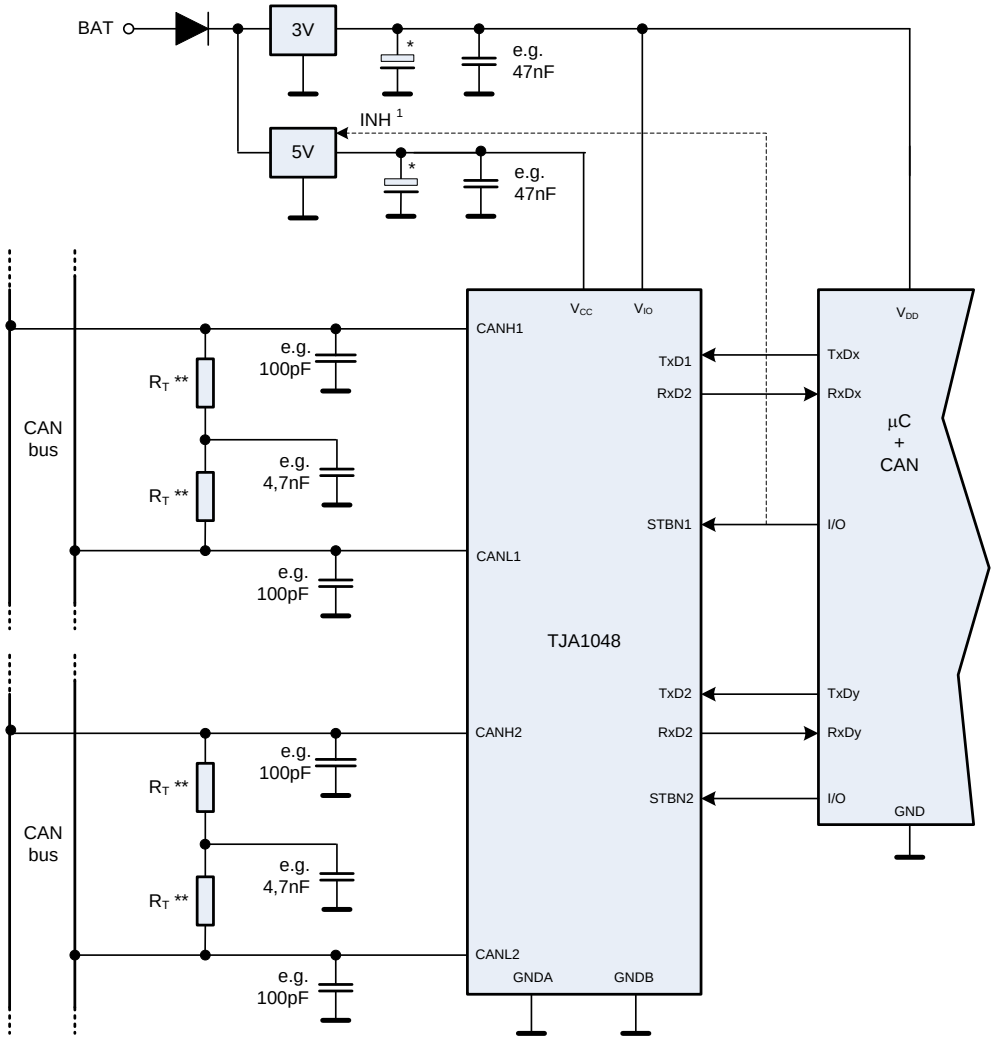
Both voltages are independent from each other. An undervoltage detection circuitry at V_{CC} and V_{IO} indicates either a V_{CC} or V_{IO} undervoltage condition that is used for mode control. A V_{CC} undervoltage condition forces both CAN channels of the TJA1048 to enter Standby Mode. The logic state of pins STBN1 and STBN2 will be ignored until V_{CC} has recovered. This allows saving current in case of switching off the supply voltage or faulty behaviour of host electronic control unit. As long as V_{IO} keeps present the TJA1048 offers the full wake-up capability. A V_{IO} undervoltage condition forces both CAN channels of the TJA1048 to switch off (OFF Mode) and to disengages from the bus (zero load) until V_{IO} has recovered. In OFF Mode both CAN transceiver behave passive to the bus. Table 6 gives an overview of the undervoltage behaviour. As long as no undervoltage is detected the TJA1048 keeps fully operational.

Table 6. Device behaviour in different power conditions

Undervoltage condition		Operating mode	CAN1 / CAN2 biasing	Bus wake-up capability
V_{CC}	V_{IO}			
no	no	Normal or Standby	$V_{CC}/2$ or GND	yes
yes	no	Standby	GND	yes
no	yes	OFF	float	no
yes	yes	OFF	float	no

5.5 Hardware application

Fig 29 shows how to integrate the TJA1048 within a typical application. The application examples assume 3V supplied host microcontroller. There is a dedicated 5V regulator supplying the TJA1048 transceiver on its V_{CC} supply pin (necessary for proper CAN transmit capability).



* Size of capacitor depends on regulator.

** For bus line end nodes R_T = 60Ohm in order to support the „Split termination concept“.
For stub nodes an optional "weak" termination of e.g. R_T = 1,3kOhm can be foreseen, if required by the OEM.

General remark: A dedicated application may depend on specific OEM requirements.

(1) Switching off the 5V supply if both channels in Standby Mode (dotted line) is optional

Fig 29. Application diagram TJA1048

Note: For detailed hardware application guidance please refer to chapter 7 explaining how the pins of the TJA1048 are properly connected in an application environment.

6. The TJA1043 – High speed CAN transceiver with Sleep Mode & diagnostics

6.1 Main features

The TJA1043 is the ideal choice for high speed CAN nodes that need to be available all time “Clamp-30”, even when the internal V_{IO} and V_{CC} supplies are switched off. It is a step up from the TJA1041A high speed CAN transceiver, offering enhanced low power management with wake up detection and recognition beside several protection and diagnostic functions. The TJA1043 builds the high end of the 3rd generation high speed CAN portfoilio from NXP Semiconductors.

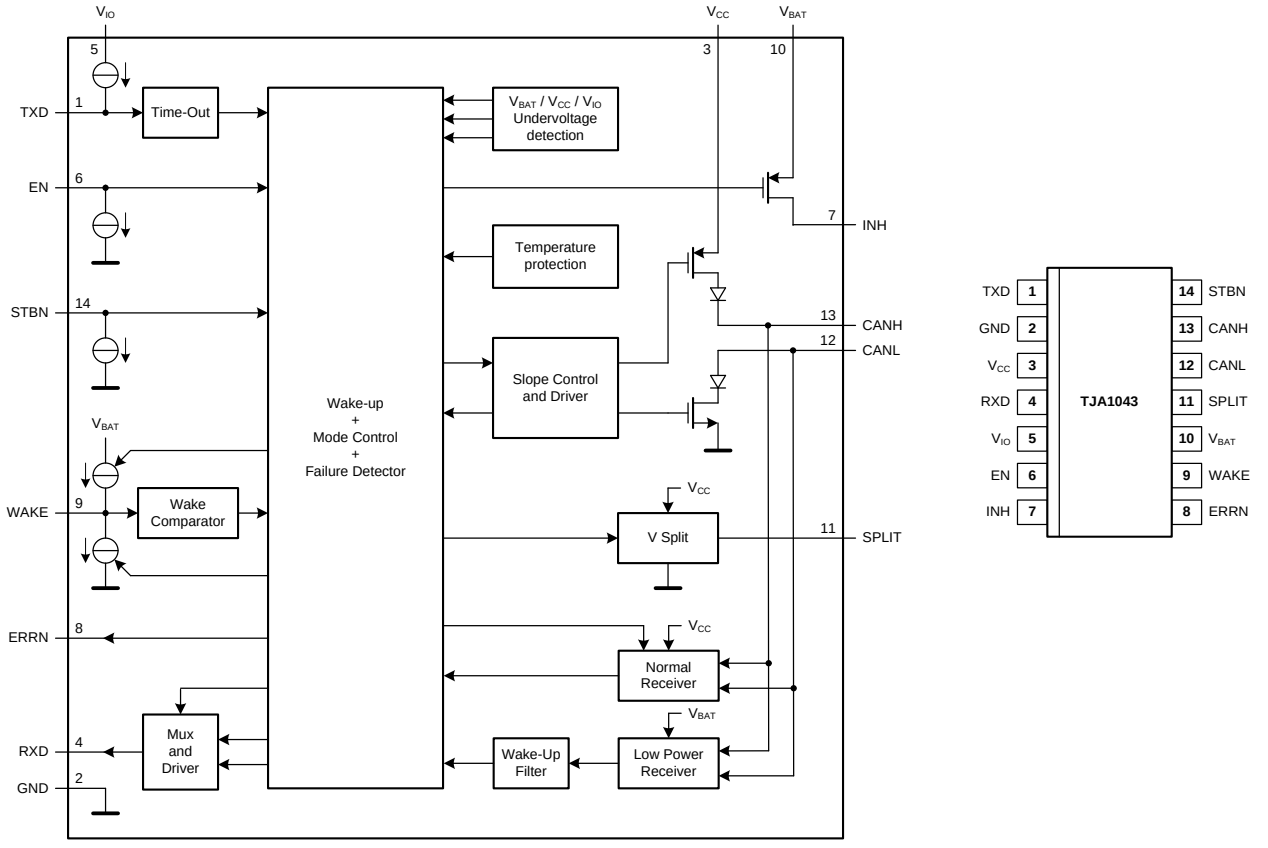


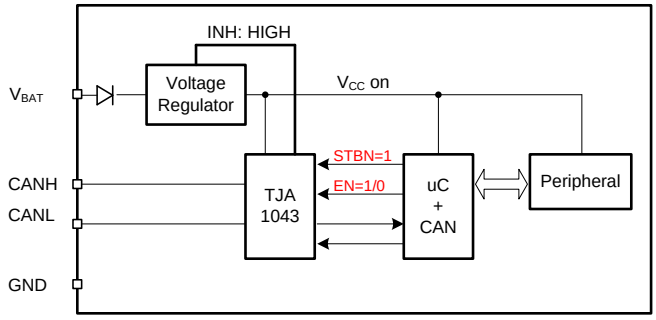
Fig 30. Block diagram and pinning of the TJA1043

Low Power Management

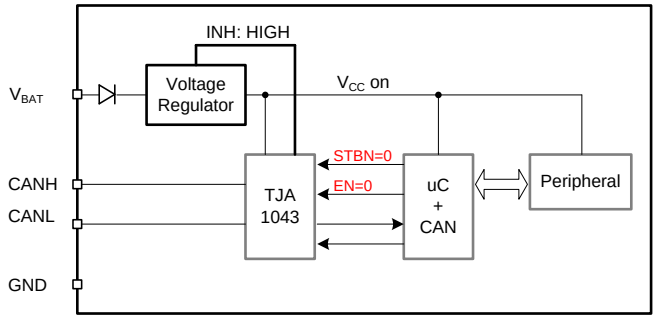
Many in-vehicle networking architectures require the availability of the high speed CAN bus even when ignition key is off. This requires permanently battery supplied ECUs with lowest current consumption. The low power management of the TJA1043 allows reducing the quiescent current consumption of an ECU to about typ. 20 µA. This current consumption is low enough to allow permanent battery supply of the transceiver and

keeping wakeup capability via the bus. This way the system can react on local events as well as on CAN messages, resulting in wakeup of the complete bus system.

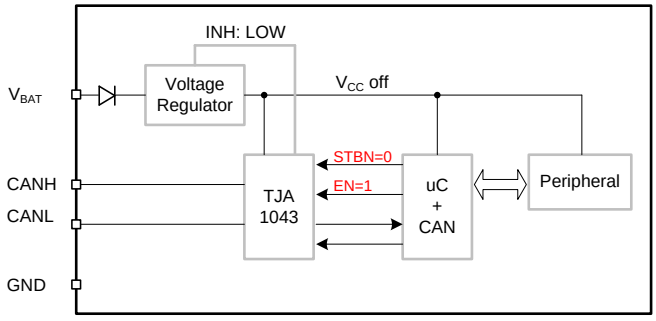
The operating modes of the TJA1043 (Normal, Listen-Only, Standby, Sleep, Go-to-Sleep) establish a low power management with three different levels as sketched in Fig 31 and Table 7. In level 0 the ECU components (voltage regulator, microcontroller, transceiver and peripherals) are active and powered. The TJA1043 is either in Normal or Listen-Only Mode. The transceiver and the host microcontroller are powered by the active V_{CC} supply.



A) TJA1043 in Normal/Listen-Only Mode (Low-power level 0)
uC and peripheral are powered by V_{CC} and are active



B) TJA1043 in Standby Mode (Low-power level 1)
uC and peripheral are powered by V_{CC}, but may be in power-down mode



C) TJA1043 in Sleep Mode (Low-power level 2)
uC and peripheral are typically un-powered

Fig 31. Low Power Management of TJA1043

The next level of low power, level 1, is achieved with the TJA1043 operating in Standby Mode. The microcontroller, transceiver and peripherals are still powered by the active V_{CC} supply, but the functionality is often reduced to a minimum in order to save current. In the case of the TJA1043 the function is reduced to detection of wakeup events only. Transmit and receive function as provided in Normal Mode is not available. The host microcontroller is often put in a power-down condition in order to save additional current.

The low power level 2 is associated to the Sleep Mode of the TJA1043. In Sleep Mode the external voltage regulator(s), supplying the transceiver and host microcontroller, is (are) typically switched off via the INH output signal of the transceiver. The V_{CC} supply for the transceiver and microcontroller is not available. While the host microcontroller and peripherals are completely un-powered, the TJA1043 keeps powered via the battery supply pin V_{BAT}. This supply is needed to ensure wakeup capability either via the bus or via a local wakeup event. The low power level 2 guarantees the lowest current consumption of a node.

Table 7. Characteristics of the different low power modes

Low power level	Operating mode	V_{CC} supply	uC	Node power consumption
Level 0 (Bus active)	Normal, Listen-only	Active	Powered	Normal
Level 1	Standby	Active	Powered	Low
Level 2	Sleep	Off	Un-powered	Very Low

Bus failure diagnosis

The TJA1043 can detect short circuits on the bus wires and signal them to the host microcontroller. While physical bus failures normally lead to interruption of bus communication, there are certain bus failures that are tolerated within the physical layer of high speed CAN. Without the bus failure diagnosis feature of the TJA1043 the application microcontroller would not have a chance to become aware of those bus failures. Apart from increasing current consumption, those bus failures are responsible for poor EMC performance.

System fail-safe features

The system fail-safe features of the TJA1043 aim to keep the impact of possible local failures, like pin short-circuits, confined to the corrupted node only. After detection of a local failure, appropriate measures are taken to keep the remaining bus operable as long as possible. There are protections against TXD Dominant Clamping, TXD/RXD Short Circuit and Bus Dominant Clamping.

6.2 Operating modes

The TJA1043 provides five different operating modes, which are controlled by the input pins STBN and EN. The reference state diagram for the operating modes can be found in the data sheet [7]. In the case of an undervoltage condition on the pin V_{CC} or V_{IO} , the transceiver is forced into Sleep Mode, overruling the current mode selection at the pins

STBN and EN. In the case of an undervoltage condition on the pin V_{BAT} the transceiver is forced into Standby Mode.

Depending on the operating mode the transceiver shows different behavior for the receiver and bus driver as well as on output pins like ERRN and RXD. Table 1 summarizes the characteristics in each operating mode.

6.2.1 Normal Mode

For CAN communication the Normal Mode is chosen. The digital bit stream input at TXD is transferred into corresponding analog bus signals. Simultaneously, the transceiver monitors the bus, converting the analog bus signals into the corresponding digital bit stream output at RXD. The external voltage regulator is active, the bus lines are biased to $V_{CC}/2$ and the transmitter is enabled. The Normal Mode is entered setting STBN and HIGH and EN to HIGH level.

In Normal Mode the transceiver provides the following functions:

- The CAN transmitter is active.
- The normal CAN receiver is active, pin RXD reflects the normal CAN Receiver.
- The local and bus wakeup function are disabled.
- INH is active (V_{BAT} level).
- CANH and CANL are biased to $V_{CC}/2$.
- SPLIT is biased to $V_{CC}/2$.
- V_{BAT}, V_{CC} and V_{IO} undervoltage detectors are active for undervoltage detection.
- Local and bus failure diagnosis is active.
- Pin ERRN provides either the Wakeup Source or the Bus Failure Flag.

6.2.2 Listen-only Mode

In general the Listen-Only Mode has two different functions. First, it realizes a Listen-Only behavior. The node is only allowed to receive messages from the bus but not to transmit onto the bus. The digital bit stream from the CAN-controller at TXD is simply ignored. In this way a node can be prevented from influencing the bus.

Secondly, the Listen-Only Mode provides the Local Failure flag and PWON flag at the pin ERRN, which can be read by the microcontroller. For flag signalling at the pin ERRN refer to Chapter 6.5. The Listen-Only Mode is entered setting STBN to HIGH and EN to LOW level.

In Listen-only Mode the transceiver provides the following functions:

- The CAN transmitter is off.
- The normal CAN receiver is active, pin RXD reflects the normal CAN Receiver.
- The local and bus wakeup function are disabled.
- INH is active (V_{BAT} level).
- CANH and CANL are biased to $V_{CC}/2$.
- SPLIT is biased to $V_{CC}/2$.
- V_{BAT}, V_{CC} and V_{IO} undervoltage detectors are active for undervoltage detection.
- Local failure diagnosis is active.
- Pin ERRN provides either the Pwon or Local Failure Flag.

6.2.3 Standby Mode

Standby Mode is used to achieve low power level 1. Power consumption of the TJA1043 is significantly reduced compared to Normal or Listen-Only Mode. In Standby Mode the TJA1043 is not capable of transmitting and receiving regular CAN messages. However, the TJA1043 monitors the bus for CAN messages. Whenever a wakeup pattern is detected on the bus, indicating bus traffic, the internal Wakeup flag is set. The TJA1043 can also receive a local wakeup via the pin WAKE. On detection of a remote or local wakeup the internal Wakeup flag is set. In Standby Mode this flag is output at the pins ERRN and RXD. To reduce the current consumption as far as possible the bus is terminated to GND rather than biased to $V_{CC}/2$ as in Normal or Listen-Only Mode. Standby Mode is selected setting STBN to LOW and EN to LOW level.

In Standby Mode the transceiver provides the following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The local and bus wakeup function are active.
- INH is active (V_{BAT} level).
- CANH and CANL are biased to GND.
- SPLIT is floating (lowest leakage current on SPLIT pin).
- V_{BAT}, V_{CC} and V_{IO} undervoltage detectors are active for undervoltage detection.
- Pin ERRN and pin RXD provide the Wakeup Flag (if V_{BAT} and V_{IO} are present)

6.2.4 Sleep Mode

Sleep Mode is used to achieve low power level 2. While the transceiver current consumption is the same as in Standby Mode, it allows further reduction of the system current consumption by switching off the external voltage regulator (V_{CC} supply) for the transceiver, host microcontroller etc.

The only difference between Sleep and Standby Mode concerns the pin INH. It provides a battery related open drain output to control one or more external voltage regulators. In Sleep Mode the pin INH is set floating compared to a HIGH signal (V_{BAT}-based) in all other modes (also Standby Mode), typically disabling the voltage regulator(s) for the transceiver and microcontroller. While the microcontroller is completely un-powered (no V_{CC} supply), the TJA1043 keeps partly alive via its battery supply. It allows the transceiver to monitor the bus for CAN messages. In fact, the transceiver is the device controlling autonomously the V_{CC} supply for the ECU.

In Sleep Mode the transceiver provides the following functions:

- The CAN transmitter is off.
- The normal CAN receiver is off.
- The local and bus wakeup function are active.
- INH is floating (lowest leakage current on INH pin).
- CANH and CANL are biased to GND.
- SPLIT is floating (lowest leakage current on SPLIT pin).

- V_{BAT}, V_{CC} and V_{IO} undervoltage detectors are active for undervoltage detection.
- Pin ERRN and pin RXD provide the Wakeup Flag (if V_{BAT} and V_{IO} are present)

Wakeup from Sleep Mode is generally possible via two channels (see also chapter 6.4):

- Wakeup via a remote wakeup sequence on the bus
- Local wakeup via an edge at pin WAKE

On wakeup, the pin INH goes HIGH enabling the external voltage regulator(s) again. The Wakeup flag is set for a local or remote wakeup. It is reflected at the pins ERRN and RXD. As in Standby Mode, the bus lines CANH and CANL are terminated to GND. Table 1 summarizes the characteristics of the TJA1043 in the different operating modes.

The only way to put the TJA1043 into Sleep Mode is using the Go-to-Sleep Mode (STBN to LOW, EN to HIGH). If it is selected for longer than the minimum hold time of go-to-sleep command $t_{h(min)}$ [7], the transceiver is automatically forced into Sleep Mode switching the pin INH to floating.

A mode transition from Sleep Mode to any other mode via STBN and EN is possible, even if the supplies V_{CC} and V_{IO} were not present all time during Sleep Mode. Once a rising edge on the pin STBN is detected (provided that the VIO is present) the selected mode on pin EN (either Normal or Listen-only) will be entered.

A continuous situation, where one part of the nodes is in Normal or Listen-Only Mode while the other part is in Standby or Sleep Mode, should be avoided due to the different bus biasing in these modes. Otherwise a continuous DC common mode current would flow from one part to the other.

6.2.5 Go-to-Sleep Mode

The Go-to-Sleep Mode has the meaning of a command rather than the meaning of a typical operating mode. It is used to put the TJA1043 into Sleep Mode. Due to the spread of the minimum hold time of go-to-sleep command $t_{h(min)}$ [7] the Go-to Sleep Mode must be selected for longer than the maximum value in order to make sure the Sleep Mode is entered reliably. Immediately after selecting the Go-to Sleep Mode the transmitter is disabled, the bus lines are terminated to GND and the Wakeup flag information is signalled at the pins ERRN and RXD. The Go-to Sleep Mode is selected with STBN to LOW and EN to HIGH level.

Remark: The Go-to Sleep Command might become overruled by a wake-up event, if this wake-up event occurs simultaneously with the Go-to Sleep Command. In this case, the wake-up will be signalled on RXD and ERRN as desired, while INH stays active HIGH.

Table 8. Characteristics of the different modes

Operating mode	STBN pin	EN pin	ERRN pin		RXD pin		Bus bias	INH pin
			Low	High	Low	High		
Normal	1	1	Bus failure flag set [1]	Bus failure flag reset [1]	Bus dominant	Bus recessive	$V_{CC}/2$	V_{BAT}
			Wakeup Source flag: Local wakeup [2]	Wakeup Source flag: Remote wakeup [2]				
Listen-only	1	0	PWON flag set [3]	PWON flag reset [3]				
			Local failure flag set [4]	Local failure flag reset [4]				
Go-to-Sleep	0	1	Wakeup flag set [5]	Wakeup flag reset [5]	Wakeup flag set [5]	Wakeup flag reset [5]	GND	
Standby	0	0						
Sleep [6]	0	X						float

[1] Valid after the 4th dominant to recessive edge at TXD after entering the Normal Mode (each dominant period should be at least 4us).

[2] Valid before the 4th dominant to recessive edge at TXD after entering Normal Mode.

[3] Valid if V_{IO} and V_{CC} are present and coming from Sleep, Standby or Go-to-Sleep Mode.

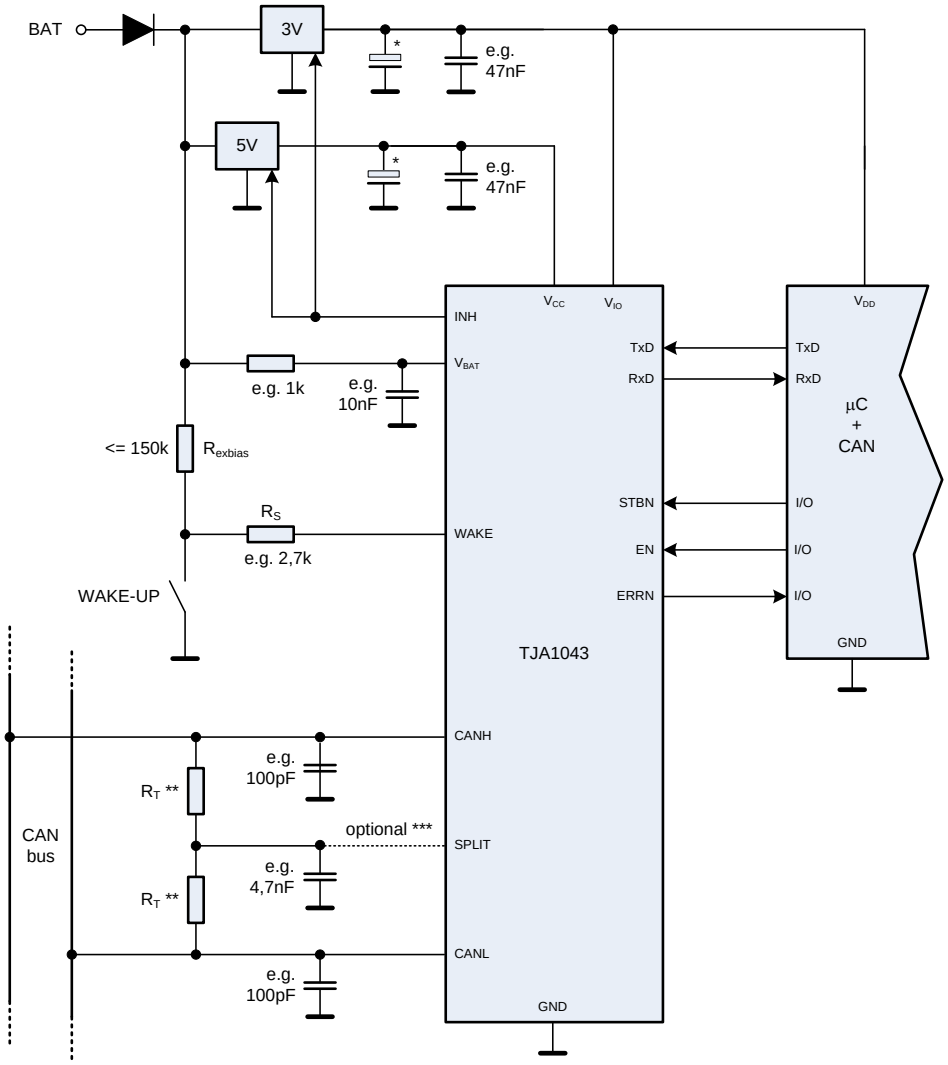
[4] Valid if V_{IO} and V_{CC} are present and coming from Normal Mode.

[5] Valid if V_{IO} and V_{BAT} are present.

[6] Transceiver will enter the Sleep Mode only if the Go-to-Sleep Mode was selected longer than the hold time of go-to-sleep command ($t_{h(min)}$ or by an undervoltage detection on V_{IO} or V_{CC}.

6.3 Hardware application

Fig 32 shows how to integrate the TJA1043 within a typical application. The application example assumes a 3V supplied host microcontroller. There is a dedicated 5V regulator supplying the TJA1043 transceiver and a dedicated 3V regulator supplying the microcontroller. Both voltage regulators are controlled via the INH output of the transceiver, so that in Sleep Mode both voltage regulators are switched off. Furthermore, the application example makes use of the pin WAKE for local wakeup possibility, connecting it to a low-side switch.



* Size of capacitor depends on regulator.

** For bus line end nodes R_T = 60Ohm in order to support the „Split termination concept".
For stub nodes an optional "weak" termination of e.g. R_T = 1,3kOhm can be foreseen, if required by the OEM.

*** Optional common mode stabilization by a voltage source of $V_{CC}/2$ at the pin SPLIT.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 32. Typical application with the TJA1043

For detailed hardware application guidance on the supply pins V_{CC} and V_{IO}, the bus pins, CANH, CANL and SPLIT as well as the host interface pins, please refer to chapter 7 explaining how the pins of the TJA1043 are properly connected in an application environment.

Note: In the following only the hardware application of the pins is explained that are unique for the TJA1043, like the VBAT, WAKE, INH and ERRN pin.

Pin V_{BAT}

The battery supply ensures the local and remote wakeup capability of the TJA1043 when the V_{CC} supply is switched off during Sleep Mode. Nevertheless the current consumption I_{BAT} via this pin is very low [7]. It is recommended to place a series resistor of e.g. 1kOhm into the battery supply line of the transceiver for enhanced protection against automotive transients. Given the max. supply current I_{BAT} of 70uA at V_{BAT}, a voltage drop of 70mV must be taken into account when calculating the minimum battery operating voltage. In addition, a capacitor of e.g. 10nF, closely connected to the V_{BAT} pin and forming a low-pass filter in conjunction with the series resistor, can be used for enhanced transient protection.

Pin ERRN

The pin ERRN is a push-pull output stage for signalling failure conditions to the microcontroller. It is typically connected to an input port pin of a microcontroller. (see [7] for drive capability).

Pin WAKE

The pin WAKE can be used to force a local wakeup event to the transceiver. A signal change of sufficient length at the pin WAKE generates a local wakeup. That means both a rising and a falling edge can be applied to launch a local wakeup. Typically, a low-side switch is used at the pin WAKE as shown in Fig 32. The series resistor R_S is for protection and limits the current when the ECU has lost its ground connection, while the external low-side switch is closed. The pull-up resistor R_{exbias} is needed to provide a sufficient current for the switch contacts. More information on the values for R_S and R_{exbias} is given in chapter 6.4.

Pin INH

The intention of the pin INH is to control one or more voltage regulators within the ECU. In Fig 32 two voltage regulators, one 5V regulator for the transceiver and one 3V regulator for the microcontroller, are controlled via the INH output of the transceiver as an example.

The pin INH provides a battery related open drain output. During Sleep Mode it is floating. Due to the typical pull-down behavior of the Inhibit input pin of common voltage regulators, this results in a LOW signal on the Inhibit input, typically disabling the voltage regulator(s). In all other operation modes the pin INH is actively pulled to battery voltage, enabling the external voltage regulator(s). The load resistance at the pin INH shall not be lower than 10 kΩ for 12 V battery systems. If the pin INH is not used for voltage regulator control, it can

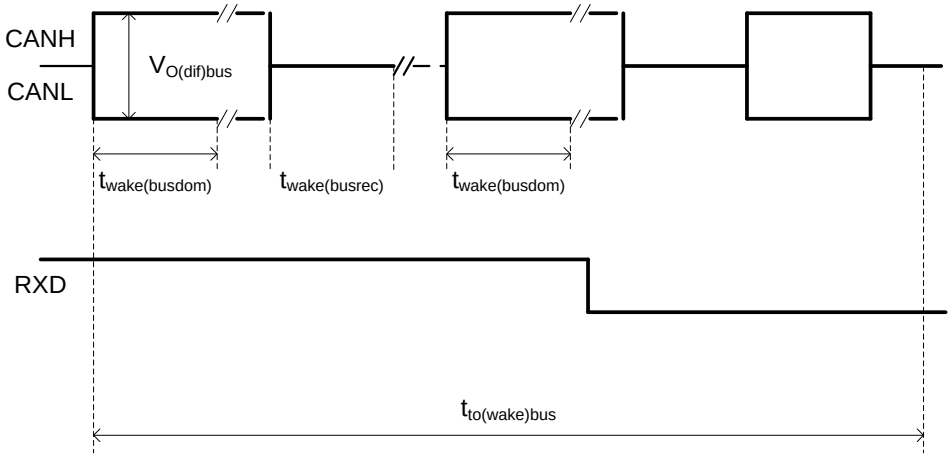
be left open. For applications it is recommended not to drive more than about 1mA out of the INH pin.

6.4 Wakeup detection

There are in general two possibilities to wake up the transceiver, either via the bus or via the WAKE pin. On detection of a wakeup event the Wakeup flag is set and signalled at RXD and ERRN.

Wakeup via bus

The TJA1043 detects a bus wake-up request when the bus shows two dominant phases of at least 5 µs duration, with the first dominant phase followed by a recessive phase of at least 5 µs (provided the complete dominant-recessive-dominant pattern is completed within the 0,5ms). Fig 33 illustrates the bus wake-up pattern requirements for the TJA1043.



$t_{to(wake)bus}$ = 0.5ms to 2ms

$t_{wake(busdom)}$ = $t_{wake(busrec)}$ = 0.5µs to 5µs

Fig 33. Wake-up timings and behaviour of the TJA1043

The bus wakeup detection offers improved robustness against unwanted wakeup in presence of bus failures, especially for large networks. There will be no unwanted bus wakeup due to a V_{BAT}-to-CANH short-circuit or CANL wire interruption, while the system is entering Bus Sleep.

At a data rate of 500 kbit/s, a single arbitrary CAN data frame is not necessarily sufficient to launch a remote wake-up. Here, two consecutive arbitrary CAN data frames are needed to reliably launch a remote wake-up. At 250 kbit/s data rate or lower speeds, any CAN data frame on the bus will lead to a remote wake-up of the TJA1043 transceiver.

In case a single CAN frame shall be used to wake-up the system reliably with 500kBit/s, the waking frame shall be designed in a way fulfilling the above mentioned timing requirements.

WAKE via pin WAKE

The pin WAKE can be used to signal a local wakeup event to the transceiver. A signal change of sufficient length at the pin WAKE generates a local wakeup. The pin WAKE of the TJA1043 features variable biasing. Depending on the external biasing the internal one switches from GND to battery level or vice versa. Fig 34 illustrates the biasing concept of the pin WAKE along with different external switching circuits.

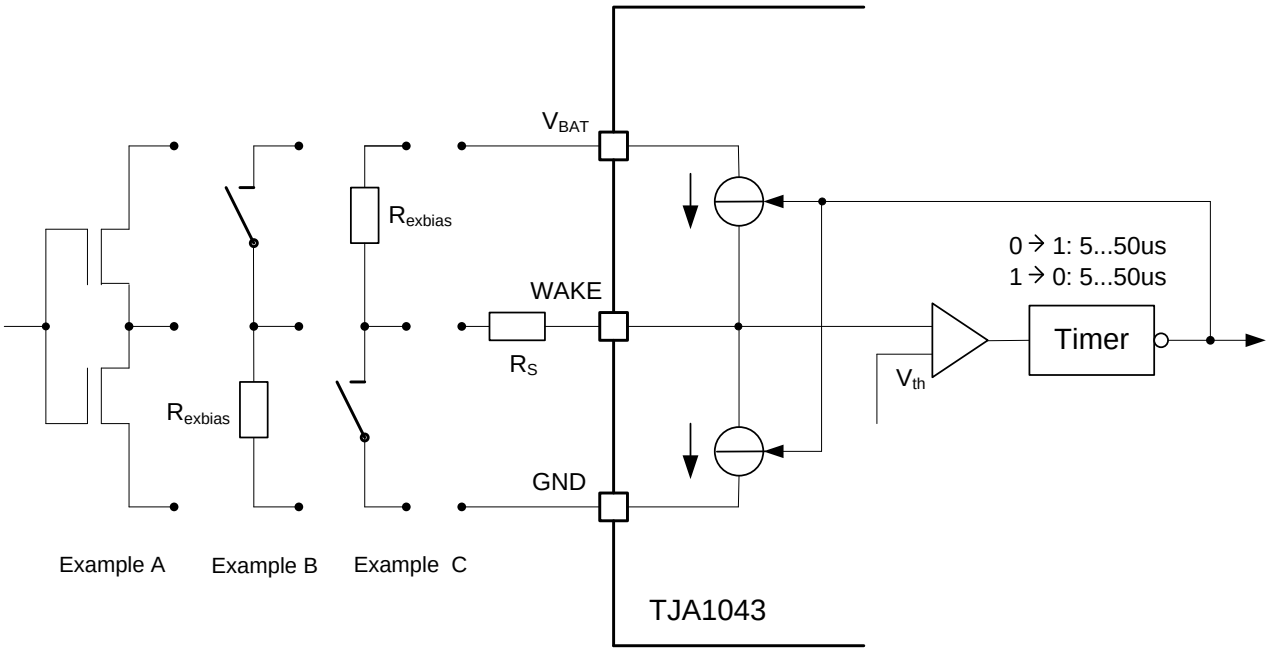


Fig 34. External switching circuits for the pin WAKE

If a voltage higher than the Wakeup Threshold Voltage $V_{th(WAKE)}$ [7] is held at the pin WAKE for longer than the maximum time t_{wake} [7], the internal biasing (current source) will switch reliably to battery level if the pin was at LOW level before. Similarly, if a voltage lower than this value is held for longer than the max. t_{wake} time, the internal biasing (current source) switches reliably to GND if the pin was at HIGH level before. The internal biasing is adapted automatically to the external biasing conditions. This concept allows using a low-side switch as well as a high-side switch or a V_{BAT} based push-pull stage without forcing undesired bias currents while there is no wakeup event.

In the case of a low-side switch, both the resistor R_{exbias} and the internal current source provide a pull-up to V_{BAT}. In order to launch a local wakeup the external switch has to be closed producing a negative pulse at the pin WAKE. The negative pulse passes the internal timer and releases a wakeup reliably if the pulse is longer than the maximum value of t_{wake} [7]. Along with passing the timer the bias switches to GND. After releasing the low-side switch the external pull-up resistor switches the internal bias back to V_{BAT}. The resistor R_{exbias} determines the current through the external switch when it is closed and is needed to guarantee a proper switch contact.

If pin WAKE is not used, connect the pin directly to ground level.

Dimensioning of R_S and R_{exbias}

The purpose of the series resistor R_S is to protect the transceiver if the ECU has a loss of ground situation while the external wakeup switch still is connected to a proper GND. The minimum required series resistor is determined by the expected maximum battery supply voltage V_{BAT_max} and the maximum allowed current at pin WAKE of 15 mA. The resistor should make sure that the current does never exceed this level. The minimum required series resistor R_S can be calculated by:

$$R_{S,min} = V_{BAT,max} / I_{WAKE,max}$$

Assuming that V_{BAT} will not exceed 40V DC, the series resistor should have a value of 3kΩ.

The resistor R_{exbias} is needed to turn the bias to its default state after the external switch has been released. That defines an upper limit for the resistor value. For example, with a low-side switch the resistor R_{exbias} together with the series resistor R_S must pull the pin WAKE above the switching threshold of the pin WAKE. The equation for determining the upper limit for R_{exbias} is:

$$(R_{exbias} + R_S) * I_{Pull,max} < V_{BAT} - V_{th(Wake),max}$$

With the maximum pull-down (pull-up) current of 10uA and the maximum threshold of $V_{th(WAKE)}$, the theoretical upper limit for R_{exbias} calculates to about 150 kOhm. A typical value is 20 kOhm.

6.5 Flag signaling

The TJA1043 provides five different flags to be signalled to the microcontroller. The status of the flags can be read by the microcontroller via the pin ERRN. Which flag is actually signalled on the pin ERRN depends on the current operating mode and on the history. Fig 35 shows the flag signaling of the pin ERRN.

Notice that when switching from one mode to another, it takes some time until the “new” flag is signaled at ERRN. To read pin ERRN with the application software, after a mode transition has been performed, first introduce a wait time in the software of at least 10 µs.

Wakeup Flag

A wakeup event from the bus or the pin WAKE sets the Wakeup Flag if the wakeup event is received while the TJA1043 is in Sleep, Standby or Go-to-Sleep Mode. In Normal or Listen-only Mode any wakeup event is ignored. The Wakeup Flag is signalled at the pin ERRN during Sleep, Standby and Go-to-Sleep Mode provided that V_{BAT} and V_{IO} are present. A LOW level signals a wakeup request to the microcontroller, received either via the bus or via the pin WAKE. It is reset when the Normal Mode is entered or when an undervoltage on V_{CC} or V_{IO} is detected (UVNOM Flag set). As long as the Wakeup Flag is set a transition into Sleep Mode is not possible. The Wakeup Flag is also signalled at the pin RXD with the same polarity as described for the pin ERRN.

The Wakeup Flag is also set together with the PWON Flag (first battery connection) in order to offer an always consistent flag setting at power-on.

PWON Flag

The PWON Flag is signalled at the pin ERRN during Listen-only Mode when coming from Standby, Sleep or Go-to-Sleep Mode. If the battery recovers from from below $V_{uvd(VBAT)}$ because it has been connected the first time to the pin V_{BAT} or if there was a temporary battery undervoltage condition, this flag is set, indicated by a LOW level at pin ERRN in Listen-only Mode. The PWON Flag is reset once the Normal Mode is entered.

Wakeup Source Flag

Entering Normal Mode, pin ERRN first reflects the Wakeup Source Flag. A LOW level signals a local wakeup via the pin WAKE, whereas a HIGH level indicates a wakeup via the bus. The Wakeup Source Flag is overwritten by the Bus Failure Flag after the node has transmitted four recessive-to-dominant bit transitions in Normal Mode. Since the application is controlling its own transmission behavior, the application has any time needed to read this Wakeup Source Flag. The Wakeup Source Flag is cleared and set to the default state HIGH whenever the Normal Mode is left.

The Wakeup source Flag is also set together with the PWON Flag (first battery connection) in order to offer an always consistent flag setting at power-on.

Bus Failure Flag

After the transceiver has transmitted four recessive-to-dominant bit transitions with a dominant bit length of at least 4us, the Bus Failure Flag overwrites the Wakeup Source Flag. A LOW level indicates a short circuit condition on the bus. The Bus Failure Flag is reset to default HIGH on leaving Normal Mode. If there is no local wakeup or power-on event meantime, leaving and re-entering Normal Mode forces pin ERRN to default state HIGH. Signalling the Bus Failure Flag requires retransmission of at least four recessive-to-dominant bit transitions. Detection of bus failures does not lead to a change of transceiver operation. Active fault tolerance as known from the TJA1055 low speed CAN transceiver is not supported.

It should be noted, that the fast phase within CAN FD frames might not be suitable for bus failure detection, because the 4µs dominant time is not supported by CAN FD at high baud rates. Here the arbitration field is the only region supporting bus failure detection, if there are enough dominant bits in a row (e.g. 2 dominant bits @ 500kBit/s).

Local Failure Flag

Entering Listen-only Mode from Normal Mode, pin ERRN signals the Local Failure Flag. A LOW level indicates those failures, which are associated with the local node only like

- TXD Dominant Clamping
- TXD/RXD Short Circuit
- Bus Dominant Clamping
- Overtemperature Condition

For a detailed description of the detected local failures refer to chapter 6.7. If any of these local failures is present, this is indicated to the application by an active LOW signal. A more differentiated diagnosis is not supported. Along with setting the Local Failure Flag, the transmitter is disabled because of fail-safe reasons. The Local Failure Flag is reset and the transmitter enabled again either by forcing a transition into Normal Mode or by receiving a dominant bit from the bus while TXD is recessive.

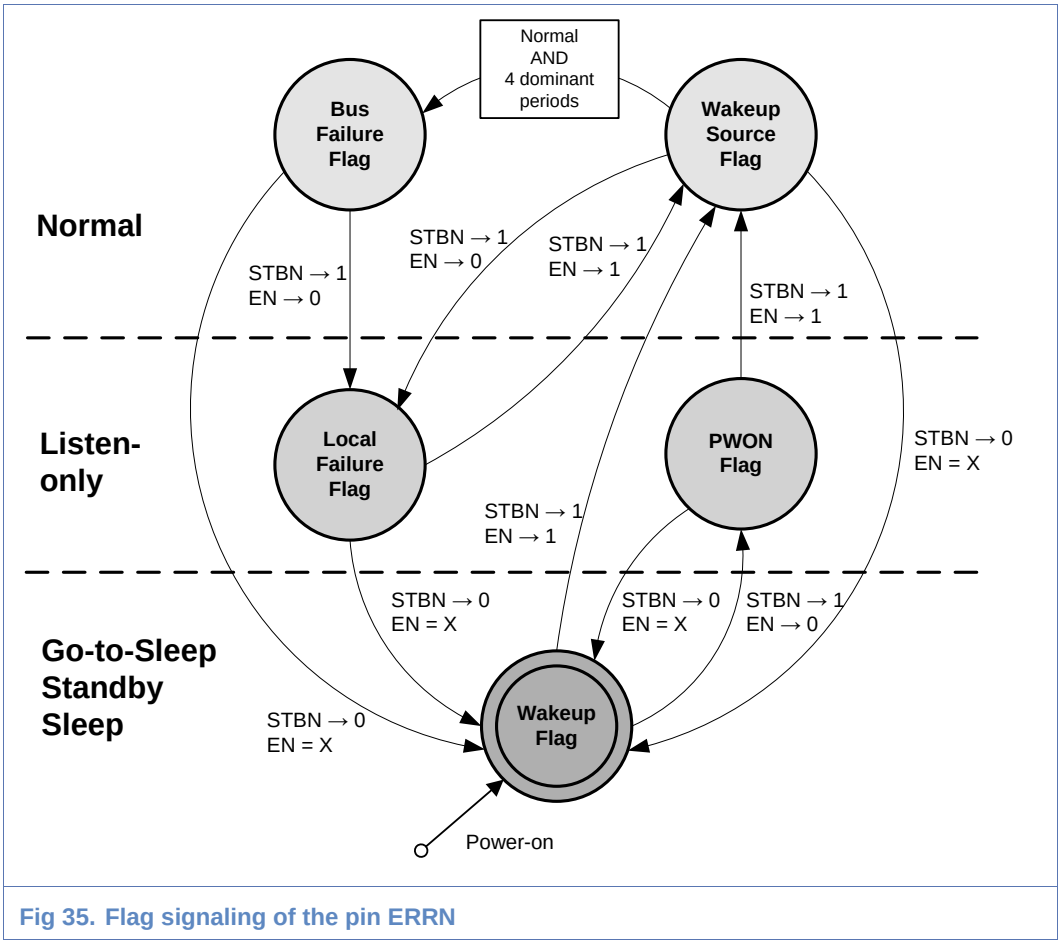


Fig 35. Flag signaling of the pin ERRN

6.6 Bus failure diagnosis

Assuming a bus load of nominal 60Ω the following bus failure conditions are detectable by the TJA1043:

- CANH x V_{BAT} (communication still possible, “hidden” bus failure)
- CANH x V_{CC} (communication still possible, “hidden” bus failure)
- CANH x GND (communication not possible)
- CANL x V_{BAT} (communication not possible)
- CANL x V_{CC} (communication not possible)
- CANL x GND (communication still possible, “hidden” bus failure)

Listed short-circuits are detected in the range 0 to 50 Ω short circuit resistance. A short-circuit between CANH and CANL or line interruption failures are not detected. For analyzing the bus the node needs to actively transmit onto the bus with an appropriate bus termination present (about 60 Ohms). Before the Bus Failure Flag becomes valid, the node must have transmitted at least four dominant bit sequences onto the bus each of at least 4us length.

As already mentioned in chapter 6.1, the bus system performance suffers from hidden bus failure conditions in terms of EMC and communication reliability. The hidden bus failures are short-circuits of CANHxV_{BAT}, CANHxV_{CC} and CANLxGND. They are normally tolerated by the CAN high speed physical layer as long as the capacitive load on the bus is not too large, otherwise dominant periods on the bus would lengthen at the expense of recessive periods, possibly causing bit timing violations. Communication between nodes might still be possible. Without additional diagnosis on physical layer level the microcontroller has no possibility to get aware of those bus failures. The bus failure diagnosis aims to detect such failure conditions and to signal them to the application microcontroller.

How to read the bus failure flag

The Bus Failure Flag is actually signalled at the pin ERRN. When entering Normal Mode, pin ERRN first reflects the Wakeup Source flag. After four dominant periods of sufficient length have been transmitted, the Bus Failure Flag gets active at the pin ERRN.

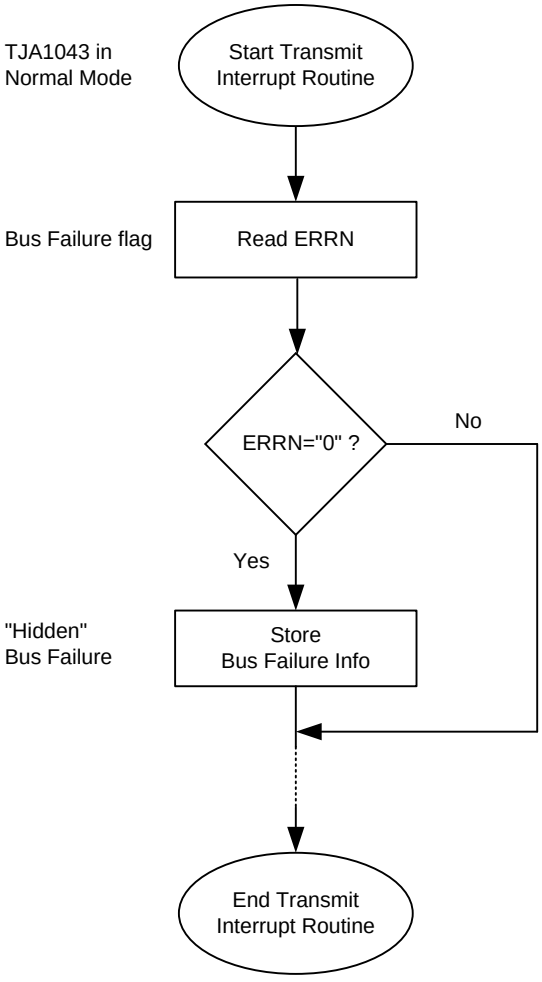


Fig 36. Flow diagram for the transmit interrupt service routine

During arbitration, when more than one node may transmit simultaneously the bus failure measurement process may be distorted, resulting in unstable bus failure information. It is

recommended that reading the Bus Failure flag from the microcontroller should take place at the end of the CAN frame only, e.g. within the transmit interrupt service routine. The read process should be completed before the transceiver sends the next CAN message. In order to be able to guarantee the four needed dominant periods each of more than 4us length, a dedicated diagnosis message with appropriate payload may be helpful, especially for high bit rates. Another option is some software filtering based on the diagnostics result of multiple message transmissions. If there is a dominance for Error signaling, there is most likely a physical problem existing like a short on the bus.

A possible flow diagram for the transmit interrupt service routine is shown in Fig 36. If reading of the pin ERRN indicates a LOW signal, a hidden bus failure must be present, because with bus failures, leading to complete corruption of communication, the transmit interrupt service routine would never be reached.

It should be noted, that even with a static bus fault condition, it cannot be guaranteed, that the ERRN pin is statically LOW and as such permanently indicating the bus fault condition. This is caused by all kind of topology related and e.g. CAN common mode choke related effects on the wiring harness. Nevertheless, the ERRN does not get LOW, if there is no bus fault condition. This includes all kind of potential GND shift situations between nodes, which is regarded to be no bus fault and a rather normal operating situation within vehicle applciations. So, any active LOW signal on ERRN is a strong indicator for a true bus short condition.

Alternative approach for bus failure flag reading

In case the earlier proposed ERRN pin evaluation during the Transmit Interrupt Service routine is not preferred an alternative approach might be chosen based on an ERRN interrupt strategy. Since the ERRN pin might toggle during error conditions, such an interrupt strategy needs to take care on potential interrupt loads to the host microcontroller. The software flow proposed in Fig 37 is showing an example, how to manage potential interrupts caused by a toggling ERRN pin.

The idea is based on the fact, that a LOW signal on ERRN is a strong indicator for a bus fault condition. As such, once this event is captured based on a ERRN falling edge interrupt, the software sets internally a kind of “Software Error Status Flag” indicating, that there is a bus fault in the system. From now onwards, it makes no sense anymore looking for edge events on the ERRN pin, which may cause high interrupt loads, if the system topology does not allow for a static ERRN signal. Instead the strategy wound be, disabling the interrupts and use the main software application flow to poll from time to time the ERRN pin. If ERRN is polled to be HIGH, a kind of simple software recovery counter is proposed to increment until a user defined threshold is reached and the failure status gets cleared. Whenever there is a LOW detected, the counter is reset, because there is still a bus error condition present. With that mechanism, the internal bus error status stays set until for a long time there is no ERRN signal found anymore. Once the error status is cleared (NERR was HIGH for a long time), the ERRN interrupt gets enabled again. With that, even very short error conditions are reliably captured and can be reported to the system, if desired.

Within the shown software flow, there is a two staged recovery mechanism shown, which can be used optionally as well. It activates the ERRN interrupt already before the software recovery counter is expired completely. Idea of that strategy is, that the polling might have missed short ERRN LOW signals. With activation of the ERRN interrupt, even such short potential ERRN signals can be captured reliably without causing high interrupt loads or clearing the internal software error status flag too early.

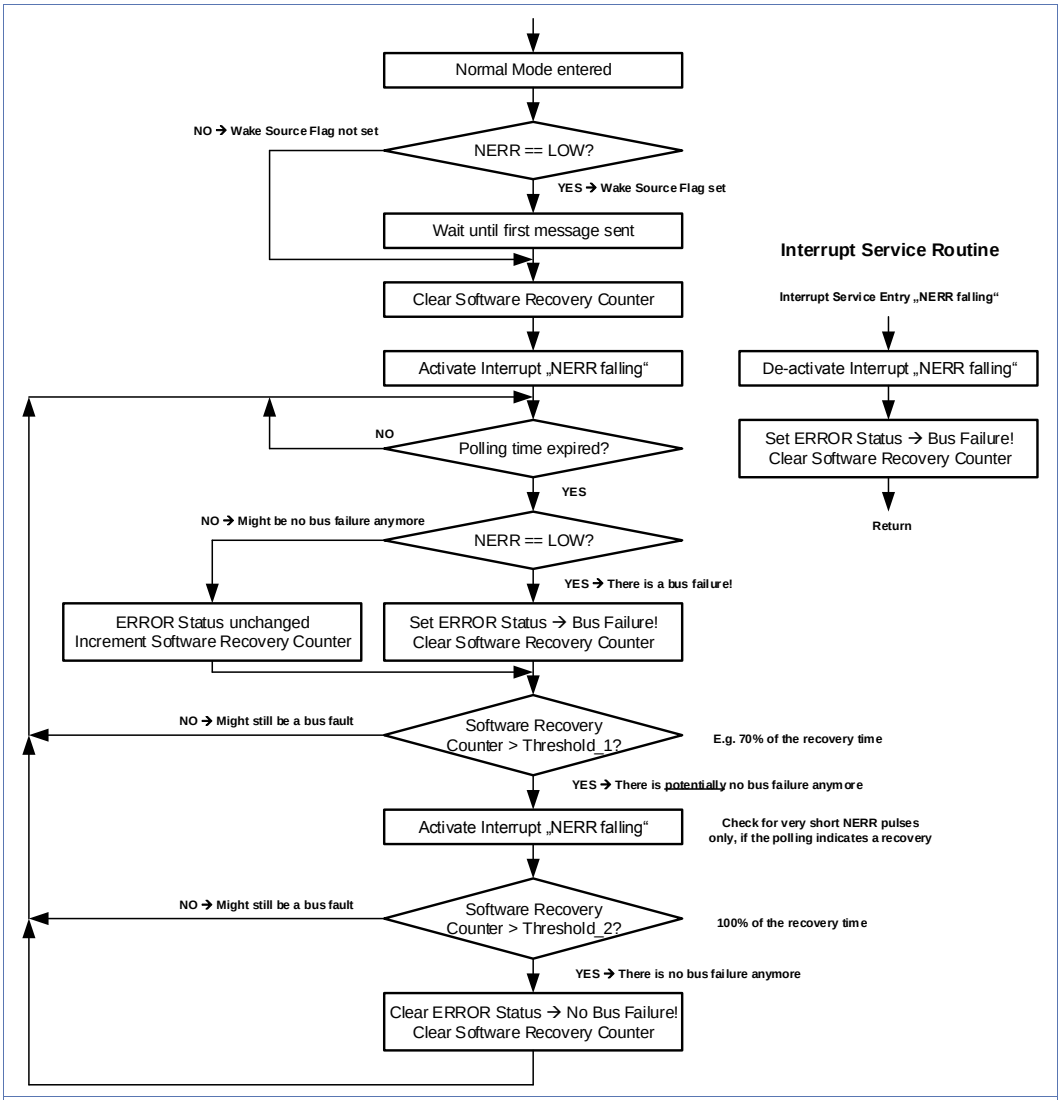


Fig 37. Optional flow diagram, ERRN monitoring by interrupt routine

6.7 Local failure diagnosis

Local failures detected and signalled at the pin ERRN in Listen-only Mode (when coming from Normal Mode) include:

- TXD Dominant Clamping
- TXD/RXD Short Circuit
- Bus dominant clamping
- Overtemperature

On detection of one of these local failures, the Local Failure Flag is set and the transmitter disabled. The failures are indicated at pin ERRN during Listen-only Mode. No other measure is taken in the case of Bus Dominant Clamping.

Recovery from local failures

Whenever the pin RXD becomes dominant while TXD is recessive, the Local Failure Flag is reset along with enabling the transmitter again. This indicates that a local failure like TXD Dominant Clamping or TXD/RXD Short Circuit does not exist. In Listen-only Mode failure recovery is immediately reflected on the pin ERRN going HIGH again.

Another way to reset the Local Failure flag and to enable the transmitter is forcing a transition into Normal Mode from any other mode. This reset option is necessary when there is no bus traffic i.e. the pin RXD does not become dominant. In this case the application microcontroller can force a transition to Normal Mode after it has read the error status in Listen-only Mode. If the failure is still present, it is detected again, disabling the transmitter. Alternatively, if the failure is cleared, normal operation is resumed. A suggested flow diagram for handling communication failures is shown in Fig 40.

TXD dominant clamping

The TXD dominant clamping detection prevents an erroneous CAN-controller from clamping the bus to dominant level by a continuously dominant TXD signal.

After a maximum allowable TXD dominant time $t_{to(dom)TXD}$ the transmitter is disabled. According to the CAN protocol only a maximum of eleven successive dominant bits are allowed on TXD (worst case of five successive dominant bits followed immediately by an error frame). Along with the minimum allowable TXD dominant time, this limits the minimum bit rate to 40 kbit/s.

TXD/RXD short circuit

Without the protection feature of the TJA1043, a TXD/RXD short circuit would result in a dead-lock situation clamping the bus dominant. If for example the transceiver receives a dominant signal, RXD outputs a dominant level. Because of the short circuit, TXD reflects a dominant signal, retaining the dominant bus state. As a result TXD and the bus are clamped continuously dominant. The resulting effect is the same as for the continuously clamped dominant TXD signal. The TXD dominant timeout interrupts the deadlock situation by disabling the transmitter. The bus and also TXD become recessive again. However, the failure scenario may still exist and with the next dominant signal on the bus the described procedure will start again. Apparently, the TXD dominant timeout alone is not sufficient to protect the bus from a local TXD/RXD short circuit.

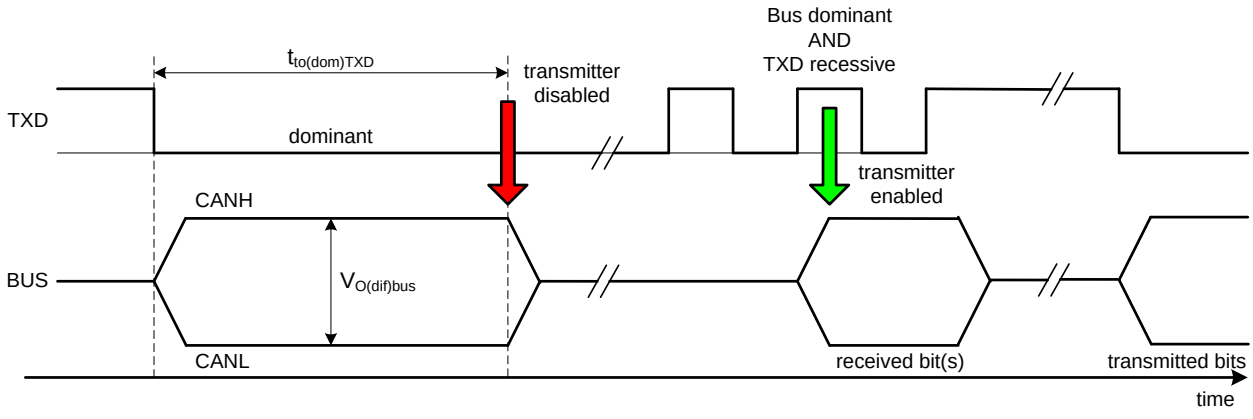


Fig 38. TXD dominant timeout and recovery mechanism

The TJA1043 keeps the transmitter off after detection of a TXD dominant clamping even if TXD gets released again. Failure recovery is performed first if the transceiver has detected a dominant bus signal while TXD is recessive. This is a clear indication that the TXD/RXD has short-circuited. Fig 38 illustrates the disabling and enabling of the transmitter with respect to a TXD/RXD short circuit. This way a local TXD/RXD short circuit will not disturb the communication of the remaining bus system.

Bus dominant clamping

In the case of a short circuit from CANH to V_{BAT}/V_{CC}, the circuit for the Common Mode Stabilization may produce a differential voltage on the bus between CANH and CANL even if there is no dominant transmitting node. This is illustrated in Fig 39. The differential voltage can be high enough to represent a dominant signal (Vdiff > 0,9 V). The result may be a permanently dominant clamped bus in the case of a short circuit from CANH to V_{BAT}.

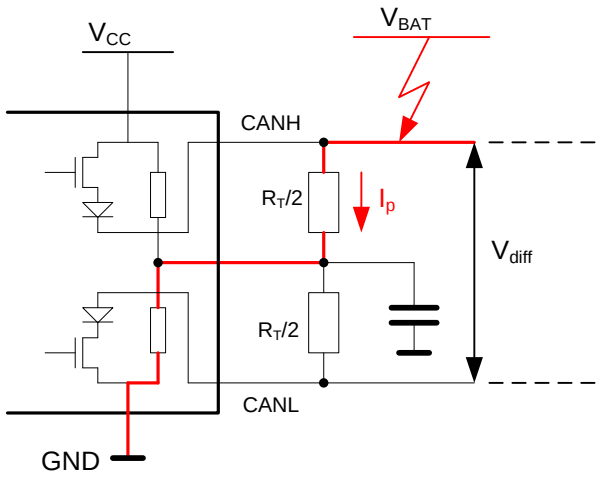


Fig 39. Bus dominant clamping in the case of a short circuit CANH to V_{BAT}

The TJA1043 can detect and report a Bus Dominant Clamping situation. If the receiver detects a bus dominant phase of longer than the bus dominant time out $t_{to(dom)bus}$, this is indicated at pin ERRN in Listen-only Mode.

Overtemperature protection

An overtemperature condition may occur either if the transceiver is operated in an environment with high ambient temperature or if there is a short circuit condition on the bus. To protect the transceiver from self-destruction the transmitter is disabled automatically whenever the junction temperature exceeds the allowed limit. In addition the Local Failure Flag is set, which can be read at pin ERRN in Listen-only Mode.

After an overtemperature condition the transmitter of the TJA1043 is released if the junction temperature is below the limit and if there is a transition into Normal Mode or reception of a dominant bus signal while TXD is recessive.

6.8 Undervoltage detection & recovery

Table 9. Supply undervoltage detection

Undervoltage on	Detection condition	Mode change to	INH pin	Bus bias
V_{CC}	$V_{CC} < V_{uvd(VCC)}$ for longer than undervoltage detection time $t_{det(uv)}$	Forced Sleep	float	GND
V_{IO}	$V_{IO} < V_{uvd(VIO)}$ for longer than undervoltage detection time $t_{det(uv)}$	Forced Sleep	float	GND
V_{BAT}	$V_{BAT} < V_{uvd(VBAT)}$	Forced Standby	V_{BAT}	float

V_{CC}/V_{IO} undervoltage detection

On detection of a V_{CC} or V_{IO} undervoltage condition the transceiver is forced autonomously into Sleep Mode by setting the internal undervoltage detection flag UVNOM, overruling the current signal combination on pin STBN and pin EN. As a result, pin INH becomes floating, disabling the voltage regulator(s).

An undervoltage condition may occur if pin V_{CC} and/or pin V_{IO} are disconnected or if there is a short circuit from V_{CC} or V_{IO} to GND e.g. due to a broken capacitor. In the case of a short circuit, disabling the voltage regulator prevents flow of high short-circuit current.

The undervoltage condition must hold at least the undervoltage detection time $t_{det(uv)}$ before the transceiver is forced into Sleep Mode. This timeout is needed to suppress the undervoltage detection during ramping up of V_{CC}/V_{IO}, e.g. on wakeup from Sleep Mode.

A wakeup event on pin WAKE or via the bus, a LOW-to-HIGH transition on pin STBN (provided that V_{IO} is present) or a battery reconnection (PWON flag) lead to reset the undervoltage detection flag UVNOM. Thus the transceiver wakes up (INH switched on) along with trying to ramp up V_{CC} and/or V_{IO} again. If there is still an undervoltage condition on V_{CC} and/or V_{IO}, the transceiver is forced into Sleep Mode again after the undervoltage detection time $t_{det(uv)}$. Hint: The recommended wake-up circuitry as proposed for the TJA1041(A) toggling WAKE after an undervoltage is not required anymore using the TJA1043 (see Fig 53).

Beside resetting the undervoltage detection flag UVNOM by external events the TJA1043 leaves the Forced Sleep Mode automatically at an undervoltage recovery on V_{CC} and V_{IO} that holds at least the undervoltage recovery time $t_{rec(uv)}$.

In all cases the TJA1043 switches to the operating mode selected by the pin STBN and pin EN after clearing the UVNOM flag (provided that also V_{BAT} is present).

Notice there is no dedicated signal to inform the microcontroller about a V_{CC} / V_{IO} undervoltage condition at the transceiver. However, the microcontroller can learn from a transceiver undervoltage condition by evaluating the pin INH. Whenever a V_{CC} or V_{IO} undervoltage has been detected by the transceiver, a pull-down resistor would pull the pin INH to LOW level.

Note: The V_{CC} undervoltage threshold is related to the V_{BAT} voltage. A V_{CC} undervoltage condition is detected only if V_{BAT} is present. The V_{IO} undervoltage threshold is related to

the V_{BAT} and the V_{CC} voltage. A V_{IO} undervoltage condition is detected if either V_{BAT} or V_{CC} is present.

Table 10. Leaving Forced Sleep Mode

Leaving Forced Sleep Mode on	Condition	Flags being set
Remote wakeup *(via CAN bus)*	Two bus dominant states of at least $t_{bus(dom)}$, with the first dominant state followed by a recessive state of at least $t_{bus(rec)}$	Wakeup
Local wakeup *(via pin WAKE)*	HIGH-to-LOW or LOW-to-HIGH level change on the WAKE pin for at least t_{WAKE}	Wakeup Wakeup Source Flag
Host wakeup *(via pin STBN)*	LOW-to-HIGH transition on STBN (provided that V_{IO} is present)	-
V_{CC} / V_{IO} undervoltage recovery	$V_{CC} > V_{uvd(VCC)}$ and $V_{IO} > V_{uvd(VIO)}$ for longer than undervoltage recovery time $t_{rec(uv)}$	-

V_{BAT} undervoltage detection

The TJA1043 monitors the battery supply voltage at the pin V_{BAT}. If the battery supply voltage falls below the undervoltage detection voltage on pin V_{BAT}, the transceiver enters autonomously the Standby Mode, overruling the mode control pins STBN and EN. In Forced Standby Mode the TJA1043 will disengage from the bus (zero load). An undervoltage condition on the pin V_{BAT} may occur for example, if the pin V_{BAT} has been disconnected, or temporarily during start of the engine (pulse 4 of ISO7637).

A V_{BAT} undervoltage condition is detected if $V_{BAT} < V_{uvd(VBAT)}$ and will recover when V_{BAT} crosses the detection threshold upwards, leaving mode control to pin STBN and EN. With first battery connection or with battery recovery the PWON flag as well as the Wakeup Flag and Wakeup Source Flag is set. The microcontroller has access to the PWON flag via the pin ERRN when the Listen-only Mode is entered from Sleep, Standby or Go-to-Sleep Mode. A transition into Normal Mode deletes the PWON flag. In this way the application microcontroller can get information about a temporary, local battery undervoltage condition suitable for applications, which need a dedicated start-up behaviour after BAT power on.

Further on setting the Wakeup and Wakeup Source Flag allows an always consistent flag setting at any power-on condition. In the previous TJA1041A the Wakeup and Wakeup Source flag got cleared at power-on. After power-on it was possible that the Wakeup and Wakeup Source flag got set without a real “local wakeup” being applied, depending on the specific V_{BAT} and WAKE pin power-up condition (differences in ramp-up times between V_{BAT} and WAKE voltage etc due to application circuitry → random start-up behaviour).

Table 11. Leaving Forced Standby Mode

Leaving Forced Sleep Mode on	Condition	Flags being set
V_{BAT} undervoltage recovery	Voltage on pin V_{BAT} recovers after previously dropping below $V_{uvd(VBAT)}$	Wakeup Wakeup Source Power-on

6.9 Software

Software flow for handling communication failures

Fig 40 suggests a software flow for handling communication failures. Starting from normal operation with the TJA1043 in Normal Mode, the host microcontroller reads the Bus Failure Flag at the pin ERRN whenever a communication failure has been reported by an error interrupt of the CAN controller or by a missing transmit interrupt.

If the Bus Failure Flag is set, the communication failure is likely to be caused by a bus failure. After a defined timeout period a new transmission attempt is performed. After a maximum number of transmission attempts have failed, an application appropriate fall-back procedure must be activated.

On the other hand, if the Bus Failure Flag is not set, the communication failure is likely to be caused by a local failure. In order to check for a local failure condition, the transceiver is forced into Listen-only Mode. If a local failure is signalled (see chapter 6.7), the application waits for recovery reading periodically the Local Failure Flag. If there was no recovery within a defined time-out period, one option can be forcing a transition into Normal Mode with releasing the transmitter. If the failure still exists, detection will disable the transmitter due to fail-safe reasons.

Another option is to use a fall-back procedure. If reading the Local Failure Flag signals that the failure is recovered, the transceiver is put into Normal Mode and normal operation continues.

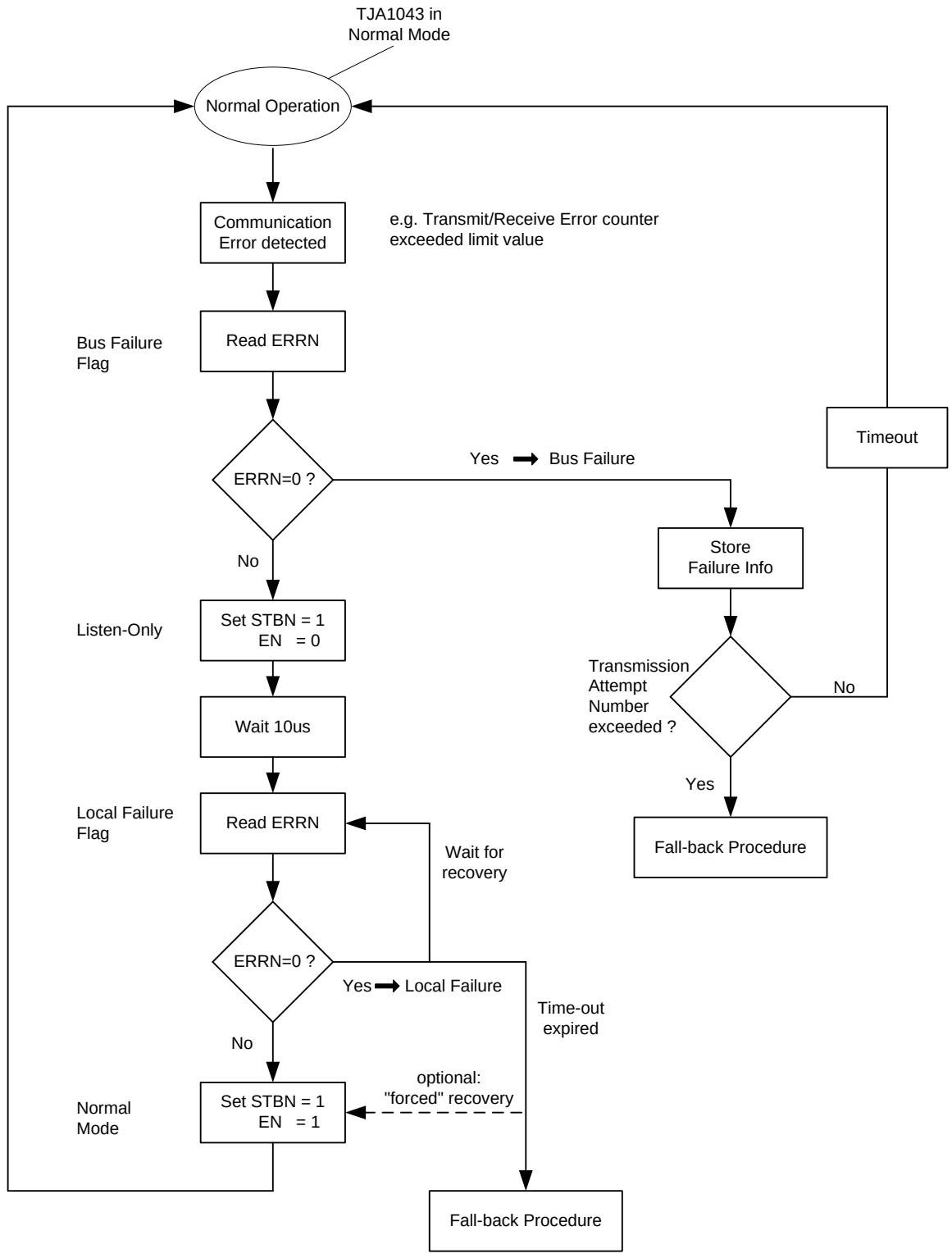


Fig 40. Flow diagram for handling communication failures

Software flow for an ECU cold start

The PWON flag of the TJA1043 indicates to the microcontroller whether a microcontroller cold start was caused by a wakeup from Sleep Mode or by a first battery power application. This information is often needed for the application to initiate some possible calibration procedures on first battery power application.

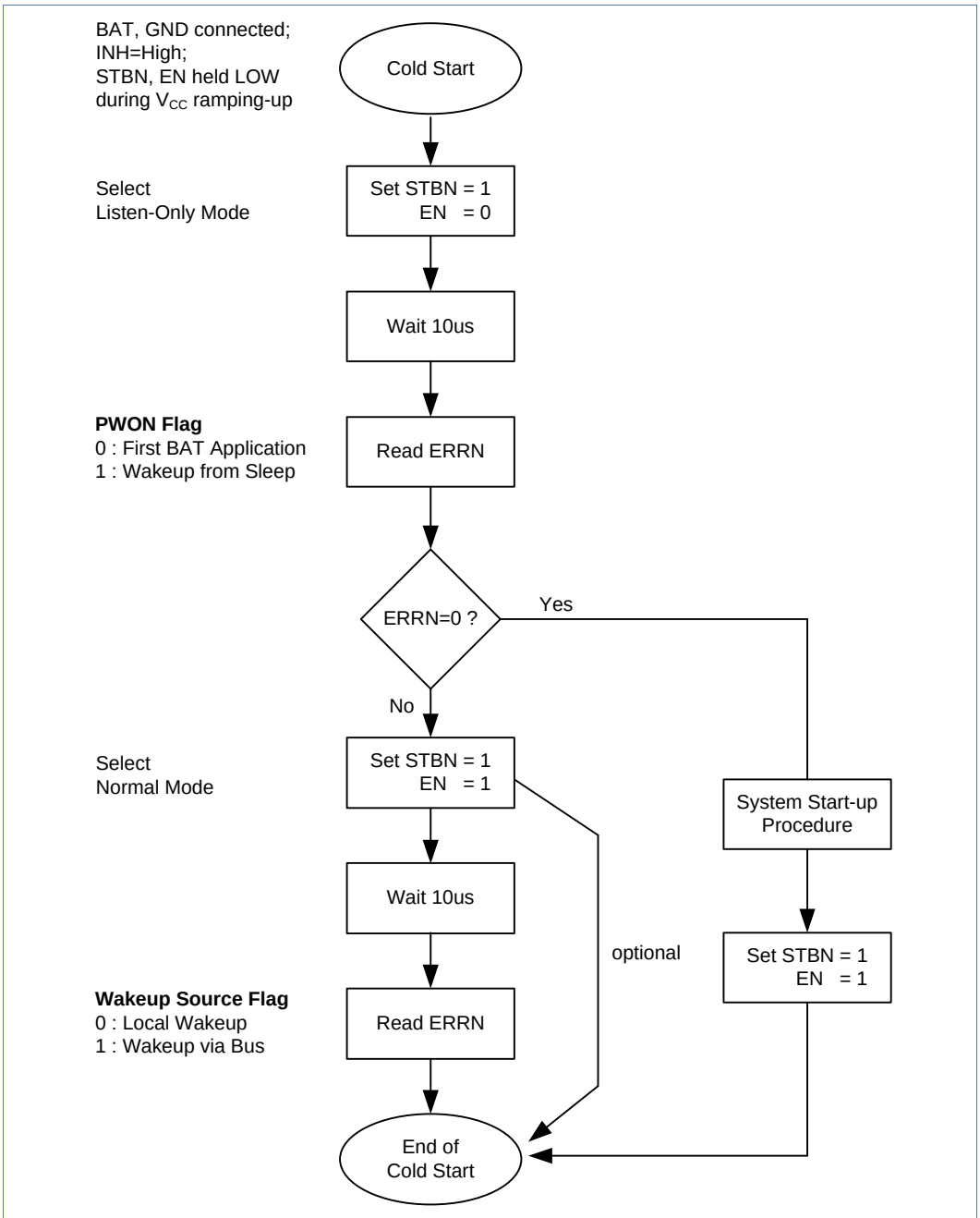


Fig 41. Flow diagram for an ECU cold start

The pin ERRN reflects the PWON flag when entering the Listen-only Mode from Standby, Sleep or Go-to-Sleep Mode. In order to offer an always consistent flag setting

at any power-on condition also the Wakeup and Wakeup Source flag get set with the PWON flag. The Wakeup and Wakeup Source flag setting thus get redundant at power-on.

Nevertheless, with a wakeup from Sleep Mode (then the PWON flag keeps cleared) the TJA1043 provides proper information on the wakeup source. Entering the Normal Mode the pin ERRN reflects the Wakeup Source Flag. A LOW signal indicates a local wakeup via the pin WAKE, whereas a HIGH signal indicates a remote wakeup via the bus.

If battery power is applied for the first time, an internal hardware reset signal is given to the transceiver for initialization. Subsequently the PWON flag is set and the pin INH is pulled to V_{BAT}, activating the voltage regulator(s) and ramping up the V_{CC} supply. Along with V_{CC} the pins RXD and ERRN go to HIGH level. With ramping up V_{CC} the microcontroller comes up. As almost all microcontrollers feature a weak pull-down or floating behavior at their port pins, the TJA1043 comes up in Standby Mode after first battery power application. This is the starting point for the application program taking over the control now. If the microcontroller comes up with a HIGH level at its port pins, the TJA1043 enters immediately the Normal Mode and the PWON flag information is irretrievably lost.

Fig 41 suggests a software flow for an ECU cold start. It considers primarily the issues related to the TJA1043 rather than representing a complete software flow. After the transceiver and microcontroller have performed their initialization, the transceiver is put into Listen-only Mode for reading the PWON flag. If a LOW signal is read on the pin ERRN, the ECU cold start was initiated by first battery power application and the microcontroller performs the corresponding system start-up procedure.

If a HIGH signal is read, the cold start was initiated by a wakeup from Sleep Mode. In order to get information on the wakeup source, Normal Mode is selected. If reading pin ERRN yields a LOW signal, there was a local wakeup via the pin WAKE. If reading yields a HIGH signal, the wakeup came via the bus. Afterwards, the cold start procedure ends and normal operation continues.

Software flow for an ECU warm start

A warm start is performed when the ECU wakes up from Standby Mode (low power level 1). Fig 42 suggests a software flow for an ECU warm start. The starting point assumes a TJA1043 transceiver in its Standby Mode and the host microcontroller in a dedicated power down mode if available. If the transceiver receives a wakeup either via the bus or via the pin WAKE, the internal Wakeup Flag is set and signalled at the pin ERRN and RXD. These signals can be used for wakeup of the microcontroller from its power down mode. The starting application program can now take control over the transceiver. If the PWON flag is of interest, the microcontroller can force the transceiver into Listen-only Mode for reading the PWON Flag. Otherwise the microcontroller can force the transceiver directly into Normal Mode for reading the Wakeup Source Flag at the pin ERRN.

As the microcontroller remains powered by the V_{CC} supply, the microcontroller can monitor its port pins for possible wakeup events. On detection of a wakeup event the microcontroller can initiate a wakeup by forcing the transceiver directly into Normal Mode. Then reading of the PWON Flag or Wakeup Source Flag is not necessary.

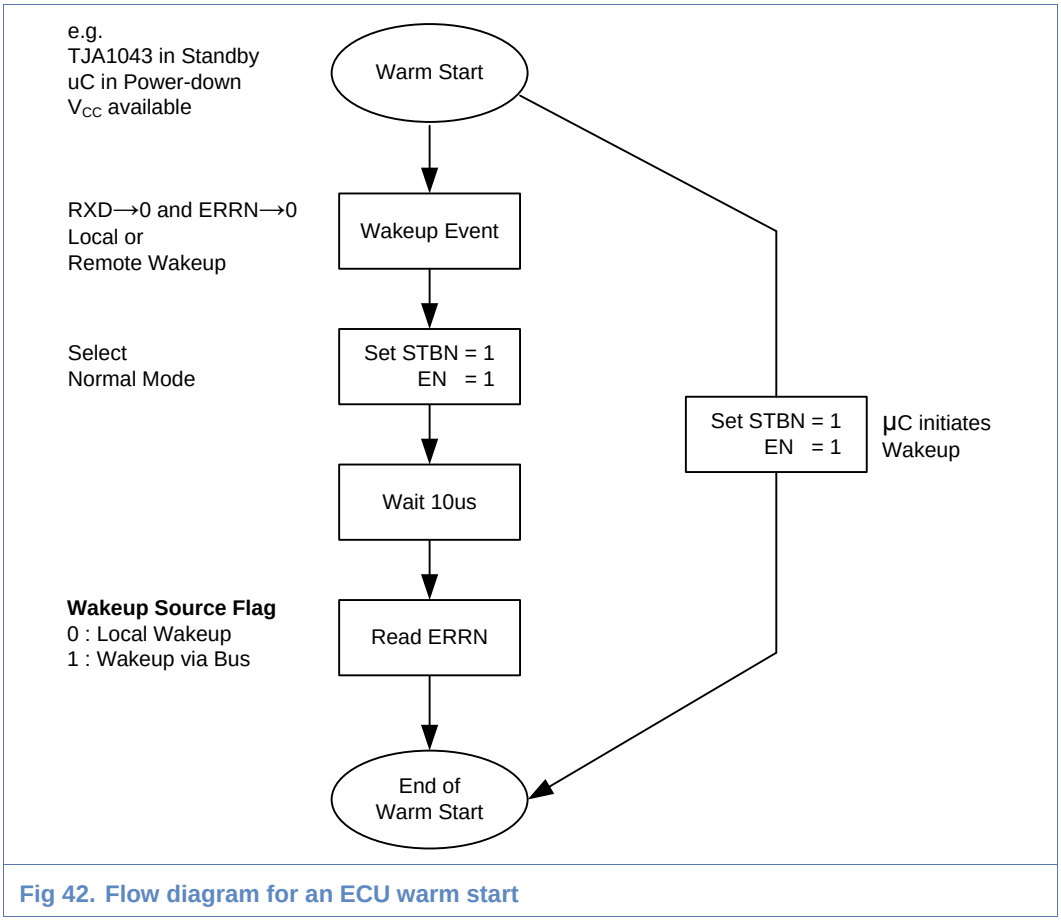


Fig 42. Flow diagram for an ECU warm start

How to enter Standby Mode (low power level 1)

When the network management decides to put the bus system into Standby, each ECU must receive an appropriate standby command. The flow diagram in Fig 43 shows the different steps in order to put the TJA1043 into Standby Mode.

On receiving a standby command (e.g. using a certain CAN message) the microcontroller has to stop all CAN transmission. In order to ensure that no CAN communication is present on the bus, caused by other nodes, the bus must have been recessive for a suitable time before the TJA1043 is put into Standby Mode by selecting STBN to LOW and EN to LOW level. If there is no system dependent “waiting period” implemented there would be the risk that a node sends out a last message while another one is already on the way towards Standby Mode. This would cause a wakeup event making it impossible to enter a system wide low-power state.

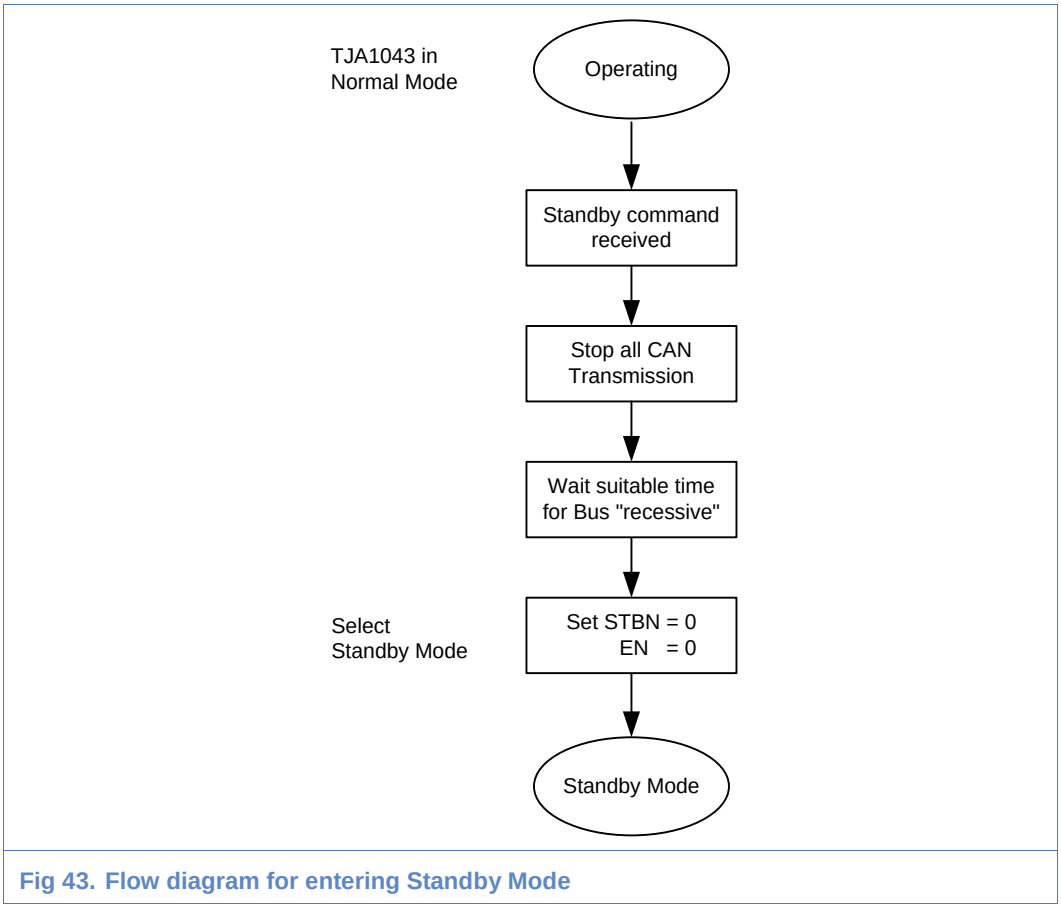


Fig 43. Flow diagram for entering Standby Mode

How to enter Sleep Mode (low power level 2)

The procedure to put an ECU into Sleep as shown in Fig 44 is similar to the previous one for entering the Standby Mode. On receiving a sleep command the microcontroller has to stop all CAN transmission. To ensure that no CAN communication is present on the bus, it must have been recessive for a suitable time before the TJA1043 is put into Sleep Mode by selecting STBN to LOW and EN to HIGH level. The difference now is that the microcontroller checks periodically for a wakeup as long as V_{CC} is not yet down. This is necessary since it might happen that a wakeup event just appears while the Go-to-Sleep Mode is processed. In this case the INH of the TJA1043 remains HIGH and the V_{CC} does not drop. Instead, the wakeup request is forwarded to the application via RXD and ERRN. Without this check the microcontroller would assume that a sleep phase follows with disabled V_{CC}, waiting forever for a power-on reset caused by a wakeup, which never happens.

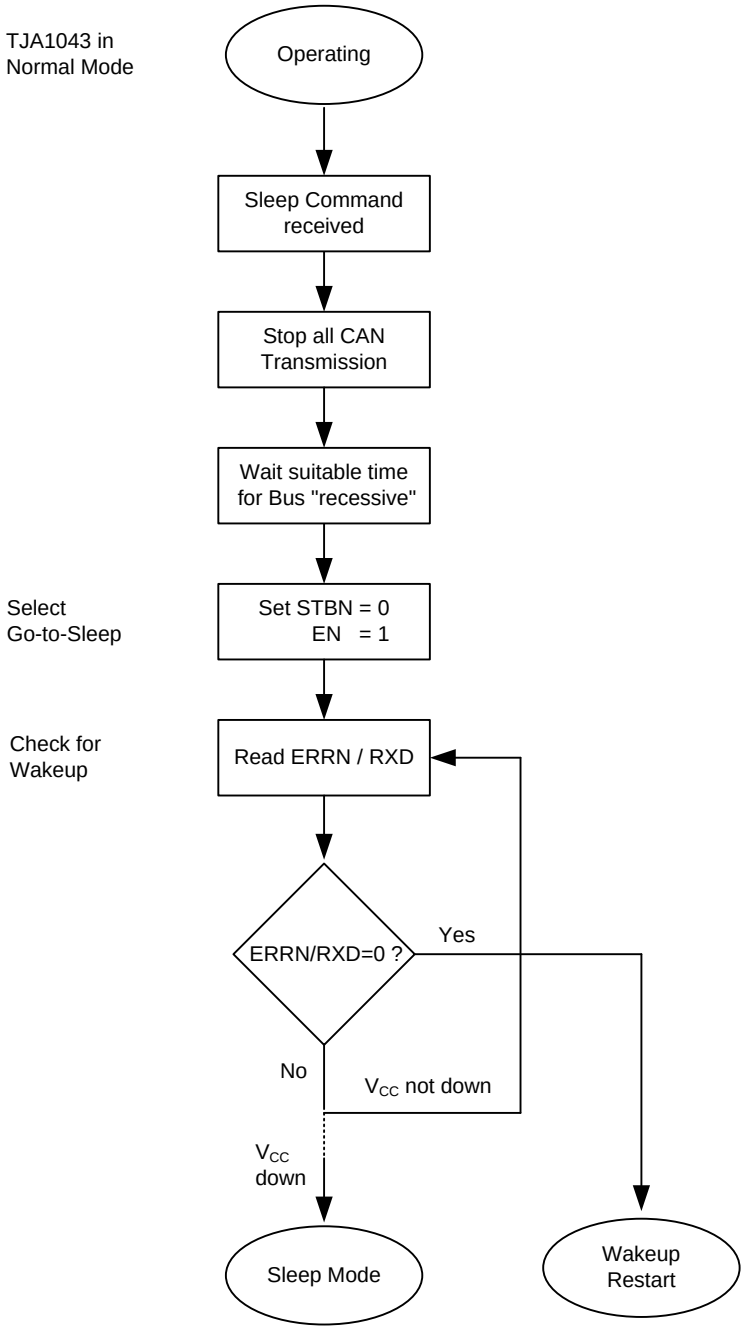


Fig 44. Flow diagram for entering Sleep Mode

7. Hardware application of common pins

7.1 Power Supply Pins

7.1.1 V_{CC} pin

The V_{CC} supply provides the current needed for the transmitter and receiver of the high speed CAN transceiver. The V_{CC} supply must be able to deliver current of 65 mA in average for the transceiver (see chapter 7.1.2).

Typically a capacitor between 47nF and 100nF is recommended being connected between V_{CC} and GND close to the transceiver. This capacitor buffers the supply voltage during the transition from recessive to dominant, when there is a sharp rise in current demand. For reliability reasons it might be useful to apply two capacitors in series connection between V_{CC} and GND. A single shorted capacitor (e.g. damaged device) cannot short-circuit the V_{CC} supply.

Using a linear voltage regulator, it is recommended to stabilize the output voltage with an additional bypass capacitor (see chapter 7.1.3) that is usually placed at the output of the voltage regulator. Its purpose is to buffer disturbances on the battery line and to buffer extra supply current demand in the case of bus failures. The calculation of the bypass capacitor value is shown in chapter 7.1.3, while in chapter 7.1.2 the average V_{CC} supply current is calculated for thermal load considerations of the V_{CC} voltage regulator. This can be done in absence and in presence of bus short-circuit conditions.

7.1.2 Thermal load consideration for the V_{CC} voltage regulator

The averages V_{CC} supply current can be calculated in absence and in presence of bus short-circuit conditions. Assuming a transmit duty cycle of 50% on pin TXD the maximum average supply current in absence of bus failures calculates to:

$$I_{CC\_norm\_avg} = 0.5 \bullet (I_{CC\_REC\_MAX} + I_{CC\_DOM\_MAX})$$

Table 12. Maximum V_{CC} supply current in recessive and dominant state

Device	$I_{CC\_REC\_MAX}$ [mA]	$I_{CC\_DOM\_MAX}$ [mA]
TJA1051	10	70
TJA1042	10	70
TJA1048	20 (both channel recessive)	140 (both channel dominant)
TJA1043	9	65

In presence of bus failures the V_{CC} supply current for the transceiver can increase significantly. The maximum dominant V_{CC} supply current $I_{CC\_DOM\_SC\_MAX}$ flows in the case of a short circuit from CANH to GND. Along with the CANH short circuit output current $I_{O(SC)}$ the maximum dominant V_{CC} supply current $I_{CC\_DOM\_SC\_MAX}$ calculates to about 120mA. This results in an average supply current of 65mA in worst case of a short circuit from CANH to GND. The V_{CC} voltage regulator must be able to handle this average supply current.

Table 13. Average V_{CC} supply current

Device	$I_{CC\_norm\_avg}$ [mA]	$I_{CC\_AVG\_SC\_MAX}$ [mA]
TJA1051	40	110
TJA1042	40	110
TJA1048	80 (both channels transmitting)	220 (both channels shorted)
TJA1043	38	109

7.1.3 Dimensioning the bypass capacitor of the voltage regulator

Depending on the power supply concept, the required worst-case bypass capacitor and the extra current demand in the case of bus failures can be calculated.

$$C_{BUFF} = \frac{\Delta I_{CC\_max\_sc} \cdot t_{dom\_max}}{\Delta V_{max}}$$

Dimensioning the capacitor gets very important with a shared voltage supply between transceiver and microcontroller. Here, extra current demand with bus failures may not lead to an unstable supply for the microcontroller. This input is used to determine the bypass capacitor needed to keep the voltage supply stable under the assumption that all the extra current demand has to be delivered from the bypass capacitor.

The quiescent current delivered from the voltage regulator to the transceiver is determined by the recessive V_{CC} supply current I_{CC_REC}.

In absence of bus failures the maximum extra supply current is calculated by:

$$\Delta I_{CC\_max} = (I_{CC\_DOM\_MAX} - I_{CC\_REC\_MIN})$$

In presence of bus failures the maximum extra supply current may be significantly higher.

Considering the worst case of a short circuit from CANH to GND the maximum extra supply current is calculated by:

$$\Delta I_{CC\_max\_sc} = (I_{CC\_DOM\_SC\_MAX} - I_{CC\_REC\_MIN})$$

Example:

With $I_{CC\_dom\_sc\_max}$ = 120 mA (estimated) and $I_{CC\_rec\_min}$ = 2 mA the maximum extra supply current calculates to

$$\Delta I_{CC\_max\_sc} = 118 \text{ mA}$$

In the case of a short circuit from CANH to GND, the bus is clamped to the recessive state, and according to the CAN protocol the uC transmits 17 subsequent dominant bits on TXD. That would mean the above calculated maximum extra supply current has to be delivered for at least 17 bit times. The reason for the 17 bit times is that at the moment the CAN controller starts a transmission, the dominant Start Of Frame bit is not fed back to RXD and forces an error frame due to the bit failure condition. The first bit of the error frame

again is not reflected at RXD and forces the next error frame (TX Error Counter +8). Latest after 17 bit times, depending on the TX Error Counter Level before starting this transmission, the CAN controller reaches the Error Passive limit (128) and stops sending dominant bits. Now a sequence of 25 recessive bits follows (8 Bit Error Delimiter + 3 Bit Intermission + 8 Bit Suspend Transmission) and the V_{CC} supply current becomes reduced to the recessive one.

Assuming that the complete extra supply current during the 17 bit times has to be buffered by the bypass capacitor, the worst-case bypass capacitor calculates to:

$$C_{BUFF} = \frac{\Delta I_{CC\_max\_sc} \cdot t_{dom\_max}}{\Delta V_{max}}$$

Whereas ΔV_{max} is the maximum allowed voltage drop at pin V_{CC} and t_{dom_max} is the dominant time of 17 bit times at 500kbit/s.

Table 14. Average V_{CC} supply current (assuming 500kbit/s)

Device	$\Delta I_{CC\_max\_sc}$	t_{dom_max}	ΔV_{max}	C_{BuFF}
TJA1051	108mA	34µs	0,5V	≈ 10µF
TJA1042	108mA	34µs	0,5V	≈ 10µF
TJA1048	216mA	34µs	0,5V	≈ 15µF
TJA1043	107mA	34µs	0,5V	≈ 10µF

Of course, depending on the regulation capabilities of the used voltage regulator the bypass capacitor may be much smaller.

7.1.4 V_{IO} pin

Pin V_{IO} is connected to the microcontroller supply voltage to provide the proper voltage reference for the input threshold of digital input pins and for the HIGH voltage of digital outputs. It defines the ratiometric digital input threshold for interface pins like TXD, EN and STBN and the HIGH-level output voltage for RXD and ERRN. All 3rd generation high speed CAN transceivers provide a continuous level adaptation from as low as 2.8V to 5.5V.

TJA1051/3

Pin V_{IO} should be connected to the microcontroller supply voltage. This will adjust the signal levels of pins TXD, RXD and S to the I/O levels of the microcontroller.

TJA1042/3

Pin V_{IO} also provides the internal supply voltage for the low-power differential receiver of the transceiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin V_{CC}. This allows applications with even less quiescent current because the 5V regulator can be switched off entirely keeping bus wake-ups still possible. For versions of the TJA1042 without a V_{IO} pin, the V_{IO} input is internally connected to V_{CC}. This sets the signal levels of pins TXD, RXD and STB to levels compatible with 5 V microcontrollers.

TJA1048

Also for the TJA1048 the low-power differential receiver is supplied out of pin V_{IO}. This allows the bus lines to be monitored for activity even if there is no supply voltage on pin V_{CC}. This allows applications with even less quiescent current because the 5V regulator can be switched off entirely keeping bus wake-ups still possible. If there is detected an undervoltage condition the transceiver will switch into OFF Mode and both CAN channels will be invisible onto the bus.

TJA1043

In Sleep Mode no current will be drawn via this pin. If the pin V_{IO} is disconnected, an undervoltage condition on V_{IO} will be detected and the transceiver is forced into Sleep Mode in order to provide defined fail-safe low-power system behavior.

7.2 Interface Pins

7.2.1 TXD pin

The transceiver receives the digital bit stream to be transmitted onto the bus via the pin TXD. When applied signals at TXD show very fast slopes, it may cause a degradation of the EMC performance. Depending on the OEM an optinal series resistor of up to 1kΩ within the TXD line between transceiver and microcontroller might be useful. Along with pin capacitance this would help to smooth the edges for some degree. For high bus speeds (close to 1 Mbit/s) the additional delay within TXD has to be taken into account. Please consult the dedicated OEM specification regarding TXD connection to the host microcontroller.

7.2.2 RXD pin

The analog bit stream received from the bus is output at pin RXD for further processing within the CAN-controller. As with pin TXD a series resistor of up to 1 kΩ can be used to smooth the edges at bit transitions. Again the additional delay within RXD has to be taken into account, if high bus speeds close to 1 Mbit/s are used. Please consult the dedicated OEM specification regarding TXD connection to the host microcontroller.

7.3 Mode control pins EN / STBN / STB / S

These input pins are mode pins and used for mode control. They are typically directly connected to an output port pin of a microcontroller.

7.4 Bus Pins CANH / CANL

The transceiver is connected to the bus via pin CANH/L. Nodes connected to the bus end must show a differential termination, which is approximately equal to the characteristic impedance of the bus line in order to suppress signal reflection. Instead of a one-resistor termination it is highly recommended using the so-called Split Termination, illustrated in

Fig 46. EMC measurements have shown that the Split Termination is able to improve significantly the signal symmetry between CANH and CANL, thus reducing emission. Basically each of the two termination resistors is split into two resistors of equal value, i.e. two resistors of 60Ω (or 62Ω) instead of one resistor of 120Ω. The special characteristic of this approach is that the common mode signal, available at the centre tap of the termination, is terminated to ground via a capacitor. The recommended value for this capacitor is in the range of 4,7nF to 47nF.

As the symmetry of the two signal lines is crucial for the emission performance of the system, the matching tolerance of the two termination resistors should be as low as possible (desired: <1%).

Additionally it is recommended to load the CANH and CANL pin each with a capacitor of about 100pF close to the connector of the ECU (see Fig 45). The main reason is to increase the robustness to automotive transients and ESD. The matching tolerance of the two capacitors should be as low as possible.

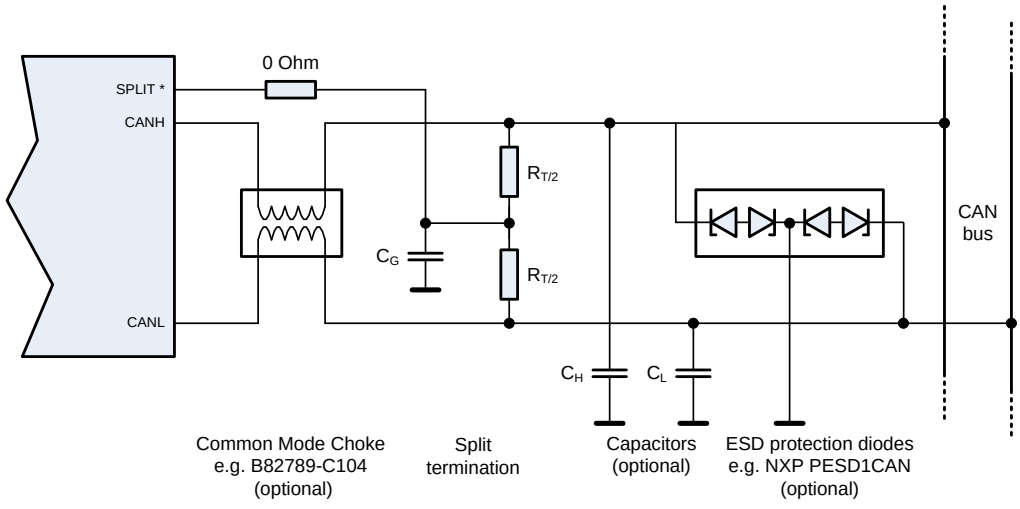
OEMs might have dedicated circuits prescribed in their specifications. Please refer to the corresponding OEM specifications for individual details.

8. EMC aspects of high speed CAN

Achieving a high EMC performance is not only a matter of the transceiver, a careful system implementation (termination, topology, external circuitry and PCB layout) is also very important.

The possibilities to further improve the EMC performance include differential and common mode filters, shielded twisted pair cable and ESD protections diodes. Additionally the PCB layout is critical to maximize the effectiveness of the EMC improvement circuit. All additional circuits could distort the signal waveform and they are also limited by the physical layer specifications.

This chapter presents some application hints (all are referenced to Fig 45) aiming to exploit the outstanding EMC performance of the 3rd generation high speed CAN transceivers.



* TJA1042, TJA1043 only.

General remark: A dedicated application may depend on specific OEM requirements.

Fig 45. Optional circuitry at CANH and CANL

8.1 Common mode choke

A common mode choke provides high impedance for common mode signals and low impedance for differential signals. Due to this, common mode signals produced by RF noise and/or by non-perfect transceiver driver symmetry get effectively attenuated while passing the choke. In fact, a common mode choke helps to reduce emission and to improve immunity against common mode disturbances without adding a large amount of distortion on CAN lines.

Former transceiver devices usually needed a common mode choke to fulfill the stringent emission and immunity requirements of the automotive industry when using unshielded twisted-pair cable. The entire 3rd generation high speed CAN transceivers have the potential to build in-vehicle bus systems without chokes. Whether a choke is needed or not

finally depends on the specific system implementation like the wiring harness and the symmetry of the two bus lines (matching tolerances of resistors and capacitors).

Besides the RF noise reduction the stray inductance (non-coupled portion of inductance) may establish a resonant circuit together with pin capacitance. This can result in unwanted oscillations between the bus pins and the choke, both for differential and common mode signals, and in extra emission around the resonant frequency. To avoid such oscillations, it is highly recommended to use only chokes with stray inductance lower than 500nH. Bifilar wound chokes typically show an even lower stray inductance. Fig 45 shows an application, using a common mode choke. As shown the choke shall be placed nearest to the transceiver bus pins.

8.2 Capacitors

Matching capacitors (in pairs) at CANH and CANL to GND (CH and CL) are frequently used to enhance immunity against electromagnetic interference. Along with the impedance of corresponding noise sources (RF), capacitors at CANH and CANL to GND form an RC low-pass filter. Regarding immunity the capacitor value should be as large as possible to achieve a low corner frequency. The overall capacitive load and impedance of the output stage establish a RC low-pass filter for the data signals. The associated corner frequency must be well above the data transmission frequency. This results in a limit for the capacitor value depending on the number of nodes and the data transmission frequency. Notice that capacitors increase the signal loop delay due to reducing rise and fall times. Due to that, bit timing requirements, especially at 500kbit/s, call for a value of lower than 100pF (see also SAE J2284 and ISO11898). At a bit rate of 125kbit/s the capacitor value should not exceed 470pF. Typically, the capacitors are placed between the common mode choke (if applied at all) and the optional ESD clamping diodes as shown in Fig 45.

8.3 ESD protection diodes

The 3rd generation high speed CAN transceivers is designed to withstand ESD pulses of up to

- ±8kV according to the IEC61000-4-2 and
- ±8kV according to the Human Body Model
- ±300V according to the Machine Model
- ±500V according to the Charged Device Model

at bus pins CANH, CANL and pin SPLIT (TJA1042, TJA1043 only) and thus typically does not need further external measures. Nevertheless, if much higher protection is required, external clamping devices can be applied to the CANH and CANL line.

NXP Semiconductors offers a dedicated protection device for the CAN bus, providing high robustness against ESD and automotive transients. The so-called PESD1CAN [11] and PESD2CAN [12] protection devices featuring a very fast diode structure with very low capacitance (typ. 11pF), is compliant to IEC61000-4-2 (level 4), thus allowing air and contact discharge of more than 15kV and 8kV, respectively. Tests at an independent test house have confirmed typically more than 20kV ESD robustness for ECUs equipped with the PESD1CAN and a choke. To be most effective the PESD1CAN diode shall be placed close to the connector of the ECU as shown in Fig 45.

8.4 Power supply buffering

Emission and immunity of transceivers also depend on signal dynamic behaviour. The capacitors placed at voltage supply pins buffer the voltage and provide the sharp rise current needed during the transition from recessive to dominant state. To calculate the size of the capacitance please refers to chapter 7.1.3.

8.5 Split termination concept

The transceiver is connected to the bus via pins CANH and CANL. Nodes connected to the bus end must show a differential termination, which is approximately equal to the characteristic impedance of the bus line in order to suppress signal reflection. Practice has shown that effective reduction of emission can be achieved by a modified bus termination concept called split termination. Instead of a one-resistor termination it is highly recommended using the split termination, illustrated in Fig 32. In addition this concept contributes to higher immunity of the bus system.

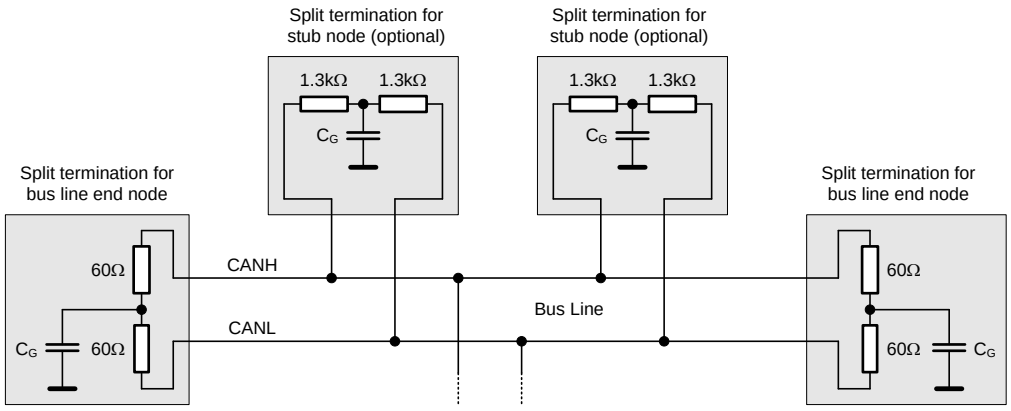


Fig 46. Typical split termination concept

Basically each of the two termination resistors of the bus line end nodes is split into two resistors of equal value, i.e. two resistors of 60Ω instead of one resistor of 120Ω. As an option, stub nodes, which are connected to the bus via stubs, can be equipped with a similar split termination configuration. The resistor value for the stub nodes has to be chosen such that the bus load of all the termination resistors stays within the specified range from 45Ω to 65Ω. As an example for up to 10 nodes (8 stub nodes and 2 bus end nodes) a typical resistor value is 1.3 kΩ. The special characteristic of this approach is that the common mode signal, available at the centre tap of the termination, is terminated to ground via a capacitor. Together with the resistors this termination concept works as a low pass filter. The recommended value for this capacitor is in the range of 4,7nF and 47nF.

In case of many high-ohmic stub nodes it can be considered to increase the main bus termination of 2 times 60Ω towards 2 times 62Ω or more. Since an automotive bus system is never “ideal” with respect to “beginning” and “end”, the overall termination is always a compromise. With that in mind, it might even be considered to have just one central bus termination in the star point of a system using 2 times 31Ω as an example.

As the symmetry of the two signal lines is crucial for the emission performance of the system, the matching tolerance of the two termination resistors should be as low as possible (desired: < 2 %).

Generally the termination strategy is prescribed by the individual OEM. Please refer to the corresponding specifications for details.

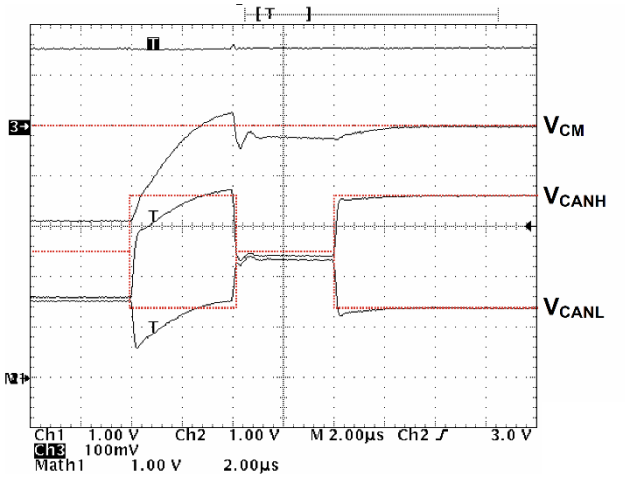
8.6 Summary of EMC improvements

The EMC performance of the 3rd generation high speed CAN transceivers has been optimized for use of the split termination without a choke. Hence, it is highly recommended to implement the split termination. The excellent output stage symmetry allows going without chokes as shown by different emission measurements. If, however, the system performance is still not sufficient, there will be the option to use additional measures like the SPLIT pin, common mode chokes, capacitors and ESD clamping diodes.

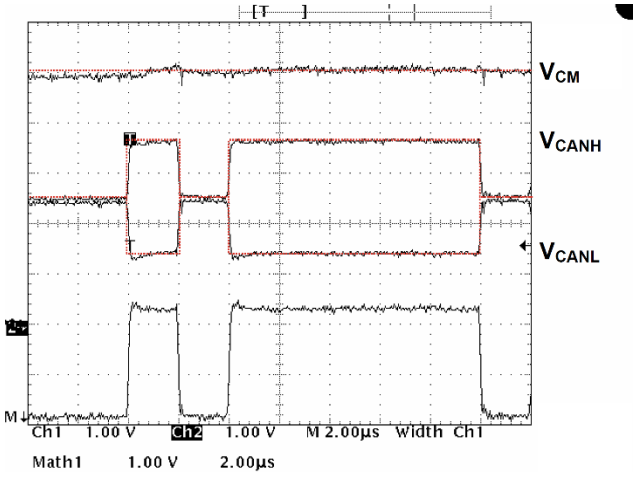
8.7 Common mode stabilization via SPLIT pin

The SPLIT pin is provided by the TJA1042 and the TJA1043.

The high impedance characteristic of the bus during recessive state leaves the bus vulnerable to even small leakage currents, which may occur with un-powered non 3rd generation or competitor high speed CAN transceivers of ECUs within the bus system. As a result the common mode voltage can show a significant voltage drop from the nominal VCC/2 value. Subsequent transmitting of the first dominant bit of a CAN-message (Start-of-Frame Bit) the common mode voltage would restore to its nominal value, leading to a large common mode step and increasing emission.



(2) Common mode ‘jump’ at the start of each CAN message without using SPLIT pin



(3) Common mode ‘jump’ effectively reduced using SPLIT pin

Fig 47. Signal common mode stabilization using SPLIT pin

The TJA1042 and TJA1043 provide means for common mode stabilization by offering a voltage source of nominal $V_{CC}/2$ at the pin SPLIT. In fact the common mode stabilization via pin SPLIT of the TJA1042 and TJA1043 significantly improves the EMC performance. It should be used if there are un-powered nodes while other nodes keep communicating. The DC stabilization aims to oppose this degradation and helps improving the emission performance. With no significant leakage currents from the bus, the pin SPLIT can be left open. According to the data sheet [7] the maximum impedance of the voltage source can be calculated to about 2kΩ.

8.8 GND offset and Common mode range

Bus systems in automotive have to deal with ground-offsets between the various nodes. This means that each node can “see” different single-ended bus voltages on the bus lines according to their own ground level, whereas the differential bus voltage remains unaffected.

NXPs 3rd generation high speed CAN transceivers allow a maximum allowable single-ended voltage of CANH is +30 V, while the maximum allowable single-ended voltage of CANL is -30 V. With single-ended bus voltages within this range, it is guaranteed that the differential receiver threshold voltage lies between 0.5 and 0.9 V in Normal Mode. The allowable single-ended voltage range is known as the common mode range of the differential receiver. The ISO11898-5 [19] calls for a common mode range from -12 V to +12 V. So, the NXP transceivers exceed the common mode range with respect to ISO11898-5.

Slightly exceeding the specified common mode range does not lead immediately to communication failures, but significant exceeding has to be avoided. There is a limitation for tolerable ground-offsets. The relation between the common mode range and the maximum allowable ground-offset is illustrated in Fig 48 and Fig 49. Fig 48 shows the case where the ground level of a transmitting node 2 lies above that of a receiving node 1. In this case the maximum allowable ground-offset corresponds to the maximum single-ended voltage of 30 V for CANH with respect to the ground level of the receiving node. The maximum allowable ground-offset can be derived from Fig 48 to be 26V ($GND_{transmit}$ - $GND_{receive}$).

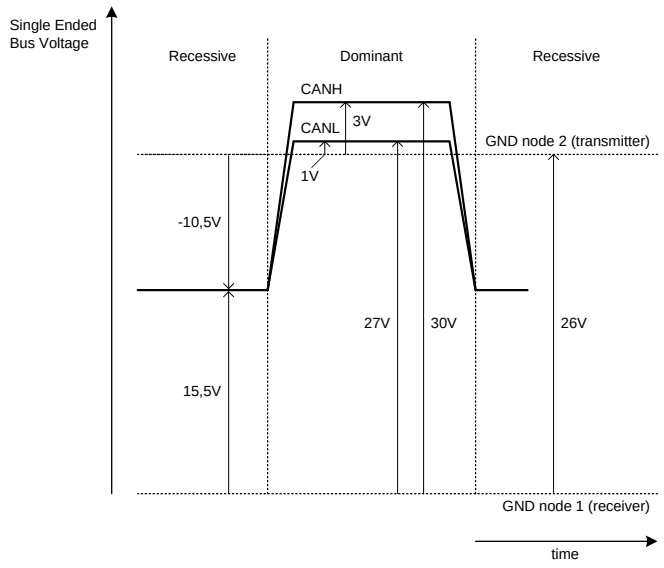


Fig 48. Ground level of the transmitting node 2 lies above that of the receiving node 1

Fig 49 shows the case where the ground level of the sending node 1 lies below that of the receiving node 2. In this case the maximum allowable ground-offset corresponds to the minimum single-ended voltage of -30 V for CANL with respect to the ground level of the receiving node 2. The maximum allowable ground-offset can be derived from Fig 49 to be -31V ($GND_{transmit}$ - $GND_{receive}$). As each node in a bus system acts temporarily as transmitter, the maximum allowable ground-offset for NXPs 3rd generation high speed CAN transceivers between any two nodes is limited to 26V. For transceivers just fulfilling the ISO11898-5 requested common mode range the allowable ground-offset is limited to 8V only.

In recessive bus state each node tries to pull the bus lines according to their biasing and ground level resulting in an average recessive bus voltage. In the example of Fig 48 the recessive bus voltage is found to be around 15,5V with respect to the ground level of the receiving node and -10,5V with respect to the ground level of the sending node.

The two examples in Fig 48 and Fig 49 indicate that ground-offsets in a bus system disturb significantly the symmetrical character of CANH and CANL with respect to the recessive voltage level. This implies the generation of unwanted common mode signals, which increase electromagnetic emission. Since emission is very sensitive towards ground-offsets, appropriate system implementation has to prevent ground-offset sources.

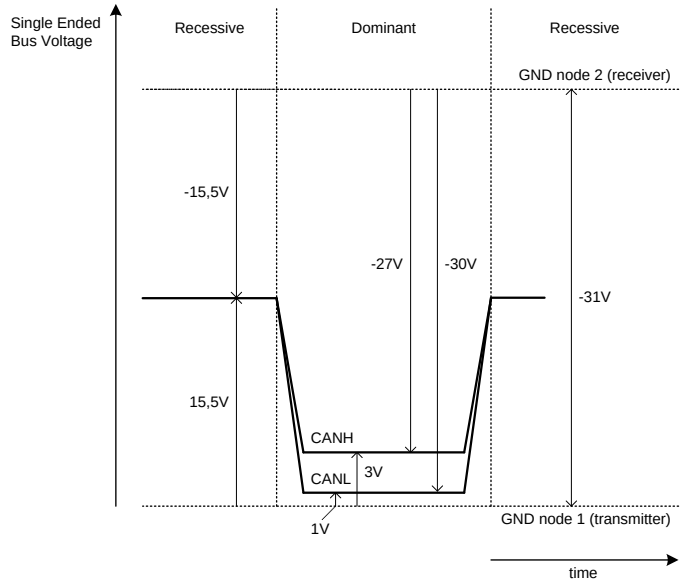


Fig 49. Ground level of the transmitting node 2 lies below that of the receiving node 1

Remark: From static (DC) point of view such high voltage shifts are not considered at all in automotive applications between different nodes. Nevertheless under electromagnetic interferences (dynamically) a high Common Mode Range enhances the immunity of a high speed CAN transceiver because of dynamic ground offsets between nodes.

8.9 PCB layout rules (check list)

Following guidelines should be considered for the PCB layout.

- When a common mode choke is used, it should be placed close to the transceiver bus pins CANH and CANL.
- The PCB tracks for the bus signals CANH and CANL should be routed close together in a symmetrical way. Its length should not exceed 10cm.
- Avoid routing other “off-board” signal lines parallel to the CANH/CANL lines on the PCB due to potential “single ended” noise injection into CAN wires.
- The ESD protection should be connected close to the ECU connector bus terminals.
- Place V_{CC} and V_{IO} capacitor close to transceiver pin.
- For TJA1051/3 and TJA1042/3: Decouple the V_{IO} pin by a capacitor to V_{CC} (instead GND) close to the transceiver pin to achieve a high-frequent short of the supplies and thus to improve the electromagnetic immunity by enabling the same HF-conditions like existing with V_{CC} connected directly to V_{IO} in 5V-only environments.
- The track length between communication controller / µC and transceiver should be as short as possible
- The ground impedance between communication controller (µC) and transceiver should be as low as possible.
- Avoid applying filter elements into the GND signal of the µC or the Transceiver. GND has to be the same for Transceiver and µC.

9. Bus network aspects of high speed CAN

This chapter deals with items like the maximum number of nodes, the maximum bus line length and topology aspects. Especially the topology appears to have a significant influence on the system performance.

9.1 Maximum number of nodes

The number of nodes, which can be connected to a bus, depends on the minimum load resistance a transceiver can drive. NXPs 3rd generation high speed CAN transceivers provide an output drive capability down to a minimum load of $R_{L,min}$ = 45Ohm for V_{CC} > 4,5 V (4,75V for the TJA1048). The overall busload is defined by the termination resistance R_T, the bus line resistance R_W and the transceiver's differential input resistance $R_{i(dif)}$. The DC circuit model of a bus system is shown in Fig 50. For worst case consideration the bus line resistance R_W is considered to be zero. This leads to the following relations for calculating the maximum number of nodes:

$$\frac{R_{T,\min} * R_{i(dif),\min}}{n_{\max} * R_{T,\min} * 2R_{i(dif),\min}} \geq R_{L,\min}$$

Rearranged to n_{max}:

$$n_{\max} \leq R_{i(dif),\min} * \left(\frac{1}{R_{L,\min}} - \frac{2}{R_{T,\min}} \right)$$

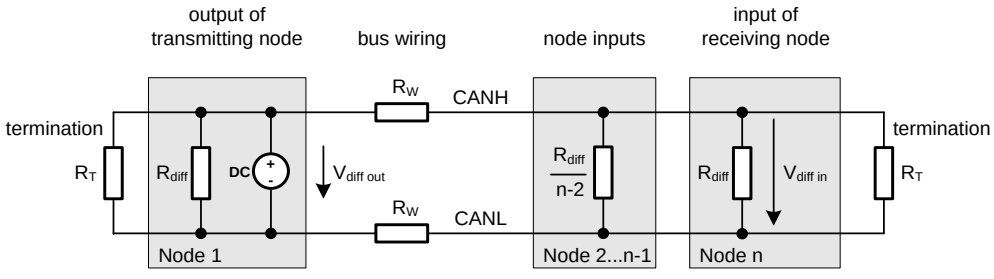


Fig 50. DC circuit model for a bus system according to ISO11898

Table 15 gives the maximum number of nodes for two different termination resistances. Notice that connecting a large number of nodes requires relatively large termination resistances.

Table 15. Maximum number of nodes (see data sheets for $R_{dif,min}$ and $R_{L,min}$)

Transceiver	$R_{i(dif),min}$(kOhm)	$R_{L,min}$(Ohm)	Nodes (maximum) ($R_{T,min}$=118Ohm)	Nodes (maximum) ($R_{T,min}$=130Ohm)
TJA1051, TJA1042 TJA1048, TJA1043	19	45	100	129

9.2 Maximum bus line length

The maximum achievable bus line length in a CAN network is determined essentially by the following physical effects:

1. Loop delays of the connected bus nodes (CAN controller, transceiver etc.) and the delay of the bus line.
2. Relative oscillator tolerance between nodes.
3. Signal amplitude drop due to the series resistance of the bus cable and the input resistance of bus nodes (for a detailed description refer to [21]).

Effects 1 and 2 result in a value for the maximum bus line length with respect to the CAN bit timing [21]. Effect 3, on the other hand, results in a value with respect to the output signal drop along the bus line. The minimum of the two values has to be taken as the actual maximum allowable bus line length. As the signal drop is only significant for very long lengths, effect 3 can often be neglected for high data rates.

Table 16. Maximum bus line length for some standards

Specification	Data rate		
	125 kBit/s (BT tol. = +/- 1,25%)	250 kBit/s (BT tol. = +/- 0,75%)	500 kBit/s (BT tol. = +/- 0,5%)
SAE J2284	50 m	50 m	33 m
TJA1051, TJA1042 TJA1048, TJA1043	80 m	80 m	40 m

(BT tol. = Bit Time Tolerance)

Table 16 gives the maximum bus line length for the bit rates 125 kbit/s, 250 kbit/s and 500 kbit/s, along with values specified in the SAE J2284 [20] standard associated to CAN. The calculation is based on effects 1 and 2 assuming a minimum propagation delay between any two nodes of 200 ns and a maximum bus signal delay of 8 ns/m. Notice that the stated values apply only for a well-terminated linear topology. Bad signal quality because of inadequate termination can lower the maximum allowable bus line length.

9.3 Topology

The topology describes the wiring harness structure. Typical structures are linear, star- or multistar-like. In automotive, shielded or unshielded twisted pair cable usually functions as a transmission line. Transmission lines are generally characterized by the length-related resistance R_{Length}, the specific line delay t_{delay} and the characteristic line impedance Z. Table 17 shows the physical media parameters specified in the ISO11898 and SAE J2284 standard. Notice that SAE J2284 specifies the twist rate r_{twist} in addition.

Table 17. Physical media parameters of a pair of wires (shielded or unshielded)

Parameter	Notation	Unit	ISO11898			SAE J2284		
			Min.	Typ.	Max.	Min.	Typ.	Max.
Impedance	Z	Ohm	95	120	140	108	120	132
Length-related resistance	R_{Length}	mOhm/m	-	70	-	-	70	-
Specific line delay	t_{delay}	ns/m	-	5	-	-	5,5	-
Twist rate	r_{twist}	twist/m	-	-	-	33	-	50

Ringing due to signal reflections

Transmission lines must be terminated with the characteristic line impedance, otherwise signal reflections will occur on the bus causing significant ringing. The topology has to be chosen such that reflections will be minimized. Often the topology is a trade-off between reflections and wiring constraints.

CAN is well prepared to deal with reflection ringing due to some useful protocol features:

- Only recessive to dominant transitions are used for resynchronization.
- Resynchronization is allowed only once between the sample points of two bits and only, if the previous bit was sampled and processed with recessive value.
- The sample point is programmable to be close to the end of the bit time.

Linear topology

The high speed CAN standard ISO11898 defines a single line structure as network topology. The bus line is terminated at both ends with a single termination resistor. The nodes are connected via not terminated drop cables or stubs to the bus. To keep the ringing duration short compared to the bit time, the stub length should be as short as possible. For example the ISO11898 standard limits the stub length to 0.3 m at 1 Mbit/s. The corresponding SAE standard, J2284-500, recommends keeping the stub length below 1 m. To minimize standing waves, ECUs should not be placed equally spaced on the network and cable tail lengths should not all be the same [20] . Table 18 along with Fig 51 illustrate the topology requirements of the SAE J2284-500 standard. At lower bit

rates the maximum distance between any two ECUs as well as the ECU cable stub lengths may become longer.

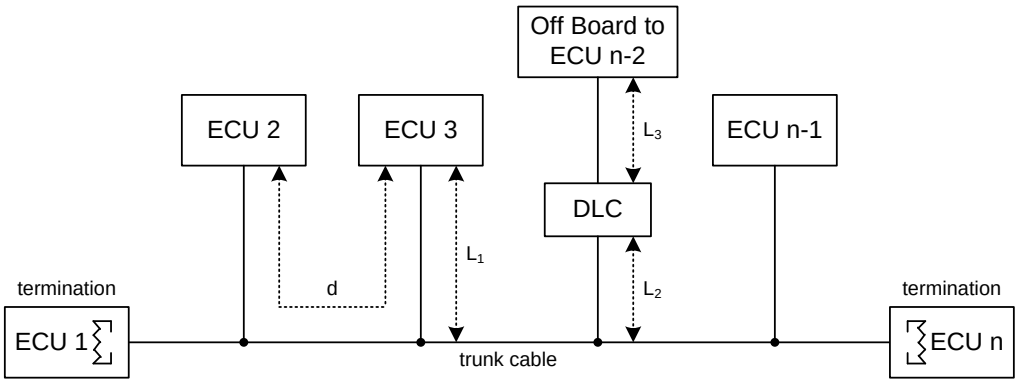


Fig 51. Topology requirements of SAE J2284

In practice some deviation from that stringent topology proposals might be necessary, because longer stub lengths are needed. Essentially the maximum allowable stub length depends on the bit timing parameters, the trunk cable length and the accumulated drop cable length.

The star topology is neither covered by ISO11898 nor by SAE J2284. However, it is sometimes used in automotive applications to overcome wiring constraints within the car. Generally, the signal integrity suffers from a star topology compared to a linear topology.

Table 18. ECU topology requirements of SAE J2284-500

Parameter	Symbol	Unit	Min.	Nom.	Max.
ECU cable stub length	L1	m	0	-	1
In-vehicle DLC cable stub length	L2	m	0	-	1
Off board DLC cable stub length	L3	m	0	-	5
Distance between any two ECUs	D	m	0,1	-	33

Note: It is recommended to prove the feasibility of a specific topology in each case by simulations or measurements on a system setup.

10. Appendix

10.1 Pin FMEA

This chapter provides an FMEA (Failure Mode and Effect Analysis) for typical failure situations, when dedicated pins of the 3rd generation HS-CAN transceivers are short-circuited to supply voltages like V_{BAT}, V_{CC}, GND or to neighbored pins or simply left open. The individual failures are classified, due to their corresponding effects on the transceiver and bus communication in Table 19.

Table 19. Classification of failure effects

Class	Effects
A	- Damage to transceiver - Bus may be affected
B	- No damage to transceiver - No bus communication possible
C	- No damage to transceiver - Bus communication possible - Corrupted node excluded from communication
D	- No damage to transceiver - Bus communication possible - Reduced functionality of transceiver

10.1.1 TJA1051

Table 20. TJA1051 FMEA matrix for pin short-circuits to V_{BAT} and V_{CC}

Pin	Short to V_{BAT} (12V … 40 V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
(1) TXD	A	Limiting value exceeded	C	TXD clamped recessive
(2) GND	C	Node is left unpowered	C	V_{CC} undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(3) V_{CC}	A	Limiting value exceeded	-	-
(4) RXD	A	Limiting value exceeded	C	RXD clamped recessive; Bus communication may be disturbed
(5) n.c.	-	-	-	-
(5) V_{IO}	A	Limiting value exceeded	C	uC may be damaged, if $V_{CC} > V_{IO}$
(5) EN	A	Limiting value exceeded	D	Off Mode not selectable
(6) CANL	B	No bus communication	B	No bus communication
(7) CANH	D	Degration of EMC;	D	Degration of EMC;

Pin	Short to V_{BAT} (12V … 40 V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
		Bit iming violation possible		Bit iming violation possible
(8) S	A	Limiting value exceeded	C	Normal Mode not selectable

Table 21. TJA1051 FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open	
	Class	Remark	Class	Remark
(1) TXD	C	TXD dominant clamping; Transmitter is disabled	C	TXD clamped recessive
(2) GND	-	-	C	Undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(3) V_{CC}	C	V_{CC} undervoltage detected; TRX enters Off Mode and behaves passive to the bus	C	V_{CC} undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(4) RXD	C	RXD clamped dominant	C	Node may produce error frames until bus-off is entered
(5) n.c.	-	-	-	-
(5) V_{IO}	C	V_{IO} undervoltage detected; TRX enters Off Mode and behaves passive to the bus	C	V_{IO} undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(5) EN	C	Normal and Silent Mode not selectable	C	Normal and Silent Mode not selectable
(6) CANL	C	Degration of EMC; Bit iming violation possible	C	Transmission not possible
(7) CANH	B	No bus communication	C	Transmission not possible
(8) S	D	Silent Mode not selectable	D	Silent Mode not selectable

Table 22. TJA1051 FMEA matrix for pin short-circuits to neighbored pins

Pin	Short to neighbored pin	
	Class	Remark
TXD - GND	C	Transmitter disabled after TXD dominant timeout
GND - V_{CC}	C	V_{CC} undervoltage detected; TRX enters Off Mode and behaves passive to the bus
V_{CC} - RXD	C	RXD clamped recessive
n.c. - CANL	-	-
V_{IO} - CANL	B	No bus communication
EN - CANL	C	TRX is not able to enter Normal or Listen-only Mode if the bus is driven dominant
CANL - CANH	B	No bus communication
CANH - S	C	TRX is not able to enter Normal Mode if the bus is driven dominant

10.1.2 TJA1042

Table 23. TJA1042 FMEA matrix for pin short-circuits to V_{BAT} and V_{CC}

Pin	Short to V_{BAT} (12V … 40 V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
(1) TXD	A	Limiting value exceeded	C	TXD clamped recessive
(2) GND	C	Node is left unpowered	C	V_{CC} undervoltage detected; TRX enters - Standby Mode (TJA1042/3) - Off Mode (TJA1042)
(3) V_{CC}	A	Limiting value exceeded	-	-
(4) RXD	A	Limiting value exceeded	C	RXD clamped recessive; Bus communication may be disturbed
(5) SPLIT	D	Bus charged to V_{BAT} level; Bit timing violation possible	D	Bus charged to V_{CC} level; Bit timing violation possible
(5) V_{IO}	A	Limiting value exceeded	C	uC may be damaged, if $V_{CC} > V_{IO}$
(6) CANL	B	No bus communication	B	No bus communication
(7) CANH	D	Degration of EMC; Bit timing violation possible	D	Degration of EMC; Bit iming violation possible
(8) STB	A	Limiting value exceeded	C	Normal Mode not selectable

Table 24. TJA1042 FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open	
	Class	Remark	Class	Remark
(1) TXD	C	TXD dominant clamping; Transmitter is disabled	C	TXD clamped recessive
(2) GND	-	-	C	Undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(3) V_{CC}	C	V_{CC} undervoltage detected; TRX enters Standby Mode	C	V_{CC} undervoltage detected; TRX enters Standby Mode
(4) RXD	C	RXD clamped dominant	C	Node may produce error frames until bus-off is entered
(5) SPLIT	D	Bus discharged to GND level; Bit timing violation possible	D	No DC common mode stabilization
(5) V_{IO}	C	V_{IO} undervoltage detected; TRX enters Off Mode and behaves passive to the bus	C	V_{IO} undervoltage detected; TRX enters Off Mode and behaves passive to the bus
(6) CANL	C	Degration of EMC; Bit timing violation possible	C	Transmission not possible
(7) CANH	B	No bus communication	C	Transmission not possible
(8) STB	D	Standby Mode not selectable	C	Normal Mode not selectable

Table 25. TJA1042 FMEA matrix for pin short-circuits to neighbored pins

Pin	Short to neighbored pin	
	Class	Remark
TXD - GND	C	Transmitter disabled after TXD dominant timeout
GND - V_{CC}	C	V_{CC} undervoltage detected; TRX enters Standby Mode
V_{CC} - RXD	C	RXD clamped recessive
SPLIT - CANL	D	Degration of EMC; Bit timing violation possible
V_{IO} - CANL	B	No bus communication
CANL - CANH	B	No bus communication
CANH - STB	C	TRX is not able to enter Normal Mode if the bus is driven dominant

10.1.3 TJA1048

Table 26. TJA1048 FMEA matrix for pin short-circuits to V_{BAT} and V_{CC}

Pin	Short to V_{BAT} (12V … 40 V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
(1) TXD1	A	Limiting value exceeded	C	TXD1 clamped recessive
(2) GNDA	C	Node is left unpowered	C	V_{CC} undervoltage detected; Both TRX enter Standby Mode
(3) V_{CC}	A	Limiting value exceeded	-	-
(4) RXD1	A	Limiting value exceeded	C	RXD1 clamped recessive; Channel 1 bus communication may be disturbed
(5) GNDB	C	Node is left unpowered	C	V_{CC} undervoltage detected; Both TRX enter Standby Mode
(6) TXD2	A	Limiting value exceeded	C	TXD2 clamped recessive
(7) RXD2	A	Limiting value exceeded	C	RXD2 clamped recessive; Channel 2 bus communication may be disturbed
(8) STBN2	A	Limiting value exceeded	D	Channel 2 Standby Mode not selectable
(9) CANL2	B	No bus communication	B	Channel 2 no bus communication
(10) CANH2	D	Degration of EMC; Bit timing violation possible	D	Channel 2 degration of EMC; Bit timing violation possible
(11) V_{IO}	A	Limiting value exceeded	C	uC may be damaged, if $V_{CC} > V_{IO}$
(12) CANL1	B	No bus communication	B	Channel 1 no bus communication
(13) CANH1	D	Degration of EMC; Bit timing violation possible	D	Channel 1 degration of EMC; Bit timing violation possible
(14) STBN1	A	Limiting value exceeded	D	Channel 1 Standby Mode not selectable

Table 27. TJA1048 FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open	
	Class	Remark	Class	Remark
(1) TXD1	C	TXD1 dominant clamping; Transmitter is disabled	C	TXD1 clamped recessive
(2) GNDA	-	-	C	Undervoltage detected; Both TRXs enter Off Mode and behave passive to the bus
(3) V_{CC}	C	V_{CC} undervoltage detected; Both TRX enter Standby Mode	C	V_{CC} undervoltage detected; Both TRX enter Standby Mode
(4) RXD1	C	RXD1 clamped dominant	C	Node may produce error frames on channel 1 until bus-off is entered
(5) GNDB	-	-	C	Undervoltage detected; Both TRX enter Off Mode and behave passive to the bus
(6) TXD2	C	TXD2 dominant clamping; Transmitter is disabled	C	TXD2 clamped recessive
(7) RXD2	C	RXD2 clamped dominant	C	Node may produce error frames on channel 2 until bus-off is entered
(8) STBN2	C	Channel 2 Normal Mode not selectable	C	Channel 2 Normal Mode not selectable
(9) CANL2	D	Channel 2 degration of EMC; Bit timing violation possible	C	Channel 2 transmission not possible
(10) CANH2	B	Channel 2 no bus communication	C	Channel 2 transmission not possible
(11) V_{IO}	C	V_{IO} undervoltage detected; Both TRX enter Off Mode and behave passive to the bus	C	V_{IO} undervoltage detected; Both TRX enter Off Mode and behave passive to the bus
(12) CANL1	D	Channel 1 degration of EMC; Bit timing violation possible	C	Channel 1 transmission not possible
(13) CANH1	B	Channel 1 no bus communication	C	Channel 1 transmission not possible
(14) STBN1	C	Channel 1 Normal Mode not selectable	C	Channel 1 Normal Mode not selectable

Table 28. TJA1048 FMEA matrix for pin short-circuits to neighbored pins

Pin	Short to neighbored pin	
	Class	Remark
TXD1 - GNDA	C	Transmitter 1 disabled after TXD dominant timeout
GNDA - V_{CC}	C	V_{CC} undervoltage detected; Both TRX enter Standby Mode
V_{CC} - RXD1	C	RXD 1 clamped recessive
RXD1 - GNDB	C	RXD 1 clamped dominant
GNDB - TXD2	C	Transmitter 2 disabled after TXD dominant timeout
TXD2 - RXD2	B	Temporary channel 2 bus blocking possible; Bus 2 is released after TXD dominant timeout
STBN2 - CANL2	B	TRX 2 enters Standby Mode of the bus is driven dominant
CANL2 - CANH2	B	No bus communication on channel 2
CANH2 - V_{IO}	D	Degration of EMC; Bit timing violation possible
V_{IO} - CANL1	B	No bus communication on channel 1
CANL1 - CANH1	B	No bus communication on channel 1
CANH1 - STBN1	D	TRX is not able to enter Standby Mode if the bus is driven dominant

10.1.4 TJA1043

Table 29. TJA1043 FMEA matrix for pin short-circuits to V_{BAT} and V_{CC}

Pin	Short to V_{BAT} (12V … 40 V)		Short to V_{CC} (5V)	
	Class	Remark	Class	Remark
(1) TXD	A	Limiting value exceeded	C	TXD clamped recessive
(2) GND	C	Node is left unpowered	C	VCC undervoltage detected; TRX goes to Sleep
(3) V_{CC}	A	Limiting value exceeded	-	-
(4) RXD	A	Limiting value exceeded	C	RXD clamped recessive; Bus communication may be disturbed
(5) V_{IO}	A	Limiting value exceeded	C	uC may be damaged, if $V_{CC} > V_{IO}$
(6) EN	A	Limiting value exceeded	D	Standby and Listen-only Mode not selectable
(7) INH	D	Voltage regulator keeps permanently on	D	Voltage regulator keeps permanently on
(8) ERRN	A	Limiting value exceeded	D	No failure signaling to uC
(9) WAKE	D	Local wake-up not possible	D	Local wake-up not possible
(10) V_{BAT}	-	-	A	Limiting value exceeded
(11) SPLIT	D	Bus charged to V_{BAT} level; Bit timing violation possible	D	Bus charged to V_{CC} level; Bit timing violation possible
(12) CANL	B	No bus communication	B	No bus communication
(13) CANH	D	Degration of EMC; Bit timing violation possible	D	Degration of EMC; Bit timing violation possible
(14) STBN	A	Limiting value exceeded	D	Standby and Go-to-Sleep Mode not selectable

Table 30. TJA1043 FMEA matrix for pin short-circuits to GND and open

Pin	Short to GND		Open	
	Class	Remark	Class	Remark
(1) TXD	C	TXD dominant clamping; Transmitter is disabled	C	TXD clamped recessive
(2) GND	-	-	C	Undervoltage detected; TRX is left unpowered and behaves passive to the bus
(3) V_{CC}	C	V_{CC} undervoltage detected; TRX enters Sleep Mode	C	V_{CC} undervoltage detected; TRX enters Sleep Mode
(4) RXD	C	RXD clamped dominant	C	Node may produce error frames until bus-off is entered
(5) V_{IO}	C	V_{IO} undervoltage detected; TRX enters Sleep Mode	C	V_{IO} undervoltage detected; TRX enters Sleep Mode
(6) EN	C	Normal and Go-to-Sleep Mode not selectable	C	Normal and Go-to-Sleep Mode not selectable
(7) INH	C	Voltage regulator keeps permanently off	C	Voltage regulator switched off
(8) ERRN	D	No failure signaling to uC	D	No failure signaling to uC
(9) WAKE	D	Local wake-up not possible	D	Local wake-up not possible
(10) V_{BAT}	C	Node is left unpowered and behaves passive to the bus	C	Node is left unpowered and behaves passive to the bus
(11) SPLIT	D	Bus discharged to GND level; Bit timing violation possible	D	No DC common mode stabilization
(12) CANL	D	Degration of EMC; Bit timing violation possible	C	Transmission not possible
(13) CANH	B	No bus communication	C	Transmission not possible
(14) STBN	C	Normal and Listen-only Mode not selectable	C	Normal and Listen-only Mode not selectable

Table 31. TJA1043 FMEA matrix for pin short-circuits to neighbored pins

Pin	Short to neighbored pin	
	Class	Remark
TXD - GND	C	Transmitter disabled after TXD dominant timeout
GND - V_{CC}	C	V_{CC} undervoltage detected; TRX enters Sleep Mode
V_{CC} - RXD	C	RXD clamped recessive
RXD - V_{IO}	C	RXD clamped recessive
V_{IO} - EN	D	TRX is not able to enter Standby and Listen-only Mode
EN - INH	D	Voltage regulator may switch off in Standby and Listen-only Mode
ERRN - WAKE	D	Local wake-up not possible, damage to TRX only with closed high-side switch
WAKE - V_{BAT}	D	Local wake-up not possible
V_{BAT} - SPLIT	D	Bus charged to V_{BAT} level; Bit timing violation possible
SPLIT - CANL	D	Degration of EMC; Bit timing violation possible
CANL - CANH	B	No bus communication
CANH - STBN	D	TRX is not able to enter Standby and Sleep Mode if the bus is driven dominant

10.2 Upgrading hints

10.2.1 TJA1050 – TJA1051

Characteristics

In Table 32 an overview on the changed and thus improved characteristics of the TJA1051 is given.

Table 32. Improved characteristics of the TJA1051

Characteristics	HS-CAN with Silent Mode			
	2nd gen.	3rd generation		
	TJA1050	TJA1051	TJA1051/3	TJA1051/E
V_{CC} operating range	4,75 to 5,25V	4,5 to 5,5V	4,5 to 5,5V	4,5 to 5,5V
V_{IO} operating range	-	-	2,8V to 5,5V	-
Voltage robustness, CAN bus	-27V to +40V	-58V to +58V	-58V to +58V	-58V to +58V
Voltage robustness, other pins	-0,3V to +6V	-0,3V to +7V	-0,3V to +7V	-0,3V to +7V
ESD robustness IEC61000-4-2	~ +/-2kV	+/-8kV	+/-8kV	+/-8kV
ESD robustness HBM	+/-6kV	+/-8kV	+/-8kV	+/-8kV
Common Mode Range	+/-12V	+/-30V	+/-30V	+/-30V
Loop Delay (TXD-RXD)	255ns	220ns	250ns[1]	220ns
Shutdown junction temperature	~165°C	~190°C	~190°C	~190°C

The TJA1051 versions are specified over a V_{CC} operating range from 4,5V up to 5,5V. Thus the supply tolerance of the used voltage regulator can be extended to 10% (see Table 33). As well the V_{IO} pin is specified over a broad range from 2,8V to 5,5V.

In order to offer full 24V application support (see Table 33) e.g. for truck applications the bus related pins CANH, CANL (and SPLIT) offer an extended voltage robustness from -58V to +58V. All I/O pins are robust up to 7V DC voltage.

Excellent ESD protection on the bus related pins offers more than state-of-the-art robustness of -/+8kV according to the standard IEC61000-4-2 (C = 150pF, R = 330Ohm). Beside of this also the ESD robustness according the HBM (Human Body Model) got increased. With this excellent ESD robustness the TJA1051 are the first-choice to be used without externally applied ESD protection measures.

Even with very high common mode shifts between different CAN nodes of up to -/+30V the new HS-CAN generation transceivers are capable to receive all data on their CAN bus pins full inline with the receiver requirements of the ISO11898-5 standard.

A much smaller loop delay from TXD to RXD at V_{CC} = V_{IO} = 5V allows to build larger network topologies.

[1] at V_{IO} = 3V

The over temperature protection is extended to a higher threshold in order to allow the TJA1051 to be used even in frequently high temperature applications (e.g. gear box applications).

Functionality

Table 33 shows the advantages of the TJA1051 from functional point of view. Items that are covered in the previous chapter are not mentioned in the detailed description below.

Table 33. Improved functionality of TJA1051

Features	HS-CAN with Silent Mode			
	2nd gen.	3rd generation		
	TJA1050	TJA1051	TJA1051/3	TJA1051/E
3V variant with V_{IO} pin	-	-	√	-
Full 24V application support	-	√	√	√
10% VCC tolerance capable	-	√	√	√
Gap-less behaviour at supply undervoltage	-	√	√	√
EMC optimized CAN slopes for big networks	-	√	√	√
HVSON8 package	-	-	√	√
Receiver hysteresis for improved noise robustness	-	√	√	√
S input pin glitch filter	-	√	√	√
V_{ref} pin for reference voltage [1]	√	-	-	-

[1] Vref obsolete in new microcontrollers. Vref was needed in CAN conrollers, offering an analog RXD input.

Hardware

The TJA1051 versions offer very low ElectroMagnetic Emission (EME), very high ESD robustness and voltage robustness on their bus pins as well as the option to choose for a 3V compatible variant instead of the known 5V types.

With these new features it is up to the hardware developer to consider the following hardware simplifications:

- Remove common mode choke, because the Electro Magnetic Emission is very low even without choke.
- Remove ESD protection components (e.g. ESD diodes), because ESD pin robustness is higher than required by main OEMs.
- If the new transceivers are to be used to replace 2nd generation HS-CAN transceivers in 24V applications (e.g. trucks) external applied zener diodes on the CAN pins to keep the voltage below 30V get redundant, because the new voltage robustness is specified up to -/+58V.
- Replacement of a 5V supplied microcontroller by a 3V supplied microcontroller if the 3V variant TJA1051/3 is chosen.

Software

From software point of view no changes need to be implemented in order to replace the TJA1050 by its successors.

10.2.2 TJA1040 – TJA1042

Characteristics

In Table 32 an overview on the changed and thus improved characteristics of the TJA1042 is given.

Table 34. Improved characteristics of the TJA1051

Characteristics	HS-CAN with Standby Mode		
	2nd gen.	3rd generation	
	TJA1040	TJA1042	TJA1042/3
VCC operating range	4,75 to 5,25V	4,5 to 5,5V	4,5 to 5,5V
VIO operating range	-	-	2,8V to 5,5V
Voltage robustness, CAN bus	-27V to +40V	-58V to +58V	-58V to +58V
Voltage robustness, other pins	-0,3V to +6V	-0,3V to +7V	-0,3V to +7V
ESD robustness IEC61000-4-2	~ +/-2kV	+/-8kV	+/-8kV
ESD robustness HBM	+/-6kV	+/-8kV	+/-8kV
Common Mode Range	+/-12V	+/-30V	+/-30V
Loop Delay (TXD-RXD)	255ns	220ns	250ns[2]
Shutdown junction temperature	~165°C	~190°C	~190°C

The TJA1042 versions are specified over a V_{CC} operating range from 4,5V up to 5,5V. Thus the supply tolerance of the used voltage regulator can be extended to 10% (see Table 33). As well the V_{IO} pin is specified over a broad range from 2,8V to 5,5V.

In order to offer full 24V application support (see Table 33) e.g. for truck applications the bus related pins CANH, CANL (and SPLIT) offer an extended voltage robustness from -58V to +58V. All I/O pins are robust up to 7V DC voltage.

Excellent ESD protection on the bus related pins offers more than state-of-the-art robustness of -/+8kV according to the standard IEC61000-4-2 (C = 150pF, R = 330Ohm). Beside of this also the ESD robustness according the HBM (Human Body Model) got increased. With this excellent ESD robustness the TJA1042 is the first-choice to be used without externally applied ESD protection measures.

Even with very high common mode shifts between different CAN nodes of up to -/+30V the new HS-CAN generation transceivers are capable to receive all data on their CAN bus pins full inline with the receiver requirements of the ISO11898-5 standard.

A much smaller loop delay from TXD to RXD at V_{CC} = V_{IO} = 5V allows to build larger network topologies.

The over temperature protection is extended to a higher threshold in order to allow the TJA1042 to be used even in frequently high temperature applications (e.g. gear box applications).

2. at V_{IO} = 3V

Functionality

Table 33 shows the advantages of the TJA1042 from functional point of view. Items that are covered in the previous chapter are not mentioned in the detailed description below.

Table 35. Improved functionality of TJA1042

Features	HS-CAN with Standby Mode		
	2nd gen.	3rd generation	
	TJA1040	TJA1042	TJA1042/3
3V variant with V_{IO} pin	-	-	√
Full 24V application support	-	√	√
10% V_{CC} tolerance capable	-	√	√
Gap-less behaviour at supply undervoltage	-	√	√
EMC optimized CAN slopes for big networks	-	√	√
Bus dominant clamping detection in Standby Mode	-	√	√
Bus wake-up without V_{CC} (V_{IO} supplied receiver)	-	-	√
HVSON8 package	-	-	√
RXD – V_{CC} reverse supply protection In Standby Mode	-	√	-
Receiver hysteresis for improved noise robustness	-	√	√
STB input pin glitch filter	-	√	√
SPLIT pin for stabilization	√	√	-

Hardware

The TJA1042 versions offer very low ElectroMagnetic Emission (EME), very high ESD robustness and voltage robustness on their bus pins as well as the option to choose for a 3V compatible variant instead of the known 5V types.

With these new features it is up to the hardware developer to consider the following hardware simplifications:

- Remove common mode choke, because the Electro Magnetic Emission is very low even without choke.
- Remove ESD protection components (e.g. ESD diodes), because ESD pin robustness is higher than required by main OEMs.

- If the new transceivers are to be used to replace 2nd generation HS-CAN transceivers in 24V applications (e.g. trucks) external applied zener diodes on the CAN pins to keep the voltage below 30V get redundant, because the new voltage robustness is specified up to -/+58V.
- Replacement of a 5V supplied microcontroller by a 3V supplied microcontroller if the 3V variant TJA1042/3 is chosen.

Software

From software point of view no changes need to be implemented in order to replace the TJA1040 by its successors.

10.2.3 TJA1041A – TJA1043

Characteristics

In Table 32 an overview on the changed and thus improved characteristics of the TJA1043 is given.

Table 36. Improved characteristics of the TJA1043

Characteristics	2nd generation	3rd generation
	TJA1041A	TJA1043
Operating range V_{CC}	4,75 to 5,25V	4,5 to 5,5V
Operating range V_{IO}	2,8 to 5,25V	2,8 to 5,5V
Operating range V_{BAT}	5,0 to 27V	4,5 to 40V
Current consumption in Standby and Sleep Mode (max.)	45uA	36uA
Voltage robustness, CAN, CANL, SPLIT	-27V to +40V	-58V to +58V
Voltage robustness V_{BAT}, INH, WAKE	-0,3V to +40V	-0,3V to +58V
Voltage robustness, other pins	-0,3V to +5,55V	-0,3V to +7V
ESD robustness CANH, CANL, SPLIT acc. IEC61000-4-2[3]	~ ±2kV	±8kV
ESD robustness CANH, CANL, SPLIT acc. HBM[4]	±6kV	±8kV
V_{CC} / V_{IO} undervoltage detection time (min.)	5ms	100ms
V_{CC} / V_{IO} undervoltage recovery time (max.)	12,5ms	5ms
V_{CC} undervoltage detection level (min.)	2,75V	3V
V_{IO} undervoltage detection level (min.)	0,5V	0,8V
V_{BAT} undervoltage detection level (min.)	2,75V	3V
Common Mode Range (Normal Mode)	±12V	±30V
Input leakage current CAN pins (V_{CANH} = V_{CANL} = 5V)	@ V_{CC} = 0V: max. 250uA	@ V_{CC} = 0V: max. 250uA @ V_{BAT} = 0V: -/+2uA
Loop Delay (TXD-RXD)	255ns	240ns[5]
Bus wake-up timeout (wake-up filter cleared, if pattern not completed in time)	not implemented	2ms
Shutdown junction temperature	~165°C	~190°C

[3] IEC 61000-4-2 (150 pF, 330 Ohm)

[4] HBM acc. AEC-Q100-002 (100 pF, 1.5 kOhm)

[5] at V_{IO} = 3V

10% V_{CC} supply tolerance

The TJA1043 is specified over an enhanced V_{CC} operating range from 4,5V up to 5,5V. Thus the supply tolerance of the used voltage regulator can be extended to 10% (see Table 37). As well the V_{IO} pin is specified over a broader range from 2,8V to 5,5V.

Extended VBAT minimum operating range

For the V_{BAT} supplied TJA1043 the operating range got extended on both sides. The minimum operating voltage is specified at 4,5V, thus the TJA1043 is more robust against cranking pulses. On top the V_{CC} pin and the V_{BAT} pin might both be shortcut and supplied via one up to 10% tolerant 5V voltage regulator if desired in specific applications because of their equal minimum operating voltage level.

Full 24V application support

In order to offer full 24V application support (see Table 37) e.g. for truck applications, the bus related pins CANH, CANL and SPLIT offer an extended voltage robustness from -58V to +58V. As well the V_{BAT} maximum operating voltage level got extended to 40V. All I/O pins are robust up to 7V DC voltage.

Excellent ESD protection

Excellent ESD protection on the bus related pins offers more than state-of-the-art robustness of -/+8kV according to the standard IEC61000-4-2 (C = 150pF, R = 330Ohm). Beside of this also the ESD robustness according the HBM (Human Body Model) got increased. With this excellent ESD robustness the TJA1043 and the other NXP 3rd generation HS-CAN transceiver are the first-choice high-speed CAN transceivers to be used without externally applied ESD protection measures.

Gap-less specification at supply undervoltage

The overall undervoltage detection on V_{BAT}, V_{CC} and V_{IO} got improved and thus offer a gap-less specification (see Table 37) of the TJA1043's functionality below the operating range. Therefore the undervoltage detection threshold levels are increased. If the transceiver's supply voltages drop below the operating range, the characteristics can not longer be guaranteed as specified in the data sheet, but the TJA1043 keeps the main functionalities (e.g. transmitting, receiving, mode control) alive down to the undervoltage detection levels and until the undervoltage detection timers react on the undervoltage. When detecting the undervoltage the TJA1043 enters defined fail-safe states like the "forced" Standby or "forced" Sleep Mode.

Extended V_{CC} / V_{IO} undervoltage detection time

An extended minimum V_{CC} / V_{IO} undervoltage detection time (5ms vs. 100ms) allows now to use even slow ramping up voltage regulators that might have caused an undesired "forced" Sleep Mode entry with the TJA1041A.

Improved common mode shift capability

Even with very high common mode shifts between different CAN nodes of up to -/+30V in the TJA1043 is capable to receive all data on the CAN bus pins fully inline with the receiver requirements of the ISO11898-5 standard.

Defined bus load at unsupplied condition

An unsupplied TJA1043 (V_{BAT} = 0V) will disengage from the bus (zero load) until V_{BAT} has recovered. (See “Input leakage current CAN pins” at V_{BAT} = 0V: -/+2uA).

Smaller loop delay

A smaller loop delay from TXD to RXD allows building larger network topologies.

Higher over temperature range

The over temperature protection is extended to a higher threshold of typical 190°C in order to allow the TJA1043 to be used even in frequently high temperature environments (e.g. gear box applications).

Functionality

Table 37 shows the advantages of the TJA1043 from functional point of view. Items that are covered in the previous chapter “Characteristics” are not mentioned in the detailed description below.

Table 37. Improved functionality of the TJA1043

Characteristics	2nd generation	3rd generation
	TJA1041A	TJA1043
10% V_{CC} tolerance capable	-	√
Full 24V application support	-	√
Gap-less specification at supply undervoltage	-	√
Passive to the bus (zero load), if V_{BAT} = 0V	-	√
Consistent power-up at all supply conditions	-	√
Entering Sleep Mode with set PWON flag	-	√
Host wake-up in Forced Sleep Mode via positive STBN edge	-	√
V_{CC} / V_{IO} undervoltage recovery in Forced Sleep Mode	-	√
Enhanced remote wake-up pattern detection - Dom-rec-dom pattern instead of dom-rec-dom-rec pattern - Remote wake-up timeout	-	√
Direct wake-up detection in “forced” Sleep Mode	-	√
RXD, ERRN wake-up signaling at V_{IO}, V_{BAT} supplied only	-	√
EMC optimized CAN slopes for big networks	-	√
HVSON8 package	-	√
Receiver hysteresis for improved noise robustness	-	√
EN / STBN input pin glitch filter	-	√

Consistent power-up at all supply conditions

At any power-up condition the TJA1043 offers a consistent behavior. In the previous TJA1041A the internal WAKE-UP flag and WAKE-UP SOURCE flag got cleared at power-on. After power-on it was possible that the WAKE-UP and WAKE-UP SOURCE flag got set without a real “local wake-up” being applied, depending on the specific V_{BAT} and WAKE pin power-up condition (differences in ramp-up times between BAT and WAKE voltage etc). Now in the TJA1043 both, the WAKE-UP flag and the WAKE-UP SOURCE flag get set together with the PWON flag at power-on in order to offer an always consistent flag setting after power-on regardless of the application circuitry connected to WAKE.

Entering Sleep Mode with set PWON flag

The TJA1043 allows entering the Sleep Mode even with set PWON flag. In the previous TJA1041A the transceiver needed to be put into Normal Mode for a short while before entering the Sleep Mode after a power-on event (PWON flag set). This was necessary because the PWON flag is cleared in Normal Mode and only with a cleared PWON flag the Sleep Mode could be entered. In the TJA1043 the PWON flag set and clear conditions are equal to the TJA1041A implementation, but now a set PWON flag will not longer block entering the Sleep Mode.

Leaving “forced” Sleep Mode

At undervoltage detection on V_{CC} or V_{IO} both, the TJA1041A and the TJA1043 enter autonomously the so-called “forced” Sleep Mode in order to disable external voltage regulator(s) by setting the INH pin floating. In case of a short circuit this measure prevents flow of a high short-circuit current. Leaving this “forced” Sleep Mode again (regardless of a battery reconnection) in the TJA1041A is only possible via a local or remote wake-up. The TJA1043 offers two more possibilities to leave the “forced” Sleep Mode:

- A recovery of both supplies, V_{CC} and V_{IO}, for at least $t_{rec(uv)}$ (max. 5ms) leads to clear the UVNOM flag again. After recovery the TJA1043 enters the mode that is selected by the mode control pins EN, STBN.
- Applying a positive edge on the STBN pin (provided that V_{IO} is supplied) leads to clear the UVNOM flag again. The TJA1043 will enter either Listen-only or Normal Mode, depending on the EN pin setting.

In both cases the undervoltage detection is observing the V_{CC} and V_{IO} pin after leaving “forced” Sleep Mode again and might force the transceiver into Sleep Mode (after $t_{det(uv)}$ (min. 100ms) again if there is still an undervoltage condition.

With these improvements of the TJA1043 dedicated wake-up circuits as proposed for TJA1041A applications are not required anymore (e.g. a microcontroller controlled transistor connected to the WAKE port).

RXD, ERRN wake-up signaling at VIO, VBAT supplied only

In contrast to the TJA1041A the TJA1043 requires only supply of V_{IO} and V_{BAT} in order to properly signal a local wake-up on its pins RXD and ERRN in Standby, Go-to-Sleep or Sleep Mode. In the TJA1041A also the V_{CC} supply is required.

Direct wake-up detection in “forced” Sleep Mode

In the TJA1041A clearing the internal undervoltage flag UVNOM is possible first after a dedicated waiting time t_{UV} = 5…12,5ms. Based on that a wake-up request applied to the TJA1041A directly after undervoltage detection gets ignored and thus does not lead to wake-up the device from “forced” Sleep Mode.

This waiting time is not implemented in the TJA1043 in order not to loose any wake-up request. Thus if an undervoltage on V_{CC} and/or V_{IO} of the TJA1043 gets detected, the UVNOM flag can be cleared directly by a local or remote wake-up.

Enhanced remote wake-up pattern detection

In comparison to the TJA1041A the TJA1043 offers a slightly enhanced remote wake-up procedure. The TJA1041A detects a bus wake-up request when the bus shows two dominant phases of at least 5us duration, with each dominant phase followed by a recessive phase of at least 5us. In contrast to that, the TJA1043 requires only a recessive phase after the first dominant phase. Fig 52 (see below) illustrates the wake-up pattern requirements for the TJA1041A and the TJA1043.

Additionally after a bus wake-up timeout time $t_{to(wake)bus}$ (min. 0,5ms) without receiving the complete dominant-recessive-dominant pattern the TJA1043 internal wake-up logic gets reset and the complete wake-up pattern needs to be re-applied to the low power CAN receiver before generating a proper remote wake-up. This increases the robustness against unwanted wake-ups caused by temporary dominant phases on the bus caused by noise or spikes.

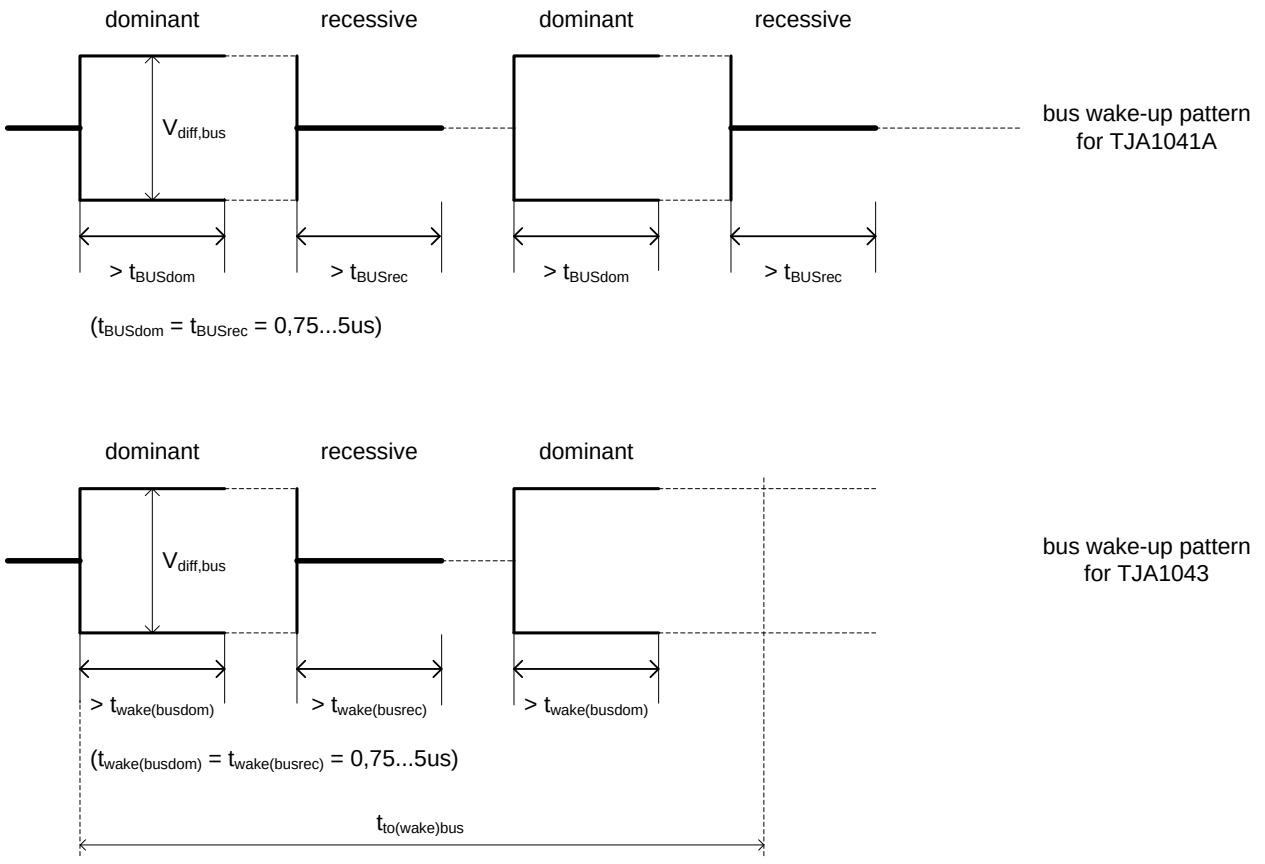


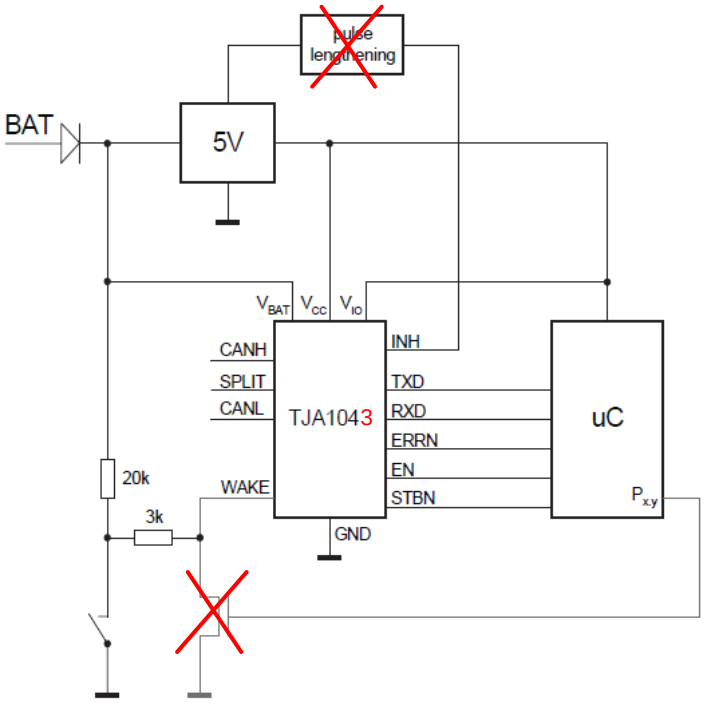
Fig 52. Bus wake-up pattern for TJA1041A and TJA1043

Hardware

The TJA1043 offers very low Electro Magnetic Emission (EME), very high Electro Magnetic Immunity (EMI) and very high ESD and voltage robustness on its bus pins (see Table 36).

With these new features it is up to the hardware developer to consider the following hardware simplifications:

- Remove common mode choke, because the Electro Magnetic Emission is very low even without choke.
- Remove ESD protection components (e.g. ESD diodes), because ESD pin robustness is higher than required by main OEMs.
- If the TJA1043 is used to replace the TJA1041A in 24V applications (e.g. trucks) external applied zener diodes on the CAN pins to keep the voltage below 30V get redundant, because the new voltage robustness is specified up to -/+58V.
- With slow-starting V_{CC} supplies (rise time >5ms, but <100ms) INH pulse lengthening and additional wake-up hardware connected to the WAKE pin gets obsolete (see Fig 53) because of the extended undervoltage detection time of min. 100ms.



Adapted figure 24 taken from "Application Note TJA1041/TJA1041A"

Fig 53. Obsolete hardware due to extended V_{CC} / V_{IO} undervoltage detection time

Software

From software point of view some minor items shall be checked.

- At PWON the WAKE-UP and the WAKE-UP SOURCE flag get set (see chapter 6.5). In order to clearly distinguish between a “real” local wake-up on pin WAKE and a “power-on” related wake-up setting the PWON flag can be checked before entering Normal Mode in the Listen-only Mode. It is recommended to check, how the application software starts-up interpreting the NERR pin.
- In order to enter Sleep Mode after power-on the TJA1043 does not necessarily need to go through the Normal Mode in order to clear the PWON flag (see chapter 6.5).
- Due to the extended V_{CC} / V_{IO} undervoltage detection time of min. 100ms (see Table 36) and the possibility to leave the “forced” Sleep Mode additionally by a positive STBN edge or a V_{CC} / V_{IO} recovery (see chapter 6.8) a local wake-up triggering via pin WAKE by the application might get obsolete.
- In case a transition from Standby or Sleep Mode to Normal Mode is performed while a wake-up flag is indicated (RXD = LOW) the RXD pin will get released HIGH at the mode transition. Before the CAN receiver is full powered and to avoid any unwanted glitches on pin RXD during this internal power-up process pin RXD is kept HIGH for about 30us before the bus traffic is signaled on pin RXD. Compared to the TJA1043 the TJA1041A starts following the bus already about 5us after the mode change.

  For typical ECU applications in which after a wake-up first the physical layer device (here the TJA1043) and than secondly the CAN controller is enabled this is no problem as long as the CAN Controller gets enabled with a delay of at least 30µs compared to the mode change of the CAN Transceiver. With slightly delayed enabling of the CAN controller it is guaranteed, that the CAN Transceiver is ready to operate and forwards the actual bus traffic to RXD as well as the TXD signal to the bus lines correctly.

  In case the CAN controller is already active during the TJA1043 Normal Mode transition and directly reading the RXD pin for a “bus idle” condition the RXD HIGH phase of about 30us might indicate to the CAN controller that a message can already be sent to the bus whereas the RXD pin does not receive any traffic yet and this might provoke a situation in which the first sent CAN frame directly after the mode switch to Normal is not correctly received via pin RXD and the CAN controller has to send an CAN ERROR frame.

  Thus it is in general recommended to start-up a system with first setting the CAN Transceiver into Normal Mode and activating the CAN Controller with a defined delay of at least 30µs in order to avoid unwanted CAN error frames at start-up of a system.

10.3 Simulation models

The following table shows the available HS-CAN transceiver models. It also indicates which Simulator tool is used. In order to receive the models or according updates please contact NXP Semiconductors.

Table 38. Available CAN Simulation Models[6]

Tranceiver Type	Model Name	Target Simulator	Description Language	Availability
HS-CAN	TJA1050	Saber	VHDL-AMS	available
	TJA1051	System Vision Saber HDL	VHDL-AMS	available
	TJA1040	System Vision Saber HDL	VHDL-AMS	available
	TJA1041A	System Vision Saber HDL	VHDL-AMS	available
	TJA1042	System Vision Saber HDL	VHDL-AMS	available
	TJA1043	System Vision Saber HDL	VHDL-AMS	available
	TJA1048	System Vision Saber HDL	VHDL-AMS	available
	TJA1049	System Vision	VHDL-AMS	available

[6] Effective from 24th August 2010

11. Abbreviations

Table 39. Abbreviations

Acronym	Description
CAN	Controller Area Network
Clamp-15	ECU architecture, Battery supply line after the ignition key, module is temporarily supplied by the battery only (when ignition key is on)
Clamp-30	ECU architecture, direct battery supply line before the ignition key, module is permanently supplied by the battery
DLC	Data Link Control
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
EME	Electromagnetic Emission
EMI	Electromagnetic Immunity
ESD	Electrostatic Discharge
FMEA	Failure Mode and Effects Analysis
LIN	Local Interconnect Network
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
SBC	System Basis Chip
SPI	Serial Peripheral Interface

12. References

[1] Data Sheet PCA82C250, CAN Controller Interface – Philips Semiconductors, 2000 Jan 13

[2] Data Sheet PCA82C251, CAN transceiver for 24V systems – Philips Semiconductors, 2000 Jan 13

[3] Data sheet TJA1040, High speed CAN transceiver – Philips Semiconductors, Rev. 06, 2003 Oct 14

[4] Data sheet TJA1041, High speed CAN transceiver – NXP Semiconductors, Rev. 06, 2007 Dec 5

[5] Data sheet TJA1041A, High Speed CAN transceiver – NXP Semiconductors, Rev. 04, 2008 Jul 29

[6] Product data sheet TJA1042, High-speed CAN transceiver with Standby Mode – NXP Semiconductors, Rev. 07, 2012 May 8

[7] Product data sheet TJA1043, High-speed CAN transceiver – NXP Semiconductors, Rev. 03, 2013 April 24

[8] Product data sheet TJA1048, Dual high-speed CAN transceiver with Standby Mode– NXP Semiconductors, Rev. 03, 2013 April 24

[9] Data sheet TJA1050, High Speed CAN transceiver – Philips Semiconductors, Rev. 04, 2003 Oct 22

[10] Product data sheet TJA1051, High-speed CAN transceiver – NXP Semiconductors, Rev. 06, 2011 Mar 25

[11] Product data sheet PESD1CAN, CAN bus ESD protection diode – NXP Semiconductors, Rev. 04, 2008 Feb 15

[12] Product data sheet PESD2CAN, CAN bus ESD protection diode – NXP Semiconductors, Rev. 01, 2006 Dec 22

[13] Product data sheet UJA1065, High-speed CAN/LIN fail-safe system basis chip – NXP Semiconductors, Rev. 07, 2010 Feb 25

[14] Product data sheet UJA1066, High-speed CAN fail-safe system basis chip – NXP Semiconductors, Rev. 02, 2009 May 5

[15] Product data sheet UJA1075A, High-speed CAN/LIN core system basis chip – NXP Semiconductors, Rev. 01, 2010 Jul 9

[16] Product data sheet UJA1076A, High-speed CAN core system basis chip – NXP Semiconductors, Rev. 01, 2010 Jul 9

[17] Product data sheet UJA1078A, High-speed CAN/dual LIN core system basis chip – NXP Semiconductors, Rev. 01, 2010 Jul 9

[18] Road Vehicles – Controller Area Network (CAN) – Part 2: High-speed medium access unit, ISO 11898-2, International Standardization Organisation, 2003

[19] Road Vehicles – Controller Area Network (CAN) – Part 5: High-speed medium access unit with low power mode, ISO 11898-5, International Standardization Organisation, 2007

[20] High Speed CAN (HSC) for Vehicle Applications at 500kbps - SAE J2284, 2009

[21] Application Note AN97046, Determination of Bit Timing Parameters for the CAN Controller SJA1000 – Philips Semiconductors, 1996

13. Legal information

13.1 Definitions

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