AH1801

Application Hints - TJA1128 LIN Mini System Basis Chip Family

Rev. 1.1

Document information

Info	Content
Title	Application Hints - TJA1128x LIN Mini System Basis Chip Family
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Keywords	TJA1128; Local Interconnect Network (LIN); ISO 17987-4; LIN 2.0; LIN 2.1; LIN 2.2; LIN2.2A; System Basis Chip; Physical Layer; SAE J2602; ISO 9141

Summary

This document provides the necessary information for hardware and software designers to create automotive applications based on the TJA1128x LIN Mini System Basis Chip Family.

Revision history

Rev	Date	Description
1.1	20180928	Section 5.4 and 11 added
1.0	20180326	Initial revision

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Contents

1. Introduction

The TJA1128x is a LIN Mini System Basis Chip (SBC) family with LIN transceiver, integrated low-drop voltage regulator (LDO), window watchdog, two WAKE inputs, one general purpose input (GPI) and one high-voltage multi-purpose (HVMPO) output. The voltage regulator can deliver up to 85 mA and is available in a 3.3 V and 5.0 V version. TJA1128 facilitates the development of compact nodes in LIN bus systems. To support robust designs, the TJA1128 offers high ESD performance and can withstand high-voltages on the LIN bus. In order to minimize current consumption, the TJA1128 supports a SLEEP mode in which the LIN transceiver and the voltage regulator are powered down while still having wake-up capability via the LIN bus or WAKE1 / WAKE2.

The TJA1128 comes in an HVSON14 package, which reduces the required board space by over 70 % compared to an SO14 package. This small footprint can be very valuable when board space is limited. Variants with or without window watchdog and with one or two WAKE inputs only are available.

Table 1. Overview of the TJA1128x variants

Part number	Voltage regulator	WAKE pins	Watchdog
TJA1128A	5 V linear regulator	1	
TJA1128B	3.3 V linear regulator	1	
TJA1128C	5 V linear regulator	2	
TJA1128D	3.3 V linear regulator	2	
TJA1128E	5 V linear regulator	1	•
TJA1128F	3.3 V linear regulator	1	•
TJA1128G	5 V linear regulator	2	•
TJA1128H	3.3 V linear regulator	2	•

1.1 Typical application

The typical application for the TJA1128 is a LIN slave with a microcontroller in which the TJA1128 is able to reset the microcontroller. In the application information of the data sheet [1] a typical application diagram is shown.

2. Power Supply

2.1 Specification of BAT pin

The BAT pin is the main supply pin of the TJA1128. The V_{BAT} specification is “gap free” starting from 0 V up to 28 V. This is illustrated in Fig 1. The maximum supply voltage is 43 V [1].

In the supply range between 28 V and 43 V general functionality is still available, but not all parameters are within the specified limits like e.g. quiescent currents. Because of the higher power dissipation (mainly by the internal voltage regulator) such high supply voltages should not be applied for a longer time. In particular, the VCC regulator, LIN communication, microcontroller interface, digital control, watchdog and VCC undervoltage monitor would be operational up to 43 V.

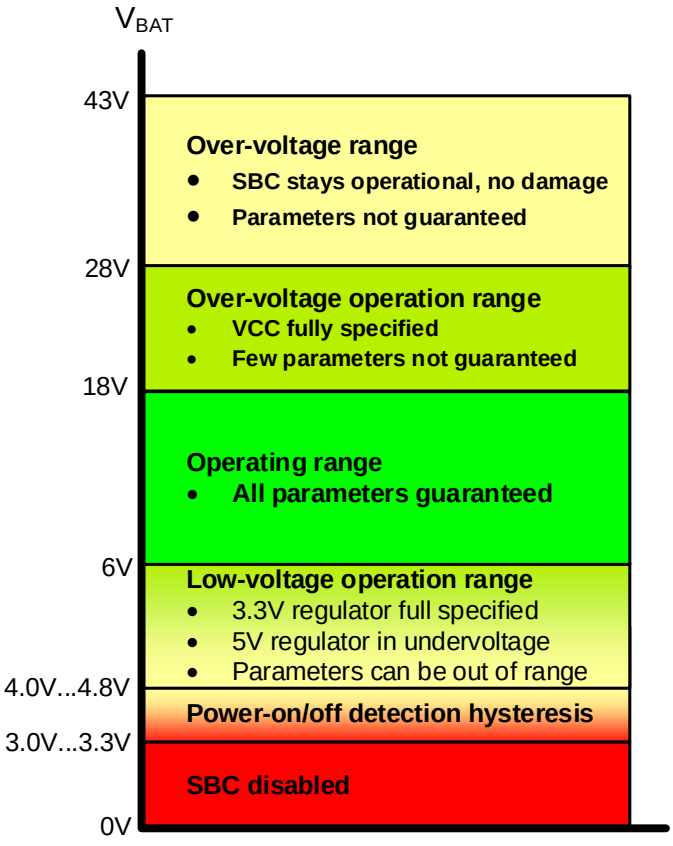


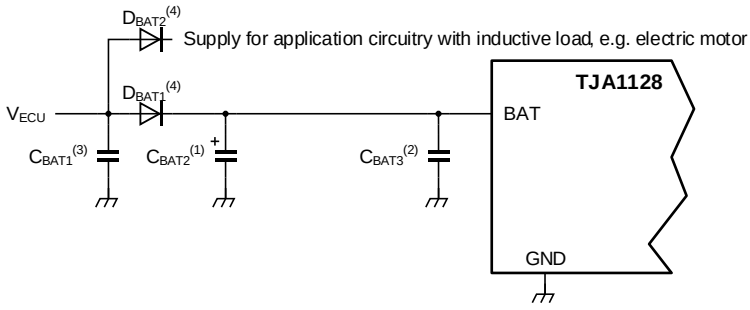
Fig 1. Supply “Gap Free” operation

The main electrical parameters with respect to the BAT pin are the power-on and -off detection thresholds. If the TJA1128 is disabled (BAT ramping up from 0V), it remains disabled as long as the BAT voltage is below power-on detection threshold ($V_{th(det)pon}$). Once being above that voltage it will stay active until the BAT voltage falls below power-off detection threshold($V_{th(det)poff}$).

2.2 Transients on the battery line

A basic requirement for automotive ECUs is that they need to be capable of sustaining automotive transients as, for example, defined in ISO 7637.

Fig 2 shows the recommended circuitry on pin BAT. First of all a reverse polarity protection diode D_{BAT1} is required, because the TJA1128 does not provide internal reverse polarity protection. Such external reverse polarity protection diode D_{BAT1} (e.g. BAS21H [6] or S07D [7]) protects the ECU (including the TJA1128x) against negative automotive transients. In addition, D_{BAT1} protects the ECU against transients, which can be caused by charge equalization between ECUs during hot-plugging. For those applications with inductive loads (e.g. electric motor) it is recommended to provide an additional dedicated reverse polarity diode for these circuits. See D_{BAT2} in Fig 2.



(1) C_{BAT2} is electrolytic capacitor (≥22 µF / ≥35V). In principle the value depends on application.

(2) C_{BAT3} is multilayer chip ceramic capacitor (e.g. 47 nF / 50V). Typically it is an open mode ceramic capacitor or two capacitors in series.

(3) C_{BAT1} is optional multilayer chip ceramic capacitor (e.g. 270 pF / 50V). Typically it is an open mode ceramic capacitor or two capacitors in series.

(4) D_{BAT1} and D_{BAT2} are typically PN-diodes (e.g. S07D, BAS21H) for reverse polarity protection

Fig 2. Typical circuitry on pin BAT

The buffer capacitors C_{BAT2} and C_{BAT3} in Fig 2 should be connected to pin BAT to suppress spikes, noise and automotive transients. Further they are used to buffer supply voltage drops. For reduction of high-frequency noise D_{BAT1}, C_{BAT1} and C_{BAT2} are recommended to be located close to the battery supply connector and C_{BAT3} should be located close to the BAT pin of the TJA1128. Furthermore, a diode with low diode capacitance for D_{BAT1} has good noise reduction characteristics.

Note, that so-called “Open-mode” capacitors are recommended on BAT inputs of ECUs in general. Alternatively two capacitors in series can be used, which are mounted at an angle of 90 deg. on the PCB to prevent mechanical shorts on BAT during bending of the PCB. Non “open mode” capacitors might tend to an internal hard short circuit after/during mechanical stress, which can be mitigated with 2 capacitors in series and placed at an angle of 90 deg.

2.3 Operation during and after cranking

During and after engine start (cranking) the battery supply voltage can drop. Such battery supply starting profiles are specified in the ISO 7637 specification and in the ISO 16750-2 specification. Typical starting profiles consist of an initial voltage drop to a very low voltage level U_S for 70 ms, followed by a slightly higher level U_A for several seconds.

The following measures can be taken to prevent operation without microcontroller reset during deep cranking:

- Use of reverse polarity protection diodes with low forward voltage, e.g. Schottky barrier diode such as S07D, BAS21H as $D_{BAT1.}$
- Choose a capacitance value for the battery supply buffer capacitor C_{BAT1} that bridges the initial voltage drop of the starting profile.

2.4 Charge pump

The TJA1128 LDO regulator concept is based on a NMOS transistor output driver. The regulator operates down to 5.5V -and 3.8V on BAT for rep. The 5V and the 3.3V version even during fast falling transients on battery input pin. A charge pump is used to provide the necessary gate voltage for the NMOS output driver. In order to save current this charge pump will only be enabled below 10.8V BAT input voltage.

For battery monitoring two scenarios need to be distinguished,See detail in Fig 3, a rising level of the battery voltage (starting from zero) and a falling level of the battery voltage. When the battery voltage is ramping up, the charge pump is switched-off at VBAT >10.8V. When ramping down, the charge pump is switched-on at VBAT <10.5V.

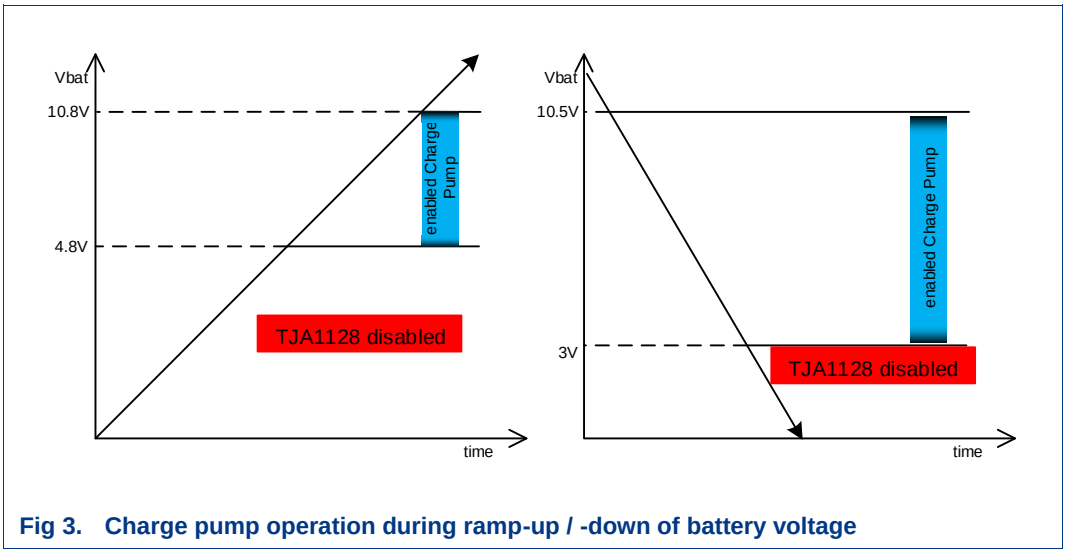
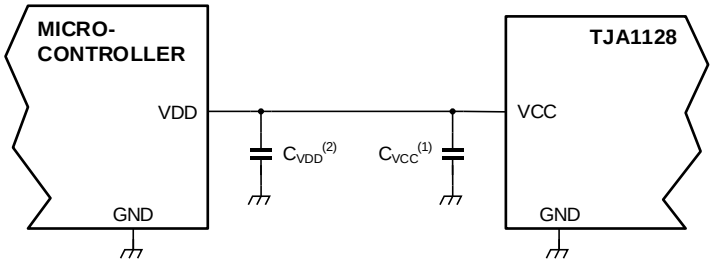


Fig 3. Charge pump operation during ramp-up / -down of battery voltage

When the charge pump is switched-on, the current consumption is higher than when the charge pump is switched off. The additional current for the charge pump is typ. 170uA, which is specified in the datasheet static parameter “additional current at low bat”.

3. VCC Voltage Regulator

The VCC voltage regulator offers the supply for the application microcontroller and its periphery. The VCC regulator can deliver up to 85 mA. The TJA1128x family provides devices with either a 5 V or a 3.3 V regulator. Fig 4 shows the typical VCC output circuitry.



(1) C_{VCC} is multilayer chip ceramic capacitor (e.g. X7R / 1 µF / 16V) .

(2) C_{VDD} is an optional multilayer ceramic capacitor; depends on microcontroller requirements.

Fig 4. Typical VCC application

3.1 VCC output capacitor

In Fig 4 for C_{VCC} a ceramic multilayer chip capacitor (MLCC) is recommended to buffer VCC because of its ultra low ESR and boardspace consumption. It is recommended to locate this capacitor close to pin VCC. The dynamic behaviour of the VCC depends on the value of the VCC capacitor. The VCC regulator is stable within a large range of capacitor values. Table 2 lists the recommended capacitor value to be applied on the VCC output.

Table 2. VCC output capacitor

Effective minimum capacitance	nominal minimum capacitor value	maximum capacitor value
$C_{O(VCC)}$ [1].	1 µF	20 µF

The effective capacitance of a ceramic capacitor may be smaller than its nominal capacitance value, depending on parameters like temperature and DC charge voltage (DC offset). In order to cope with these effects, the recommended nominal capacitor value is at least 1µF.. For details please refer to the data sheet of the selected capacitor (e.g. Murata GCM188R71C105MA64, X7R, 1µF, 16Vdc).

3.2 VCC regulator operation and undervoltage monitor

The VCC voltage regulator is active in STANDBY / NORMAL / PORT / GOTOLSP and RESET mode. In SLEEP Mode it is switched off in order to achieve lowest quiescent

current. Besides this, VCC is also disabled in OFF mode to protect the device and to take care of that the system is not running into an unstable condition.

If VCC is active, it is monitored by an internal undervoltage detector. In case the VCC voltage drops below the undervoltage threshold V_{uvd}[1], for longer time than td(uvd), the TJA1128 pulls down the RSTN pin, if enabled.

4. Thermal design considerations

The TJA1128 is available in a HVSON14 package with an exposed die pad.

It is strongly recommended to solder the heatsink to the PCB ground. This way, the thermal resistance $R_{th(vj-a)}$ can be improved significantly. Furthermore, following PCB layout options can be used to improve the thermal resistance:

- Number of PCB layers (e.g. 4 layers)
- Cu thickness (35 µm / 70 µm; the thicker the better)
- Heatsink area on the PCB available for the SBC (the larger the better)
- Number of vias (the more the better)

Thermal resistance from virtual junction to ambient ($R_{th(vj-a)}$) based on a 4 layer board and from junction to case ($R_{th(vj-c)}$) are specified in the TJA1128 data sheet [1].

5. Microcontroller interface

5.1 Mode control (hints on regular mode transitions)

The TJA1128 supports nine operating modes: NORMAL, STANDBY, PORT, GOTOSLP, SLEEP, RESET, CONFIG, OVERTEMP and OFF. You can find the detailed descriptions in data sheet [1] (chapter operating modes).

This chapter describes hints for the microcontroller software on regular TJA1128 operating mode transitions. In Fig 5 the transitions of the regular operating modes STANDBY, PORT, NORMAL, GOTOSLP and SLEEP are illustrated.

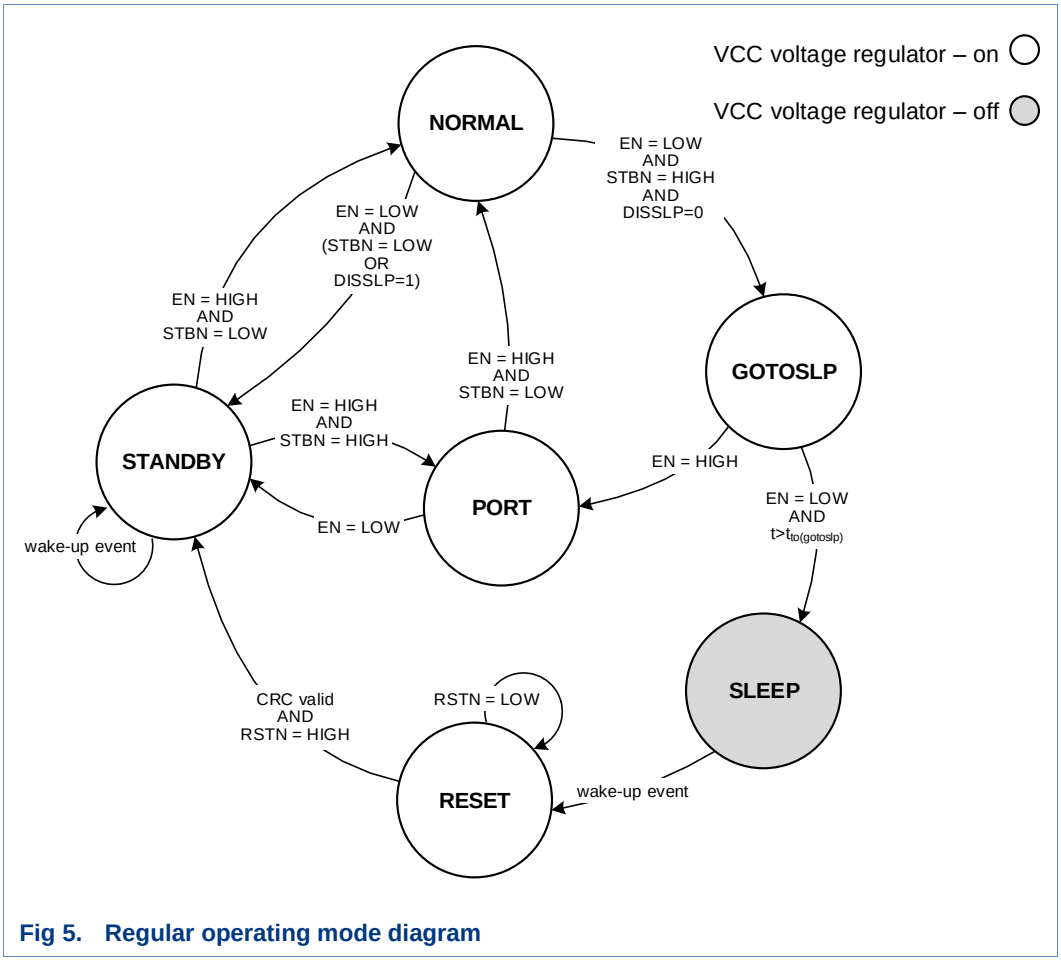


Fig 5. Regular operating mode diagram

5.1.1 Transition summary

The transitions from STANDBY, PORT, NORMAL, GOTOSLP mode are summarized in Table 3 below:

Table 3. Mode transition summary

#	Current mode	Next mode	SW control steps in short	Remark
1	STANDBY	NORMAL	STBN=0, (delay)[1], EN=1, delay	See detail in 5.1.2
		PORT	STBN=1, (delay)[1], EN=1, delay	
2	PORT	NORMAL	STBN=0, EN=1, delay	See detail in 5.1.3
		STANDBY	(STBN=1)[1], EN=0, delay, STBN=0	
3	NORMAL	STANDBY	STBN=0, (delay)[1], EN=0, delay	See detail in 5.1.4
		GOTOSLP	STBN=1, (delay)[1], EN=0, delay	
4	GOTOSLP	PORT	CHECK RXD=0, →EN=1, (STBN=1)[1], delay	See detail in 5.1.5
		SLEEP	EN=0	

[1] The delay in the breaket is the optional sw step, see detail in 5.1.2 / 3 / 4 / 5.

5.1.2 STANDBY mode transitions

STANDBY mode is the first level low-power mode that offers low current consumption. In STANDBY mode, the voltage regulator is on and able to supply a microcontroller. The LIN transmitter is switched off. The TJA1128 supports monitoring the LIN bus line and the local WAKE inputs for wake-up events and will signal them by a LOW level on RXD.

5.1.2.1 Transition RESET to STANDBY mode

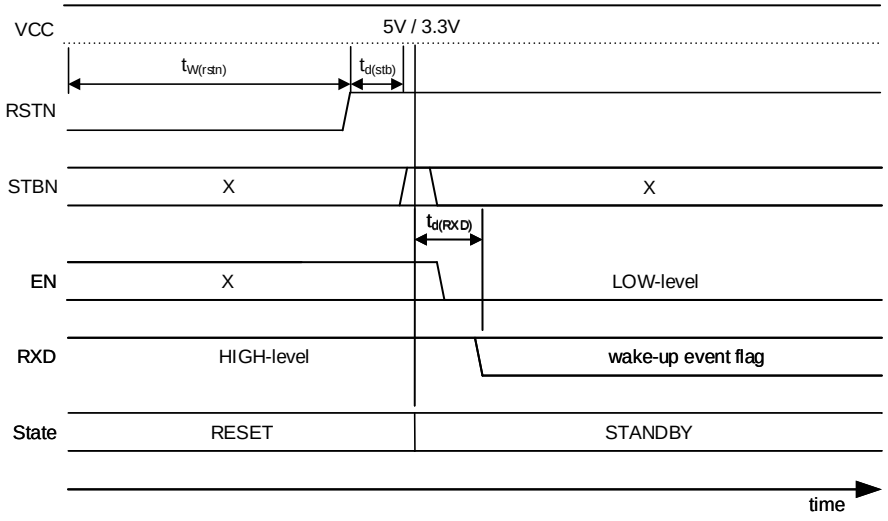


Fig 6. Transition from RESET to STANDBY mode

Regardless the level of EN/STBN, the STANDBY mode is entered when the status of the RSTN is high and the MTP is correctly configured (refer to chapter 5.3). In Fig 6, a transition from RESET mode towards STANDBY mode is illustrated. The transition to STANDBY mode can be delayed when RSTN is driven low by an external source. After entering the STANDBY mode, the microcontroller has full control over the operation modes by using the EN and STBN pins. For keeping the device in STANDBY mode, EN should always be pulled LOW level.

In RESET mode the LDO is enabled. The RSTN is initially pulled low but released when VCC voltage is OK (no undervoltage) after a pre-defined reset pulse width time $t_{w(rst)}$ [1]which is set by the MTP configuration bit RSTTIM. This allows the VCC voltage to ramp-up while the microcontroller remains in reset.

5.1.2.2 Transition STANDBY to NORMAL mode

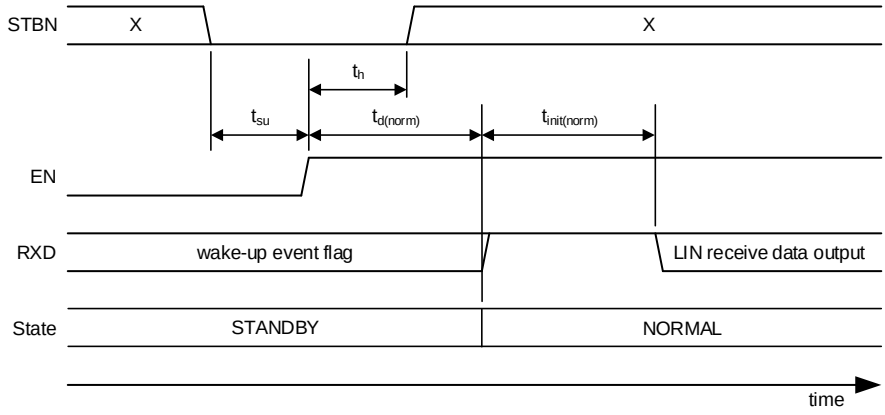


Fig 7. Transition from STANDBY to NORMAL mode

For a successful transition from STANDBY to NORMAL mode the set-up time t_{su} [1] and the hold time t_h [1] need to be taken into account. Fig 7 shows that for this transition STBN must be pulled LOW for at least t_{su} before EN is pulled HIGH. Afterwards STBN must remain LOW for at least t_h [1]. Otherwise an unintended transition towards to NORMAL mode, either directly or via PORT mode might take place.

It is recommended for the microcontroller software to incorporate t_{su} [1]and t_h [1], e.g. by adding wait times. Furthermore, the normal mode delay time $t_{d(norm)}$ [1] and the LIN initialization time $t_{init(norm)}$ [1] should be taken into account.

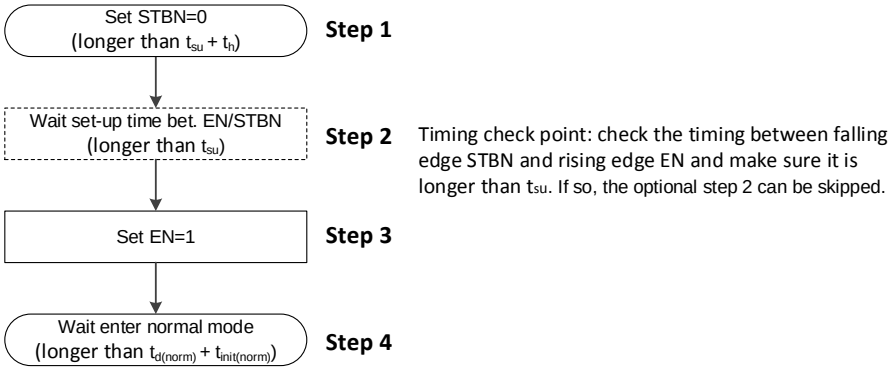


Fig 8. Example software sequence for the transition from STANDBY to NORMAL mode

5.1.2.3 Transition STANDBY to PORT mode

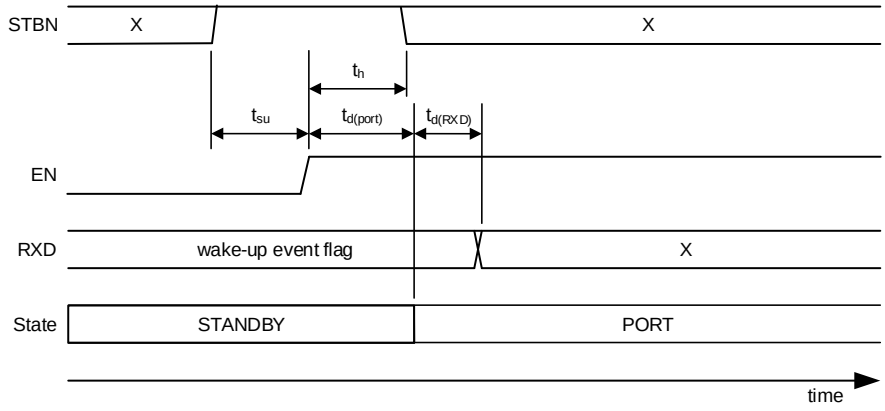


Fig 9. Transition from STANDBY to PORT mode

For a successful transition from STANDBY to PORT mode the set-up mode time t_{su} [1] and the hold time t_h [1] need to be taken into account. Fig 9 shows that for this transition STBN must be pulled HIGH for at least t_{su} [1]before EN is pulled HIGH. Afterwards STBN must remain HIGH for at least t_h [1]. Otherwise an unintended transition towards NORMAL mode might take place.

It is recommended for the microcontroller software to incorporate t_{su} [1]and t_h [1], e.g. by adding wait times. Furthermore, the port mode delay time $t_{d(port)}$ [1] and the RXD delay time $t_{d(RXD)}$ [1] should be taken into account.

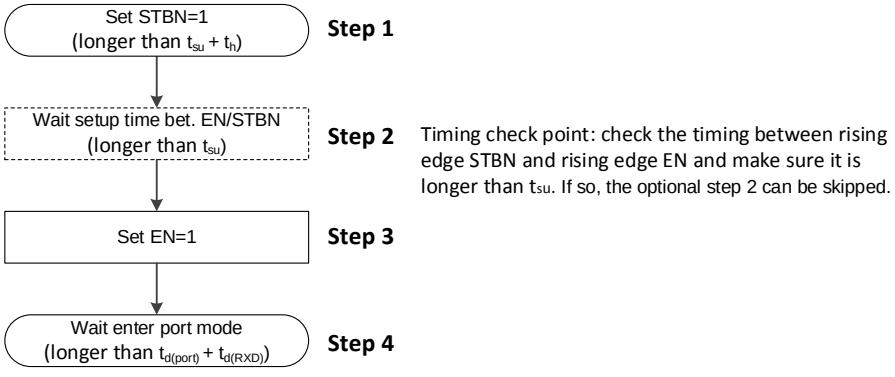


Fig 10.Example software sequence for the transition from STANDBY to PORT mode

5.1.3 PORT mode transitions

The PORT mode can be used by the microcontroller to detect the mode of the TJA1128 either CONFIG or PORT mode and read the wake-status and wake-event information. The operation mode differs from STANDBY mode in the RXD and TXD functionality. See detail description from TJA1128 datasheet, chapter “Differentiation between CONFIG and PORT”.

5.1.3.1 Transition PORT to NORMAL mode

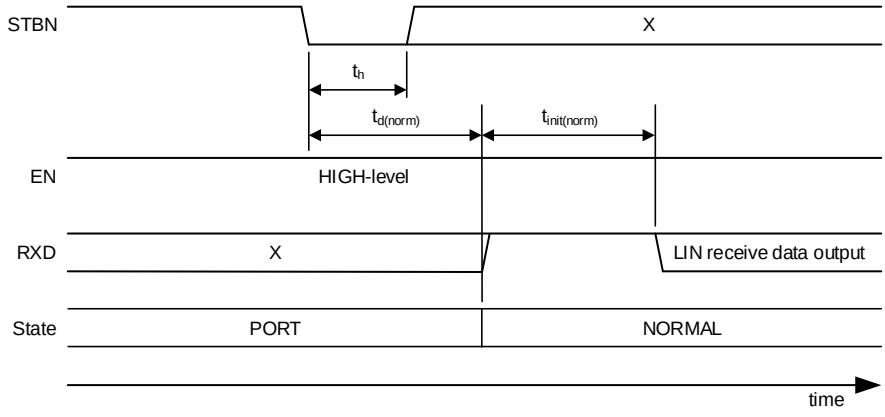


Fig 11.Transition from PORT to NORMAL mode

A successful transition from PORT to NORMAL mode takes place when STBN is pulled LOW for at least the hold time t_h [1] while EN is HIGH and remains HIGH for at least $t_{d(norm)}$ [1]. If STBN becomes HIGH again before t_h has exceeded, the TJA1128 might remain in PORT mode. See detail in Fig 11.

Although for this transition typically no wait times are needed for the microcontroller software the hold time t_h [1], the normal mode delay time $t_{d(norm)}$ [1] and the LIN initialization time $t_{init(norm)}$ [1] should be taken into account.

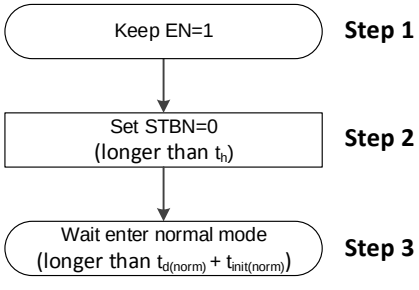


Fig 12.Example software sequence for the transition from PORT to NORMAL mode

5.1.3.2 Transition PORT to STANDBY mode

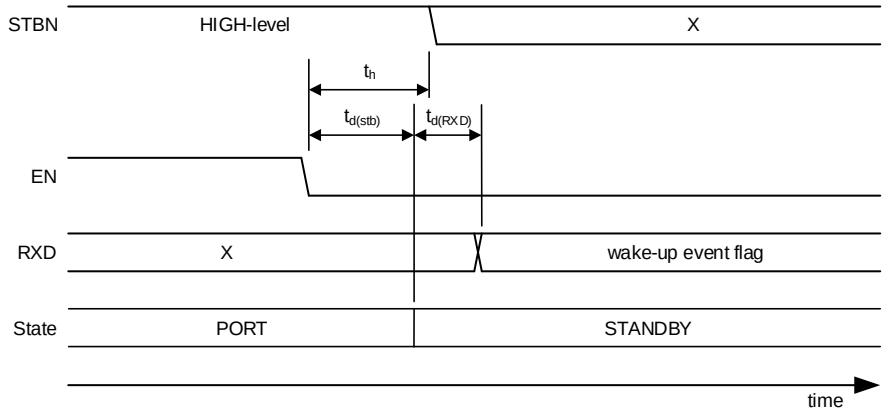


Fig 13.Transition from PORT to STANDBY mode

A successful transition from PORT to STANDBY mode takes place when EN is pulled LOW while STBN is HIGH and remains HIGH for at least the hold time t_h [1]. If STBN becomes LOW before t_h [1] has exceeded, an unintended transition via NORMAL to STANDBY mode might happen. See detail in Fig 13.

Although for this transition typically no wait times are needed for the microcontroller software, the hold time t_h [1], the standby mode delay time $t_{d(stb)}$ [1] and the RXD delay time $t_{d(RXD)}$ [1] should be taken into account.

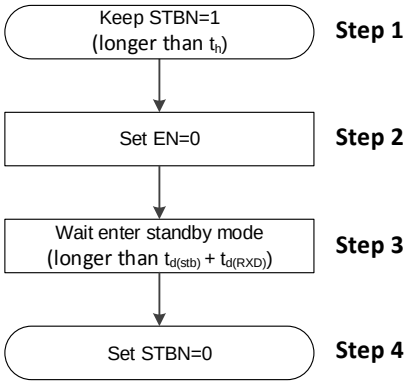


Fig 14.Example software sequence for the transition from PORT to STANDBY mode

5.1.4 NORMAL mode transitions

The NORMAL mode is used to transmit and receive data via the LIN bus line.

5.1.4.1 Transition NORMAL to STANDBY mode

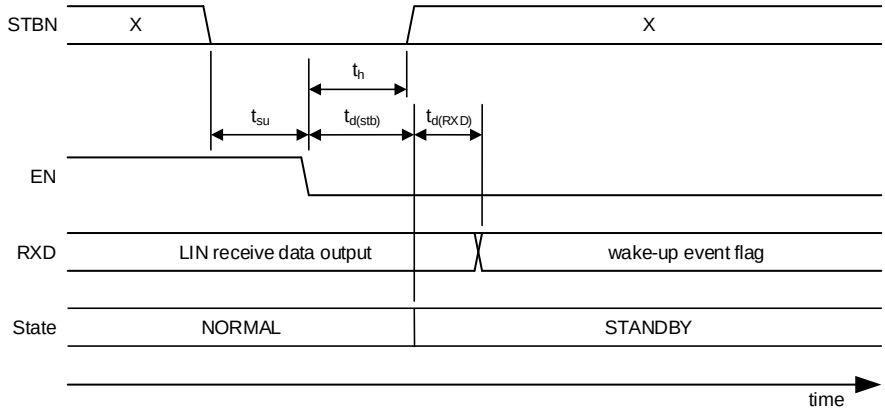


Fig 15.Transition from NORMAL to STANDBY mode

For a successful transition from NORMAL to STANDBY mode the set-up time t_{su} [1] and the hold time t_h [1] need to be taken into account. Fig 15 shows that for this transition STBN must be pulled LOW for at least t_{su} [1] before EN is pulled LOW. Afterwards STBN must remain LOW for at least t_h. Otherwise an unintended transition towards SLEEP mode might take place.

It is recommended for the microcontroller software to incorporate t_{su} [1]and t_h [1], e.g. by adding wait times. Furthermore, the standby mode delay time $t_{d(stb)}$ [1] and the RXD delay time $t_{d(RXD)}$ [1] should be taken into account.

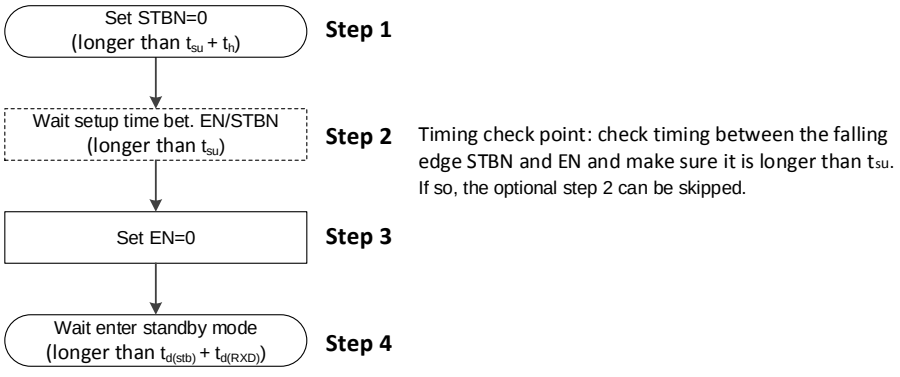


Fig 16.Example software sequence for the transition from NORMAL to STANDBY mode

When the MTP register DISSLP=1 (enter SLEEP mode is disabled), step 3 + step 4 are sufficient to enter STANDBY from NORMAL.

5.1.4.2 Transition NORMAL to GOTOSLP mode

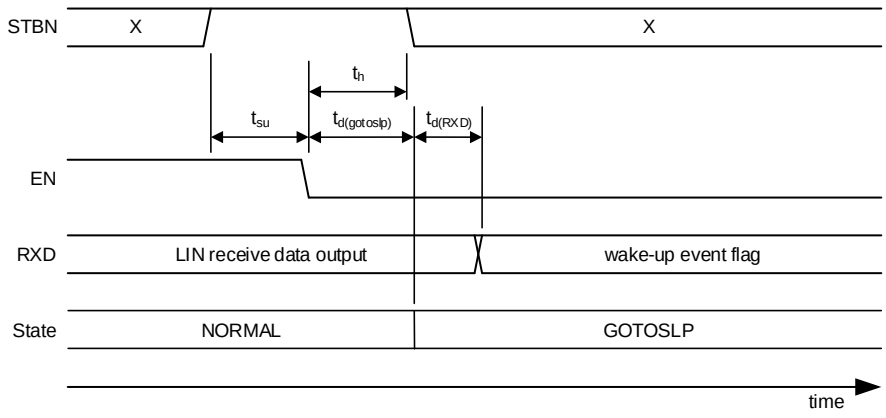


Fig 17.Transition from NORMAL to GOTOSLP mode

For a successful transition from NORMAL to GOTOSLP mode the set-up time t_{su} [1] and the hold time t_h [1] needs to be taken into account. Fig 17 shows that for this transition STBN must be pulled HIGH for at least t_{su} before EN is pulled LOW. Afterwards STBN must remain HIGH for at least t_h [1]. Otherwise an unintended transition towards STANDBY mode might take place.

It is recommended for the microcontroller software to incorporate t_{su} [1] and t_h, e.g. by adding wait times. Furthermore the GOTOSLP mode delay time $t_{d(gotoslp)}$ [1] and the RXD delay time $t_{d(RXD)}$ [1] should be taken into account.

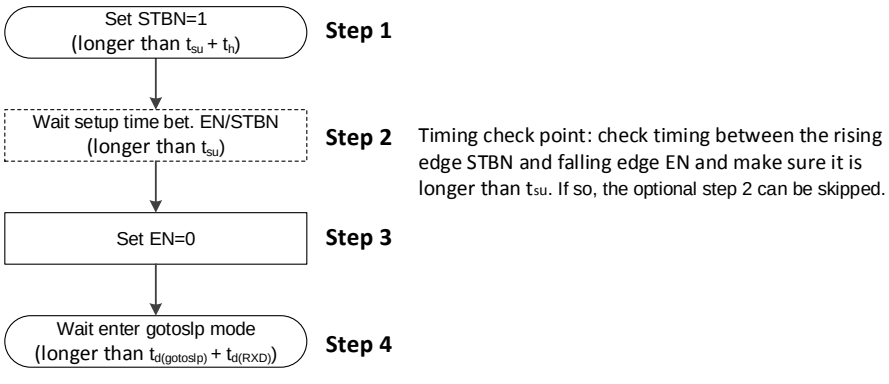


Fig 18.Example software sequence for the transition from NORMAL to GOTOSLP mode

5.1.5 GOTOSLP mode

The GOTOSLP mode is an intermediate mode between NORMAL and SLEEP mode.

5.1.5.1 Transition GOTOSLP to PORT mode

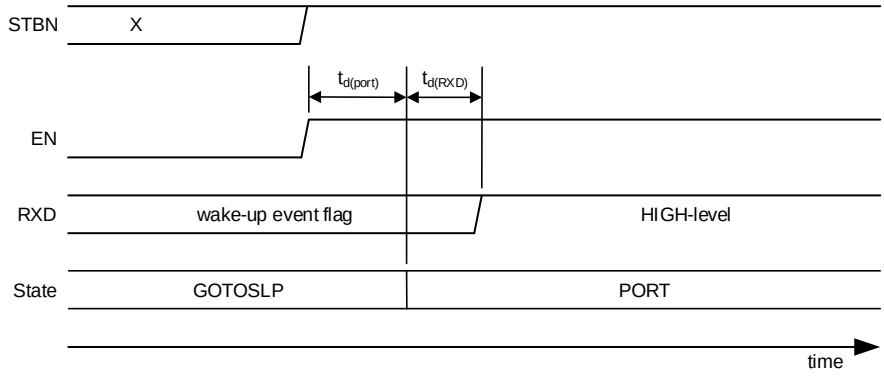


Fig 19.Transition from GOTOSLP to PORT mode

The GOTOSLP mode is used for proper hand-over of the wake-event monitoring from microcontroller to the TJA1128. A new wake-event is signaled to the microcontroller by driving the RXD LOW (same as STANDBY mode). The microcontroller controller can then decide to interrupt the transition to SLEEP mode by pulling EN to HIGH level, which will result in a transition to PORT mode. See detail in Fig 19.

For the microcontroller software the PORT mode delay time $t_{d(port)}$ [1] and the RXD delay time $t_{d(RXD)}$ [1] should be taken into account.

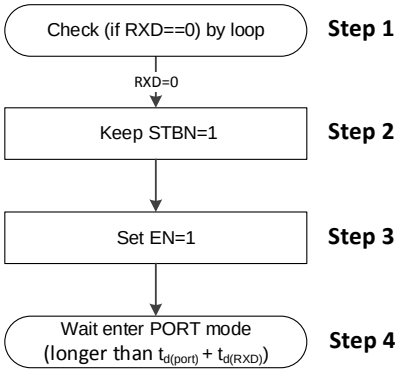


Fig 20.Example software sequence for the transition from GOTOSLP to PORT mode

5.1.5.2 Transition GOTOSLP to SLEEP mode

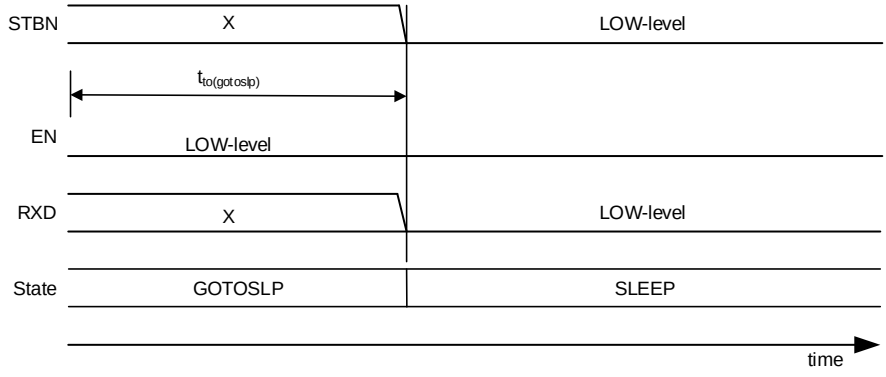
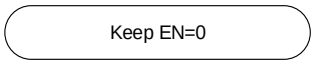


Fig 21.Transition from GOTOSLP to SLEEP mode

The TJA1128 will enter SLEEP mode after EN pin remains low for more than $t_{to(gotoslp)}$ [1].

If the wake-up event happened and wake-up flag is set and microcontroller did not pull EN HIGH level during $t_{to(gotoslp)}$ [1], the device will skip the SLEEP mode and enters RESET followed by STANDBY mode. See detail in Fig 21.



Step 1

Fig 22.Example software sequence about the transition from GOTOSLP to SLEEP mode

5.1.6 SLEEP mode

Sleep mode features very low power consumption. The voltage regulator and the LIN physical layer are disabled in SLEEP mode. Pin RSTN is forced low. Remote wake-up detection and local Wake-up are still active.

It is not recommended to disable all the wake-up sources and enter SLEEP mode. Otherwise the TJA1128 cannot be woken-up from SLEEP mode with having all wake-up sources disabled. In this case, power-on cycle is required.

5.2 Reset interface

The TJA1128x family offers a bidirectional RSTN pin for triggering a system reset.

On one hand, the TJA1128 generates a reset pulse on the RSTN pin at power-on or any system condition that requires a system reset. The RESET length $t_{w(rst)}$ [1] is configurable via bit RSTTIM in the system register [1], which offers higher design-in flexibility compared to a fixed reset length. It provides higher system predictability compared to a reset length that is determined by the time VCC is below the undervoltage level (which is undefined).

On the other hand, the reset of the TJA1128 is triggered if the RSTN pin is forced active low externally e.g. by the microcontroller.

5.3 Device configuration via SPI interface in CONFIG mode

The CONFIG mode is available for customers to configure the MTPNV and thus the TJA1128 with customer application specific settings, as illustrated in Table 4. The SPI interface is provided for the programming procedure during CONFIG mode. In CONFIG mode the LDO is enabled (VCC = on) and the RSTN pin is released HIGH. The TXD, RXD, EN and STBN pins are used as an SPI interface.

Table 4. MTPNV memory registers configurable for customers

Addr	Register block	Function description
10h	System	Reset output pulse width option: 0.7 / 4.0 ms; SLEEP mode entry enabled / disabled
11h	Wake	LIN bus wake-up enabled / disabled; Pin WAKE1/(WAKE2) rising / falling / both edges wake-up enabled / disabled
12h	LDO	VCC undervoltage detection enabled / disabled
13h	LIN	LIN transceiver enabled / disabled; High-speed mode enabled / disabled; TXD dominant time-out enabled / disabled
14h	Watchdog	Watchdog mode: timeout / window / autonomous / software development / disabled; Watchdog period: 16 / 32 / 64 / 128ms
15h	HVMPO	Cyclic wake settle time: 64 / 128us; Cyclic wake-up period time 16 / 64ms; HVMPO output polarity based on GPI input: invert (low → high level) / not invert (low → low level) HVMPO function: GPI controlled / bias output for cyclic wake-up / Limp home / mode indication / disabled
30h	MTPNV CRC	8 bits CRC value
31h	MTPNV status	MTPNVM write access enabled / disabled, error status, write counter status (MTPNV status, read access only)

Table 5. Conditions for entering CONFIG

Device is	The condition for enter CONFIG mode	Remark
un-configured	power-on and BAT > $V_{th(config)min}$[1]	CONFIG mode is entered automatically
configured	Factory restore condition. See data sheet [1], section “Restoring factory preset values”.	Used for re-configuration of the device: All the customer MTPNVM registers get cleared and restored to the default value (factory setting).
configured and contains with MTPNV fault	MTPNV fault detected (bit NVERR=1) after power-on.	CONFIG mode will be entered automatically and the error status bit NVERR is set and can be read out.

5.3.1 Programming procedure of the MTPNV memory

The following steps describe the basics of the MTPNV memory programming procedure. Further details about the recommended software flow can be found in Chapter 10.

5.3.1.1 Step 1: Check if TJA1128 is ready for programming the MTPNV memory

1) Check if TJA1128 is in CONFIG mode by reading the RXD pin level

In CONFIG mode pin RXD (or SDO) is pulled LOW when pin STBN (or SCSN) is HIGH to allow the microcontroller to detect the SPI configuration. See also section “Differentiation between CONFIG and PORT” in the data sheet [1].

2) Emulate TJA1128 control pins as SPI interface

TXD→SDI, RXD→SDO, EN→SCK, STBN→SCSN

The TJA1128 supports a SPI bit rate of up to 100kHz. Bit sampling is performed on the falling edge of the clock and data is shifted in / out on the rising edge.

Two byte (16 bits, 1st byte is address, 2nd byte is data), or three byte (24 bits, 1st byte is address, 2nd / 3rd byte is data) commands will be accepted by TJA1128 for read and write operations.

The microcontroller SPI command detail requirements can be found in the data sheet.

3) Check if TJA1128 is available for MTPNV programming

Check the MTPNVM write access status, error status and write counter status via SPI read commands. See the detail from section ”Programming of MTPNVM” in the datasheet [1].

5.3.1.2 Step 2: Program the MTPNV memory

1) Write the application specific TJA1128 configuration values to the MTPNV memory registers via SPI.

2) Write the correct CRC value to the MTPNV CRC register via SPI command to confirm the previously received TJA1128 configuration values are correct and thus to trigger the start of the actual programming of the MTPNV memory registers.

A mismatch in the CRC-value will abort the programing after setting the NVERR status bit in MTP and incrementing the write counter.

3) Check if a system reset of the TJA1128 is generated within 80ms.

A system reset of the TJA1128 is generated to indicate that the MTPNVM has been programmed successfully. For instance, this can be checked by adding a time-out of 80ms. If the time-out expires without reset, the configuration was not successful. The MTPNV status and configuration registers should be read and checked again. (Further details can be found in Chapter 10)

Table 6 shows a MTPNV memory setting value example based on TJA1128H and the MTPNV memory preset value below:

Table 6. TJA1128H and the MTPNV memory preset value example

Addr	Preset value	Remark
10h	0x00	reset plus width setting: 4ms
11h	**0x1F**	LIN bus wake-up enabled, WAKE1 / WAKE2 both edges wake-up enabled [2]
12h	0x00	VCC undervoltage detection enabled
13h	0x00	LIN transceiver enabled, LIN high-speed mode disabled, TXD dominant timeout enabled
14h	0x00	software development mode disabled, watchdog disabled
15h	**0x03**	HVMPO operation mode setting is LIMP home
20h	0x00	additional fixed value to be used for CRC calculation
21h	0x01	additional fixed value to be used for CRC calculation
initial_CRC	**0x81**	depends on TJA1128 variant: TJA1128H
30h	0x00	CRC final value, calculate based on data above

The preset value in bold font means an example value that is different from the default value or the preset values that is relevant with variant and CRC calculation.

[2] It is recommended not to disable all the wake-up sources and enter SLEEP mode. This is to prevent that the TJA1128 cannot be woken-up from SLEEP mode with having all wake-up sources disabled. In this case, power-on cycle is required.

5.4 Sequence to restore factory preset

The TJA1128 factory preset can be restored. The conditions for the restore of the factory preset is specified in the data sheet [1].

In this section the step-by-step sequence to restore the factory preset is described.

As start condition the TJA1128 power supply must be off. In addition the pin RSTN must be LOW and the pin LIN must be dominant. This can be realized with a short-ciruit to ground.

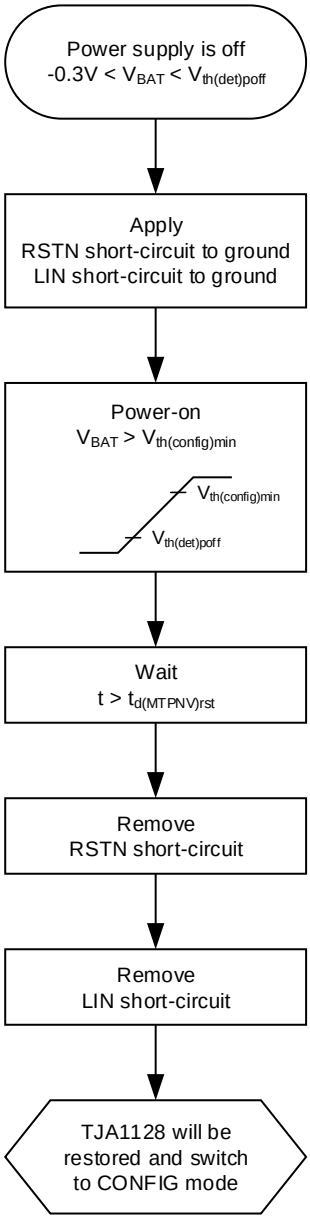


Fig 23. Sequence to restore factory preset

Next the TJA1128 power supply must be switched on to a supply voltage level higher than $V_{th(config)min}$. After the reset MTPNV restore delay time $t_{d(MTPNV)rst}$ the pins RSTN and LIN can be released again, i.e. the short-circuit can be removed, respectively.

Subsequently the factory preset is restored and the TJA1128 will switch to the CONFIG mode.

In Fig 23 the sequence to restore factory preset is illustrated.

5.5 Watchdog interface

5.5.1 Watchdog overview

The TJA1128E / F / G / H contains a programmable watchdog, which can be operated in two main operating modes:

- **Window mode** (triggering in the 2nd half of the watchdog period)

- **Timeout mode** (triggering at any time within the watchdog period)

Furthermore, the TJA1128 provides for special purposes the possibility to adapt the behavior of the watchdog by two additional configurations:

- **Autonomous mode** (the watchdog stops after mode transition to any low power mode and restarts after a wake-up event or mode transition to NORMAL mode)

- **Software Development mode** (the watchdog can be enabled / disabled as needed during software development)

5.5.2 Watchdog usage during module development

5.5.2.1 1st level: Watchdog off (Factory delivery)

In order to allow an easy start with the TJA1128 E / F / G / H at first battery connection after factory delivery, the device enters CONFIG mode with watchdog off. This configuration is useful for first flashing of the microcontroller during production. It is recommended to keep the watchdog off in CONFIG mode (WDMOD = 0).

After correct programming of the MTPNV memory, the device will quit the CONFIG mode. After a following system RESET of the TJA1128, the device will directly enter STANDBY mode. The watchdog keeps disabled.

The watchdog off setting can be used e.g. for initial prototyping during development.

5.5.2.2 2nd level: Watchdog enabled by SW (Software Development Mode)

During software development it gets necessary to enable or disable the watchdog for testing and debugging purposes. The Software Development mode is enabled and disabled via the WDSDM bit in the watchdog register. During the transition from RESET to STANDBY mode the input level on the WWD pin of the TJA1128 gets checked: with HIGH-level the watchdog gets enabled and with LOW-level the watchdog stays disabled.

Other functionalities of TJA1128 E / F / G / H than the watchdog are not influenced by this mode. Thus software testing and debugging on the TJA1128 can be done without triggering the watchdog.

If the application does not use the watchdog at all or if it is required to start the watchdog individually by software, the TJA1128E / F / G / H can also be operated continuously in Software Development Mode.

5.5.2.3 3rd level: Watchdog automatically enabled (Normal Operation)

After finalizing the software or after flashing the microcontroller during production, the watchdog can finally be enabled by re-programming the MTPNV memory in CONFIG mode (see chapter 5.3). Then the watchdog is automatically running and can only be stopped temporarily by SW with selecting Autonomous mode (WDAUTO = 1 and WDMOD = 01/10, in the Watchdog register). In this mode the watchdog automatically switches off after a transition from NORMAL mode to either STANDBY mode or GOTOSLP mode. The watchdog is switched on again after a wake-up event or after a transition to NORMAL mode.

The three described levels of watchdog configuration ease flashing of the ECU's microcontroller and software development in the design phase before the TJA1128E / F / G / H gets enabled for full operation with full watchdog supervision.

5.5.3 Configuration of the watchdog mode and period

The TJA1128E / F / G / H support 4 watchdog time periods: See WDPER in the watchdog register [1]. At start-up the default watchdog period is the maximum watchdog period and the default watchdog operating mode is timeout mode. Afterwards the watchdog mode and period will be changed by the watchdog setting.

A watchdog trigger event during the allowed trigger window resets the watchdog timer. A watchdog trigger event is a negative pulse on the WWD pin with a width of at least $t_{trig(wd)low}$ [1].

Table 7 shows the watchdog functionality in each operation mode based on different watchdog register bit settings.

Table 7. Watchdog functionality

	Window Mode	Timeout Mode	Autonomous Mode
TJA1128 E / F / G / H watchdog configuration			
WDAUTO WDMOD	0 [default] 01	0 [default] 10	1 01/10
Watchdog main behavior			
Severity level	High	Medium	Low
WD active	always	always	only in Normal Mode
WD trigger	2nd half of window	anytime in window	selectable: 2nd half of window or anytime in window
Watchdog behavior in different modes			
NORMAL mode	Window	Timeout	Window / Timeout
STANDBY mode	Window	Timeout	Off (if RXD is high, i.e. no wake event detected)
PORT mode	Window	Timeout	Off (if no wake event detected)

	Window Mode	Timeout Mode	Autonomous Mode
GOTOSLP mode	Window	Timeout	Off (if RXD is high, i.e. no wake event detected)
SLEEP / RESET / other mode (e.g. CONFIG)	Off	Off	Off

Changing the watchdog configuration (bit change of WDAUTO and WDMOD) is only possible in CONFIG mode by re-programming the MTPNV memory (see chapter 5.3)

5.5.4 Watchdog triggering

In timeout mode the watchdog timer can be reset at any time within the watchdog period by a negative pulse watchdog trigger on the WWD pin for at least $t_{trig(wd)low}$ [1]. If the watchdog overflows due to a missing trigger event, the system reset immediately occurs. In Window mode the watchdog timer can only be reset in the second half of the watchdog period (“open window”) by a watchdog trigger on the WWD pin for at least 60µs ($t_{trig(wd)low}$). If the watchdog is triggered in the first half of the watchdog period (“closed window”) or overflows, a system reset is immediately performed.

In both modes at a wrong or missing watchdog trigger the device switches to RESET mode and a low-level pulse on pin RSTN will be generated.

To select the correct trigger moment the tolerances of the watchdog timer must be taken into account. The software has to provide the trigger signal after the latest possible window opening $t_{trig(wd)1,max}$ [1] and before the earliest end of a period $t_{trig(wd)2,min}$ [1] (see Fig 24).

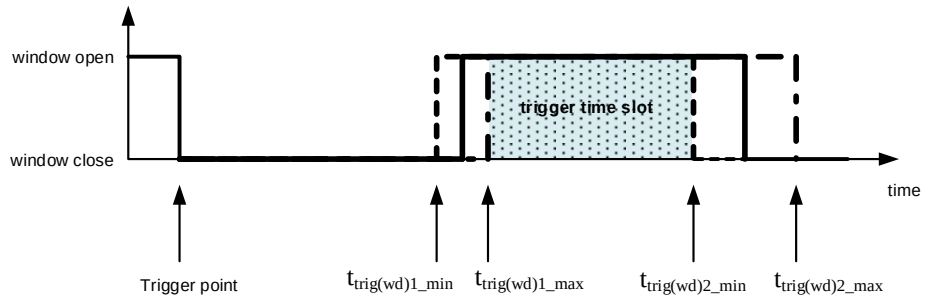


Fig 24. Allowed trigger area, when watchdog is in Window mode

The related values can be found in the TJA1128 data sheet [1]. In case the tolerances of the microcontroller's clock generator cannot be neglected, the following equations should be used to define the correct trigger moment:

$$t_{trigger\_\min} > \frac{t_{trig(wd)1\_\max}}{1-F}, \qquad t_{trigger\_\max} < \frac{t_{trig(wd)2\_\min}}{1+F}$$

Where ‘F’ is the magnitude of relative deviation of the microcontroller’s clock frequency. It is calculated by:

$$F = \left| \frac{f - f_0}{f_0} \right|$$

Where ‘f’ is the actual frequency and f_0 is the nominal frequency. $t_{trigger\_min}$ and $t_{trigger\_max}$ limit the area where the software has to choose the trigger point supposing the nominal frequency of the clock generator.

Changing the watchdog trigger period (bit WDPER) is only possible in CONFIG mode by re-programming the MTPNV memory (see chapter 5.3).

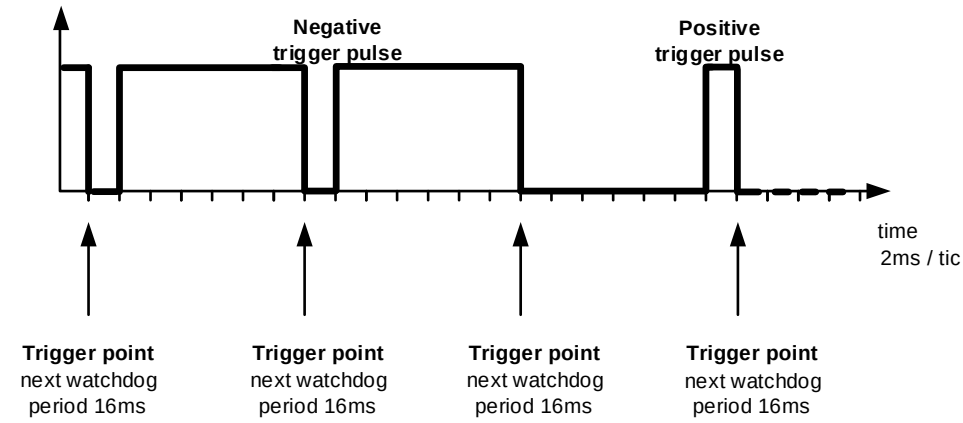
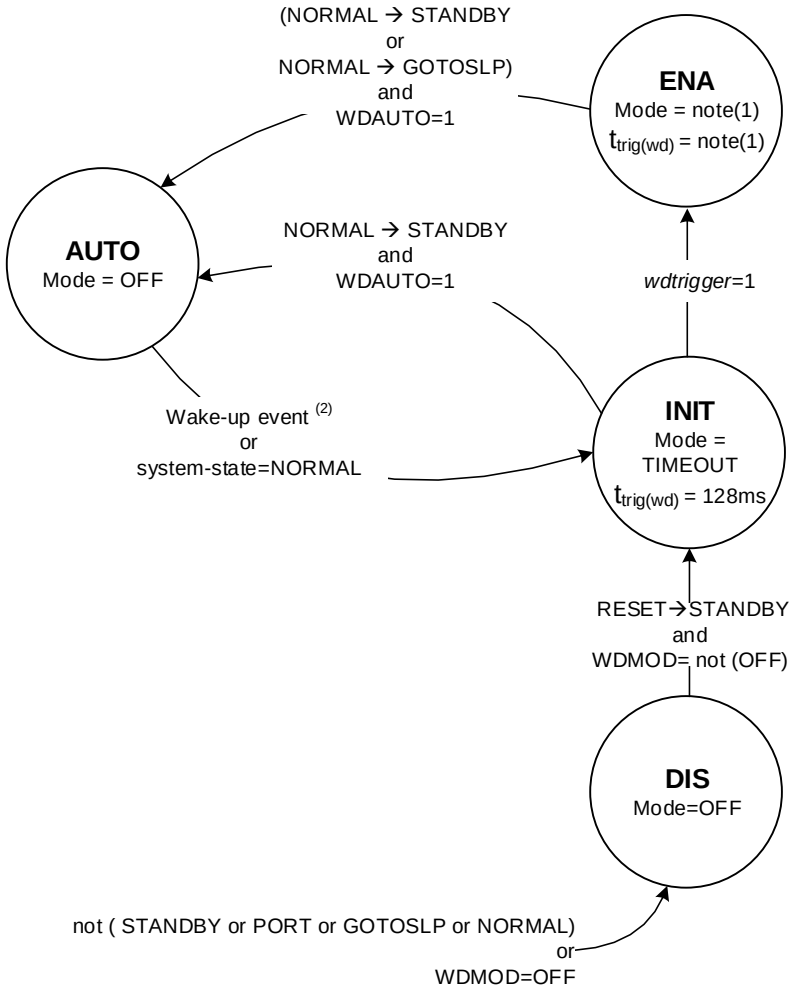


Fig 25. Watchdog triggering with different trigger pulse

5.5.5 Watchdog start-up behavior

Independent of the watchdog setting, the watchdog start-up behavior is always identical. For the first trigger the watchdog mode is timeout mode with the maximum nominal watchdog period. Afterwards the watchdog mode and period will be configured to the watchdog setting (see Fig 26).



Notes:
(1) The watchdog is configured as defined by the WDMOD and WDPER bits
(2) At least one local or remote wake-up event is set (wake-event-flag)

ENA: watchdog enabled
INIT: initial mode when watchdog start-up
DIS: watchdog disabled
AUTO: watchdog in autonomous mode

Fig 26. Watchdog start-up behavior

5.6 GPI (General Purpose Input) pin

The GPI pin can be configured to be used as control input for the HVMPO (High Voltage Multi Purpose) output pin, e.g. for a “Low Side Switch” application.

Changing the GPI configuration (via change of bits MPOINV and MPOMOD) is only possible in CONFIG mode by re-programming the MTPNV memory (see chapter 5.3).

Table 8 shows the correlation between the GPI input pin level and the HVMPO output depending on the MPOINV and MPOMOD bit settings in the HVMPO register. An application example with a HVMPO pin controlled LED (based on the GPI input) is shown in Fig 27.

In case the GPI pin is not used in the application, it can be left open or connected to ground. Furthermore, for disabling the GPI pin functionality the according MPOMOD bit should NOT be set to 001.

Table 8. The correlation between GPI input and HVMPO output

HVMPO register setting	GPI input level	HVMPO switch status	HVMPO output	LED status
MPOINV =X & MPOMOD = 000	X	OFF	Floating	OFF
MPOINV =0 & MPOMOD = 001	LOW	ON	LOW	ON
	HIGH	OFF	Floating	OFF
MPOINV =1 & MPOMOD = 001	LOW	OFF	Floating	OFF
	HIGH	ON	LOW	ON

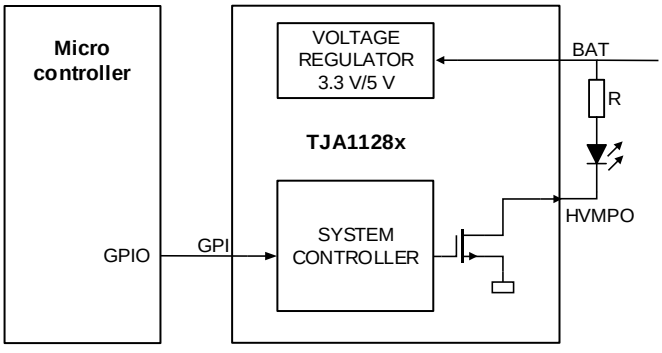


Fig 27. GPI and HVMPO application example

6. LIN transceiver interface

6.1 LIN transceiver overview

The TJA1128 includes an integrated LIN transceiver that is directly supplied out of V_{BAT}. The slope timings and propagation delay symmetry meets ISO 17987-4:2016 (12 V LIN), all LIN 2.x versions and SAE J2602-1 in order to allow maximum bit rate tolerance in the system while offering excellent EMC performance.

6.2 LIN transceiver operating modes

The LIN transceiver supports two operating modes depending on the TJA1128 mode.

Enabled:

When the LIN transceiver is enabled it can transmit and receive data. The LIN transceiver is enabled when below conditions are fulfilled:

- DISLIN = 0 in LIN register
- TJA1128 is in NORMAL mode
- The RESET pin is HIGH

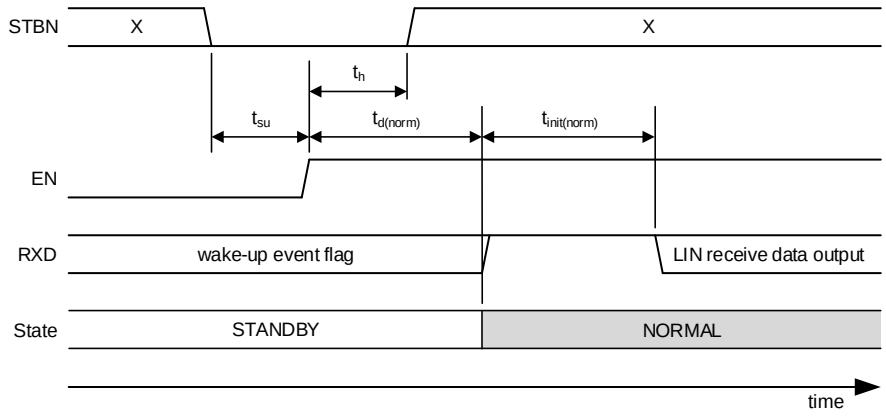


Fig 28. Timing diagram for activation of the LIN transceiver

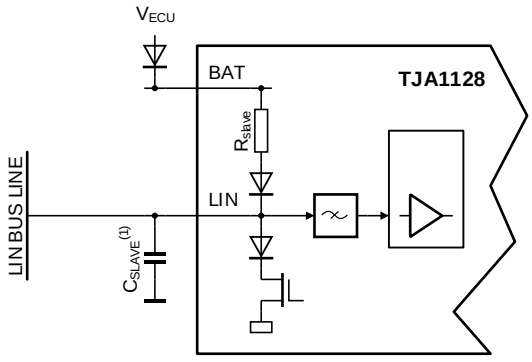
Disabled:

The LIN transceiver is disabled if at least one of the conditions mentioned above is not met. When the LIN transceiver is disabled it is not possible to transmit or receive LIN data, but depending on the device configuration and the applied mode, remote wake-ups via LIN, as described in chapter 6.4, will be detected.

In addition the LIN transceiver transmit path is disabled, if TXD dominant failures are detected; see initial TXD dominant check and TXD dominant time-out in the data sheet [1].

6.3 LIN termination

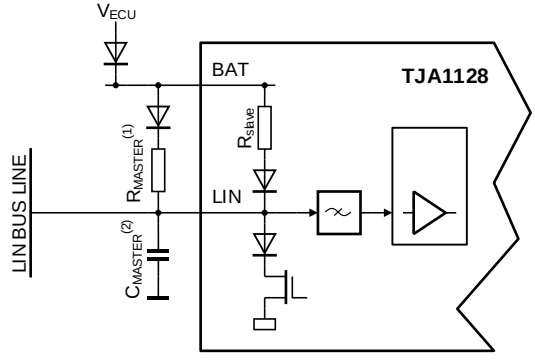
In general the termination circuitry of the LIN transceiver shall be designed according to the specification of the car manufacturer. The TJA1128 provides an integrated slave termination consisting of a diode in series with a resistor between the pins BAT and LIN (see Fig 29).



(1) C_{SLAVE} depends on OEM specification: typ. 220pF

Fig 29. Typical LIN slave application (minimal required circuitry)

To use the TJA1128 as LIN master, the LIN master termination needs to be applied externally. According to the LIN standard the LIN master termination consists of a diode and a series resistor R_{MASTER} between the polarity protection diode of the ECU and the LIN wire (see Fig 30).



(1) R_{MASTER} depends on OEM specification: typ. 1kΩ

(2) C_{MASTER} depends on OEM specification: typ. 680pF

Fig 30. Typical LIN master application (minimal required circuitry)

6.4 Remote wake-up detection

The TJA1128 supports detection of remote wake-up events when the LIN transceiver is not active, e.g. in STANDBY mode. In STANDBY mode wake-up events will be signalled with a LOW level at the RXD pin. This can be used e.g. as a wake-up interrupt request for the microcontroller. For further details, see data sheet [1], section “Remote wake-up via LIN bus.

The wake-up source information can be read in PORT mode. See section “PORT mode” in the data sheet [1].

6.5 ISO 9141 (K-Line) Support

The standards ISO 9141-2:1994 “Road Vehicles – Diagnostic Systems – Part 2” [2] and ISO 14230-1:2012 “Road vehicles -- Diagnostic communication over K-Line (DoK-Line) – Part 1” [3] specify the interchange of digital (diagnostic) information between on-board ECUs of road vehicles and a scan/test tool. The appropriate bus is the so-called “K-Line Bus”.

Although the LIN physical layer has been derived from the ISO 9141 standard there are some differences as shown in Table 9.

Table 9. Comparison ISO 9141-2 / ISO 14230-1 (12V) with ISO 17987-4 (12V) and TJA1128

Description	**ISO 9141** [2] **/ ISO 14230-1 (12V)** [3]	**ISO 17987-4 (12V)** [4]	**TJA1128**
ECU Operating Voltage Range V_B	8 V to 16 V	8 V to 18 V	✓
Receiver High Mode	> 70% V_B	> 60% V_B	✓
Receiver Low Mode	< 30% V_B	< 40% V_B	✓
Temperature Range	0 °C to 50 °C	-40 °C to 125 °C	✓
Capacitance			
Diagnose Tester / LIN Master	< 2 nF	-	✓
ECU / LIN Slave	< 500 pF	< 250 pF	✓
Wiring	< 2 nF	< 6 nF	✓
Total	< 9.2 nF	< 10nF	✓
Resistance			
Diagnose Tester / LIN Master	510 Ω	0.9 kΩ to 1.1 kΩ	✓
ECU / LIN Slave	> 100 kΩ	20 kΩ to 60 kΩ	LIN Slave pull-up is integrated. For reliable operation the overall network pull-up shall be above 500 Ω.
Timings			
Transmission Rate	10.4 kbit/s	1 kbit/s to 20 kbit/s (>20 kbit/s in LIN high speed mode)	✓
Slew Rate / Slope Time	< 10 % T_{BIT} = 9.6 µs	1 - 5µs	✓, TJA1128 in LIN high-speed mode
		duty cycle specification	Timing with disabled LIN high-speed mode is acc. the LIN duty cycle specification, which is optimized for communication up to 20kbit/s. This offers better EMC compared to ISO 9141 / ISO 14230.

Although the LIN physical layer is not fully compliant to ISO 9141-2:1994 and ISO 14230-1:2012 (12V), the TJA1128 LIN transceiver will work in K-Line networks. Only the number of K-Line nodes could be limited, if LIN transceivers are applied. In a K-Line bus the overall network load is mainly caused by the Diagnose Tester (the master in a K-Line bus [2]), which is terminated with a pull-up of R_{TESTER} = 510 Ω. But each LIN transceiver with integrated LIN slave resistor R_{SLAVE}, like the TJA1128, will cause a decrease of the K-Line network resistance. The K-Line network resistance reduction can be calculated with following equation:

Minimum K-Line network load:

$$R_{K(BUS-BAT)\min} = \frac{R_{TESTER,\min} \times \frac{R_{SLAVE,\min}}{N}}{R_{TESTER,\min} + \frac{R_{SLAVE,\min}}{N}}$$

with

$R_{TESTER,min}$	minimum Diagnose Tester pull-up resistor
$R_{SLAVE,min}$	minimum LIN slave pull-up resistor
N	number of transceivers with integrated LIN slave resistor

Thus the maximum number of LIN transceivers in a K-Line bus is limited by the strength of the weakest bus driver. The TJA1128 is specified for the minimum network resistance of $R_{L(LIN-BAT)}$= 500 Ω [1].

Summary:

Though there are some deviations between the LIN and the ISO 9141 specification, the TJA1128 is able to support the K-Line bus from functional point of view. From a formal specification point of view, no LIN transceiver supports by 100% ISO 9141-2:1994 and ISO 14230-1:2012 (12V) specification.

6.6 LIN high-speed mode

TJA1128 supports applications (i.e. end of line ECU flashing via LIN bus), with bit rates above 20 kbit/s. For this LIN high-speed mode, the device must be configured as LIN high-speed mode via bits HSMODE. The configuration is only possible in CONFIG mode.

For small sized LIN nodes it can be difficult to add a dedicated programming connector. In this case the LIN connection is an option for end of line programming. In order to reduce the programing time via LIN bus the TJA1128 LIN high-speed mode can be used with higher data rates, e.g. 100 kbit/s. The maximum bit rate depends on the LIN network RC time constant, but it is typically a point-to-point connection with low RC time constant.

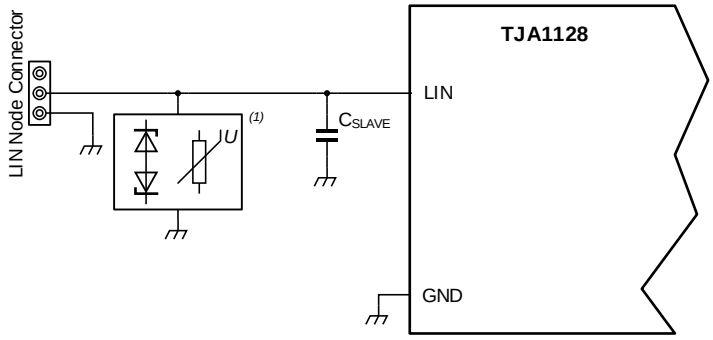
The TJA1128 provides two LIN high-speed mode configuration options, the difference is shown in Table 10.

Table 10. LIN high-speed mode

Register setting	Function	Remark
HSMODE = 00	LIN high speed mode disabled	Default value
HSMODE = 01	LIN high speed mode enabled until next BAT power-on event	After the configuration and entering NORMAL mode, LIN high-speed mode is enabled termporarily until next BAT power-on event
HSMODE = 10	LIN high speed mode enabled	After the configuration and entering NORMAL mode, LIN high-speed mode is enabled permanently unless the CONFIG is entered again. (HSMODE bit restores to the default value). In LIN high-speed mode a higher electromagnetic emission can be expected since the curve shaping of the LIN output signal is disabled
HSMODE = 11	LIN high speed mode disabled	

6.7 LIN ESD protection

The TJA1128 is designed to withstand ESD pulses up to ±8 kV according to the Human Body Model (HBM, C = 100 pF, R = 1.5 kΩ) and at least ±6 kV according to the IEC61000-4-2 (C = 150 pF, R = 330 Ω) at the LIN bus pin. Thus, typically no further external measures are needed. Nevertheless, if higher ESD protection is required, external clamping circuits can be applied to the LIN bus line, e.g. PESD1LIN. The ESD measurements were performed without external bus filters at the LIN bus pin and confirmed an ESD robustness for pulses even higher than ±6kV according to IEC61000-4-2 (C = 150pF, R = 330Ω) (For further information see Fig 31).



(1) Optional external ESD protection with suppressor diode (e.g. PESD1LIN) or varistor

Fig 31. External ESD protection set-up

7. WAKE interface

7.1 Functionality of WAKE pins

The TJA1128x offers 1 or 2 dedicated wake-up pins, WAKE1 and WAKE2. In most applications these pins are connected with external wake-up switches to GND. The wake-up pins can be configured to either be sampled continuously or to be sampled cyclically with two different periods.

In case the WAKE pins are not used in the application, they should either

- be disabled via configuration in CONFIG mode (LCWK1 = 00 and LCWK2 = 00, in the Wake register) and can then be left open or
- be connected to ground or BAT via a series resistor (>10kΩ) to avoid an unintended wake up.

If an external wake-up circuitry is connected to a WAKE pin, it is recommended to keep this circuitry independently from the VCC output voltage of TJA1128x. Otherwise a wake-up from this circuitry via the WAKE pin may not be possible, while the TJA1128x is in SLEEP mode, i.e. while VCC is off.

7.2 WAKE ESD protection

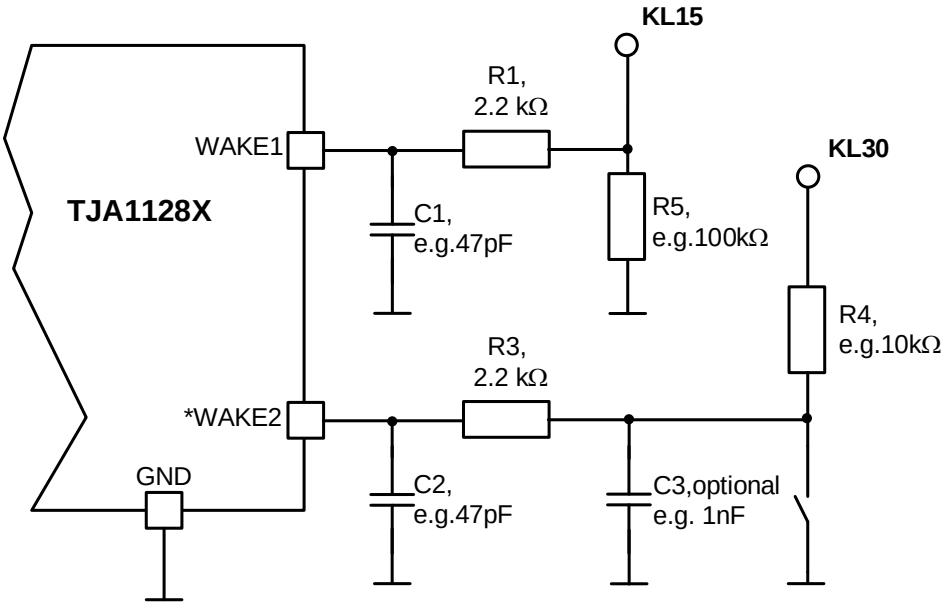
The WAKE pins of the TJA1128 are designed to withstand ESD pulses up to ±4 kV according to the Human Body Model (HBM, C = 100 pF, R = 1.5 kΩ). In case the WAKE pins are used off-board, a series resistor R1 / R3 = 2.2 kΩ and C1 / C2 (optional for better immunity performance) are recommended, when ±6 kV according to IEC61000-4-2 (C = 150 pF, R = 330 Ω) is required (see Fig 32).

7.3 Continuously sampled wake-up mechanism

The WAKE pins can be connected directly to control signals that shall trigger a device wake-up (e.g. KL15 = battery signal that is turned on by the ignition key, or a hard switch to GND or a transceiver's INH signal). To sample the wake-up pins continuously, the edge sensitivity (falling, rising or both) of the wake-up pins can be configured via the LC1WKE and LC2WKE bits in the wake register.

Changing the configuration is only possible in CONFIG mode by re-programming the MTPNV memory (see chapter 5.3)

Fig 32 shows an example for a typical application of the continuously sampled wake-up mechanism. A WAKE input is connected to KL15. Furthermore, an external pull-down resistor is required to ensure that the WAKE pin level is LOW in case KL15 is deactivated.



*optional, depends on the variant

KL15 = battery signal that is switched by the ignition key

Fig 32. Typical application for continuously sampling the WAKE pins

7.4 Cyclic sampled wake-up mechanism for power saving

A significant reduction of quiescent current can be achieved when the cyclic biasing and sampling feature of the TJA1128x is used to detect status changes at the WAKE inputs. This is realized by synchronizing the sampling of the WAKE inputs with the HVMPO signal and by using the cyclic HVMPO signal for supplying the switches.

The HVMPO pin is a battery-related, active-LOW, open-drain output pin that controls the bias transistor of the switches. The synchronization between HVMPO output pin and the

WAKE pins is enabled via the MPOMOD bits (MPOMOD = 010) in the HVMPO register. The bias and sampling period is configurable via the WKBPER bit in the HVMPO register. The sampling time is configurable via the WKBSET bit in the HVMPO register.

Fig 33 shows a typical application for cyclic sampled wake-up inputs. WAKE1 and WAKE2 are connected via switches to GND, with pull-up resistors that are supplied by the bias transistor, under control of the HVMPO pin [1].

Note that for selection of the values of the pull-up resistors in Fig 33, it should be taken into account that optional capacitors at the switch signals need to be charged in time. In order to detect an open contact correctly, the charge time of all capacitive loads connected to the WAKE pins has to be considered. That means, the upper WAKE threshold voltage has to be passed in order to start the wake-up filter time (t_{wake}), which must be elapsed before the HVMPO signal is switched off again (sample of WAKEx).

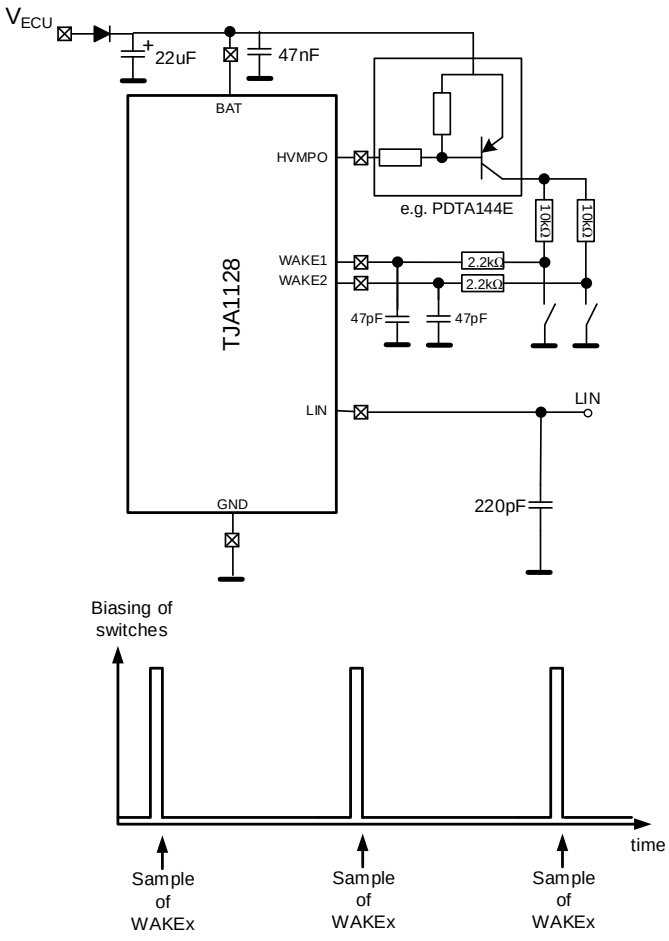


Fig 33. Typical application of cyclic sampling of switches

7.5 Wake-up source recognition

Once the microcontroller detects a wake-event (RXD driven low in STANDBY or GOTOSLP mode), it can enter PORT mode to identify which wake-up event(s) occurred. In PORT mode the RXD/TXD pins are used with a serial asynchronous UART data frame format. This frame format is used to transfer the info about the wake-status and -events to the microcontroller via pin RXD. See section PORT mode in the data sheet [1].

The recommended bit width on TXD can be calculated as follows:

TXD bit width in PORT mode ($t_{bit(TXD)}$): 30µs (min. bit width of TXD) + 10µs (TXD to RXD max. delay) + 2µs (max. jitter time) + 8µs (buffer) = 50µs.

The TJA1128 event capture implementation guarantees that the events will be cleared only when they have been communicated to the microcontroller.

So, if the application requires the wake-up source information, the data can be read out in PORT mode after wake-up from low-power mode. The wake-up source information will be cleared once the serial data (55h) has been applied on pin TXD in PORT mode.

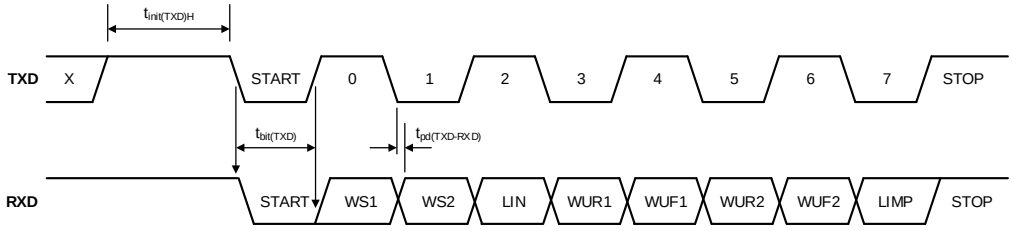


Fig 34. Serial data format in PORT mode

Please see the recommended software flow in Chapter 10.

The UART data frame consists of: a start bit, 8 data bits and a stop bit.

Table 11.UART data-byte contents

Bit	Name	Description
0	wk1_status	0: WAKE1 < Vth(wake1) 1: WAKE1 > Vth(wake1)
1	wk2_status	0: WAKE2 < Vth(wake2) 1: WAKE2 > Vth(wake2)
2	lin_wake_event	0: LIN bus wake event detected 1: no event
3	wk1_rise_event	0: wake1 rise event detected 1: no event
4	wk1_fall_event	0: wake1 fall event detected 1: no event
5	wk2_rise_event	0: wake2 rise event detected 1: no event
6	wk2_fall_event	0: wake2 fall event detected 1: no event
7	limphome_flag	0: limp-home flag is set 1: no limp-home condition

8. High Voltage Multi Purpose Output pin

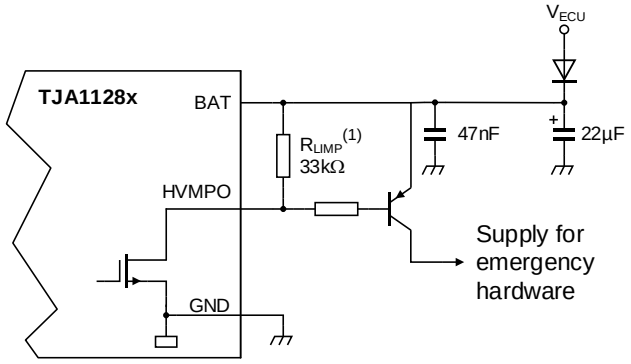
The High-Voltage Multi-Purpose Output pin can be configured to meet application specific requirements, which are shown in Table 12. Changing the HVMPO configuration (bit change of MPOMOD) is only possible in CONFIG mode by re-programming the MTPNV memory (see chapter 5.3)

Table 12. HVMPO functionality and application

HVMPO register setting	Functionality	Application example	Remark
MPOMOD = 000	All HVMPO functions are disabled	none	
MPOMOD = 001	HVMPO output is controlled via GPI input. The output polarity can be reversed via bit MPOINV in CONFIG mode	HVMPO is configured for driving some application loads like a LED, or for software control of the HVMPO output by a microcontroller GPIO (use case example: turn the resistive voltage divider 'on' for only the measurement time of an ADC)	See detail in 5.6
MPOMOD = 010	HVMPO outputs a specific sample bias signal in SLEEP, STANDBY, PORT, GOTOSLP, RESET modes for cyclic wake-up detection via WAKE pins	HVMPO is configured for ultra low-power consumption in SLEEP mode and cyclic sampling of wake-ups via a hard switch	See detail in 7.4
MPOMOD = 011	HVMPO is switched on (LOW) to activate external limp home circuitry, in case the limp home event is detected and the limp-home flag is set. The flag is read and cleared in PORT mode. In OFF mode the flag is also cleared.	HVMPO is used to activate emergency hardware in case of a serious system malfunction. System fail-safe control LOW level output is available via pin HVMPO in case of VCC undervoltage, RSTN short-circuit to ground, watchdog failure or device overtemperature	See detail in 8.1
MPOMOD = 100	HVMPO is switched on (LOW) if the device enters NORMAL mode	HVMPO is configured as state indicator. This can be used for bias control of a voltage divider for battery voltage monitoring, e.g. to disable the bias current when the product is in low power mode. Several state indicator combinations are available for different application scenarios	See detail in 8.2
MPOMOD = 101	HVMPO is switched on (LOW) if the device enters NORMAL or STANDBY or PORT mode		
MPOMOD = 110	HVMPO is switched on (LOW) if the device enters NORMAL or STANDBY or PORT or GOTOSLP mode		
MPOMOD = 111	HVMPO is switched on (LOW) if the device enters SLEEP mode		

8.1 LIMP home output

The HVMPO can be used to activate application-specific 'Limp-Home' hardware automatically in the event of a serious system malfunction. Detectable failure conditions are device overtemperature events, wrong watchdog service, VCC undervoltage and RSTN clamped LOW externally.



(1) R_{LIMP} value is exemplary. On principle the value depends on application.

Fig 35. Application example: HVMPO set as limp home

8.2 State controlled output

HVMPO can be configured as state indicator (MPOMOD = 1xx), which can be used for bias control of voltage divider for battery voltage monitor.

Battery monitoring is needed when application data needs to be stored before MCU undervoltage takes place, i.e. after a battery supply drop.

It is also needed for actuators and sensors, which depend on the battery voltage level.

Battery monitor circuits are typically connected to the battery supply before the protection diode and the output signal is connected to the ADC of the MCU.

Typically, in low power mode, battery monitoring is not needed. So, the bias current for the voltage divider could be switched off.

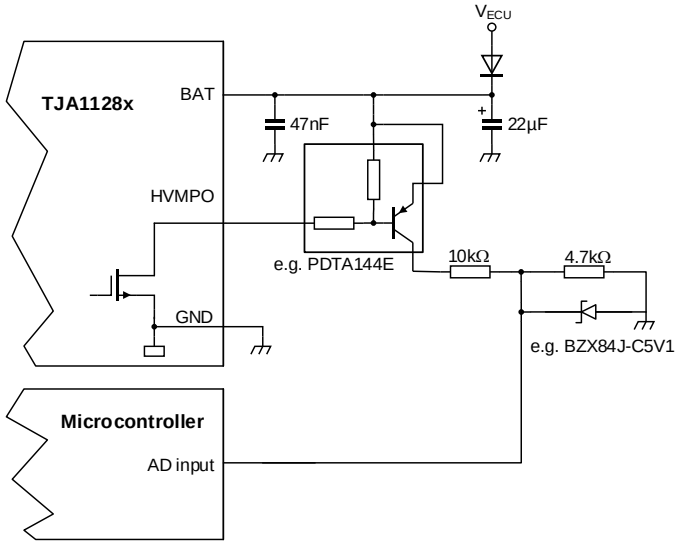


Fig 36. Application example: HVMPO set as state controlled output

9. Pin FMEA

Table 14 shows the pin FMEA for the TJA1128x. Classes of severity are listed in Table 13.

Table 13. Classification of severity of effects

Severity Class	Effects
A	- Damage to device - LIN network communication may be affected globally
B	- No damage to device - LIN network communication in the overall system not possible (global problem)
C	- No damage to device - LIN network communication of other nodes in the system possible - Corrupted node not able to communicate via LIN (local problem) - Application might shut-down
D	- No damage to device - LIN communication in the overall system possible - Reduced functionality of application

Severity Class	Effects	
E	-	No effect on device

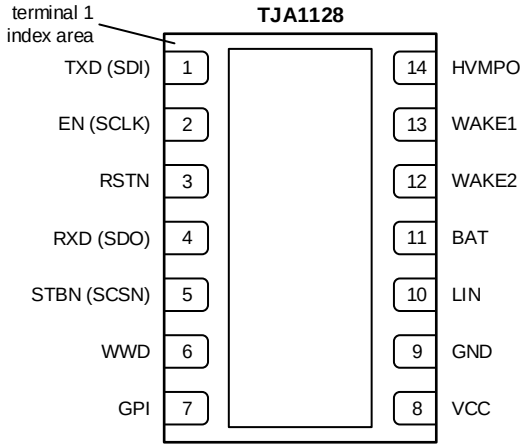


Fig 37. Pin configuration diagram

Table 14. Pin FMEA for TJA1128x

Pin Name	Failure	Remark	Severity Class
Pin 1: TXD (SDI)	Shorted to neighbor pin EN	• device configuration not possible • LIN transmission not possible the operating mode depends on the port structure of microcontroller: either device is in NORMAL mode with LIN bus in recessive state or device is put into STANDBY mode (if STBN=0) or SLEEP mode (if STBN=1) or it changes between these states	C
	Short to ground (incl. exposed die pad)	• device configuration not possible • LIN transmission not possible	C
	Short to VCC	• device configuration not possible • LIN transmission not possible	C
	Short to Vbat	• Limiting value exceeded	A
	Open Circuit	• device configuration not possible • LIN transmission not possible	C

Pin Name	Failure	Remark	Severity Class
Pin 2: EN (SCLK)	Shorted to neighbor pin RSTN	• device configuration not possible • STANDBY and SLEEP cannot be used; RSTN becomes LOW when EN goes LOW	D
	Short to ground (incl. exposed die pad)	• device configuration not possible • LIN communication not possible • device stuck in STANDBY mode, if configured	C
	Short to VCC	• device configuration not possible • device stuck in NORMAL mode, if configured	D
	Short to Vbat	• Limiting value exceeded	A
	Open Circuit	• device configuration not possible • LIN communication not possible • device stuck in STANDBY mode, if configured	C
Pin 3: RSTN	Shorted to neighbor pin RXD	• device configuration not possible • LIN communication not possible; reception of LIN dominant drives RXD and RSTN to LOW	C
	Short to ground (incl. exposed die pad)	• device will stay in RESET mode	C
	Short to VCC	• VCC undervoltage overruled • no reset time	D
	Short to Vbat	• Limiting value exceeded	A
	Open Circuit	• software supervising via WD not possible • VCC undervoltage supervising not possible • effect for the system needs to be assessed by system development team	D
Pin 4: RXD (SDO)	Shorted to neighbor pin STBN	• device configuration not possible • LIN communication affected; depends on port structure of microcontroller port for STBN	C
	Short to ground (incl. exposed die pad)	• device configuration not possible • LIN reception not possible	C
	Short to VCC	• device configuration not possible • LIN reception not possible	C
	Short to Vbat	• Limiting value exceeded	A
	Open Circuit	• device configuration not possible • LIN reception not possible	C

Pin Name	Failure	Remark	Severity Class
Pin 5: STBN(SCSN)	Shorted to neighbor pin WWD	• WD service affected; results in RSTN becoming LOW • mode selection affected • LIN communication affected • above effects depend on port structure of microcontroller ports for STBN and WWD	C
	Short to ground (incl. exposed die pad)	• device configuration not possible • SLEEP and PORT mode cannot be used	D
	Short to VCC	• device configuration not possible • LIN communication not possible • SLEEP and NORMAL mode cannot be used	C
	Short to Vbat	• Limiting value exceeded	A
	Open Circuit	• device configuration not possible • SLEEP and PORT mode cannot be used	D
Pin 6: WWD	Shorted to neighbor pin GPI	• if WDD and GPI are not used, then no effect on device and application • WD service affected; results in RSTN becoming LOW (i.e. LIN communication affected); if configured • control of HVMPO affected; if configured • above effects depend on port structure of microcontroller ports for GPI and WWD	C
	Short to ground (incl. exposed die pad)	• if WDD is not used, then no effect on device and application • WD service not possible; results in RSTN becoming LOW (i.e. LIN communication not possible); if configured	C
	Short to VCC	• if WDD is not used, then no effect on device and application • WD service not possible; results in RSTN becoming LOW (i.e. LIN communication not possible); if configured	C
	Short to Vbat	• Limiting value exceeded	A
	Open Circuit	• if WDD is not used, then no effect on device and application • WD service not possible; results in RSTN becoming LOW (i.e. LIN communication not possible); if configured	C
Pin 7: GPI	Short to ground (incl. exposed die pad)	• if GPI is not used, then no effect on device and application • control of HVMPO affected; if configured	D

Pin Name	Failure	Remark	Severity Class
	Short to VCC	• if GPI is not used, then no effect on device and application • control of HVMPO not permitted; if configured	D
	Short to Vbat	• Limiting value exceeded	A
	Open Circuit	• if GPI is not used, then no effect on device and application • control of HVMPO affected; if configured	D
Pin 8: VCC	Short to ground (incl. exposed die pad)	• no VCC available; device stuck in Reset mode	C
	Short to Vbat	• Limiting value exceeded	A
	Open Circuit	• no VCC supply for microcontroller (typical effect: device configuration and LIN communication not possible; device stuck in STANDBY mode, if configured)	C
Pin 9: GND	Open Circuit	• device not supplied (typically effect: application will not run; LIN communication not possible) • fundamental ECU problem: device and external components on ECU might become damaged through other GND paths on the board.	A
Pin 10: LIN	Short to ground (incl. exposed die pad)	• LIN network clamped to dominant • remote wake-up events on LIN cannot be detected	B
	Short to VCC	• external LIN circuit might cause voltage which exeeds the limiting value of VCC	A
	Short to Vbat	• LIN network clamped to recessive • remote wake-up events on LIN cannot be detected	B
	Open Circuit	• LIN communication not possible	C
Pin 11: BAT	Shorted to neighbor pin WAKE2	• wake-up events on WAKE2 cannot be detected • external wake-up circuit check needed: switch to ground might cause battery-to-ground short circuit	D
	Short to ground (incl. exposed die pad)	• device not supplied (typically effect: application will not run; LIN communication not possible) • fundamental ECU problem: polarity protection might be damaged, fuse may blow, etc. LIN network clamped to dominant • remote wake-up events on LIN cannot be detected	C

Pin Name	Failure	Remark	Severity Class
	Open Circuit	• device not supplied (typical effect: application will not run; LIN communication not possible) LIN communication not possible	C
Pin 12: WAKE2	Shorted to neighbor pin WAKE1	• wake-up source of WAKE1 and WAKE2 might not be distinguished (depends on wake-up edge configuration) • external wake-up circuit check needed: one switch to ground and other switch to battery voltage might cause battery-to-ground short circuit	D
	Short to ground (incl. exposed die pad)	• wake-up events on WAKE2 cannot be detected • external wake-up circuit check needed: switch to battery voltage might cause battery-to-ground short circuit	D
	Short to VCC	• wake-up circuit with switch to battery exeeds the limiting value of VCC • wake-up circuit with pull-up to battery might cause voltage which exeeds the limiting value of VCC • wake-up events on WAKE2 cannot be detected	A
	Open Circuit	• wake-up events on WAKE2 cannot be detected • unwanted wake-up events on WAKE2 might be detected, due to transient	D
Pin 13: WAKE1	Shorted to neighbor pin HVMPO	• wake-up events on WAKE1 might not be detected; depends on external circuit on both pins	D
	Short to ground (incl. exposed die pad)	• wake-up events on WAKE1 cannot be detected • external wake-up circuit check needed: switch to battery voltage might cause battery-to-ground short circuit	D
	Short to VCC	• wake-up circuit with switch to battery exeeds the limiting value of VCC • wake-up circuit with pull-up to battery might cause voltage which exeeds the limiting value of VCC • wake-up events on WAKE1 cannot be detected	A
	Short to Vbat	• wake-up events on WAKE1 cannot be detected • external wake-up circuit check needed: switch to ground might cause battery-to-ground short circuit	D
	Open Circuit	• wake-up events on WAKE1 cannot be detected • unwanted wake-up events on WAKE1 might be detected, due to transient	D

Pin Name	Failure	Remark	Severity Class
Pin 14: HVMPO	Short to ground (incl. exposed die pad)	• external HVMPO circuit check needed: e.g. with cyclic sampled wake-up function the external pull-up current might be permanent on, with limp home function the limp circuit might be permanent active, etc.	D
	Short to VCC	• external HVMPO circuit check needed: with battery related circuit the limiting value of VCC might be exeeded	A
	Short to Vbat	• external HVMPO circuit check needed: e.g. with cyclic sampled wake-up function the external pull-up current might be permanent off, with limp home function the limp circuit might be permanent inactive, etc.	D
	Open Circuit	• external HVMPO circuit check needed: e.g. with cyclic sampled wake-up function the external pull-up current might be permanent off, with limp home function the limp circuit might be permanent inactive, etc.	D

10. Software Flow

This chapter introduces the software perspective of the TJA1128x. Fig 38 provides a quick overview about the different kind and the order of possible operations.

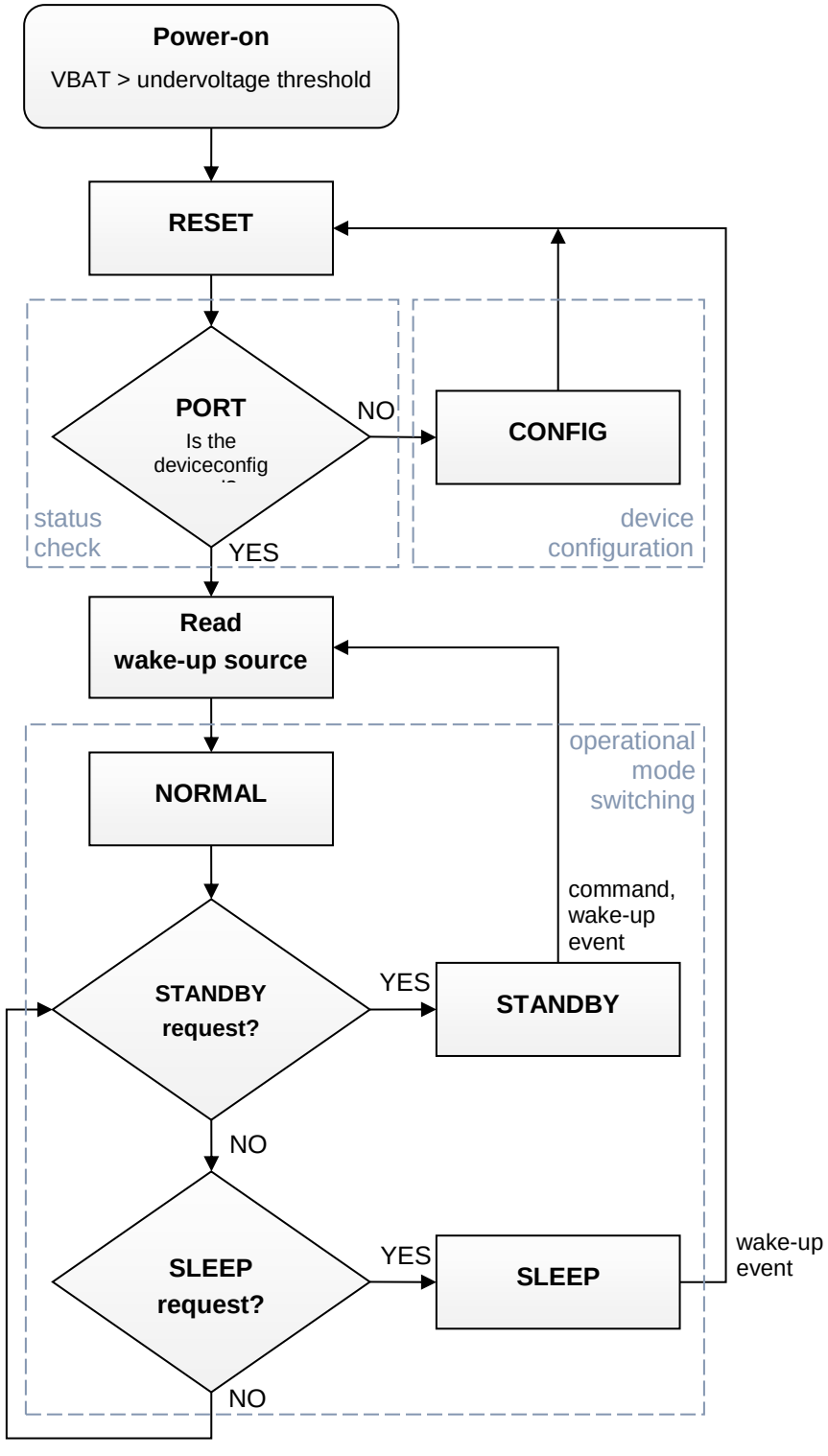


Fig 38. Software operation overview

After power-on the device enters RESET mode and the microcontroller is reset. After clock pin and peripheral initialization the microcontroller software should check (in TJA1128 PORT mode), whether the device has been configured before or if the first power-on occurred. If the device is not configured, configuration over SPI should follow. After valid configuration the device will automatically switch to RESET mode.

Once the software recognizes that the device is configured, the microcontroller reads the wake-up source and continues to normal operation. During normal operation different operational modes can be selected (NORMAL, STANDBY, or SLEEP if enabled) and the watchdog should be triggered (if enabled). The normal operation depends on the user application.

The following subchapters discuss each operation in more detail.

10.1 Device power-on and status check

After the device power-on and microcontroller reset, the device is switched to PORT mode through STANDBY mode (with appropriate delays to ensure correct mode switching). In PORT mode it is checked if the device is in CONFIG mode (first time power-on, or at invalid configuration). The status of the configuration is detected by reading the RXD pin level. In case of a low RXD pin level the device needs to be configured using the SPI interface. (see Fig 39)

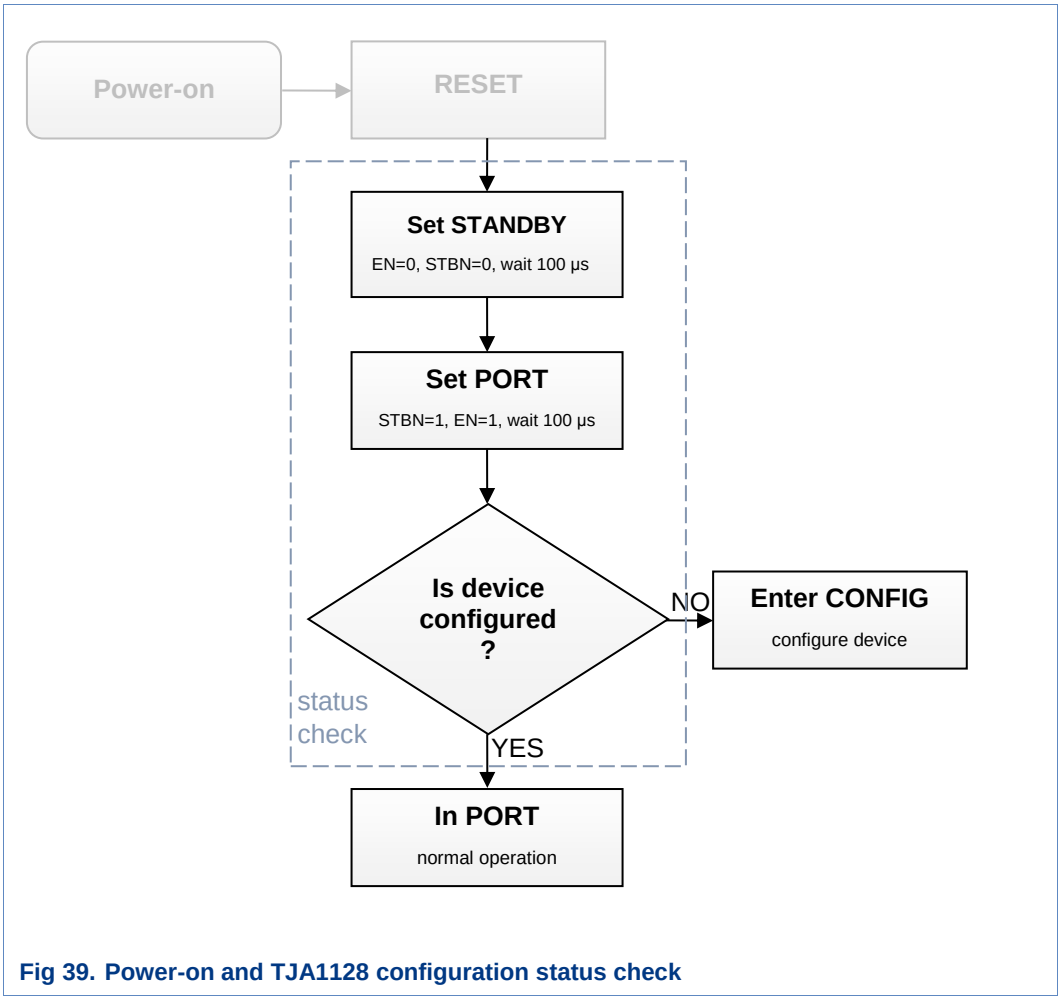


Fig 39. Power-on and TJA1128 configuration status check

10.2 Device configuration

When the device enters CONFIG mode, the device pins TXD, RXD, EN and STBN pins are reconfigured as an SPI interface (TXD→SDI, RXD→SDO, EN→SCK, STBN→SCSN) supporting up to 100 kHz clock frequency and 16bit/24bit command frame length. In case the microcontroller pins have no SPI hardware functionality, the SPI interface needs to be emulated by software.

The device contains MTPNV status registers, which can be used to check if the device is configurable (programming status bit NVMPS = 1 and write counter WRCNTS < 63). If device configuration is given, the required configuration values shall be written to the registers using SPI, followed by a correct CRC value written into the MTPNV CRC register. In case of successful MTPNV memory programming a system reset is generated within 80 ms. Otherwise the write counter is increased and the device needs to be configured again with a valid configuration and CRC value.

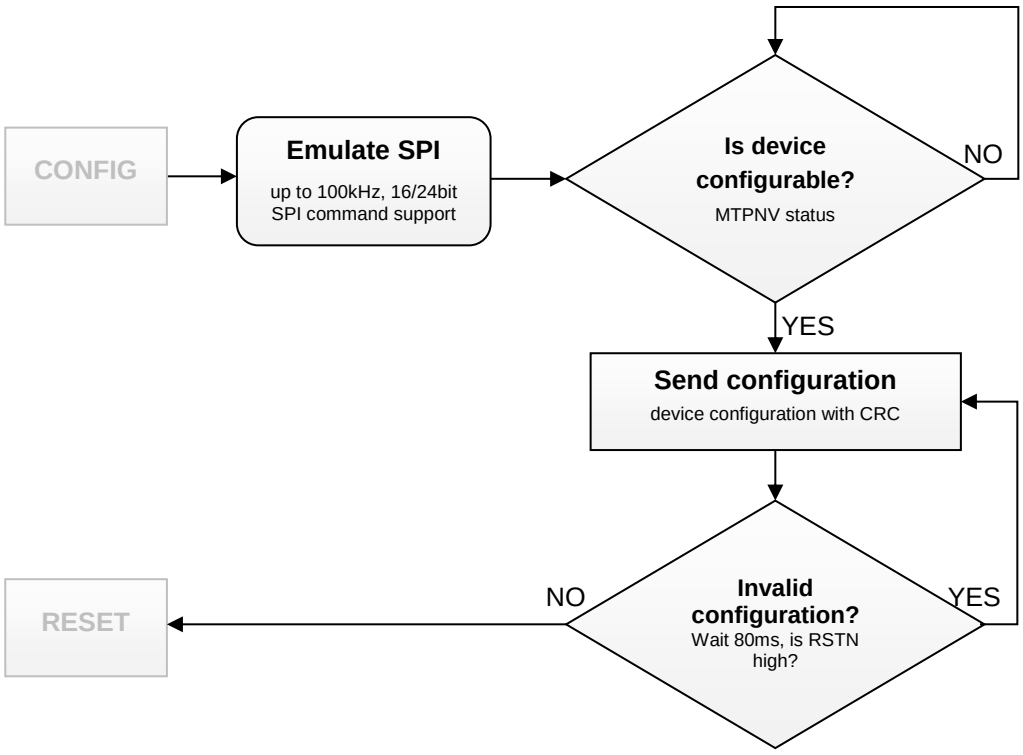


Fig 40. Device configuration flow in CONFIG mode

10.3 Normal operation

During normal operation different operational modes can be set. Four basic modes are supported by the software, transitions between them should follow the operational modes diagram and mode control hints (see chapter 5.1). Switching between these modes is done via EN and STBN with appropriate delay times. Transitions between some of the modes are not directly possible (see chapter 5.1).

In NORMAL mode the device is used to transmit and receive data via the LIN bus (if enabled). Both, the voltage regulator and LIN transmitter (if enabled) are turned on.

In STANDBY mode the LIN transmitter is switched off and the device has very low current consumption. The STANDBY mode is also entered while SLEEP mode is requested, but is not enabled (DISSLP bit = 1).

In SLEEP mode both the LIN transmitter and the VCC voltage regulator supplying the microcontroller are switched off providing extremely low power consumption. Remote wake-up detection and local wake-up are active, if enabled during configuration.

PORT mode is used after power-on to detect the configuration status or after wake-up to detect the wake-up source or to read the WAKE1/2 pin input state or to clear limp home (if enabled).

In a typical application the LIN slave is in one of the low power modes (STANDBY, or SLEEP) most of the time and is woken-up by the LIN master over the the LIN bus. The device goes back to low power mode usually by a LIN go-to-sleep command from the master, or when the LIN bus idle timeout occurs (no LIN bus traffic for a defined period of time).

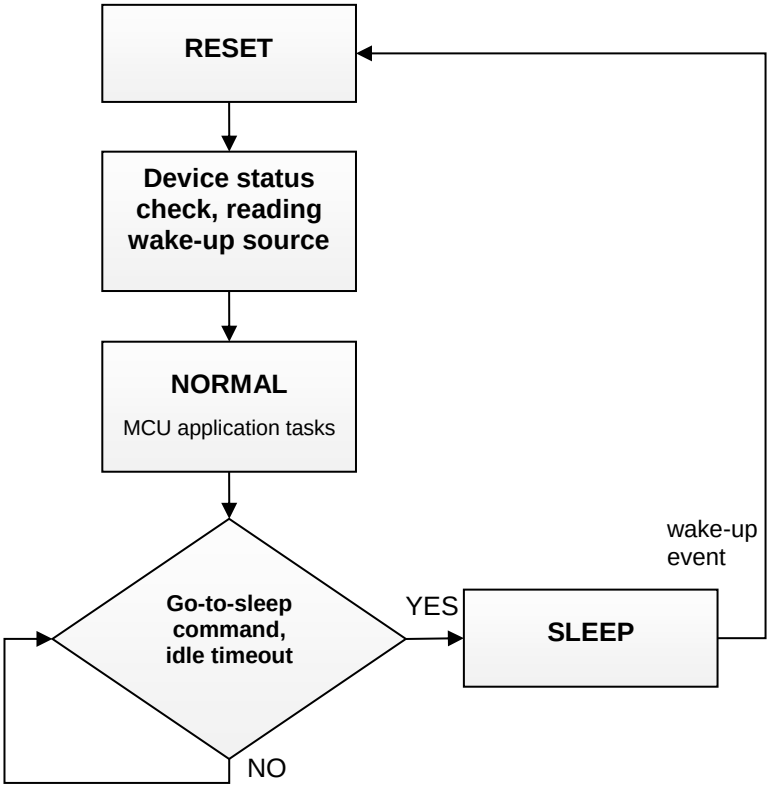


Fig 41. Normal operation flow

11. Software example

The software example is intended to help the customer getting started the software development when the TJA1128 is applied.

For the TJA1128 you can find on NXP DocStore (NDA required) software source code for example driver and an example project:

NXP DocStore: In-Vehicle Networking → LIN → TJA1128

11.1 Software example driver description

This chapter briefly describes the example software driver. Detailed description of the driver functions and the functions parameters can be found in the driver files.

11.1.1 Driver structure

The SW driver consists of multiple files. In Table 15 an overview of the SW driver files is listed

Table 15. Software driver files

File name	Description
nxp_tja1128.c/.h	TJA1128 device related configuration and mode control functions
nxp_tja1128_registers.h	TJA1128 device register map
nxp_tja1128_defines.h	generic defined types and constants

The SW driver utilizes MCU peripherals such as CPU delay time, SPI, UART and GPIO control. The user is responsible for the definition of the functions related to the MCU used in the application. These functions are declared in nxp_tja1128.c file in the following way:

```
extern void CPU_DelayUs(uint32_t us);
extern void GPIO_InitAsSpi(void);
extern void GPIO_InitAsUart(void);
extern bool GPIO_ReadPin(uint8_t pinPort, uint8_t pinNumber);
extern void GPIO_WritePin(uint8_t pinPort, uint8_t pinNumber, bool setClear);
extern Std_ReturnType SPI_Send(uint8_t spiDevice, uint8_t numOfBytes, uint8_t*
sendDataPtr, uint8_t* rcvDataPtr);
extern Std_ReturnType UART_Send(uint8_t uartDevice, uint8_t numOfBytes, uint8_t*
sendDataPtr, uint8_t* rcvDataPtr);
```

11.1.2 Driver functions

The nxp_tja1128.c/.h files contain functions related to the device configuration, operational mode handling and device status.

Table 16. Software driver functions from nxp_tja1128.c/.h

Function	Description
TJA1128_Init	checks if device is configured, and if not, initializes device configuration
TJA1128_RWRegister	creates command to send using SPI driver send/receive function
TJA1128_GetWakeupReason	reads wake-up event source
TJA1128_SetOperationalMode	sets the operational mode of the device
TJA1128_WatchdogTrigger	resets the watchdog timer

12. Abbreviations

Table 17. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
CRC	Cyclic Redundancy Check
ECU	Electronic Control Unit
EMC	Electro Magnetic Compatibility
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
FMEA	Failure Mode and Effect Analysis
GPI	General Purpose Input
HVMPO	High Voltage Multi Purpose Output
LDO	Low Dropout Regulator
LED	Light Emitting Diode
LIN	Local Interconnect Network
MCU	Microcontroller
MLCC	Multi-layer Ceramic Capacitor
MTPNV	Multi Time Programmable Non Volatile
NMOS	N-Metal-Oxide-Semiconductor
PCB	Printed Circuit Board
SBC	System Basic Chip
SPI	Serial Peripheral Interface
SW	Sofware

13. References

[1] Product data sheet, TJA1128, LIN Mini System Basis Chip, NXP Semiconductors

[2] International Standard ISO 9141, Road Vehicles – Diagnostic Systems – CARB requirement for interchange of digital information, International Standardization Organization, 1994

[3] International Standard ISO 14230-1, Road Vehicles – Diagnostic communication over K-Line (DoK-Line) – Part 1: Physical layer, International Standardization Organization, 2012

[4] International Standard ISO 17987-4, Road vehicles – Local Interconnect Network (LIN) – Part 4: Electrical physical layer (EPL) specification 12 V/24 V, International Standardization Organization, 2016

[5] Product data sheet PNS40010ER, 400 V, 1 A high power density, standard switching time PN-rectifier, Nexperia

[6] Product data sheet, BAS21H, Single high-voltage switching diode, Nexperia

[7] Product data sheet, S07D, Single high-voltage switching diode, Vishay

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