Freescale RF Devices in **Laser Application**

AUG.2015

freescale™

External Use

Agenda

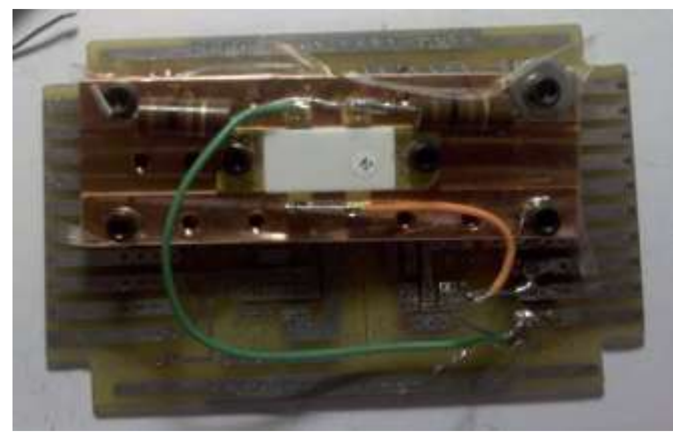
- Rugged device UIS test
- LDMOS UIS test result vs VDMOS
- Mismatch test on dummy mismatch load
- CO_2 SLAB laser test driven by Freescale devices

UIS Testing of Freescale RF Power Transistors

Unclamped Inductive Switching - The Equipment

- Individual test sockets or automated handlers can be used with the ITC55100B Tester, Has GPIB interface
- Uses high speed 16bit DAC for better accuracy
- Can test Single and Dual N/P Channel or a combination
- Capable of a Setting the Supply Voltage (Vdd) from 10 to 150V in 1 Volt steps
- Capable of switching up to 200A
- Test up to an Avalanche Voltage of 2500V
- Capable of EAS, EAR, RPF (repetitive pulse to failure), Up to 20 Joules

ITC55100B Tester



Mounting the Device

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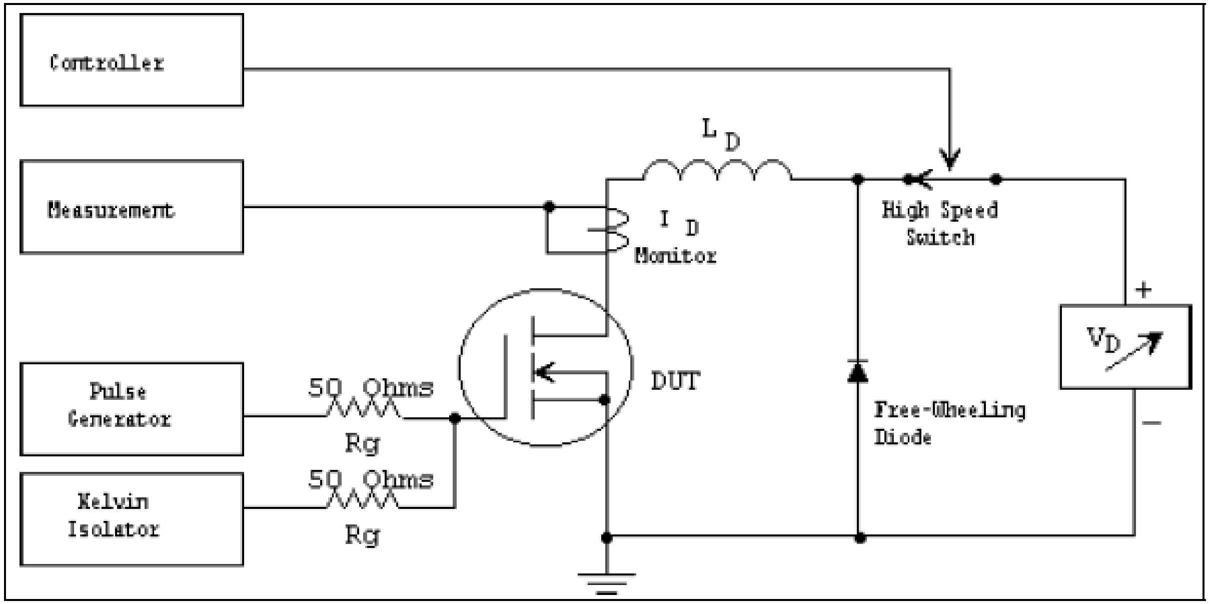
Unclamped Inductive Switching Setup – Sequence of Events

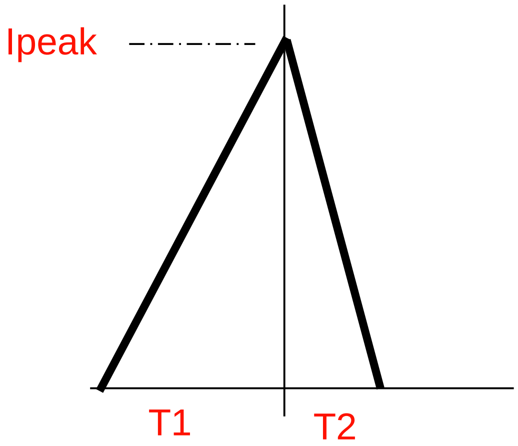
1. Kelvin Continuity check of all three device leads and a device leakage test at zero gate bias
2. If Passed, the high-speed switch closes and drain voltage (VD) is applied to the inductor.
3. Tester controller then activates the pulse generator to turn on the DUT through the limiting and terminating resistor Rg.
4. After Id reaches the peak current setting the gate is forced to 0 volts.
5. The high speed switch opens back up at the Drain allowing the voltage to spike.
6. Drain Voltage and Current is monitored and recorded until either the set test time (Max T2) elapses or the Drain voltage drops below the initial VD setting
7. The final Energy is calculated by; E = ½*L*I^2, where L is the inductance value and I is the peak current within the inductor.

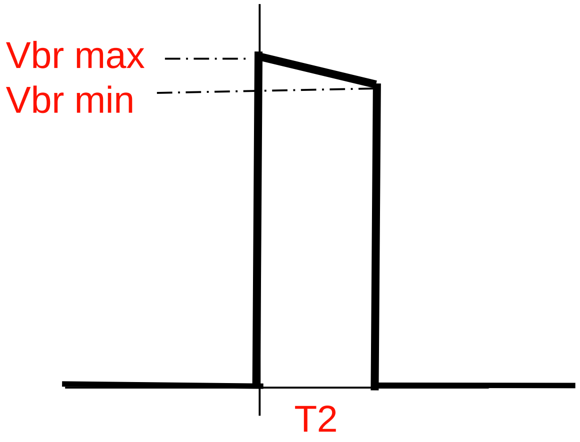


Component	
Ld	2mH

Sketch of Current and Voltage Waveforms

- T1 is the time that it takes the device to charge up to Peak current
- T2 is the time it take for the DUT to discharge the current stored in the inductor

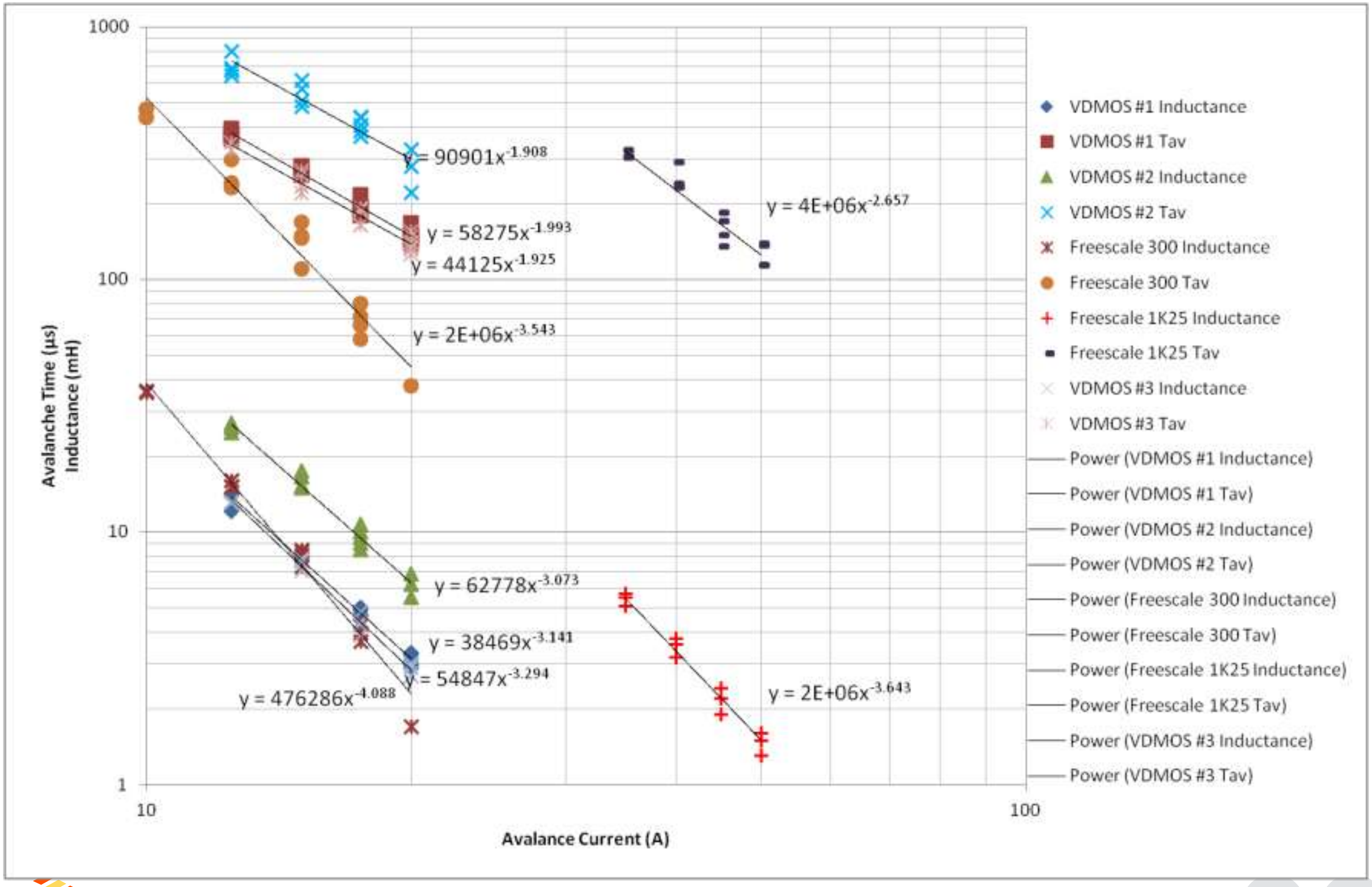




High Power RF LDMOS UIS Test Procedure

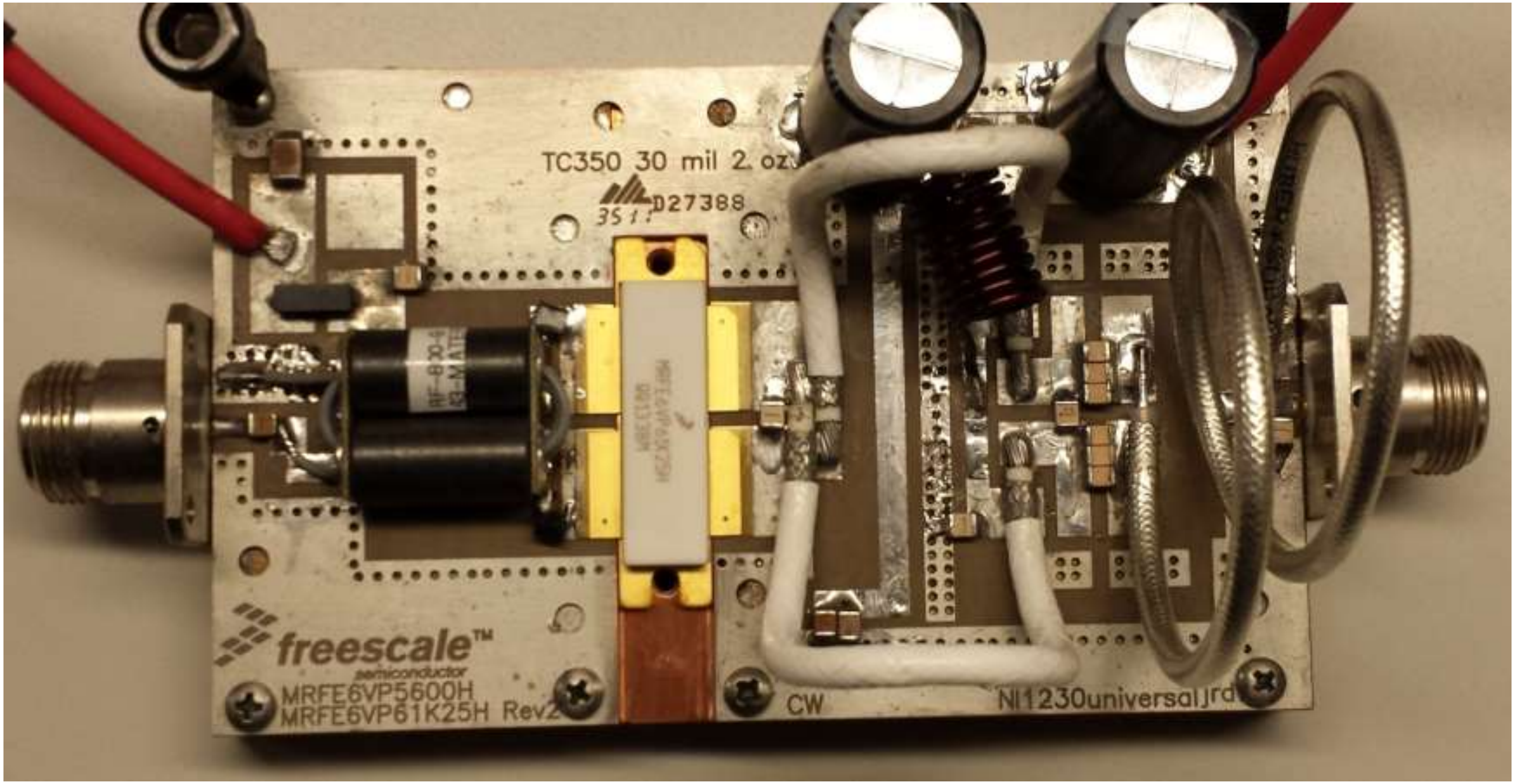
- Linearly increase the avalanche energy by stepping the inductor value at constant drain current until device failure.
  - Drain Current (IAV)
    - MRFE6VP6300HR3 - 10, 12.5, 15, 17.5, and 20 A.
    - MRFE6VP61K25HR6 - 35, 40, 45, and 50 A.
  - L_{init} – 0.1 mH, inductance increases by 0.1 mH.
  - Duty Cycle – 1%.
  - Device Rated Drain Voltage – 130 V
  - Inductor Charging Voltage – 125 V.
  - Gate Drive Voltage – 10 V.
- Each device of the push-pull pair was tested independently.
- An oscilloscope was used to observe the front panel gate drive and drain current monitors.

UIS Test Results - Freescale



MRFE6VP61K25 Mismatch Load Test at 64MHz

MRFE6VP61K25 64MHz Demo

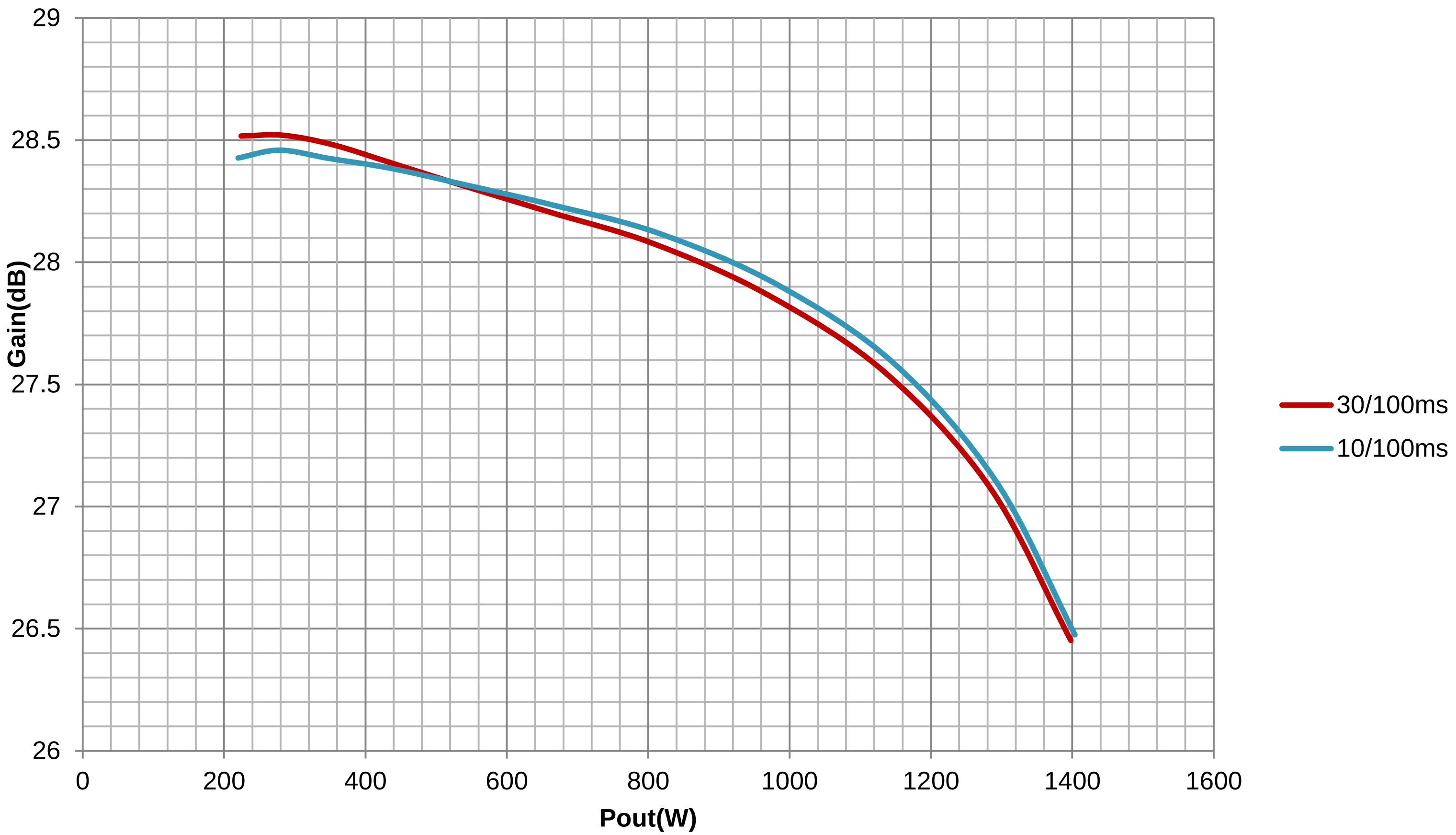


CW Performance

Part ID	Freq (MHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Gain (dB)	IRL (dB)	H2 (dB)	H3 (dB)	Eff (%)	Vds (V)	IdSupply (A)	Vgs (V)	IdSupplyq (A)
CW	64	34.0	60.9	1231.1	26.9	-13.5	-28.1	-19.3	78.7	50.0	31.3	2.4	0.1
CW	64	33.0	60.3	1083.2	27.3	-13.6	-27.8	-19.2	74.1	50.0	29.2	2.4	0.1
CW	64	32.0	59.7	923.2	27.6	-13.8	-27.5	-19.2	68.8	50.0	26.8	2.4	0.1
CW	64	31.0	58.9	767.9	27.8	-14.1	-27.1	-19.3	63.2	50.0	24.3	2.4	0.1
CW	64	30.0	58.0	633.0	28.0	-14.3	-26.8	-19.8	57.9	50.0	21.9	2.4	0.1

- The CW Pout is >1200W at 34dBm input, with better than -18dBc harmonics and 78%.

Pulse data—50ohm load



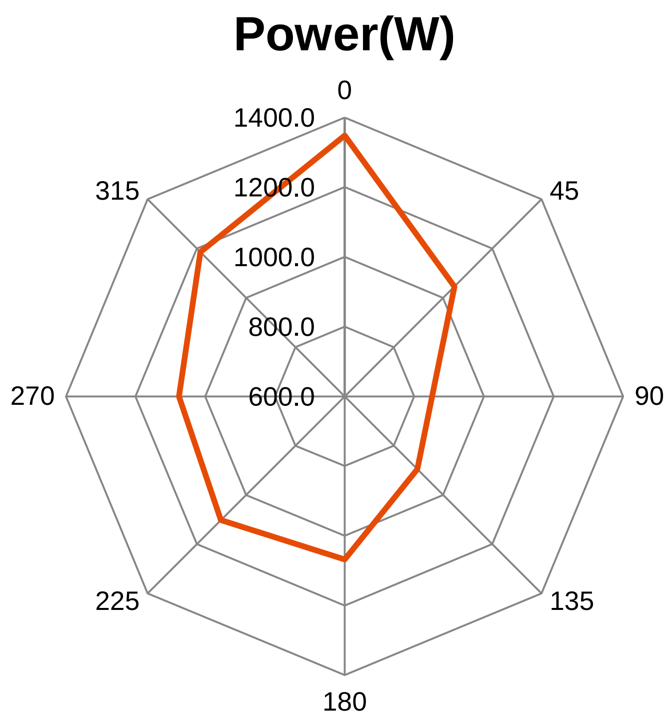
- Performance consistent when pulse increased from 10/100ms to 30/100ms;
- The mismatch resistor 100Ohm can handle 100W average power. All the mismatch data is collected under 10/100ms pulse.

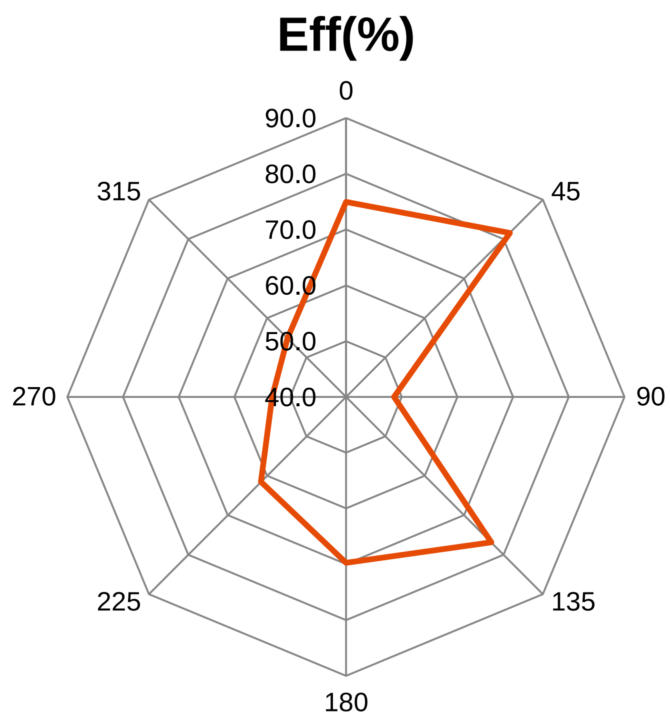
Mismatch data—VSWR=2:1

Phase(degree)	Freq (MHz)	Pin (dBm)	Pout (dBm)	Gain (dB)	IRL (dB)	Period (msec)	Width (msec)	DCycle (%)	Eff (%)	Vds (V)	Idmm (A)	Pout (W)
0	64	34.0	61.3	27.3	-14.1	100.0	10.0	10.0	75.0	50.3	35.7	1348.3
45	64	34.0	60.2	26.2	-12.1	100.0	10.0	10.0	81.6	50.0	25.6	1045.7
90	64	34.0	59.3	25.3	-13.5	100.0	10.0	10.0	48.6	50.0	35.0	850.9
135	64	34.0	59.5	25.5	-16.7	100.0	10.0	10.0	76.9	50.2	23.2	895.0
180	64	34.0	60.3	26.3	-16.5	100.0	10.0	10.0	69.8	50.0	30.6	1067.6
225	64	34.0	60.4	26.4	-16.5	100.0	10.0	10.0	61.5	50.1	35.7	1102.3
270	64	34.0	60.3	26.3	-17.2	100.0	10.0	10.0	53.2	49.9	40.5	1075.2
315	64	34.0	60.7	26.7	-16.7	100.0	10.0	10.0	54.8	50.4	42.9	1185.2

- Pout>800W and eff>45% under VSWR=2:1 all phase mismatch.

Mismatch data—VSWR=2:1





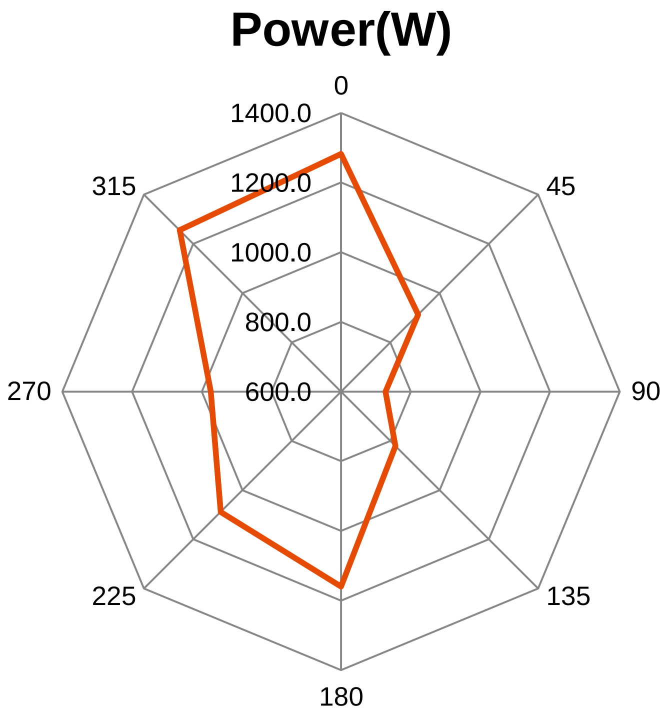
- Pout>800W and eff>45% under VSWR=2:1 all phase mismatch

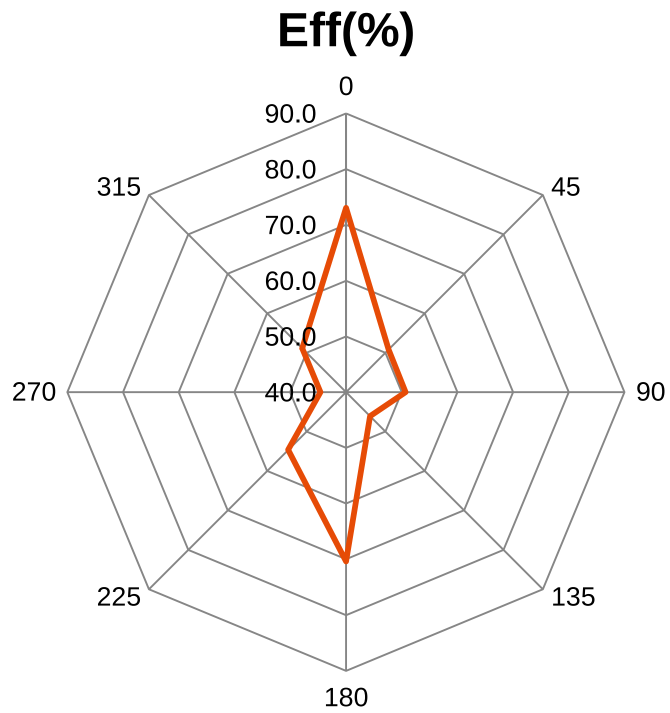
Mismatch data—VSWR=3:1

Phase(degree)	Freq (MHz)	Pin (dBm)	Pout (dBm)	Gain (dB)	IRL (dB)	Period (msec)	Width (msec)	DCycle (%)	Eff (%)	Vds (V)	Idmm (A)	Pout (W)
0	64	34.0	61.1	27.0	-12.5	100.0	10.0	10.0	73.0	50.3	50.3	1282.3
45	64	34.0	59.6	25.6	-13.3	100.0	10.0	10.0	50.8	50.0	50.0	912.2
90	64	34.0	58.6	24.6	-9.4	100.0	10.0	10.0	50.7	50.0	50.0	727.4
135	64	34.0	59.1	25.1	-16.3	100.0	10.0	10.0	46.1	50.0	50.0	820.7
180	64	34.0	60.6	26.6	-17.7	100.0	10.0	10.0	70.4	50.2	50.2	1160.1
225	64	34.0	60.4	26.4	-18.1	100.0	10.0	10.0	54.7	50.1	50.1	1089.2
270	64	34.0	59.9	25.9	-16.3	100.0	10.0	10.0	44.5	49.9	49.9	974.3
315	64	34.0	61.0	27.0	-11.1	100.0	10.0	10.0	51.1	50.5	50.5	1255.7

- Pout>700W and eff>40% under VSWR=3:1 all phase mismatch.

Mismatch data—VSWR=3:1





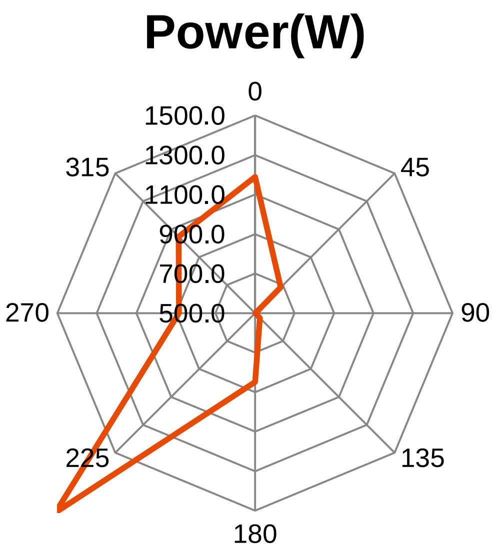
- Pout>700W and eff>40% under VSWR=3:1 all phase mismatch

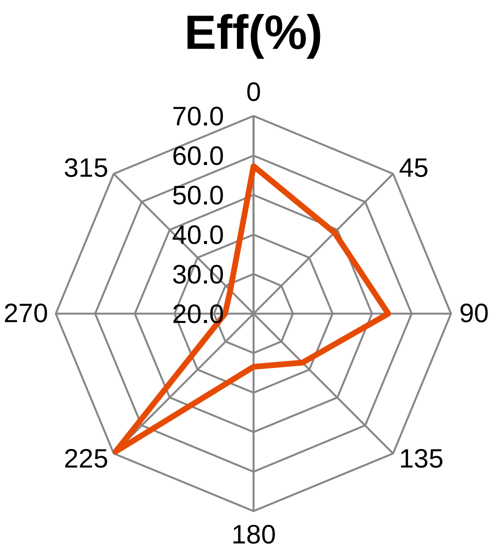
Mismatch data—VSWR=6:1

Phase(degree)	Freq (MHz)	Pin (dBm)	Pout (dBm)	Gain (dB)	IRL (dB)	Period (usec)	Width (usec)	DCycle (%)	Eff (%)	Vds (V)	Idmm (A)	Pout (W)
0	64	34.0	60.8	26.8	-8.1	120.0	12.0	10.0	57.3	50.0	41.5	1189.6
45	64	34.0	58.4	24.4	-8.3	120.0	12.2	10.1	49.0	50.0	28.0	684.7
90	64	34.0	57.0	23.0	-9.3	120.0	12.1	10.1	54.1	50.0	18.6	503.2
135	64	34.0	57.3	23.3	-11.8	120.0	12.1	10.0	37.5	50.0	28.5	534.4
180	64	34.0	59.3	25.3	-15.9	119.8	12.0	10.0	33.5	50.0	50.7	848.8
225	64	34.0	62.9	28.9	-15.2	120.1	12.1	10.1	69.3	50.0	55.6	1928.0
270	64	34.0	59.5	25.5	-15.7	120.0	11.9	9.9	27.2	50.0	65.1	884.7
315	64	34.0	60.2	26.2	-12.6	120.0	11.8	9.8	28.3	50.0	74.1	1047.4

- *Note :The data @ 225 degree is not accurate, due to the bad harmonics.*

Mismatch data—VSWR=6:1





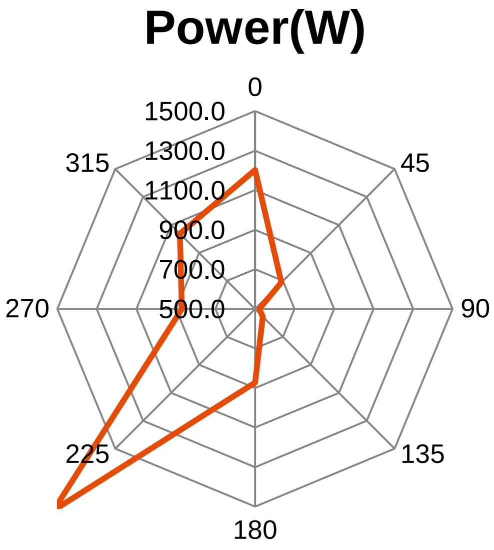
- *Note :The data @ 225 degree is not accurate, due to the bad harmonics.*

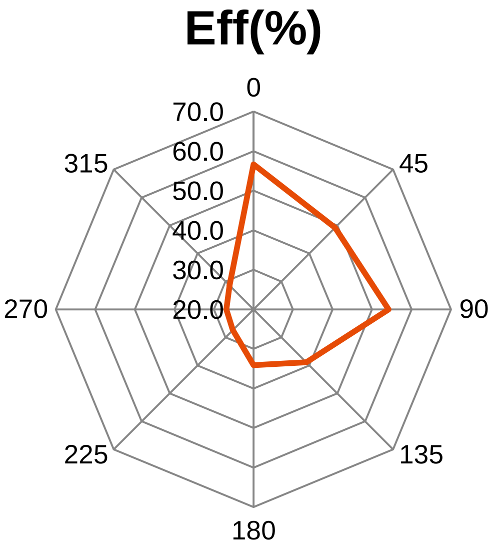
Mismatch data—VSWR=8:1

Phase(degree)	Freq (MHz)	Pin (dBm)	Pout (dBm)	Gain (dB)	IRL (dB)	Period (usec)	Width (usec)	DCycle (%)	Eff (%)	Vds (V)	Idmm (A)	Pout (W)
0	64	34.0	60.8	26.8	-8.1	120.0	12.1	10.1	56.6	50.0	42.4	1201.4
45	64	34.0	58.4	24.4	-8.4	120.0	12.2	10.1	49.2	50.0	28.0	689.9
90	64	34.0	57.2	23.2	-9.4	120.0	12.2	10.2	54.2	50.0	19.3	522.3
135	64	34.0	57.5	23.5	-11.9	120.0	12.2	10.2	39.0	50.0	28.6	556.3
180	64	34.0	59.4	25.4	-15.9	120.1	11.9	9.9	34.1	50.0	51.1	872.4
225	64	34.0	62.9	28.9	-15.3	119.9	4.7	3.9	27.4	50.0	141.7	1940.9
270	64	34.0	59.4	25.4	-15.6	120.1	11.9	9.9	26.8	50.0	64.9	870.2
315	64	34.0	60.2	26.1	-12.8	120.0	11.8	9.9	28.6	50.0	72.6	1037.5

- *Note :The data @ 225 degree is not accurate, due to the bad harmonics.*

Mismatch data—VSWR=8:1

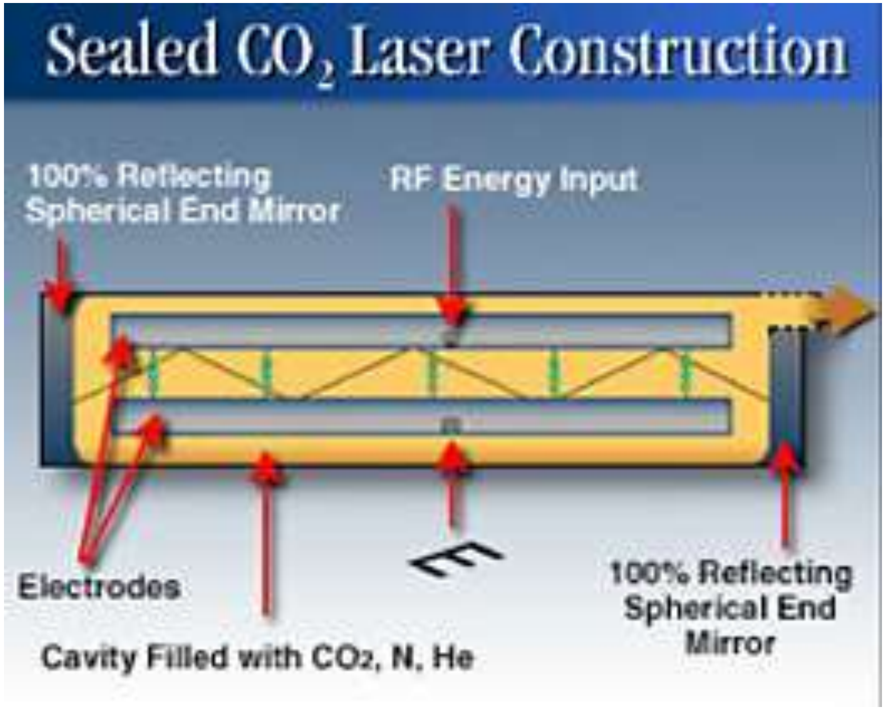




- *Note :The data @ 225 degree is not accurate, due to the bad harmonics.*

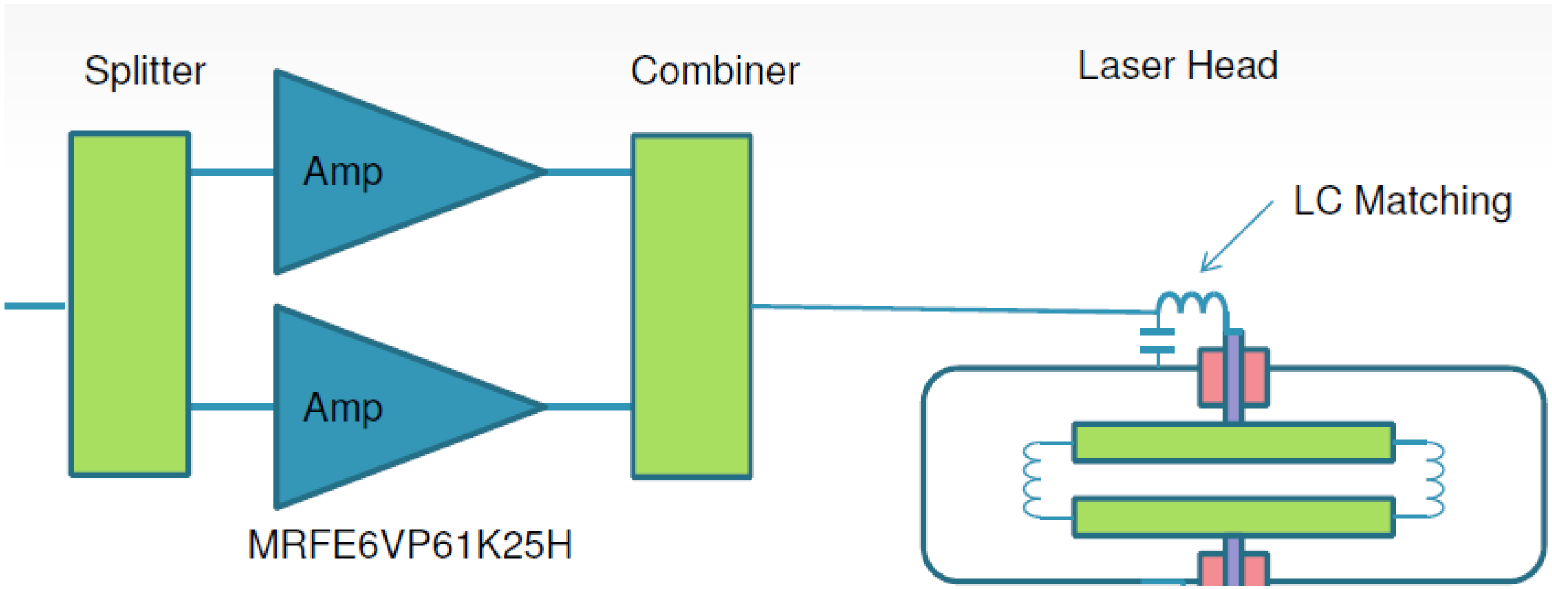
CO_2 SLAB LASER Driven by MRFE6VP61K25 RF Module

Laser from Universal Laser, Inc:

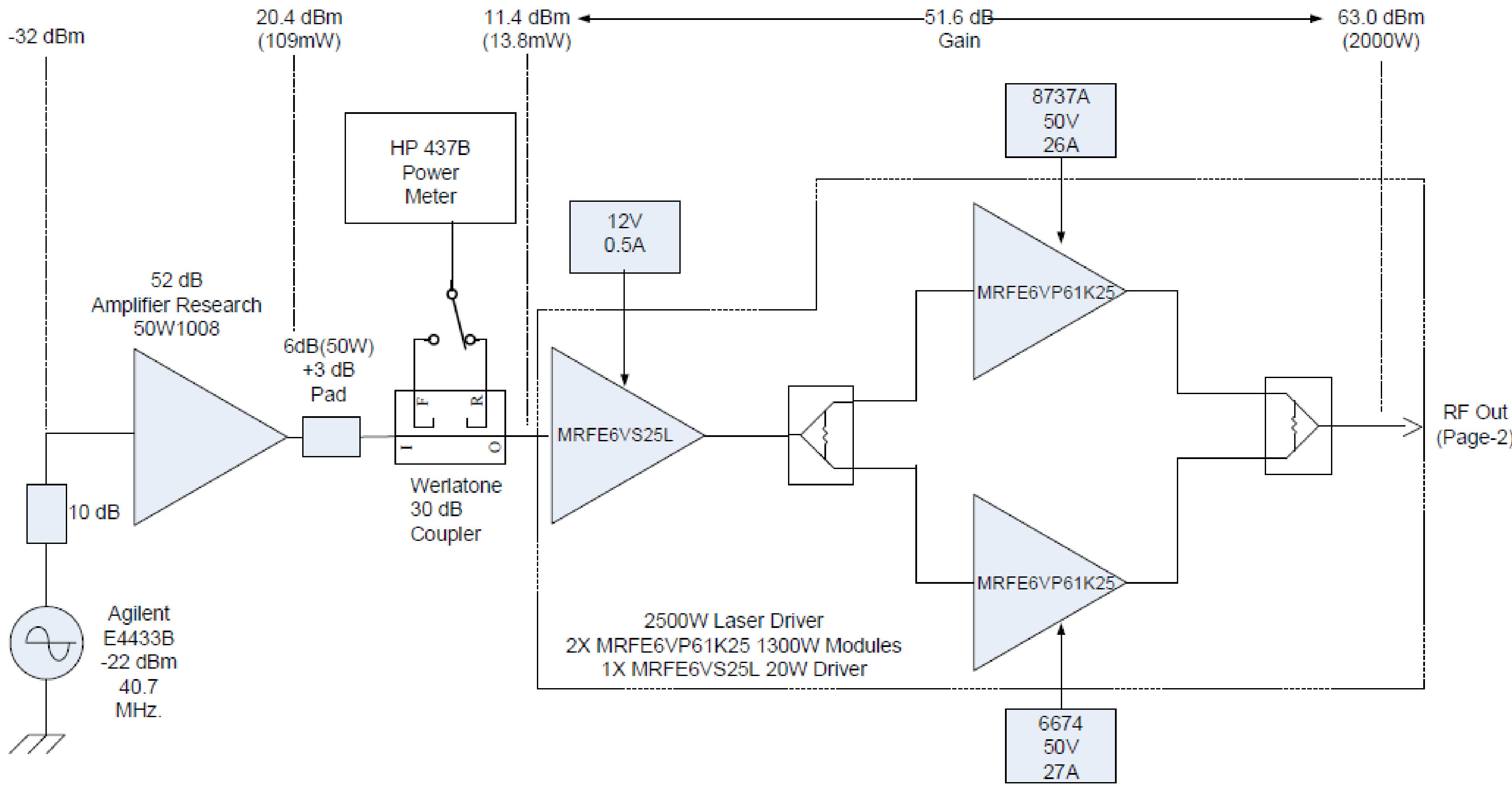


200W Optical Power from laser

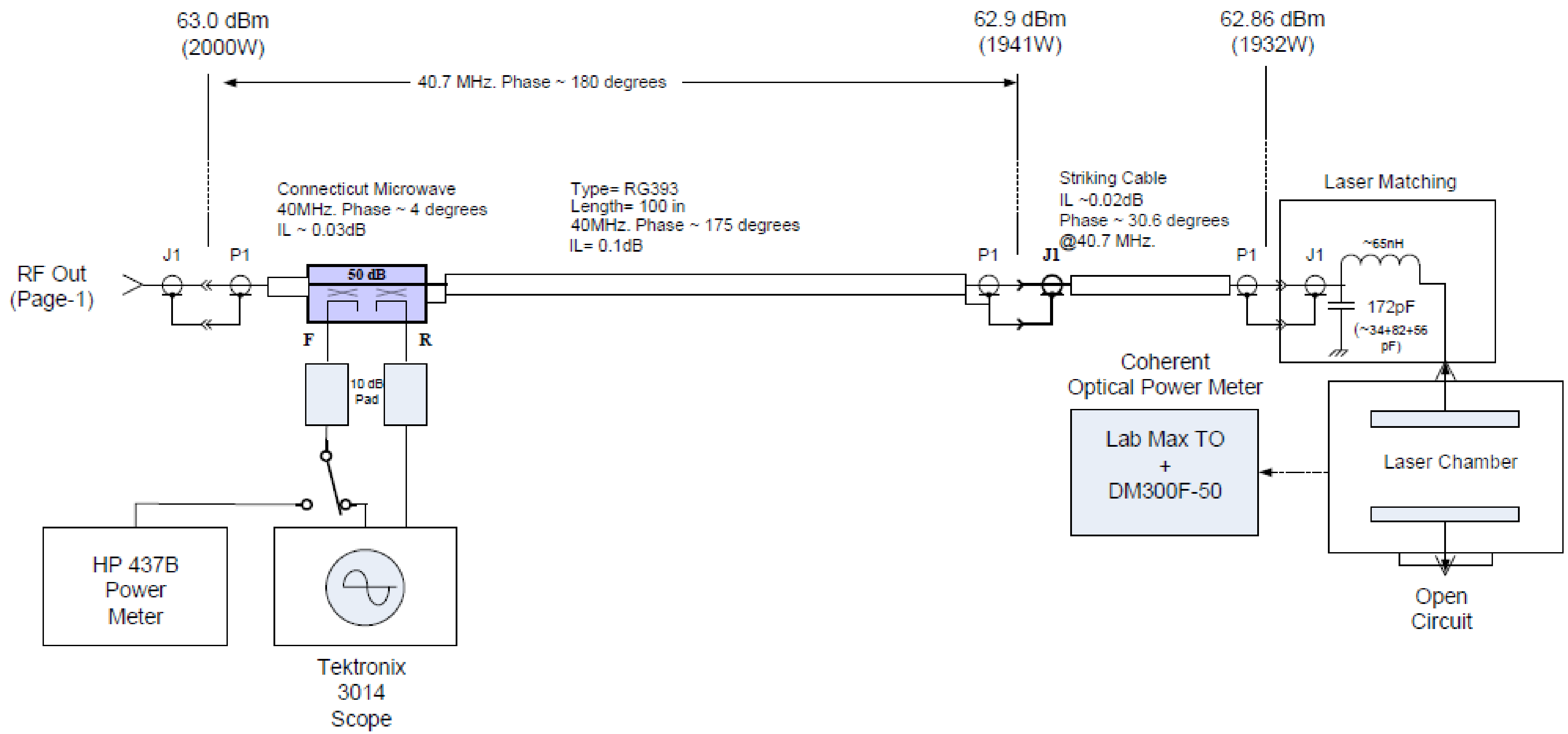
Combining Topology:



Test Setup: Diagram 1



Test Setup: Diagram 2



Laser Strike:

Vforward (Yellow)
Vreflected (Blue)

199W of Optical Output Power

Test Data: Freescale 2700W Laser Driver 50Ω

Part ID	Freq (MHz)	Pin (W)	Pin (dBm)	Pout (W)	Po (dBm)	Gain (dB)	IRL (dB)	Eff (%)	Vd (V)	Shunt (A)	50V I2 (A)
UVL2	40	0.0164	12.1	1002.3	60.0	47.87	-5.8	51.6	50.0	18.91	19.91
UVL2	40	0.0179	12.5	1101.5	60.4	47.88	-6.07	53.2	50.0	20.22	21.22
UVL2	40	0.0192	12.8	1202.3	60.8	47.96	-6.24	55.1	50.0	21.32	22.32
UVL2	40	0.0206	13.1	1297.2	61.1	48	-6.4	56.9	50.0	22.29	23.29
UVL2	40	0.0219	13.4	1396.4	61.4	48.05	-6.56	58.8	50.0	23.26	24.26
UVL2	40	0.0234	13.7	1503.1	61.8	48.08	-6.73	60.6	50.0	24.32	25.32
UVL2	40	0.0248	13.9	1599.6	62.0	48.1	-6.87	62.2	50.0	25.23	26.23
UVL2	40	0.0263	14.2	1698.2	62.3	48.1	-7.02	63.8	50.0	26.12	27.12
UVL2	40	0.028	14.5	1803.0	62.6	48.09	-7.17	65.5	50.0	27.03	28.03
UVL2	40	0.0296	14.7	1896.7	62.8	48.06	-7.32	66.9	50.0	27.84	28.84
UVL2	40	0.0317	15.0	2004.5	63.0	48.01	-7.47	68.6	50.0	28.74	29.74
UVL2	40	0.0321	15.1	2094.1	63.2	48.14	-7.47	70.4	50.0	29.24	30.24
UVL2	40	0.0345	15.4	2197.9	63.4	48.04	-7.65	71.9	50.0	30.07	31.07
UVL2	40	0.0372	15.7	2301.4	63.6	47.91	-7.83	73.3	50.0	30.89	31.89
UVL2	40	0.0401	16.0	2393.3	63.8	47.76	-7.96	74.5	50.0	31.64	32.64
UVL2	40	0.044	16.4	2494.6	64.0	47.54	-8.27	75.8	50.0	32.40	33.40
UVL2	40	0.0498	17.0	2600.2	64.2	47.18	-8.64	77.1	50.0	33.21	34.21
UVL2	40	0.0581	17.6	2697.7	64.3	46.67	-8.98	78.2	50.0	33.99	34.99

2700W CW

78%
Efficiency

Test Data: Laser Strike

PW	Sig Gen	Pfor	Pref	I1	I2	Popt
uS	dBm	dBm	dBm	A	A	W
100	-5.56	-25.2	-26.6	3.87	4.2	14.5
200	-5.56	-22.1	-25.8	7	7.4	46
300	-5.56	-20.3	-25.2	9.96	10.4	75
400	-5.56	-19.1	-24.6	12.9	13.5	102
500	-5.56	-18.3	-24.2	15.7	16.4	126
600	-5.56	-17.6	-23.8	18.4	19.1	152
700	-5.56	-16.96	-23.4	21.1	21.8	173
800	-5.56	-16.4	-23	23.7	24.9	192
900	-5.56	-15.9	-22.7	26.1	27	214
992	-5.56	-15.56	-22.4	28.6	29.6	228

228W Optical Power

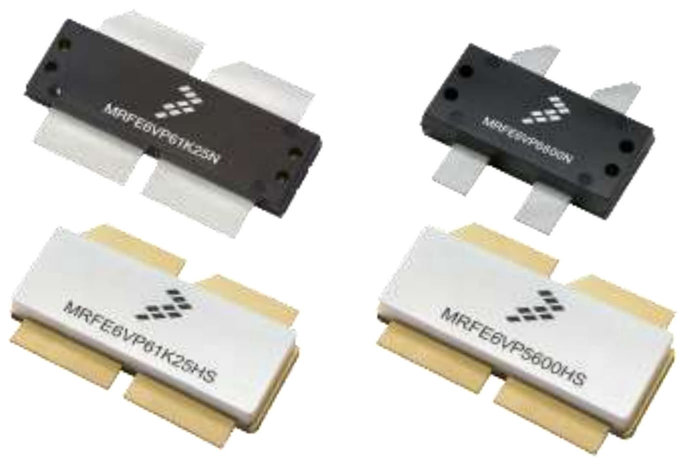
Freescale Lab “Testing”:

ISM (Industrial, Scientific, Medical) and FM/VHF Roadmaps

Freescale RF 2015 Strategy for ISM applications

- Bring leading-edge rugged transistors in **plastic packages**, adding the 2 industry's highest power devices in plastic package, completing the MRF 'E' Series of Extremely rugged transistors: **5 in ceramic housing and 5 in plastic.**

- **Top benefits of plastic over ceramic**:
  1. Lower thermal resistance (30%), enabling smaller heatsink or better reliability
  2. Tighter dimensional tolerance, enabling assembly automation
  3. Same thermal expansion (copper on copper), enabling better reliability (no mismatch at solder joint)
  4. More power in smaller and lighter package

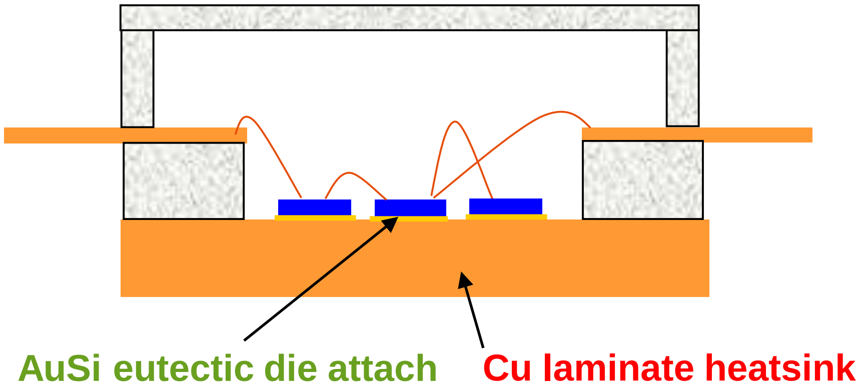


1,250W 600W

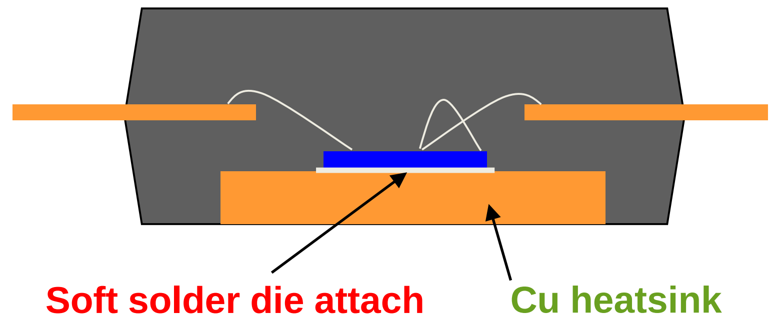
Green: good thermal resistance
Red: poor thermal resistance

How do we achieve this?

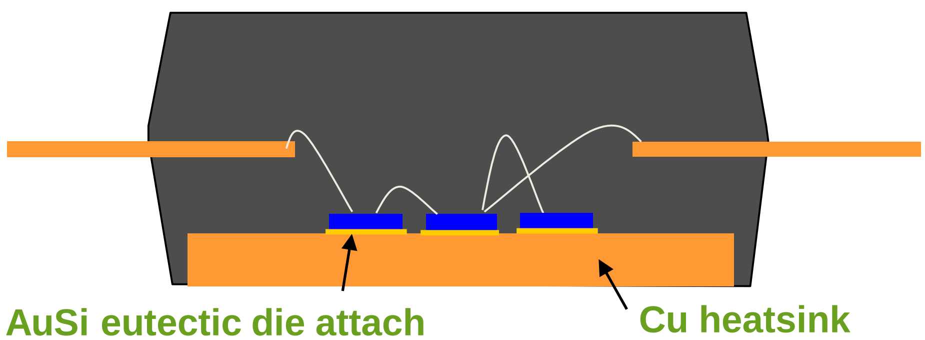
Air Cavity Ceramic (NI)



Traditional Plastic Packages (TO)

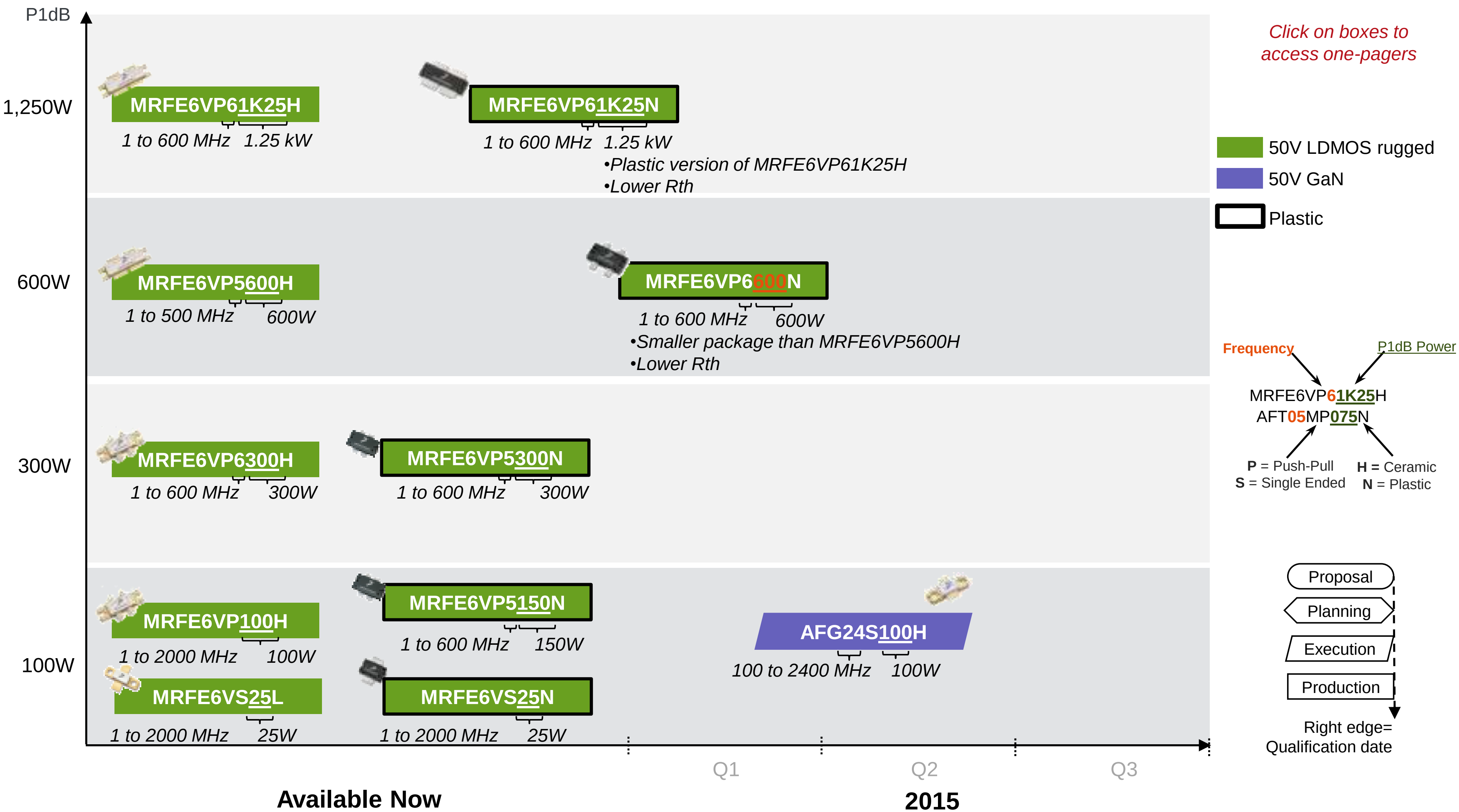


Freescale's OMNI Over Molded plastic



ISM roadmap – Final stage transistors <600 MHz

All watts are CW.



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