Fundamentals of DDR in QorIQ Processing Platforms

AMF-SNT-T1044

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External Use

Session Introduction

Understanding the DDR and memory controller fundamentals is key to a successful selection and design of a DDR interface

- In this session you will learn about:
  - DDR fundamentals
  - DDR4 compared to DDR3
  - QorIQ devices memory controller features
  - QCS DDRv tool main features
- Who would benefit by attending this session?
  - HW, SW and system design engineers planning to implement a DDR interface in their design would benefit from understanding the basics of DDR and memory controller
- Session length is 2 hours

Learning Objectives

- **By completing this training, you will be able to:**
  - Configure and run operate the memory controller in QorIQ devices
  - Decide whether to include DDR4 or DDR3 in your board design
  - Apply the DDR operational information in optimizing your SW application
  - Apply the DDR4 information on your board design
  - Feel more at ease with the DDR interface

Agenda

- **Industry trends**
- Basic DDR SDRAM structure
- DDR3 vs. DDR4 SDRAM differences
- QorIQ DDR4 controller features
- Configurations and validation via QCS DDRv tool

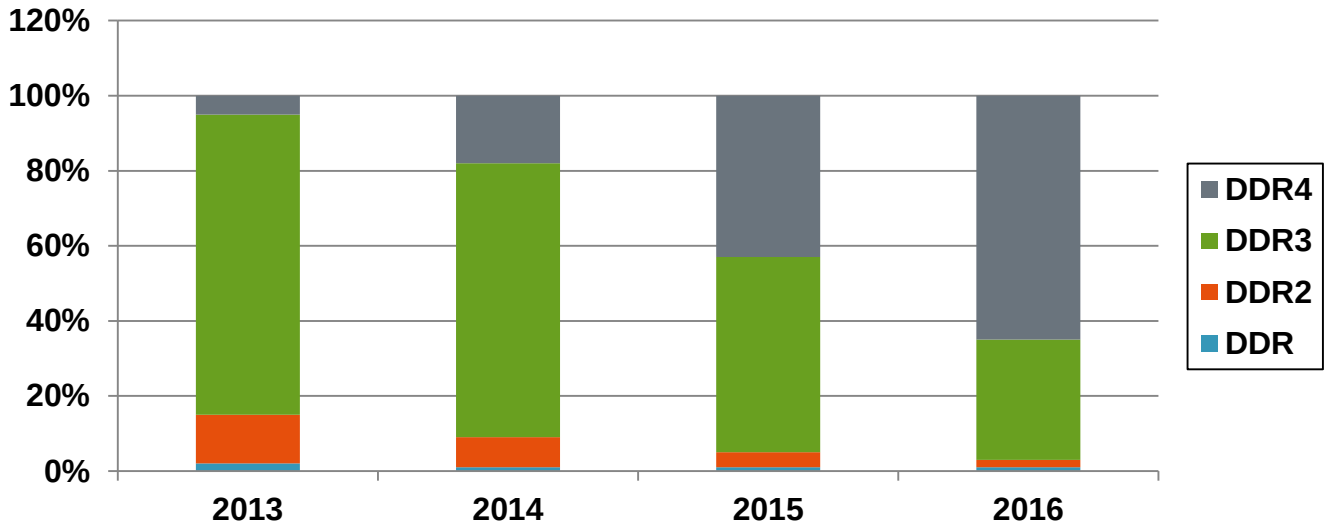
Industry Trend

- The current industry mainstream DRAM product is DDR3/3L. This trend is expected sometime in 2015 when the pricing cross-over is expected to occur
- Almost all Freescale networking devices offer and support DDR3/3L
- DDR4 has been introduced and DRAM vendors ramped production in 2014
- Our first Freescale device with DDR4 support, the T1040, is available today.
  - All future QorIQ products including our newer LS1 parts will support DDR4.

DDR3 and DDR4 – Major Vendors

- Supported by all major memory vendors

DRAM Migration Roadmap



	2013	2014	2015	2016
DDR	2%	1%	1%	1%
DDR2	13%	8%	4%	2%
DDR3	80%	73%	52%	32%
DDR4	5%	18%	43%	65%

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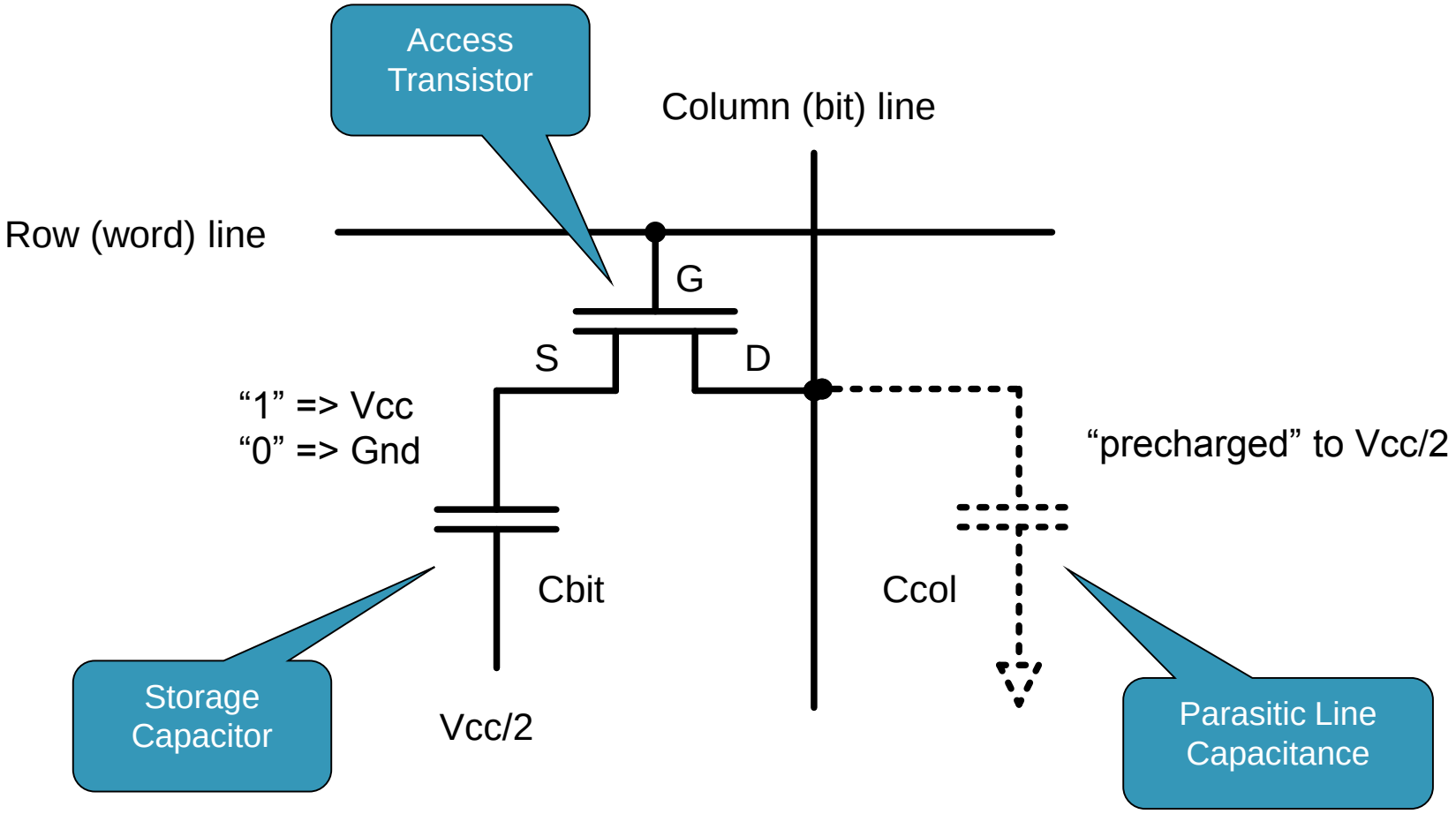
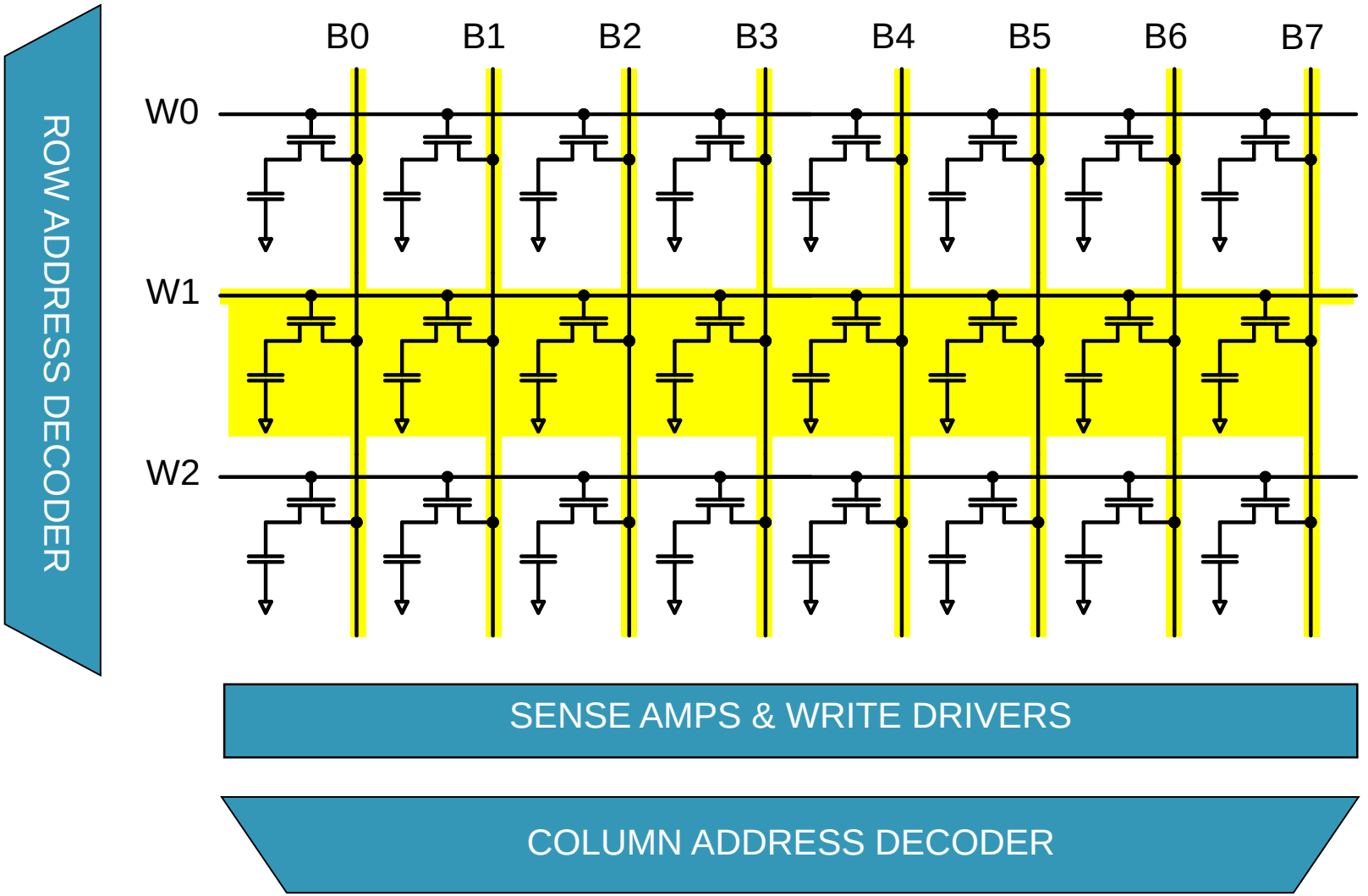
Single Transistor Memory Cell

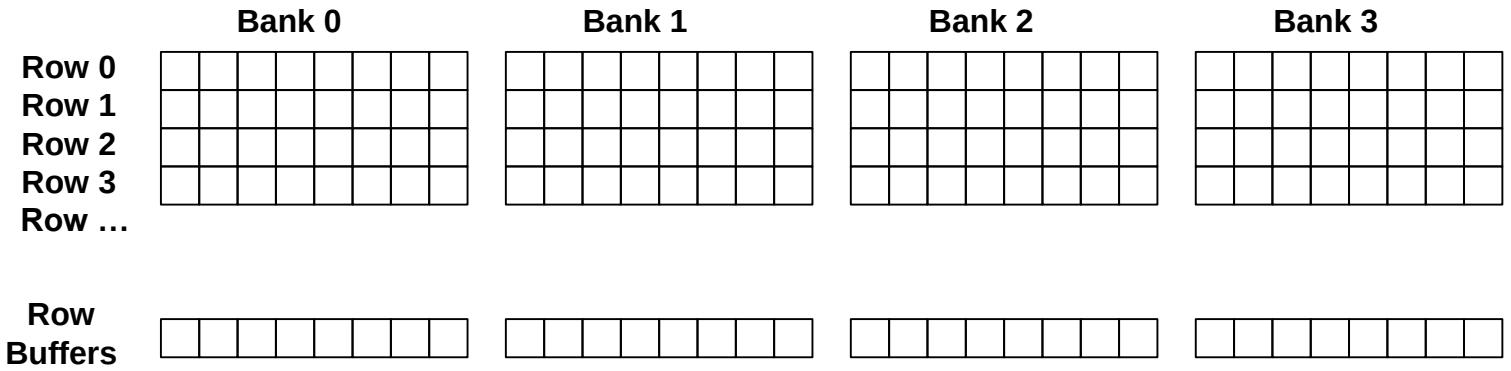


Memory Arrays



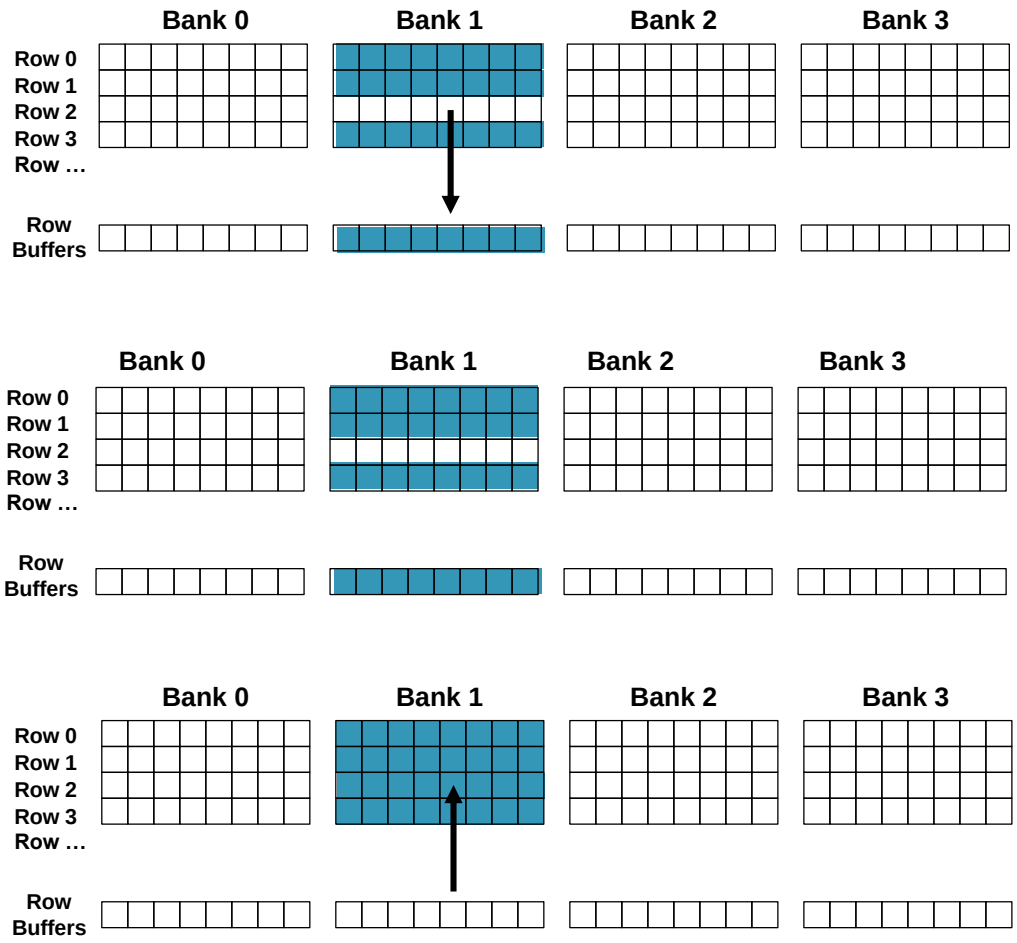
Internal Memory Banks

- Multiple arrays organized into banks
- Multiple banks per memory device
  - DDR3 – 8 banks, and 3 bank address (BA) bits
  - DDR4 -16 banks with 4 banks in each of 4 sub bank groups
  - Can have one active row in each bank at any given time
- Concurrency
  - Can be opening or closing a row in one bank while accessing another bank

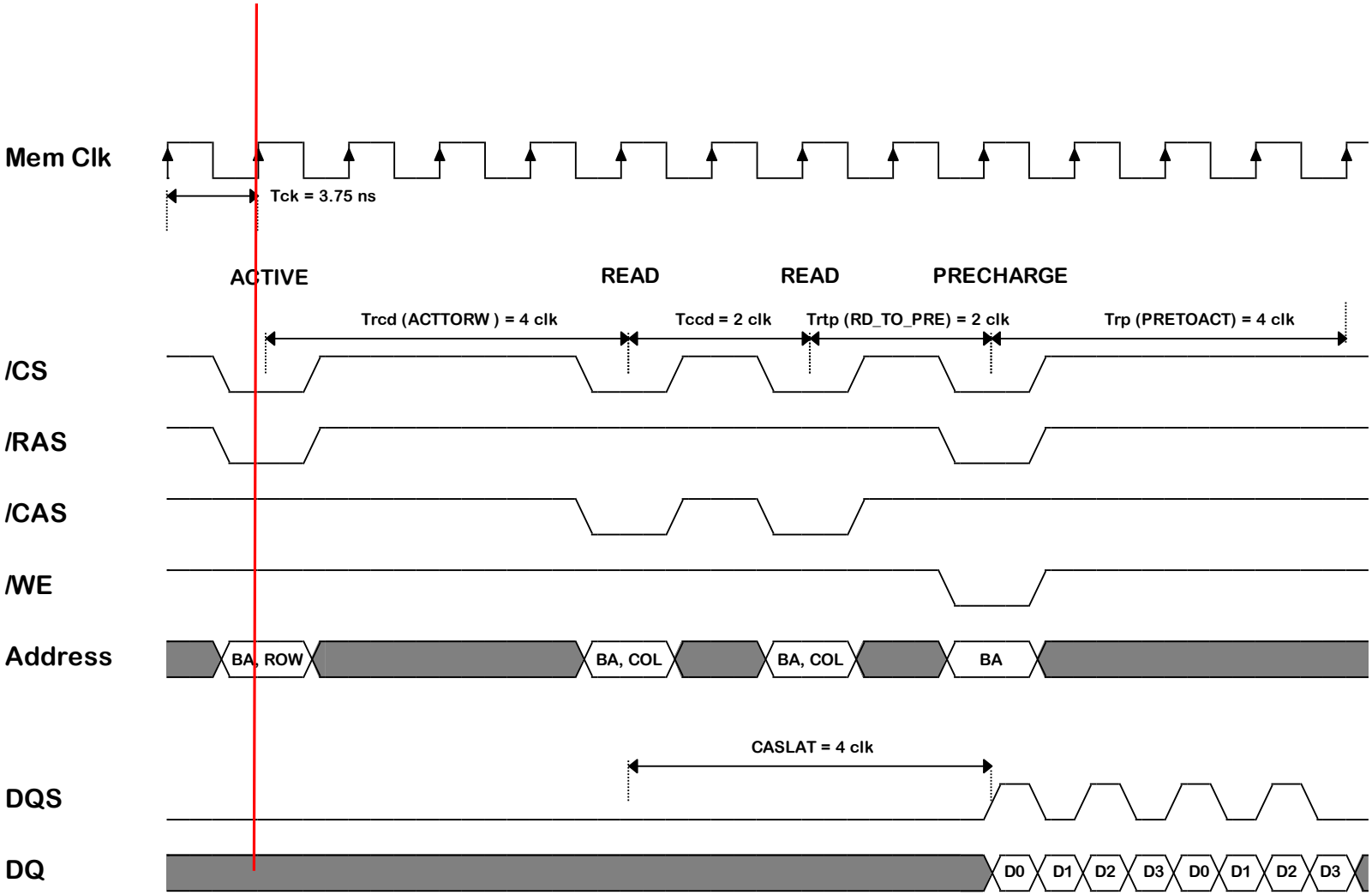


Memory Access

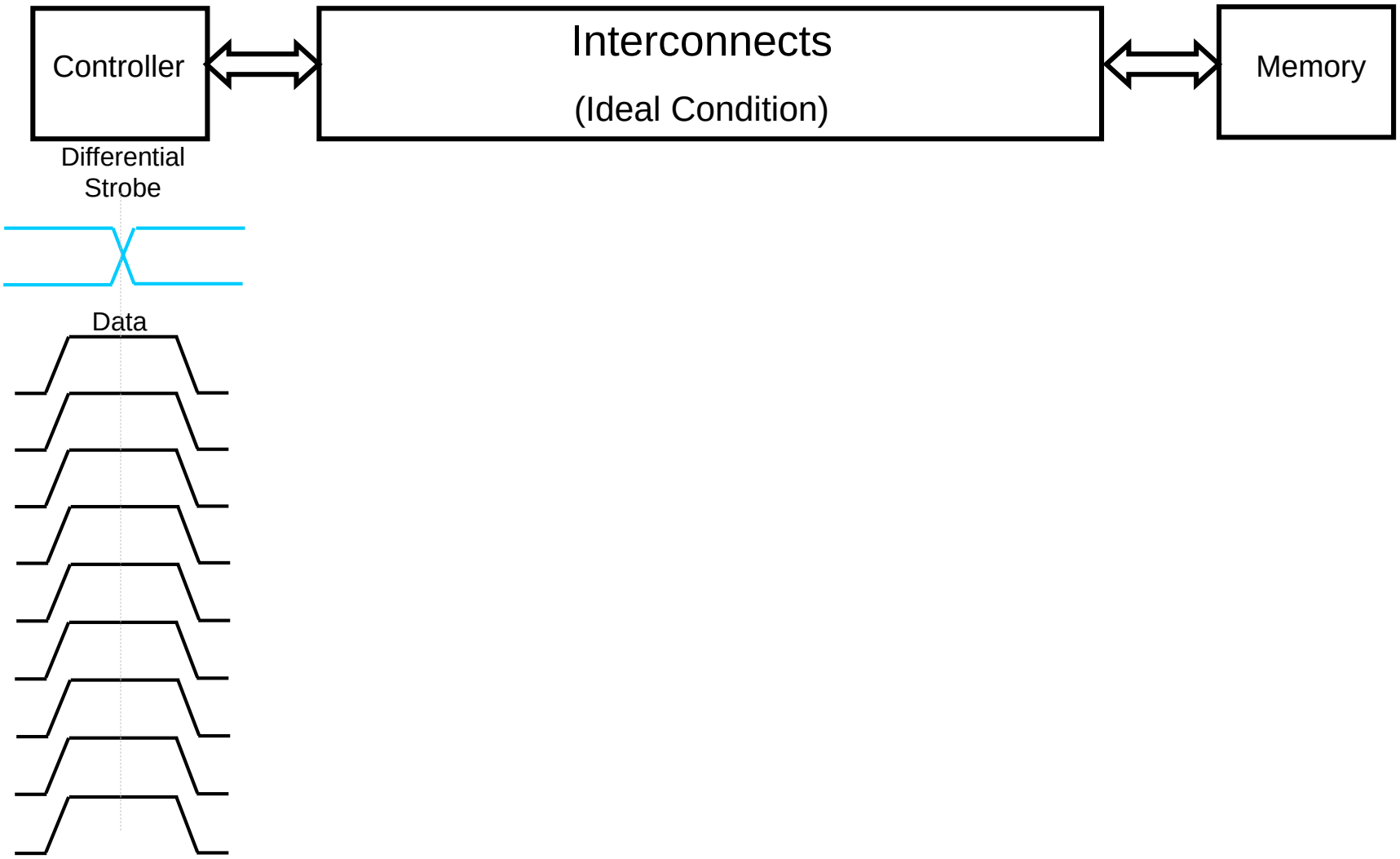
- A requested row is **ACTIVATED** and made accessible through the bank's row buffers
- **READ** and/or **WRITE** are issued to the active row in the row buffers
- The row is **PRECHARGED** and is no longer accessible through the bank's row buffers



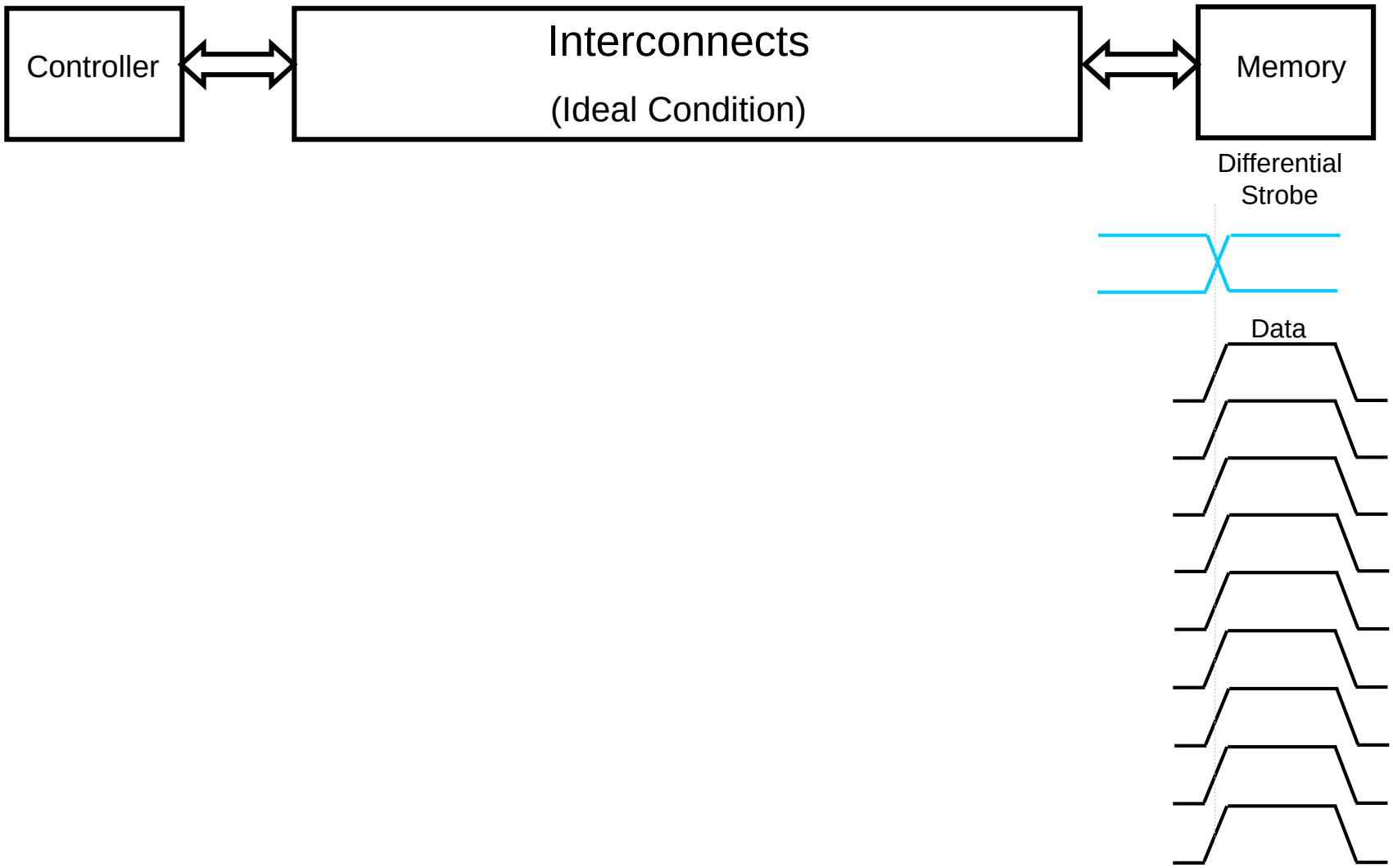
DDR2-533 Read Timing Example



Data Write Cycle

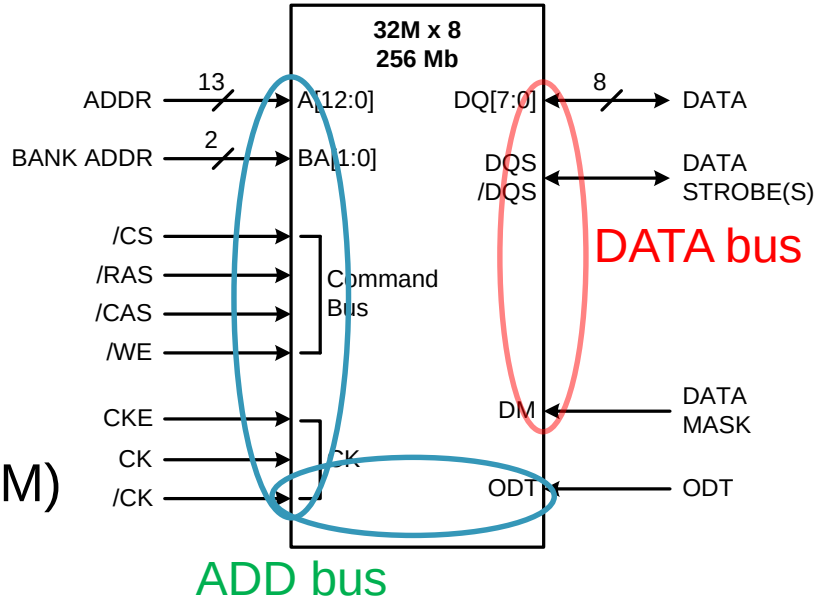


Data Read Cycle



Example – DDR2/3/4 SDRAM

- Micron MT47H32M8
- 32M x 8 (8M x 8 x 4 banks)
- 256 Mbits total
- 13-bit row address
  - 8K rows
- 10-bit column address
  - 1K bits/row (1KB in x8 data with DRAM)
- 2-bit bank address
- Data bus: DQ, DQS, /DQS, DM
- ADD bus: A, BA, /CS, /RAS, /CAS, /WE, ODT, CKE, CK, /CK

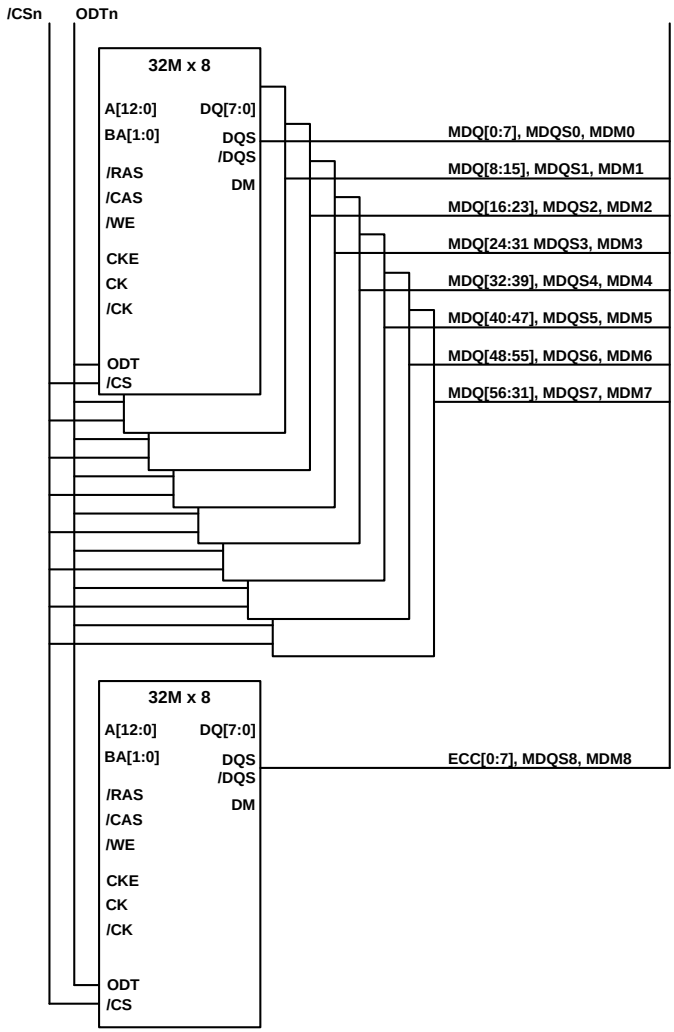


Example – DDR2/3/4 DIMM

- Micron MT9HTF3272A
- 9 each 32M x 8 memory devices
- 32M x 72 overall
- 256 MB total, single “rank”
- 9 “byte lanes”

Two Signal Bus

- 1- Address, command, control, and clock signals are shared among all 9 DRAM devices
- 2- Data, strobe, data mask not shared



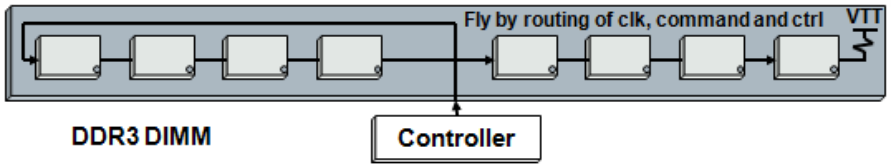
DRAM Module Type

UDIMM: Unbuffered Desktop standard

MiniDIMM:
Computing and Networking

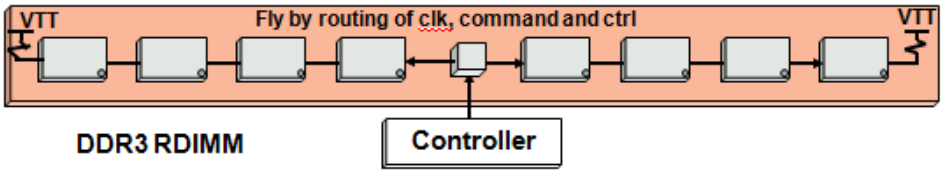
SODIMM: Notebook standard

VLP MiniDIMM:
Computing and Networking



RDIMM: Registered Server standard

VLP RDIMM: Very Low Profile
Computing and Networking



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- Basic DDR SDRAM structure
- **DDR3 vs. DDR4 SDRAM differences**
- QorIQ DDR4 controller features
- Configurations and validation via QCS DDRv tool

DDR SDRAM Highlights and Comparison

Feature/Category	DDR3	DDR4
Package	BGA only	BGA only
Densities	512Mb -8Gb	2Gb -16Gb
Voltage	DDR3L:1.35V Core & I/O DDR3: 1.5V Core & I/O	1.2V Core 1.2V I/O, also 2.5V external VPP
Data I/O CMD, ADDR I/O	Center Tab Termination (CTT) CTT	Pseudo Open Drain (POD) CTT
Internal Memory Banks	8	16 for x4/x8 8 for x16
Data Rate	800 DDR3/3L:2133/1866 Mbps	1600–3200 Mbps
VREF	VREFCA & VREFDQ external	VREFCA external VREFDQ internal
Data Strobes/Prefetch/Burst Length/Burst Type	Differential/8-bits/BC4, BL8/ Fixed, OTF	Same as DDR3
Additive/read/write Latency	0, CL-1, CL-2/ AL+CL/ AL +CWL	Same as DDR3

DDR SDRAM Highlights and Comparison (continued)

Feature/Category	DDR3	DDR4
CRC Data Bus	No	Yes
Boundary Scan/Connectivity test (TEN pin)	No	Yes
Bank Grouping	No	Yes
Data Bus Inversion (DBI_n pin)	No	Yes
Write Leveling / ZQ	Yes	Yes
ACT_n new pin & command	No	Yes
Low power auto self-refresh	No	Yes

DDR3/DDR3L/DDR4 Power Saving

- DDR3 DRAM provides 20% power savings over DDR2
- DDR3L DRAM provides 10% power saving over DDR3
- DDR4 DRAM provides 37% power saving over DDR3L

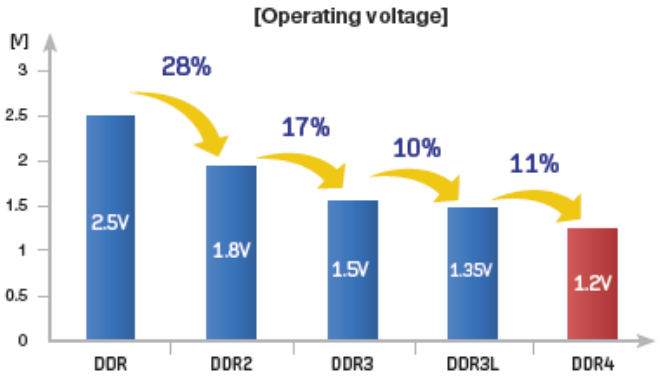

Figure 4. Reduced operating voltage requirements of DDR4 compared to DDR3L

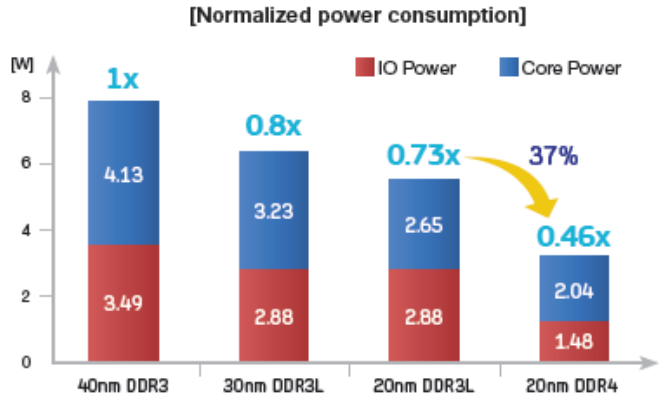

Figure 5. Reduced normalized power consumption requirements of DDR4 compared to DDR3L

SAMSUNG

DDR3 vs. DDR4 DRAM Pinouts

- DDR4 Pins Added
  - VDDQ (2) : 1.2V pins to DRAM
  - VPP : 2.5V external voltage source for DRAM internal word line driver
  - Bank Group (2): pins to identify the bank groups
  - DBI_n: Data Bus Inversion
  - ACT_n: Active command
  - PAR: Parity error signal for address bus
  - Alert_n: Both, Parity error on C\A and CRC error on data bus
  - TEN: Connectivity test mode

- DDR3 Pins Eliminated
  - VREFDQ
  - Bank Address (1): one less BA pin
  - VDD (1), VSS (3), VSSQ (1)

DRAM Densities DDR3 VS. DDR4

- 16 Banks for x4 and x8 DRAM DDR4, 8 Banks for x16
- 4Gb is DRAM's vendors choice for starting DDR4 density.
- Larger memory size is one reasons to use x4 vs. x8 vs. x16 DRAM
- Data mask or Data bus inversion (DBI), not available in x4 DRAM

	Density	1Gb			2Gb			4Gb			8Gb			16 Gb		
	Width	x4	x8	x16	x4	x8	x16	x4	x8	x16	x4	x8	x16	x4	x8	x16
DDR3	Banks	8	8	8	8	8	8	8	8	8	8	8	8			
	Rows	14	14	13	15	15	14	16	16	15	16	16	16			
	Columns	11	10	10	11	10	10	11	10	10	12	11	11			
	Row Size (KB)	1	1	2	1	1	2	1	1	2	2	2	2			
DDR4	Banks				16	16	8	16	16	8	16	16	8	16	16	8
	Rows				15	14	14	16	15	15	17	16	16	18	17	17
	Columns				10	10	10	10	10	10	10	10	10	10	10	10
	Row Size (KB)				0.5	1	2	0.5	1	2	0.5	1	2	0.5	1	2

Modules DDR3 vs. DDR4

- U/RDIMM Pin count of 240 vs. 288, Pin pitch of 1.0mm vs. 0.85mm
- Bottom edge step ramp vs. flat. Height & width increased by ~1mm
- DRAM ball count and ball pitch not changed
- DIMM topology of fly-by for address/command bus not changed
- SoDIMM Pin count of 204 vs. 260
- SoDIMM will have native ECC support vs. non compatible pinout in DDR3

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Common DDR3 and DDR4 Controller Features

- Supports most JEDEC standard x8, x16 DDR3L & DDR4 devices
- Memory device densities from 1Gb – through 8Gb
- Data rates up to: 1600 MT/s DDR3L and DDR4
- Devices with 12-16 row address bits, 8-11 column address bits, 2-3 logical bank address bits
- Data mask signals for sub-double word writes
- Up to four physical banks (ranks / chip selects)
- Physical bank (rank) sizes up to 8GB/16GB for DDR3L/DDR4
- Physical bank interleaving between 2 or 4 chip selects
- Memory controller interleaving when more than 1 controller is available
- Un-buffered or registered DIMMs

Common DDR3 and DDR4 Controller Features (continued)

- Up to 32 / 64 open pages for DDR3L / DDR4
  - Amount of time rows stay open is programmable
- Auto pre-charge, globally or by chip select
- Self refresh
- Up to 8 posted refreshes
- Automatic or software-controlled memory device initialization
- ECC: 1-bit error correction, 2-bit error detection, detection of all errors within a nibble
- ECC error injection
- Read-modify-write for sub-double word writes when using ECC
- Automatic data initialization for ECC
- Dynamic power management

Common DDR3 and DDR4 Controller Features (continued)

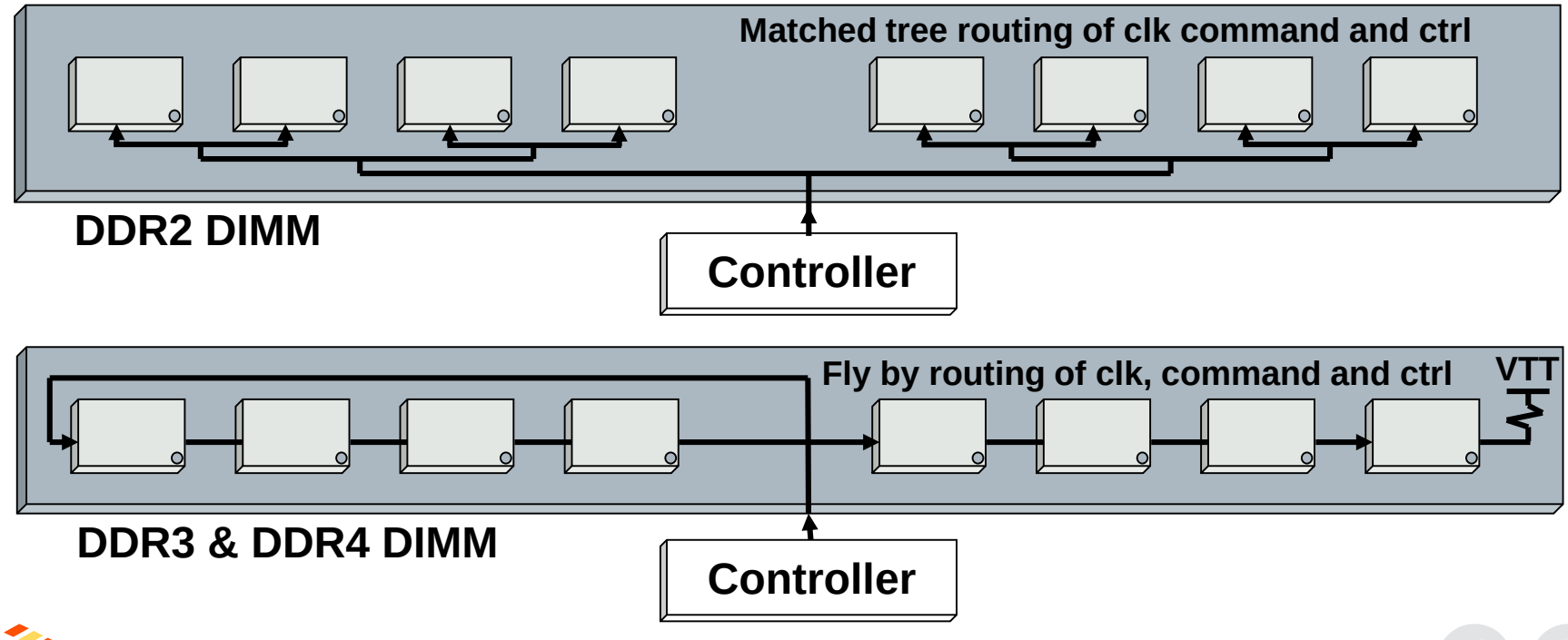
- Partial array self refresh (DDR3 only)
- Address and command parity for registered DIMM (DDR3 only)
- Independent driver impedance setting for data, address/command, and clock
- Synchronous and Asynchronous clock-in option
- Write-leveling
- Automatic CPO
- Asynchronous RESET
- Automatic ZQ calibration
- Fixed or On-the-Fly burst chop mode
- Mirrored DIMM supported

DDR4-only Controller Features

- Internal DQa Vref supply and calibration, both controller and DRAM
- Data write CRC
- Data inversion bus
- Address bus parity error
- 16 banks for higher concurrency
- Connectivity test mode
- ODT park and buffer disable
- DRAM mode register readout capability
- Low power auto self refresh
- Temp controlled auto refresh
- Pseudo open drain (POD) driver and termination
- Command Address latency (CAL)

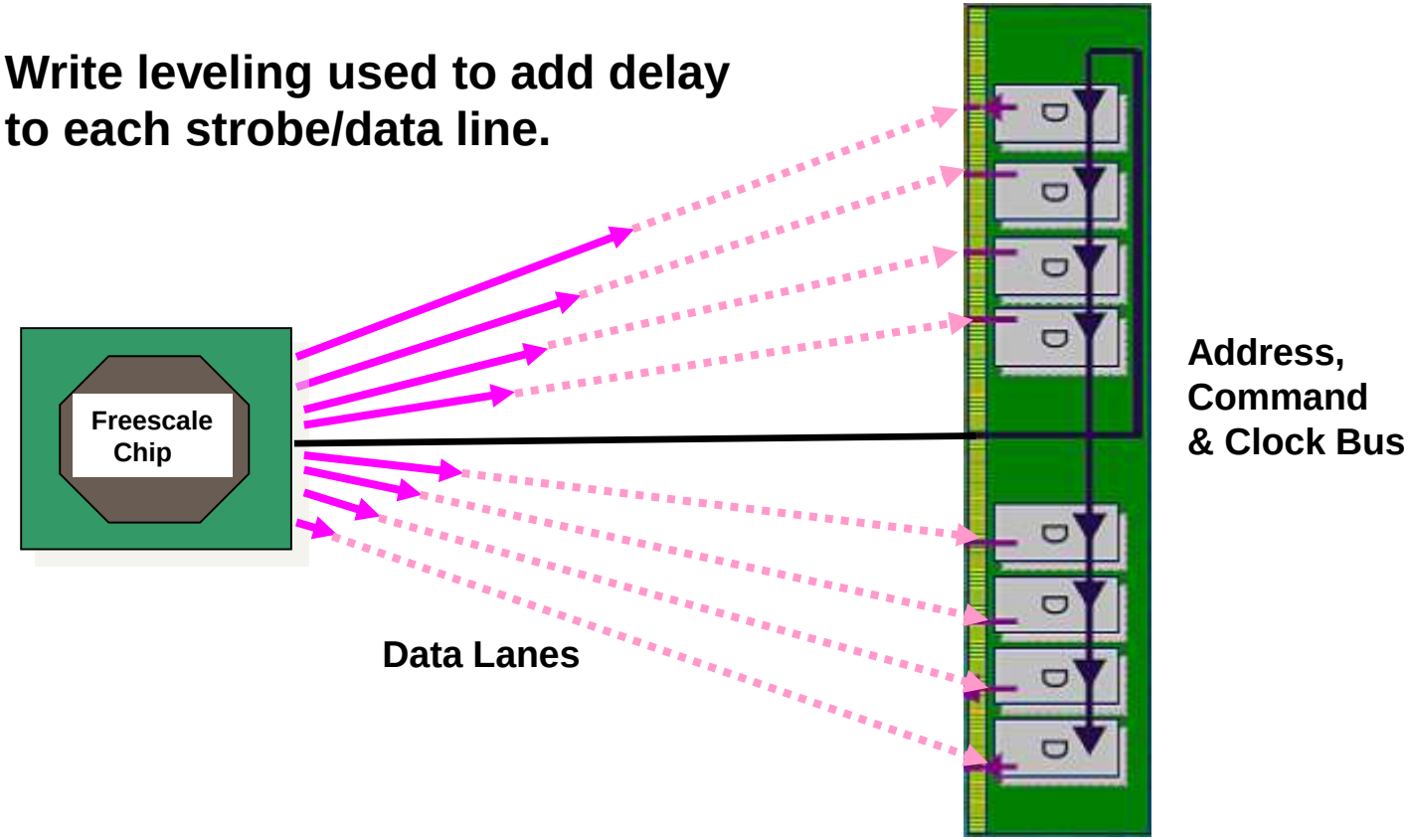
Fly By Routing Topology

- Introduction of “Fly-by” architecture
  - Address, command, control & clocks
  - Improved signal integrity…enabling higher speeds
  - On module termination



Write Adjustment

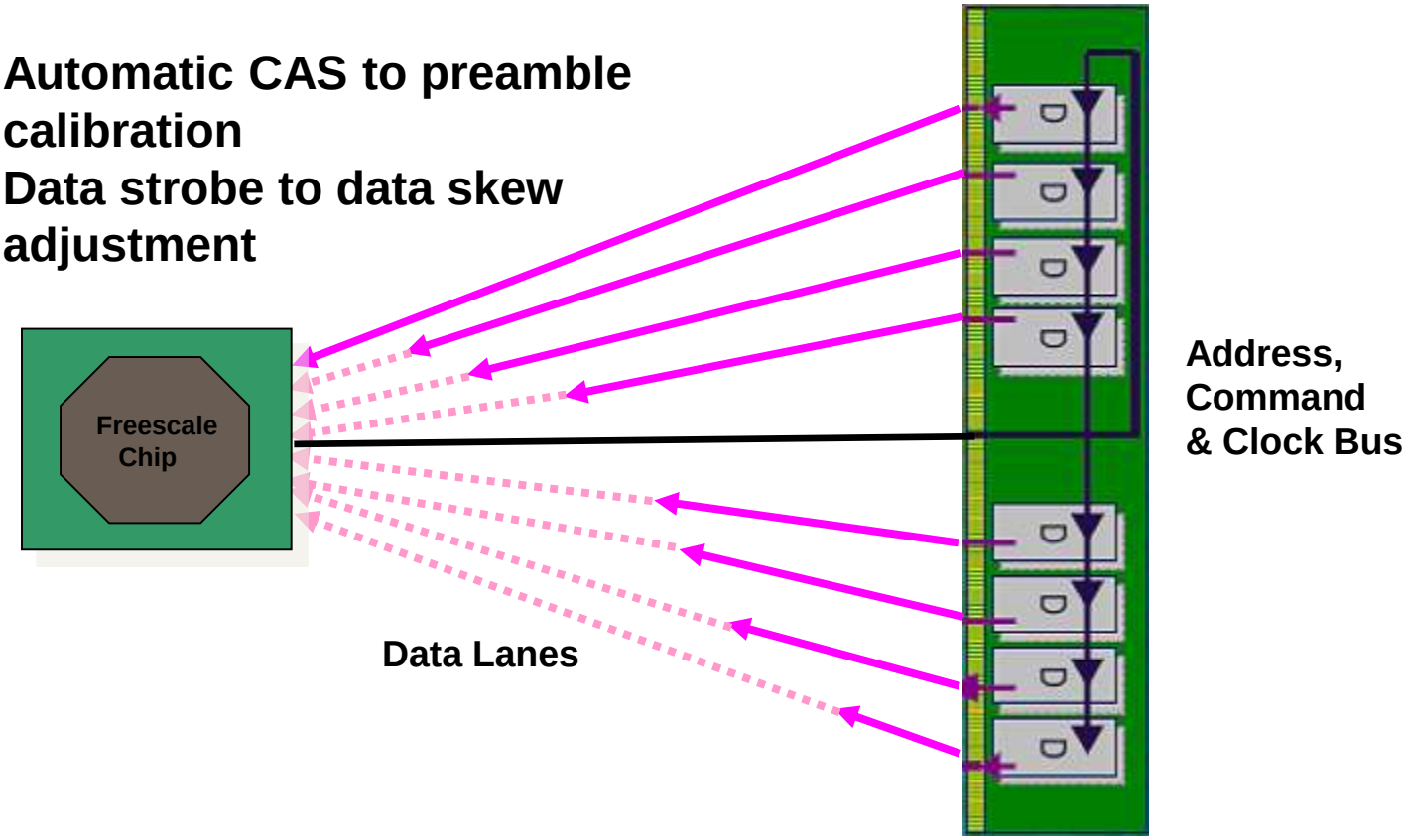
- **Write leveling used to add delay to each strobe/data line.**



Write leveling sequence during the initialization process will determine the appropriate delays to each strobe/data byte lane and add this delay for every write cycle.

Read Adjustment

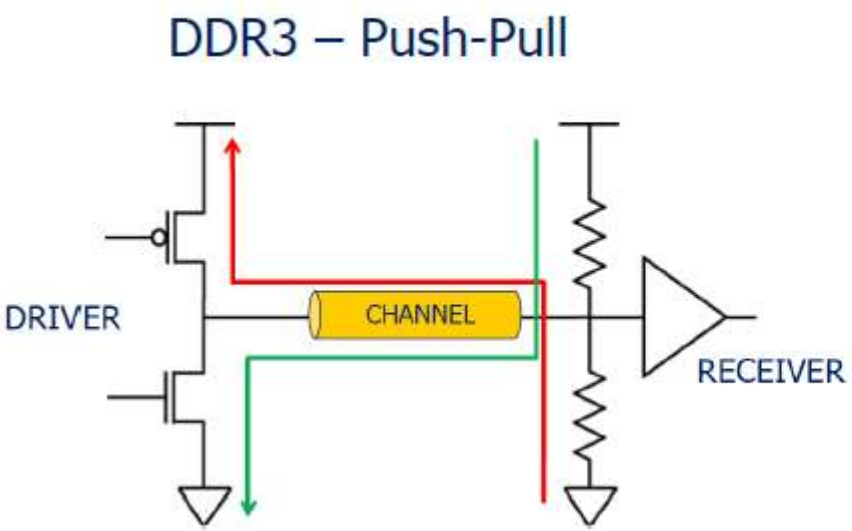
- **Automatic CAS to preamble calibration**
- **Data strobe to data skew adjustment**

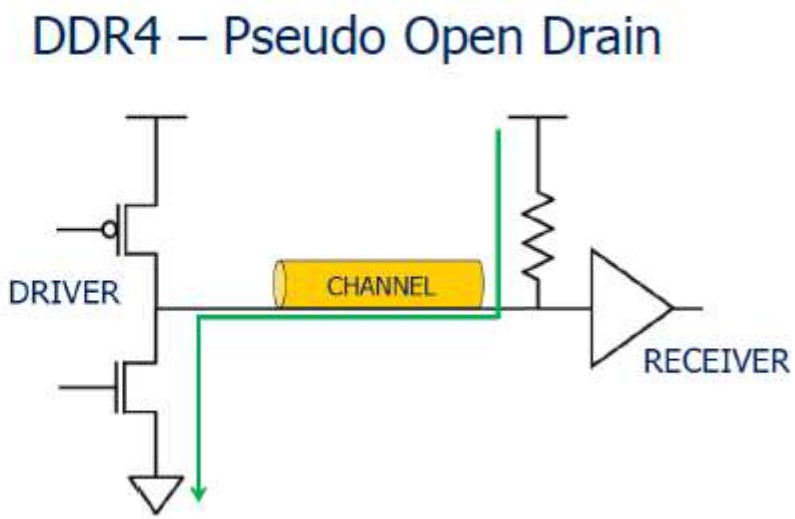


Auto CPO will provide the expected arrival time of preamble for each strobe line of each byte lane during the read cycle to adjust for the delays cased by the fly-by topology.

DDR4 Output Driver / Termination

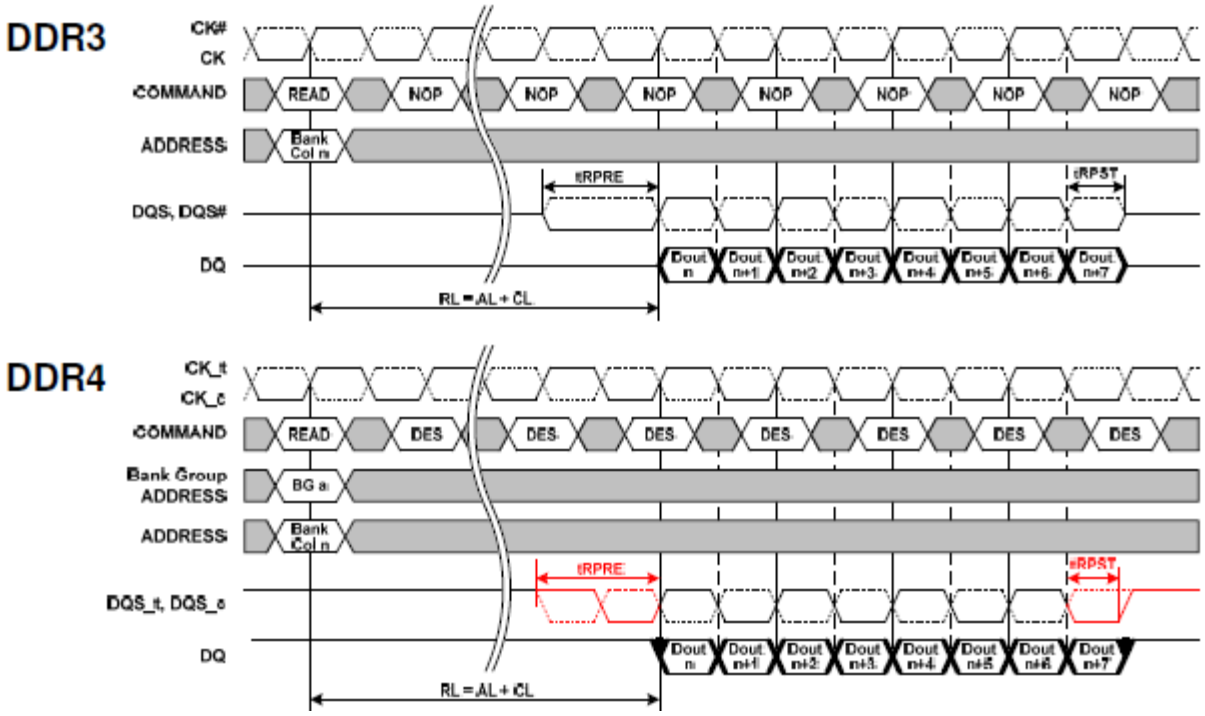
- Center tap termination is used in DDR3 receiver
- POD termination or pull up is used in DDR4 receiver
- Push-Pull driver in DDR3 and POD driver in DDR4
- Less power is consumed using POD driver & termination.





DDR3 & DDR4 Preamble and Idle signal differences

- DQ and DQS signals stay high during idle time
- DQS preamble is same for Read and Writes.



Pin Muxing in DDR4 Memory Controller

- DDR4 support up to 16Gb vs. 8Gb in DDR3
- DDR4 uses A0-A13 for column accesses (i.e. MA[14] & MA[15] not used for column access)
- DDR4 has 4 banks within each group (i.e. MBA[2] not used)

DDR3	DDR4
MRAS	MRAS/ MA[16]
MCAS	MCAS/ MA[15]
MWE	MWE/ MA[14]
MA[15]	ACT_n
MA[14]	BG1
MBA[2]	BG0
MDM[0-8]	MDM / DBI
MAPAR_ERR	Alert_n
MAPAR_OUT	PAR

New pin: ACT_n

- ACT_n is a single pin for Active command input

- When ACT_n is low:
  - ACT Command is asserted
  - WE/CAS/RAS pins will be treated as address pins (A14:A16)

- When ACT_n is high
  - WE/CAS/RAS pins will be treated as command pins

New pin: DBI_n

- Active low input/output for data bus inversion mode
- As an input to DRAM, a low on DBI_n indicates that the DRAM inverts write data received on the DQ inputs
- As an output from the DRAM, a low on DBI_n indicates that the DRAM has inverted the data on its DQ outputs.
- Maximum of half of the bits driven low including DBI_n pin
- Available only on x8 and x 16 DRAM
- PROs: Fewer bits driven low means less noise, better data eye and lower power consumption
- CONs: Data mask is not available, performance is affected with read-modify-writes when writes are not multiples of 8 bytes or not aligned to 0 or 8 address. CAS_LAT is increased by 2 clocks.

Data Bus Inversion - DBI

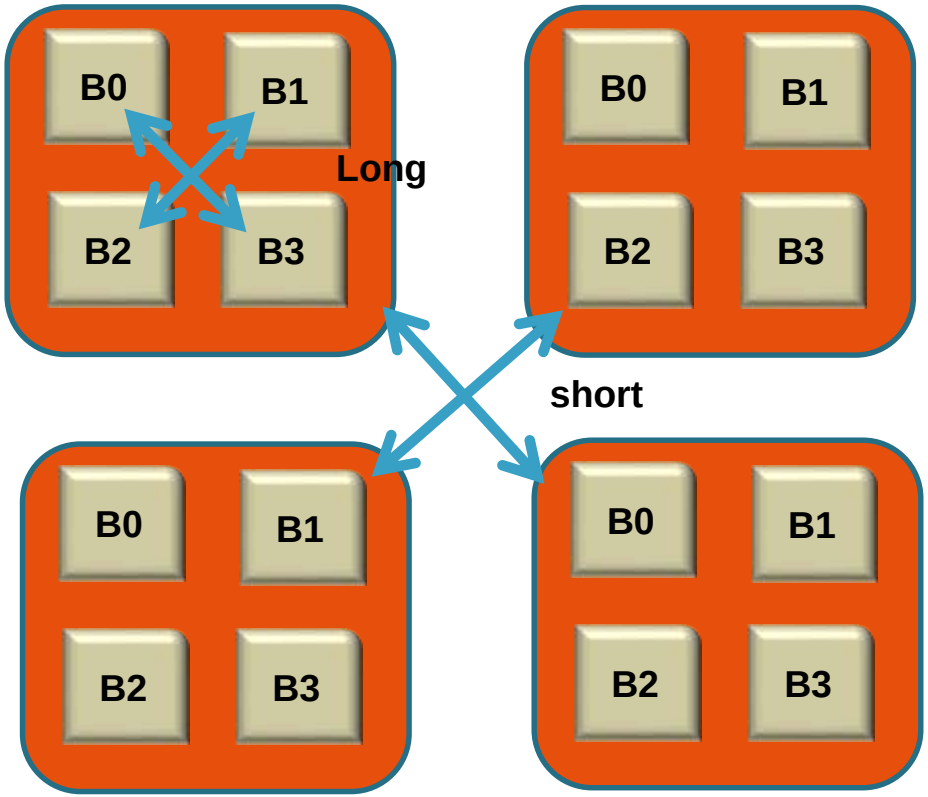
- If more than 4 bits of a byte lane are low, invert the data and drive the DBI_n pin low
- If 4 or less bits of a byte lane are low, do not invert the data and drive the DBI_n pin high

	Controller				Data Bus				Memory			
DQ0	0	1	0	0	1	1	0	1	0	1	0	0
DQ1	1	1	0	0	0	1	0	1	1	1	0	0
DQ2	0	0	0	0	1	0	0	1	0	0	0	0
DQ3	0	1	1	0	1	1	1	1	0	1	1	0
DQ4	0	1	0	0	1	1	0	1	0	1	0	0
DQ5	1	0	1	0	0	0	1	1	1	0	1	0
DQ6	1	1	1	0	0	1	1	1	1	1	1	0
DQ7	0	0	1	0	1	0	1	1	0	0	1	0
DBI_n					0	1	1	0				
# low bits	5	3	4	8	4	3	4	1				

New Pin: BGn Bank Group Address

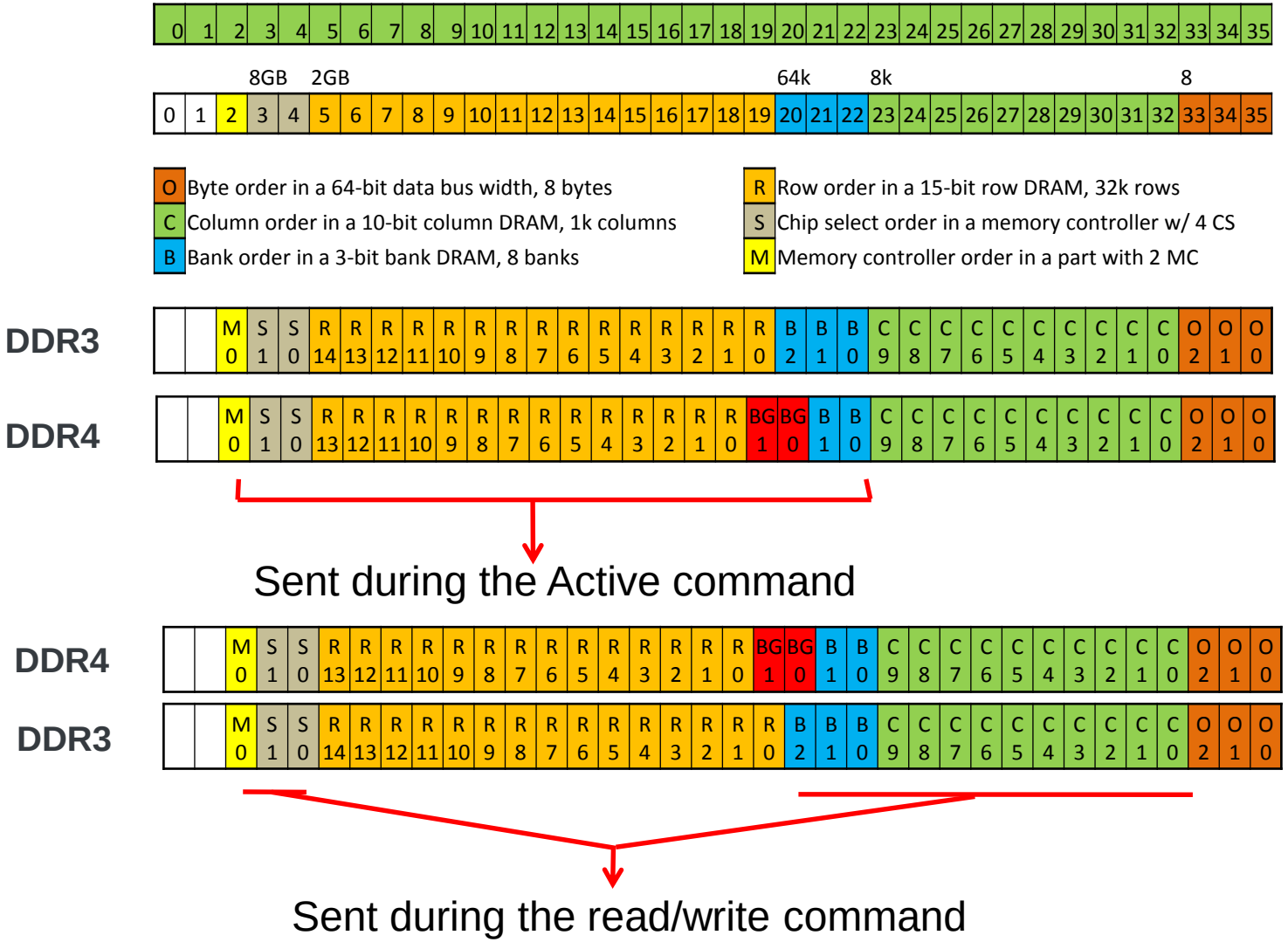
- Different timing within a group and between groups
  - Active to active (tRRD_L)
  - Write to read (tWTR_L)
  - Read to read (tCCD_L)
  - Write to write (tCCD_L)
- Controller to maintain

Timing requirements for both Within a group (Long) and Between groups (short)



Data rate	1600	1866	2133	2400
tCCD_S	4	4	4	4
tCCD_L	5	5	6	6

Address decoding for DDR



New Pin: Parity

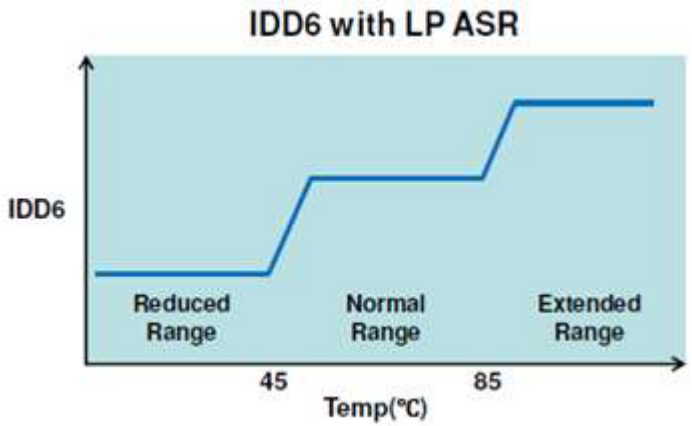
- C/A Parity signal (PAR) covers ACT_n, RAS_n, CAS_n, WE_n and the address bus. Control signals CKE, ODT, CS_n are not included
- Even parity, i.e. valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. The parity bit is chosen so that the total number of ‘1’s in the transmitted signal, including the parity bit is even
- Commands must be qualified by CS_n
- Alert_n used to flag error to memory controller
- PROs: Better reliability
- CONs: PL (4clk for 2133, 5clk for 2400) is added to read latency

New Pin Alert_n & Cyclic Redundancy Check (CRC)

- Alert_n – Active low output signal that indicates an error event for both the C/A Parity Mode and the CRC Data Mode
- CRC Data mode:
  - To detect data errors during write cycles .
  - Polynomial encoding is used to generate the CRC for every 8-bit
  - Two beats added to the write burst to transfer the CRC header
  - DRAM generates a CRC checksum per each write burst and DQS lane
  - DRAM compares the generated checksum to controllers checksum
  - If Data Mask is disabled, corrupt data is written, with the Alert_n flag sent to controller to retry the write.
  - If Data Mask is enabled, corrupt data is not written, with the Alert_n flag sent to controller to retry the write.

Low Power Auto Self Refresh

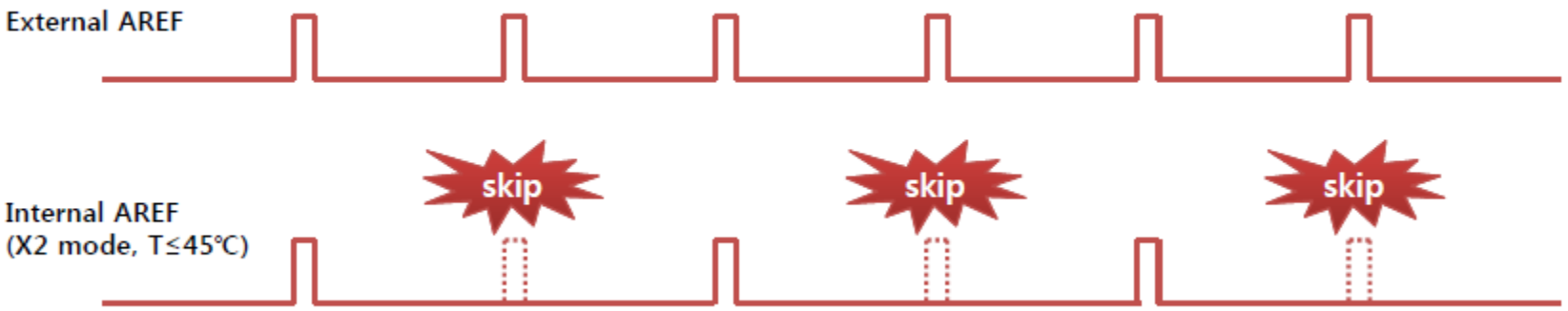
- While DRAM is in self-refresh mode, four refresh mode options available:
  - Manual mode, normal temperature (45C – 85C)
  - Manual mode, extended temperature (85C – 95C)
  - Manual mode, reduced temperature (0C – 45C)
  - Automatic mode: automatically switches between modes based on temperature sensor measurements
- Power savings by reducing refresh rate when possible



Auto Self Refresh	DDR4	DDR3
Extended Range	85˚C-95˚C	85˚C-95˚C
Normal Range	45˚C-85˚C	0˚C-85˚C
Reduced Range	0˚C-45˚C	

Temperature controlled auto refresh

- Enabled or disabled in MR4.
- In extended temp mode controller sends refresh commands every 3.9us
- DRAM based on the internal temp sensor will skip refresh commands automatically to save power



Command Address Latency (CAL)

- DDR4 supports CAL as a power savings feature.
- In default mode, DRAM C/A input receivers are always on
- In CAL mode, only CS receiver is always on. all remaining C/A input receivers are kept in a low power state while not in use. CS signal is sent N number of cycles earlier to allow DRAM time to wake up C/A input receivers.

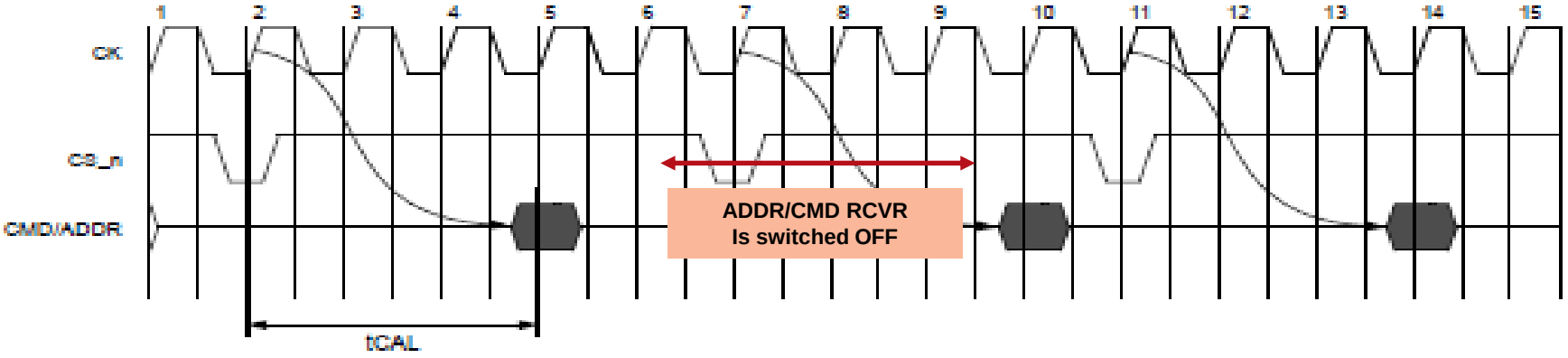
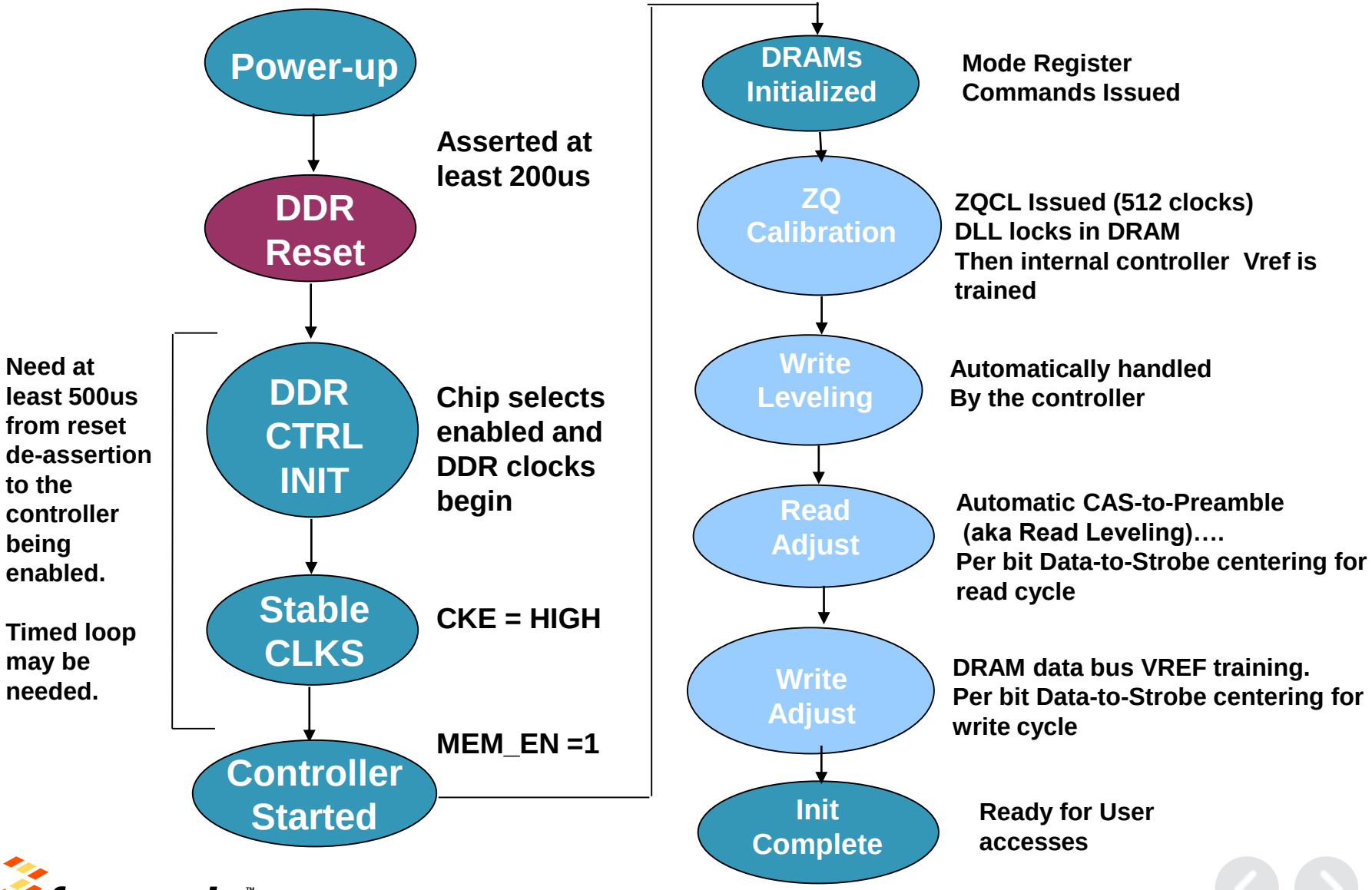


Figure 34 — Definition of CAL

Agenda

- Industry trends
- Basic DDR SDRAM structure
- DDR3L vs. DDR4 SDRAM differences
- QorIQ DDR4 controller features
- **Configurations and validation via QCS DDRv tool**

DDR4 Initialization Flow



Register configuration

Two general type of registers to be configured in the memory controller

- First register type are set to the DRAM related parameter values, that are provided via SPD or DRAM datasheet. Over 100 register fields fall under this category.

- Second register type are the Non-SPD values that are set based on customer's application. For example:
  - On-die-termination (ODT) settings for DRAM and controller
  - driver impedance setting for DRAM and controller
  - Clock adjust value selection
  - Write-leveling start value (WRLVL_START)

Using QCS DDRv Tool

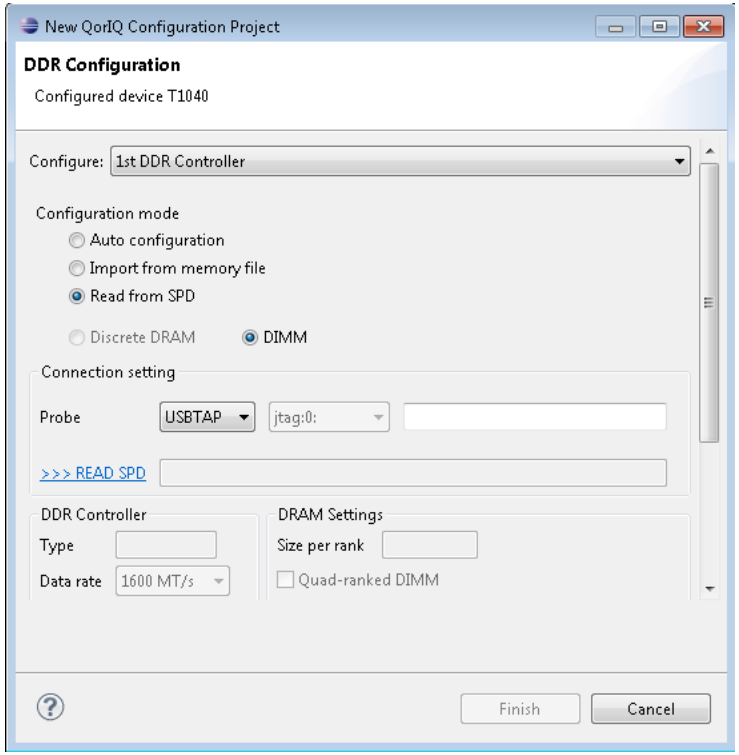
- Configure, and optimize your DDR interface in matter of hours.

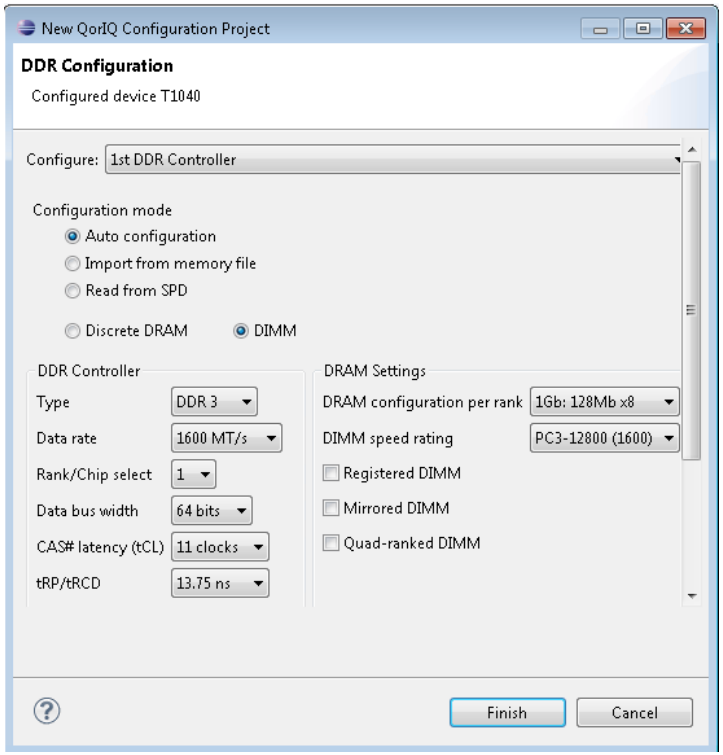
1. Use the tool to generate the DDR register settings
   - Use the latest revision
   - Select the SPD option in configuration wizard when DIMM is used
   - Select Auto Configuration when Discrete DRAM is used
2. Optimize the DDR register setting on your QorIQ board
   - Run the clock centering test
   - Optimize the ODT and drive strength for read and write

- DDRv DEMO: http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=PE_QORIQ_DDRV

Generate The DDR Register settings

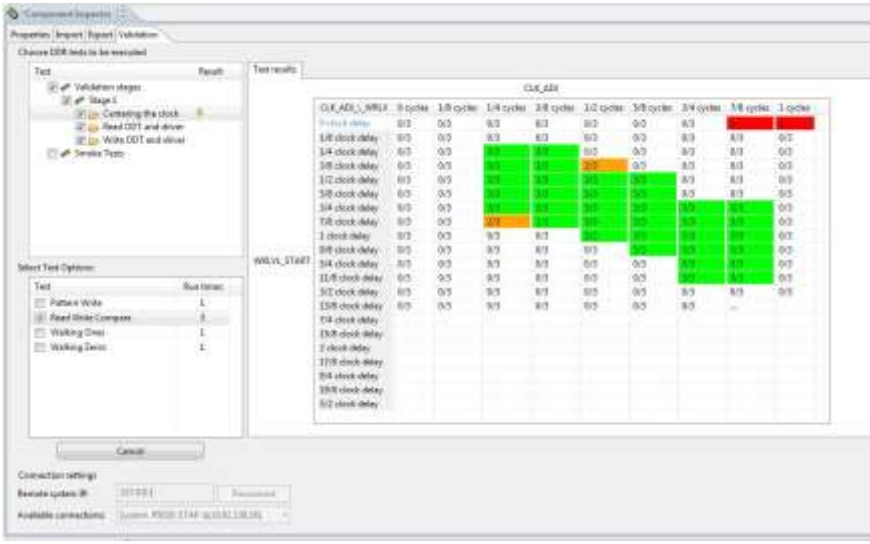
- Using DDR wizard, Select the SPD option for DIMMs, or Auto configure for DIMMs or Discrete DRAM. Press finish and you have generated DDR Register settings.





Optimize/validate the DDR interface on your board

- The board dependent parameters are optimized by connecting to your board and running targeted tests. After this stage, the DDR interface in your board is optimized/validated.



Summary

Summary

- DDR3/3L is mainstream now.
- DDR4 is expected to gain major market share in 2015 and become mainstream by early 2016
- T1, LS1, and LS2 devices support DDR4
- Most features of DDR4, such as write leveling, ZQ calibration, ODT, DBI, C/A Parity, etc., are supported in T1, LS1 & LS2 QorIQ devices
- DDR4 offers higher densities, better reliability and low power consumption in comparison to DDR3/3L.
- Follow JEDEC recommended topologies for discrete DRAM
- Using QCVS DDRv tool configuration and initialization of memory controller is easily achieved

Useful References

- Books:
  - DRAM Circuit Design: A Tutorial, Brent Keeth and R. Jacob Baker, IEEE Press, 2001
- Freescale AppNotes:
  - AN2582 Hardware and Layout Design Considerations for DDR Memory Interfaces
  - AN2910 Hardware and Layout Design Considerations for DDR2 Memory Interfaces
  - AN2583 Programming the PowerQUICCIII / PowerQUICCII Pro DDR SDRAM Controller
  - AN3369 PowerQUICC DDR2 SDRAM Controller Register Setting Considerations
  - AN3939 PQ & QorIQ Interleaving
  - AN3940 Layout Design Considerations for DDR3 Memory Interface
  - AN4039 PowerQUICC DDR3 SDRAM Controller Register Setting Considerations
- Micron AppNotes:
  - TN-46-05 General DDR SDRAM Functionality
  - TN-47-02 DDR2 Offers New Features and Functionality
  - TN-47-01 DDR2 Design Guide
  - TN-41-07 DDR3 Power-Up, Initialization, and Reset
  - TN-41-08 DDR3 Design Guide
- JEDEC Specs:
  - JESD79E Double Data Rate (DDR) SDRAM Specification
  - JESD79-2F DDR2 SDRAM Specification
  - JESD79-3F DDR3 SDRAM Specification
  - JESD79-4A DDR4 SDRAM Specification
- Tools
  - QCS DDRV tool
  - http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=PE_QORIQ_DDRV

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