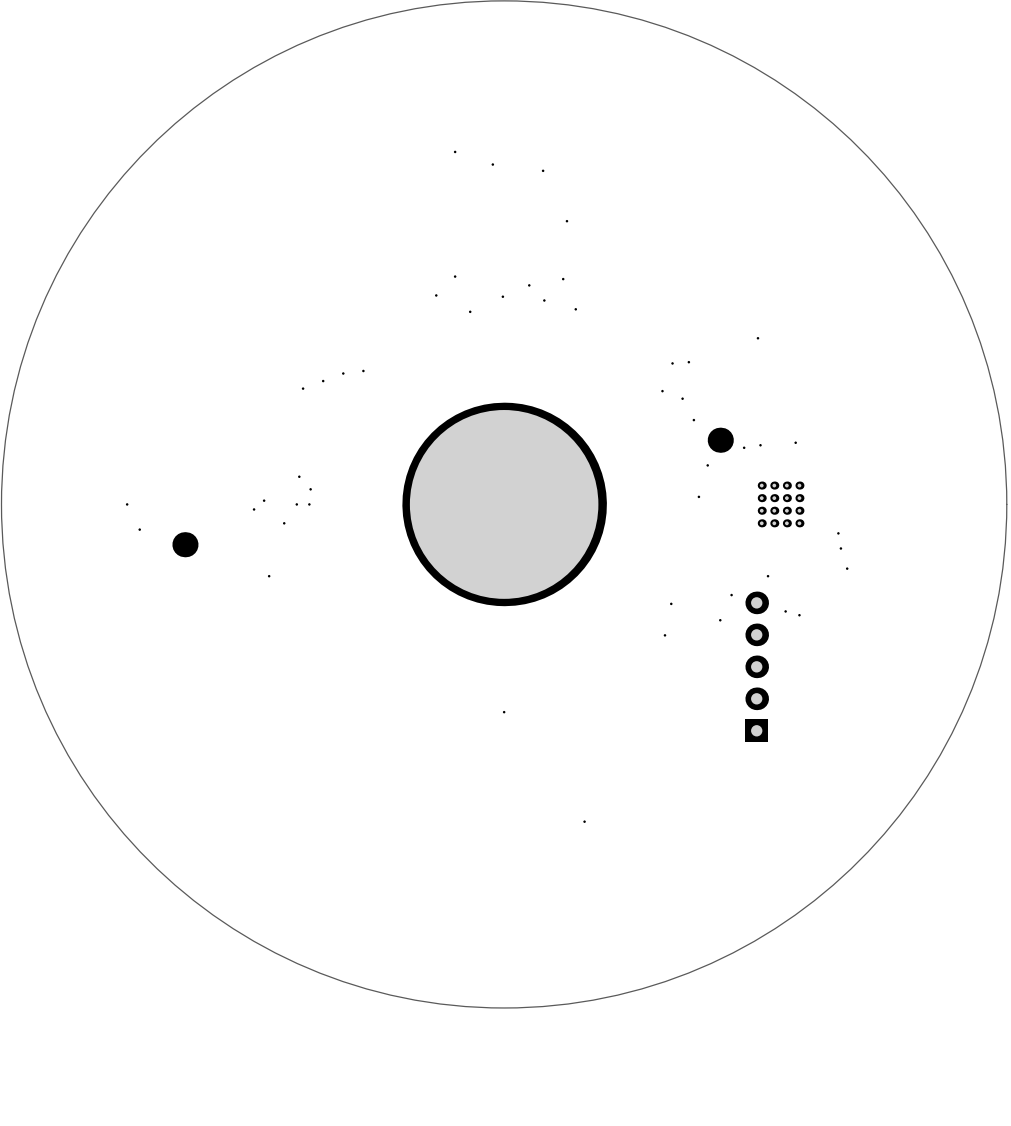


Title: NTAG_1v0.SchDoc			Project Title:	
Size: A2	Number:	Revision:*	NTAG_1v0.PrjPcb	
Date: 10.02.2017	Time: 09:30:52	Sheet * of *		
File: D:\mpa\Designs\NXP_Ntag_Demo\NTAG_1v0\NTAG_1v0.SchDoc				



NXP

RGB LED

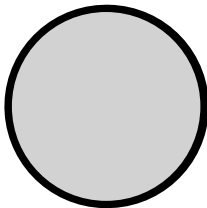
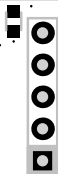
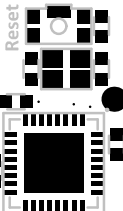


Accélèromèter
MMA8451Q



Temp Sensor
LM75A

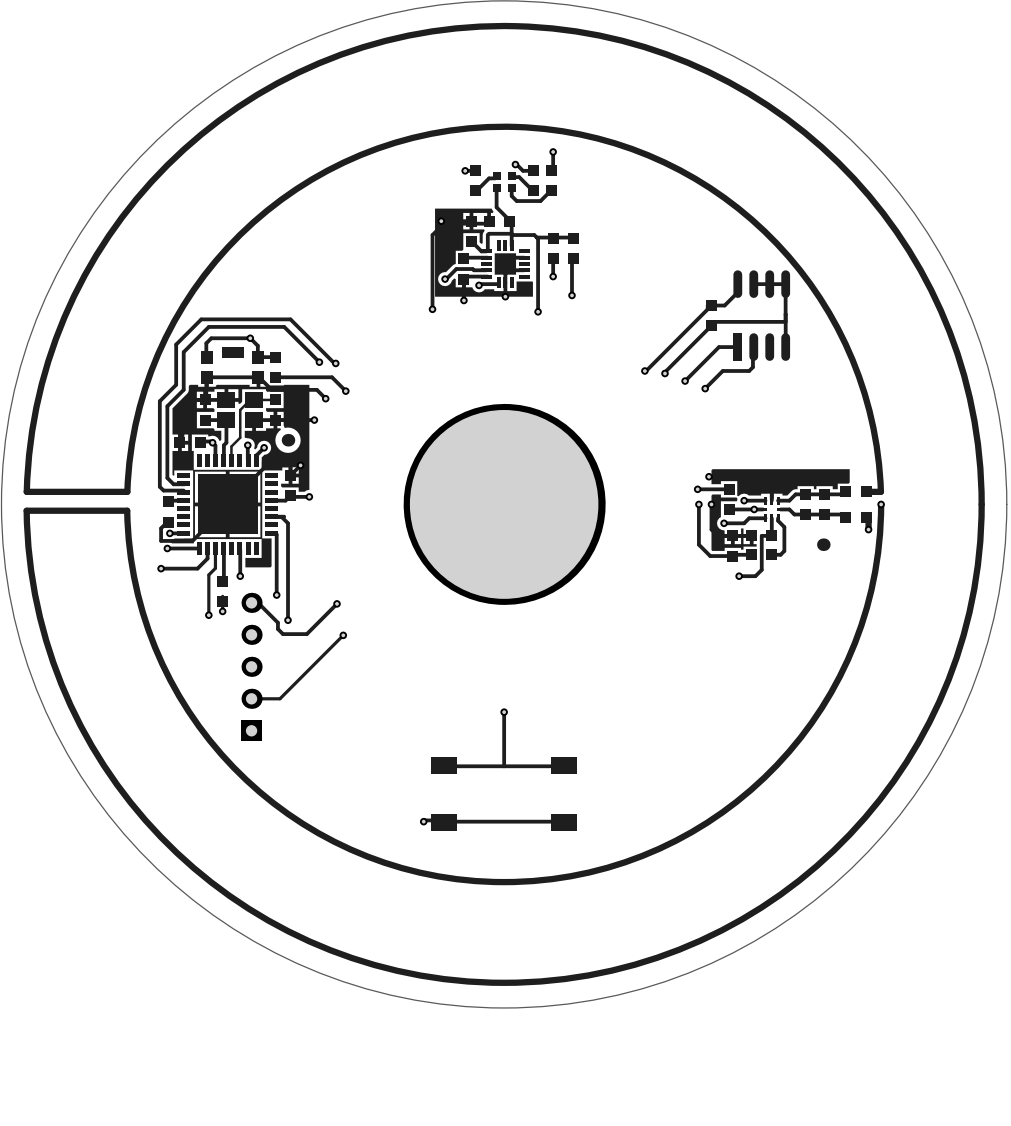
μ-Controller
LPC11U24

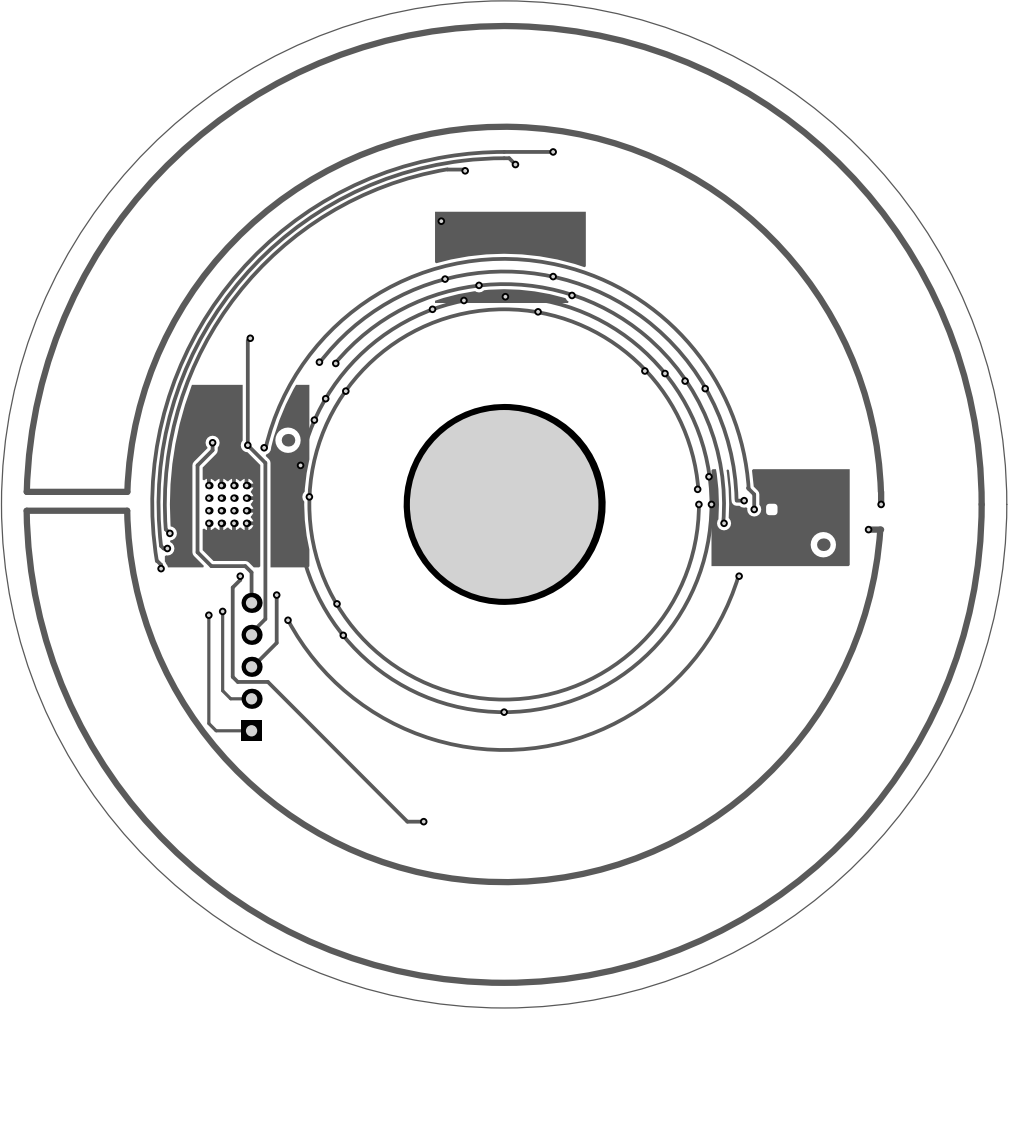


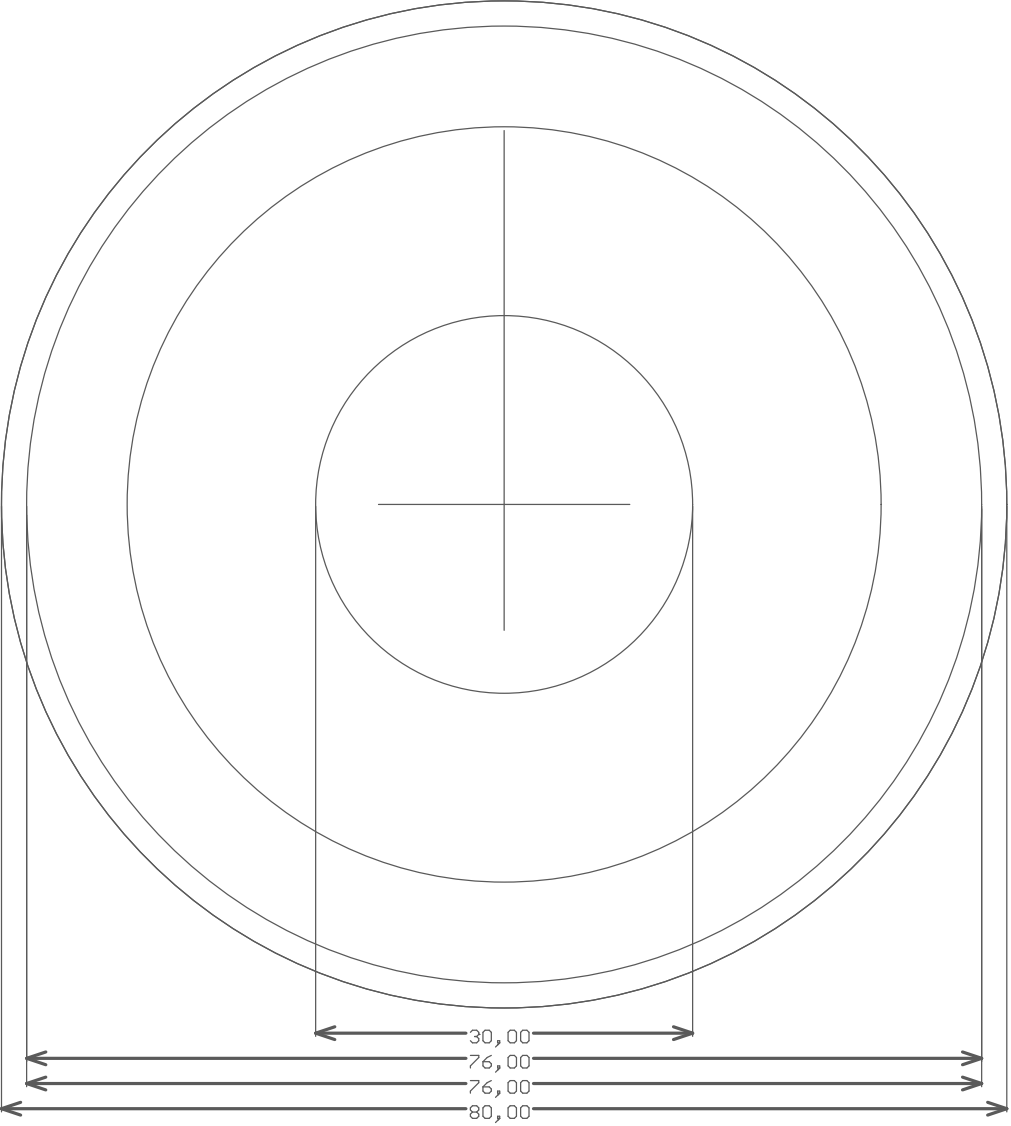
NTAG I2C plus
NT3H1101



ACTION 3







30,00

76,00

76,00

80,00

Design Rules Verification Report

Filename : D:_mpa_Designs\NXP_Ntag_Demo\NTAG_1v0\NTAG_1v0.PcbDoc

Warnings 0
Rule Violations 1

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.15mm) (All),(All)	0
Clearance Constraint (Gap=0.25mm) (IsRegion),(All)	0
Clearance Constraint (Gap=0.5mm) (HasFootprint('FIDUCIAL')),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Width Constraint (Min=0.15mm) (Max=2mm) (Preferred=0.3mm) (All)	0
Routing Via (MinHoleWidth=0.3mm) (MaxHoleWidth=0.8mm) (PreferredHoleWidth=0.3mm) (MinWidth=0.6mm)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.254mm) (Max=0.254mm) (Prefered=0.254mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.5mm) (Conductor Width=0.2mm) (Air Gap=0.2mm)	0
Hole Size Constraint (Min=0.3mm) (Max=6mm) (All)	1
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=0.2mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.15mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Component Clearance Constraint (Horizontal Gap = 0.1mm, Vertical Gap = 0.2mm) (All),(All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	1

Hole Size Constraint (Min=0.3mm) (Max=6mm) (All)	
Hole Size Constraint: (15mm > 6mm) Pad Free-1(50mm,50mm) on Multi-Layer Actual Hole Size = 15mm	

