RT10XX OPTIMIZATION FOR LCD PERFORMANCE

ZHIHAO MO

Content

- Application Background
- RT10xx Configuration
- Emwin/LCD Configuration

Application Background

Note:
1. The LCD request LVDS clock speed is higher than 40.8MHz. RGB and LVDS need to use the same clock source.
2. The optimization is suitable for using RGB LCD too and the RGB LCD is connected to RT10xx directly by LCDIF.

RT10xx Configuration

1. Reduce the core and other master access SDRAM, especially frequently used variables
2. Improve LCD controller and PXP priority, the below example code set them to highest priority.

```
*(uint32_t *)(0x41000000 + 0x44000 + 0x100) = 15;
*(uint32_t *)(0x41000000 + 0x44000 + 0x104) = 15;
```

3. Change the LCD controller burst length and the outstanding capability in the LCDIF_CTRL2 register.

Recommended to set APP_ELCDIF->CTRL2 = 0x00700000; if the performance is not enough, try to set to 0x00900000.

4. Don’t set the LCD controller clock speed is higher than expected refresh rate. The clock speed should be close to expected refresh rate.
5. Configure the SDRAM clock speed to maximum frequency

Register Name	Port Name	Module Name	Absolute Address	Reset Value	Descriptions
read_qos	m_a_2	LCD	GPV0_BASE + 0x44000 + 0x100	1	Set the priority of master’s read. The priority level would be used when the master’s read transaction is being arbitrated by the NIC. Legal programmable values are from 0 to 15. Higher number sets higher priority (0: the lowest arbitration priority; ...; 15: the highest priority).
read_qos	m_a_3	CSI	GPV0_BASE + 0x45000 + 0x100	4	Same as above
read_qos	m_a_4	PXP	GPV0_BASE + 0x46000 + 0x100	2	Same as above

LCDIF_CTRL2*n* field descriptions

Field	Description
31–24 RSRVD5	This field is reserved. Reserved bits. Write as 0.
23–21 OUTSTANDING_REQS	This bitfield indicates the maximum number of outstanding transactions that LCDIF should request when it is acting as a bus master. Default is 2 outstanding transactions. 0x0 **REQ_1** — 0x1 **REQ_2** — 0x2 **REQ_4** — 0x3 **REQ_8** — 0x4 **REQ_16** —
20 BURST_LEN_8	By default, when the LCDIF is in the bus master mode, it will issue AXI bursts of length 16 (except when in packed 24 bpp mode, it will issue bursts of length 15). When this bit is set to 1, the block will issue bursts of length 8 (except when in packed 24 bpp mode, it will issue bursts of length 9). Note that this bitfield is only applicable when LCDIF_MASTER is set to 1.

Emwin Configuration

1. If the LCD bit width is 16 bits, please follow below setting

   #define LCD_BITS_PER_PIXEL 16

   Use 16 bits pixel image, do not use 8/24/32 bits

2. If the LCD bit width is 24/32 bits, please #define LCD_BITS_PER_PIXEL 32

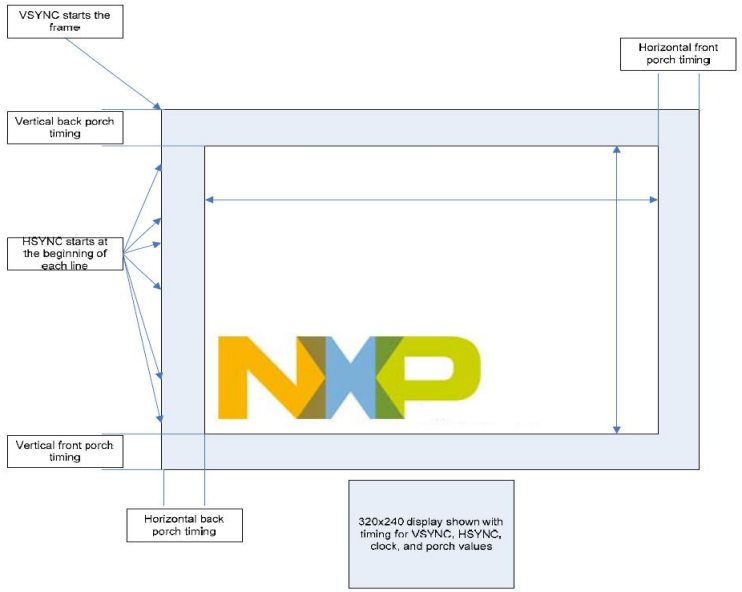
   #define LCD_BITS_PER_PIXEL 32

   Use 32 bits pixel image, do not use 8/16/24 bits

3. Based on this usage application, the RGB clock speed need to be higher than 40.8MHz. The refresh rate is higher than 60 frames. You can refer to below setting to reduce SDRAM access loading.

```
Default setting          -->     New setting
#define APP_HFP 160      -->     #define APP_HFP 180
#define APP_HBP 160      -->     #define APP_HBP 180
#define APP_VFP 20       -->     #define APP_VFP 80
#define APP_VBP 18       -->     #define APP_VBP 80
```

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK frequency	F_{CLK}	40.8	51.2	67.2	MHz
Horizontal display area	T_{HD}		1024		CLK
HS period time	T_H	1114	1344	1400	CLK
HS blanking	$T_{HBP}+T_{HFP}$	90	320	376	CLK
Vertical display area	T_{VD}		600		H
VS period time	T_V	610	635	800	H
VS blanking	$T_{VBP}+T_{VFP}$	10	35	200	H



SECURE CONNECTIONS
FOR A SMARTER WORLD