Embedded Connectivity Summit 2004

DSP-Controlled UPS System with TCP/IP Protocol to Enable Network Communications

DSCO

Launched by Motorola
freescale semiconductor

Online UPS System with TCP/IP Protocol

Uninterruptible power supplies (UPS) have been widely used for office equipment, computers, communication systems, medical/life support and many other systems providing clean and continuous power to a load regardless of power grid conditions. Freescale's DSP controlled on-line triple conversion UPS reference design provides backup power for networks, web servers, telecommunications applications and other critical electronic equipment with Ethernet communications allowing for Local, Network or remote monitoring and management

Online UPS System with TCP/IP Protocol Agenda

Introduction

Hardware Implementation

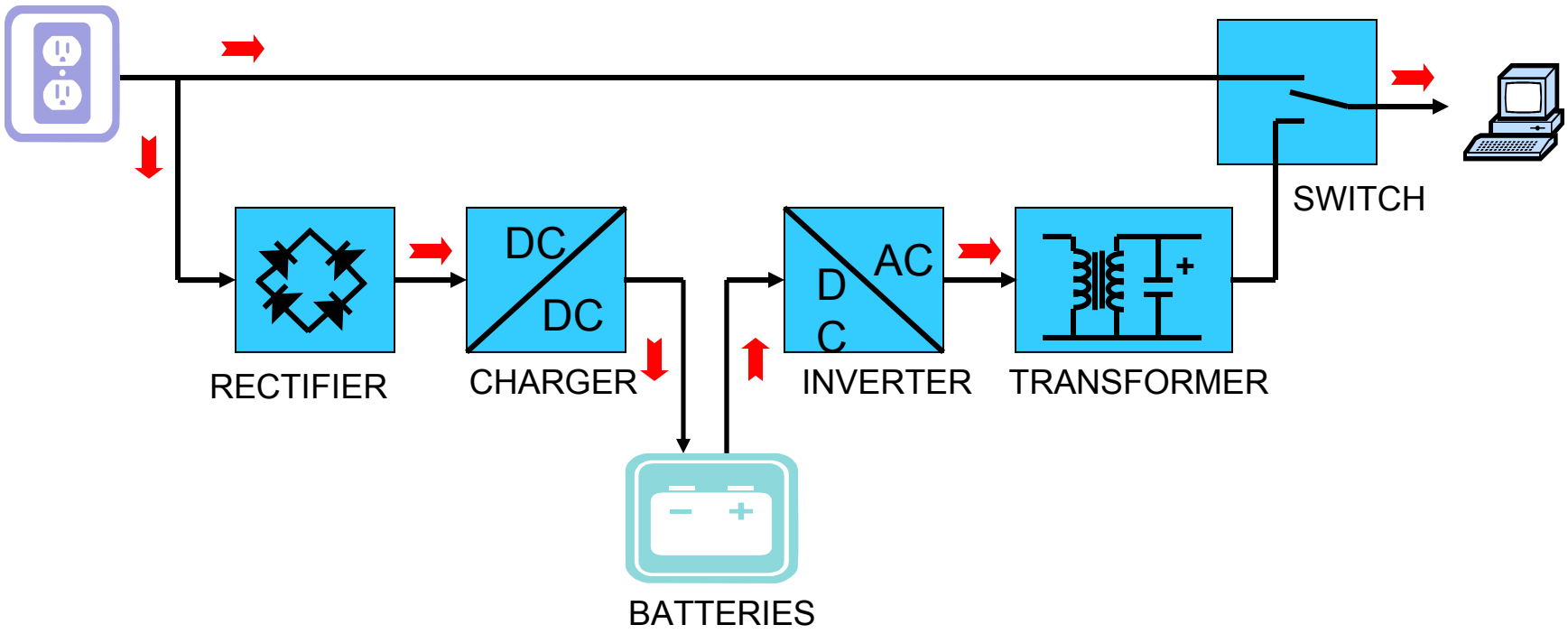
UPS Connectivity

Software Implementation

Competitive Differentiators

Basic UPS Topology

Off-Line UPS – Standby System



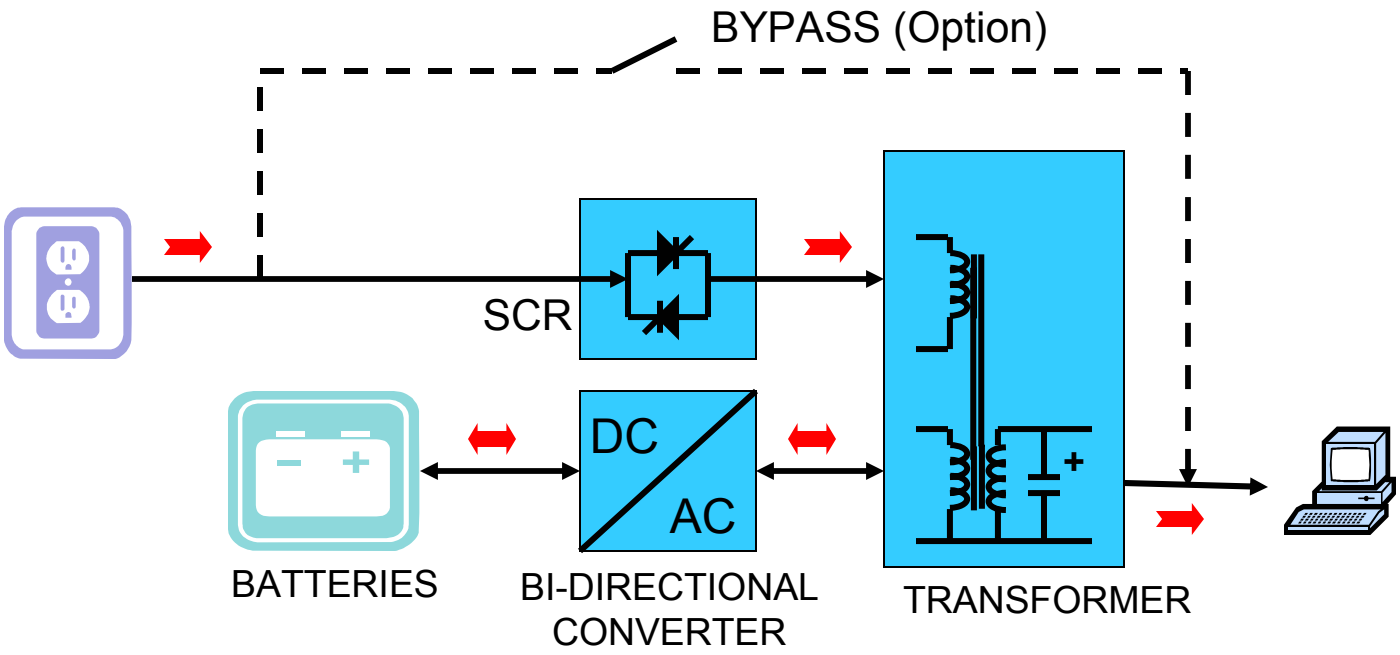
Advantage:
- *High efficiency*
- *High reliability*
- *Compact*
- *Low cost*

Disadvantage:
- *Slow transfer time*
- *Low power factor*
- *No power conditioning*

Limitation:
- *Uses battery during Brownouts*
- *Application below 2 KVA*

Basic UPS Topology

Line Interactive on-line UPS



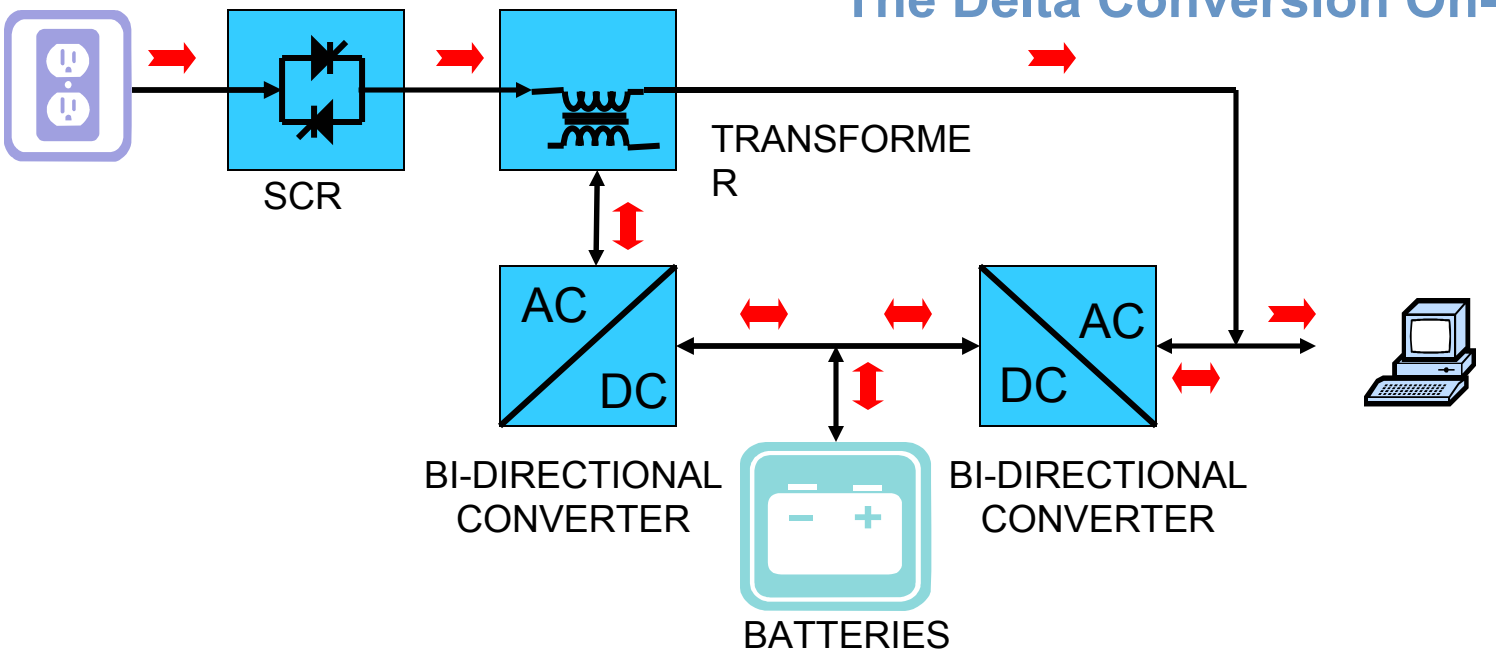
Advantage:
- *High efficiency*
- *High reliability*
- *Good Overload capability*
- *Compact size*

Disadvantage:
- *Transfer time realizable*
- *Unable to control Power factor and frequency*
- *Poor voltage regulation*
- *Control difficult*

Limitation:
- *Application below 5 KVA*

Basic UPS Topology

The Delta Conversion On-line UPS



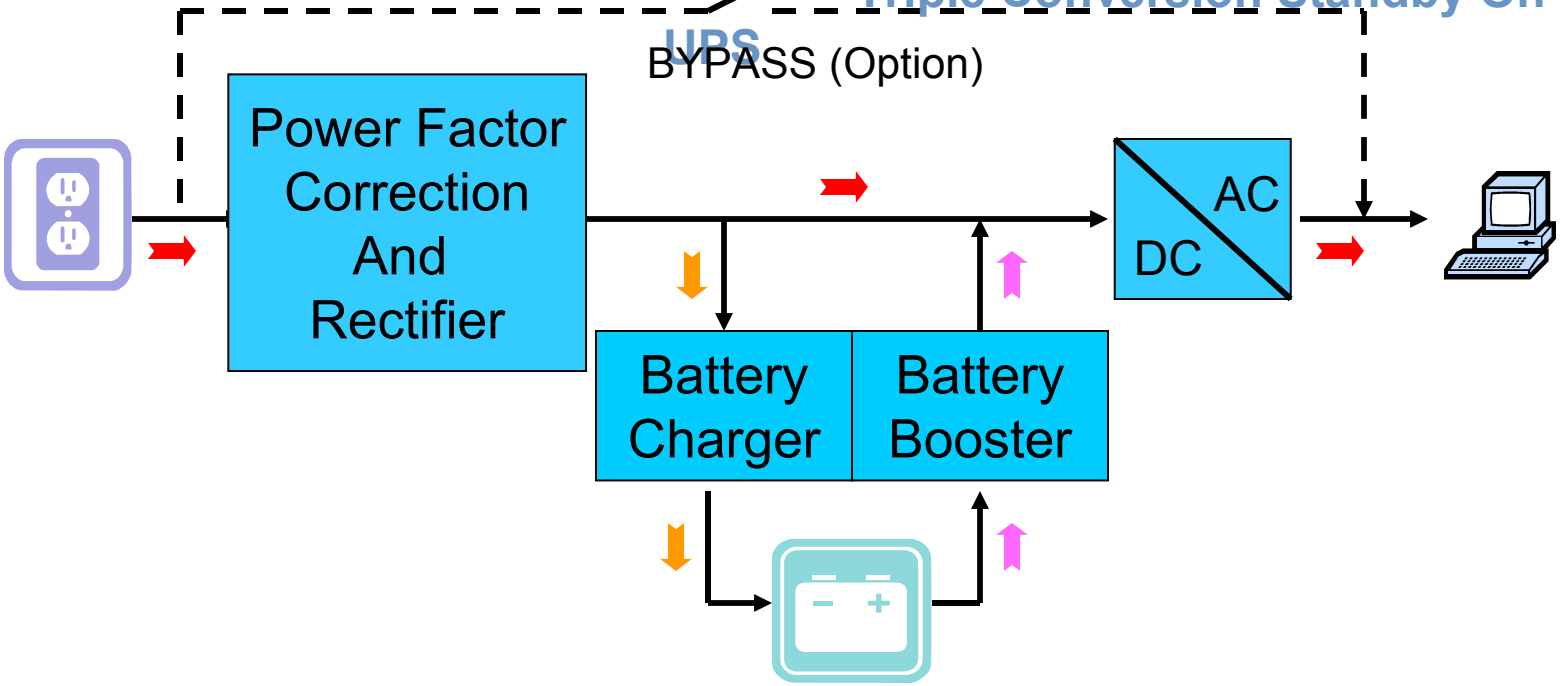
Advantage:
- *Excellent Power Conditioning*
- *High efficiency*
- *High reliability*
- *Excellent Overload capability*

Disadvantage:
- *Control difficult*
- *Unable to control output frequency*
- *Need High voltage battery Packs*

Limitation:
- *Application Over 5 KVA*
- *Three Phase UPS*

Basic UPS Topology

Triple Conversion Standby On-Line UPS



Advantage:
- *Excellent Power Conditioning*
- *No transfer time*
- *Excellent power factor*
- *Full protection*
- *High power density*

Disadvantage:
- *Low efficiency*
- *High Cost*

Limitation:
- *Application Over 2 KVA*

UPS Technology and Trends

- 5.0 KVA and under are accounted for the high volume portion of global UPS market.
- Lower pricing and an increasingly converged technology should produce a spike in both the number and power of personal and home computer purchases.
- MCUs have been used in majority of low-end off-line and on-line UPS.
- Increased use of Digital Signal Processors in high end on-line UPS is providing both significant performance increases and cost reductions.
- New UPS topology requires high performance controller, such as DSP and 16/32-bit MPU.
- Primary function of UPS has shifted for pure backup power supply to AC/AC power supply with backup and power protection and connectivity features
- The DSP/MCU that is used in industrial and motor control applications can be used for UPS control.
- Leading global suppliers continue to gather market share from more niche-focused regional supplies.
- Total UPS market will be an estimated $5.21 B by 2006.

What is an Triple Conversion On-line UPS?

- An On-line Uninterruptible power supply that is always active, even when the line is available.
- The UPS that has a triple conversion topology consisting of
  - ✓ Power Factor Correction
  - ✓ AC/DC converter
  - ✓ Battery charger
  - ✓ Battery Booster
  - ✓ DC/AC inverter.

Online UPS System with TCP/IP Protocol Agenda

Introduction

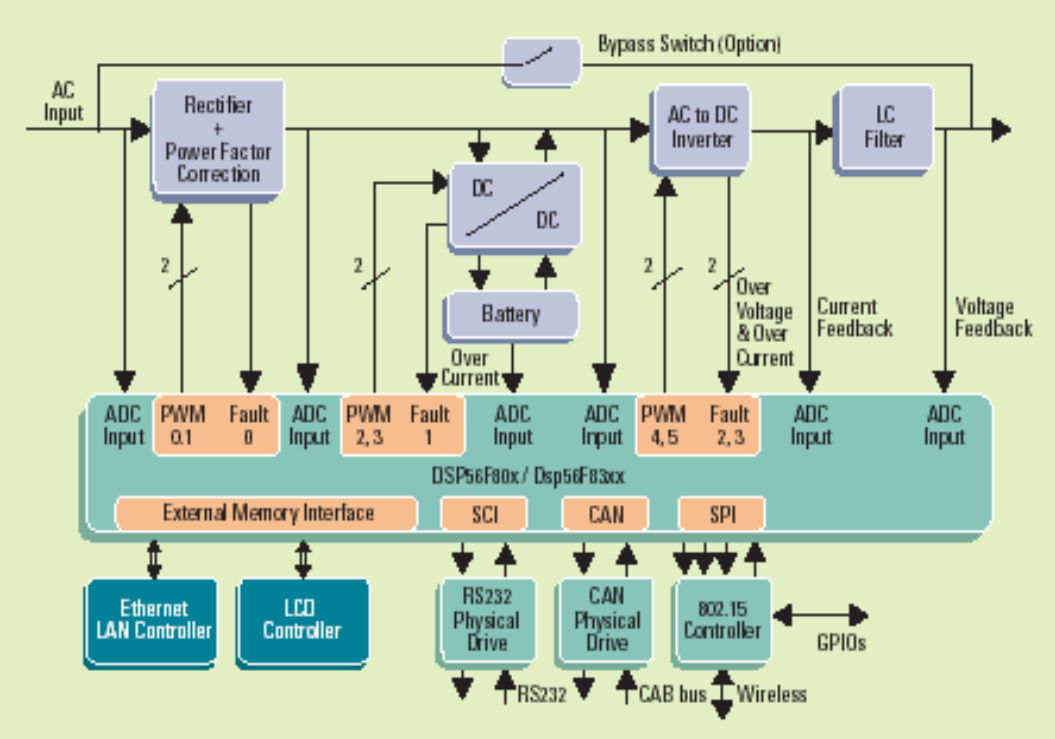
Hardware Implementation

UPS Connectivity

Software Implementation

Competitive Differentiators

Freescale On-line UPS Solution



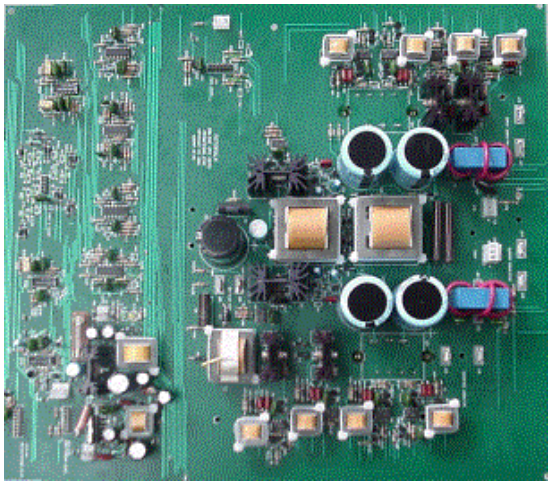
BENEFITS

- Single chip, low cost solution
- Fully digital control
- High input power factor and low power pollution to the power grid
- Advanced battery management, Extended battery life
- Power source and load conditioning that can be monitored and controlled in real time
- Network communication capability
- Low maintenance cost

Single Phase On-Line UPS Using 56F8346

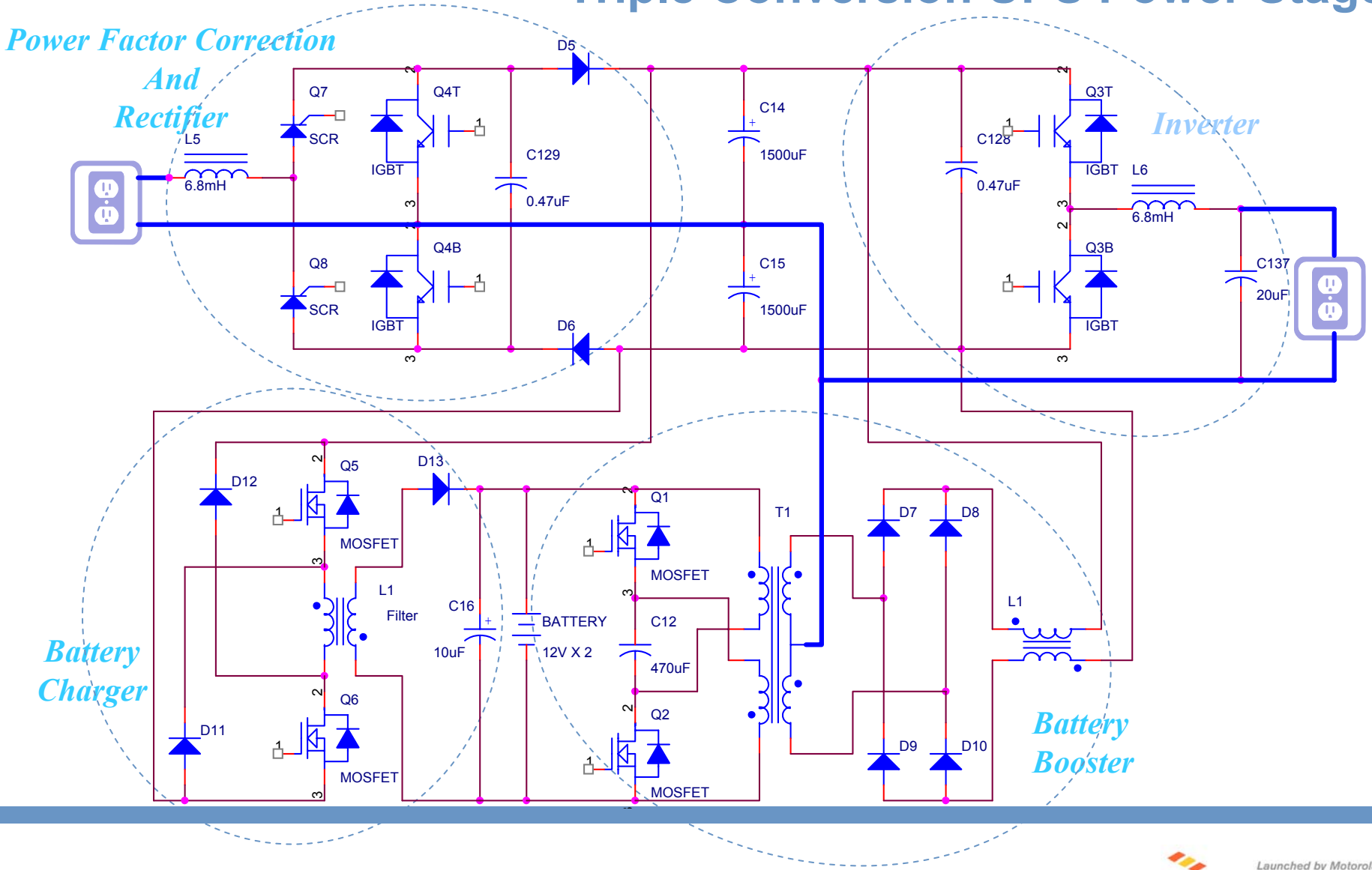
Demo Feature:

- Single Phase Triple Conversion Topology
- 300 VA Output Power
- 120 V or 230 V at 50 Hz/60 Hz Input
- Automatic Synchronizing the frequency of input and output
- Software controlled soft start for PFC and Battery Booster
- Controlled by Hybrid Controller –56F8346
- Communication Ports – RS232 and Ethernet
- Graphical User Interface on PC
- On board LCD display
  - ✓ Input /Output Voltage and Current
  - ✓ Input /Output frequency
  - ✓ Battery Status



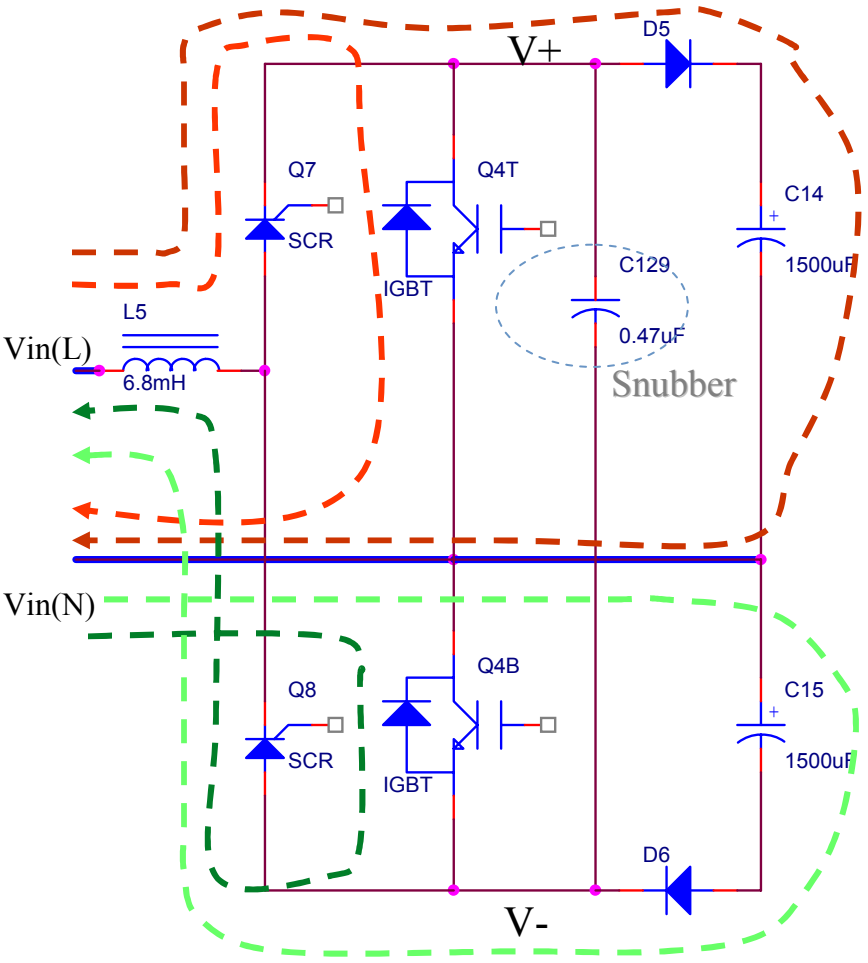
Hardware Implementation

Triple Conversion UPS Power Stage



Hardware Implementation

Power Factor Correction And Rectifier



Functionality:

- •Soft Start
- •Voltage double rectifier
- •Power factor correction

Control technique

- •Full digital controlled PFC
- •PI Control for both Current and voltage loop
- •SCR used to control soft start and as a switch
- •20 KHz switching frequency

PFC Operation

- •Boost operation during input positive half cycle

Q4T on:

➢**Vin(L)→L5→Q7→Q4T→Vin(N): Storing Energy in L5**

Q4T off:

➢**Vin(L)→L5→Q7→D5 → C14→Vin(N): Charging in C14**

- •Boost operation during input negative half cycle

Q4B on:

➢**Vin(N)→Q4B→Q8→L5→Vin(L): Storing Energy in L5**

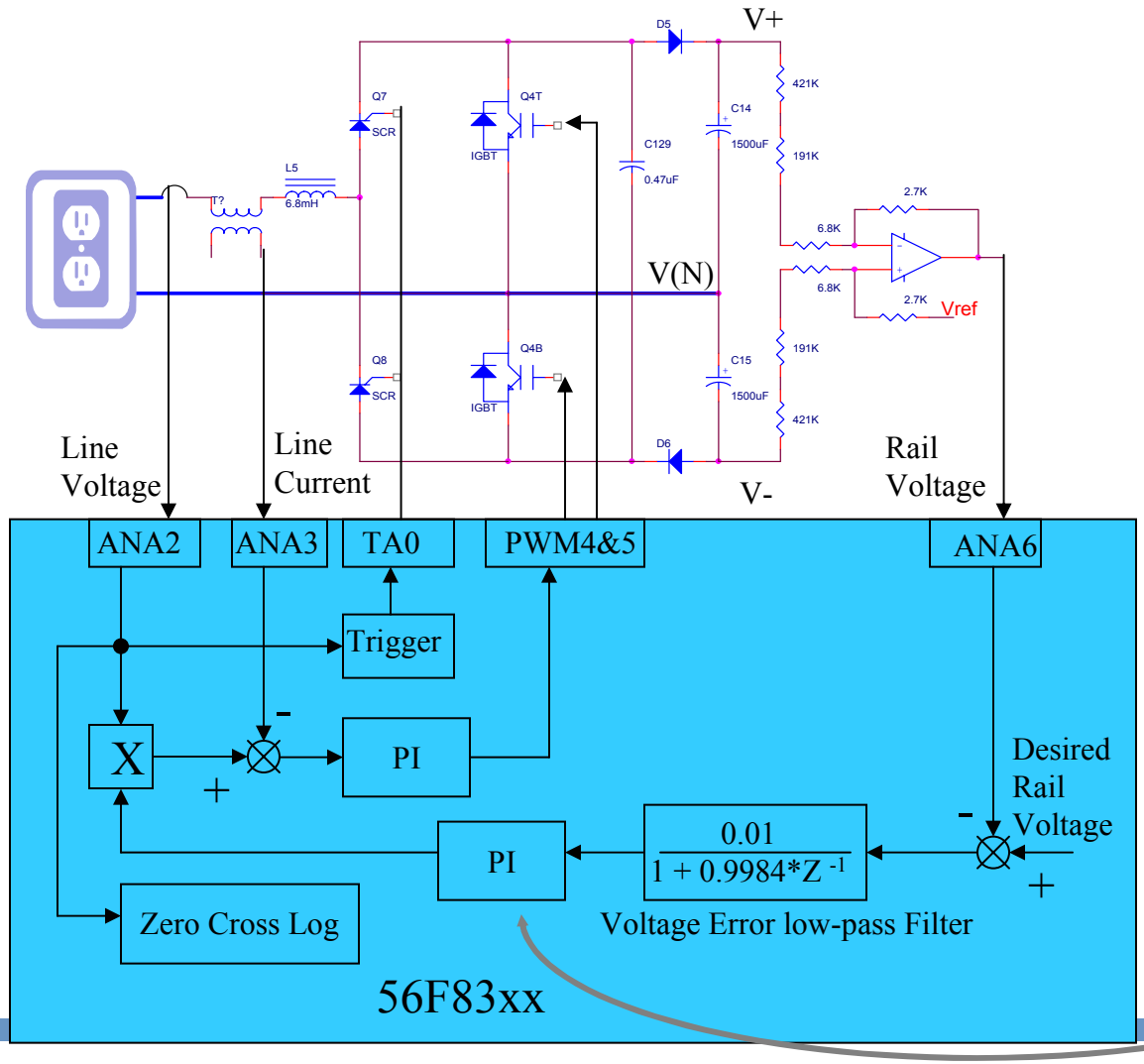
Q4B off:

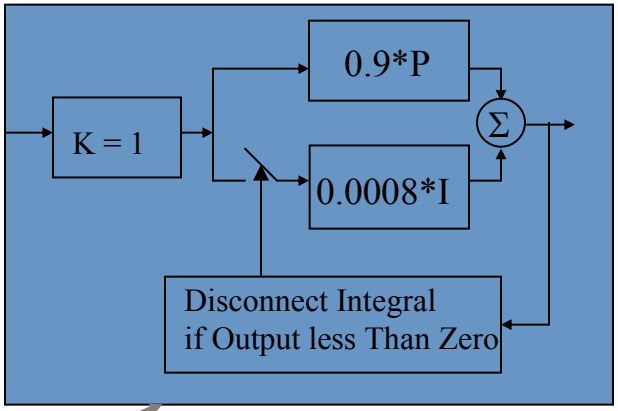
➢**Vin(N)→C15→D6→Q8 → L5→Vin(L): Charging in C14**

Hardware Implementation

Power Factor Correction Control Loop

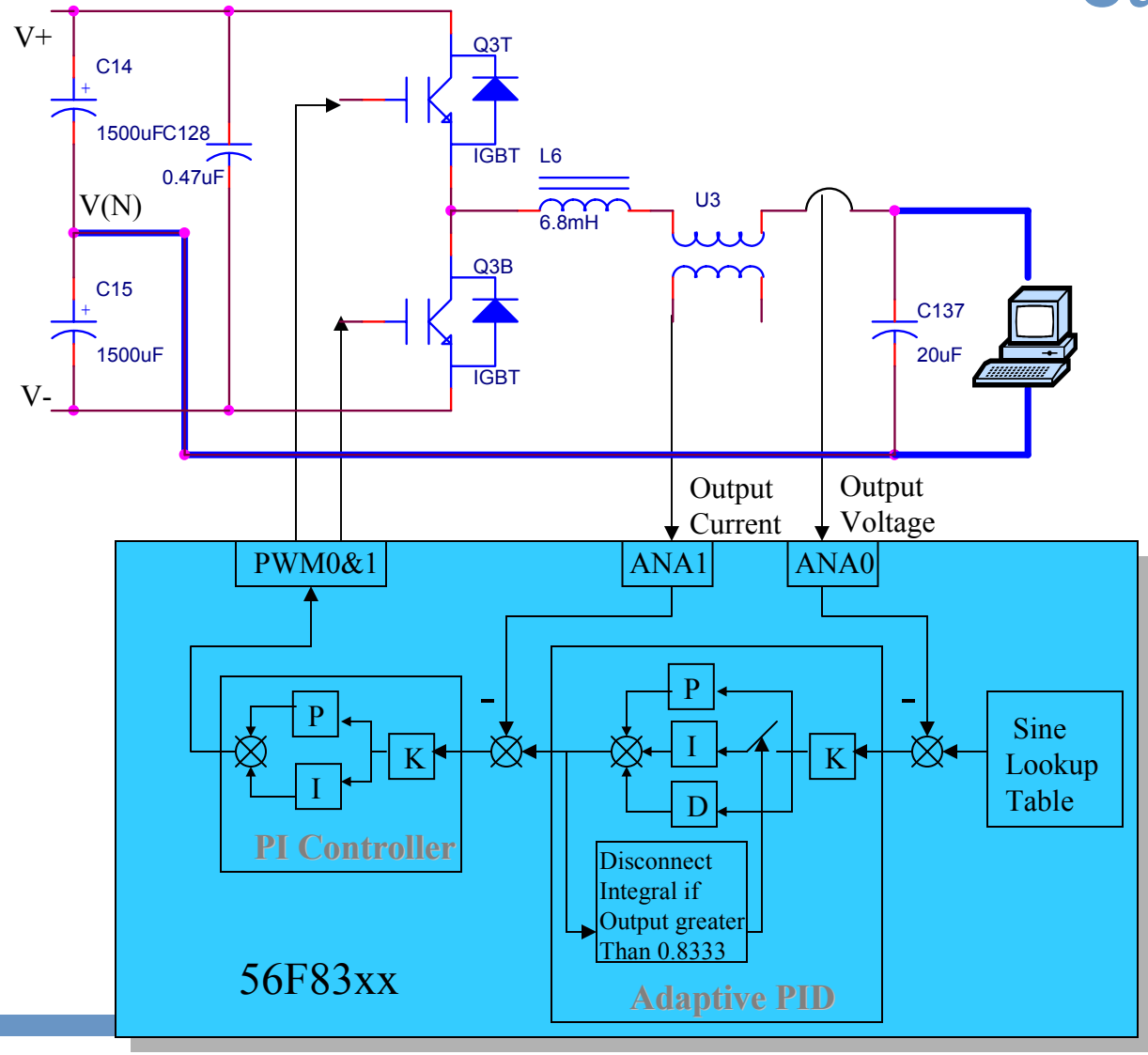
- **Average Current control mode**
  - ✓Best performance
- **20 KHz switching frequency and sampling rate**
- **Fully controlled by DSP**
- **50 μs control loop for both current and voltage**
- **Both control loops used Proportional-Integral Controller**
- **Adaptive PI controller for Voltage loop**





Hardware Implementation

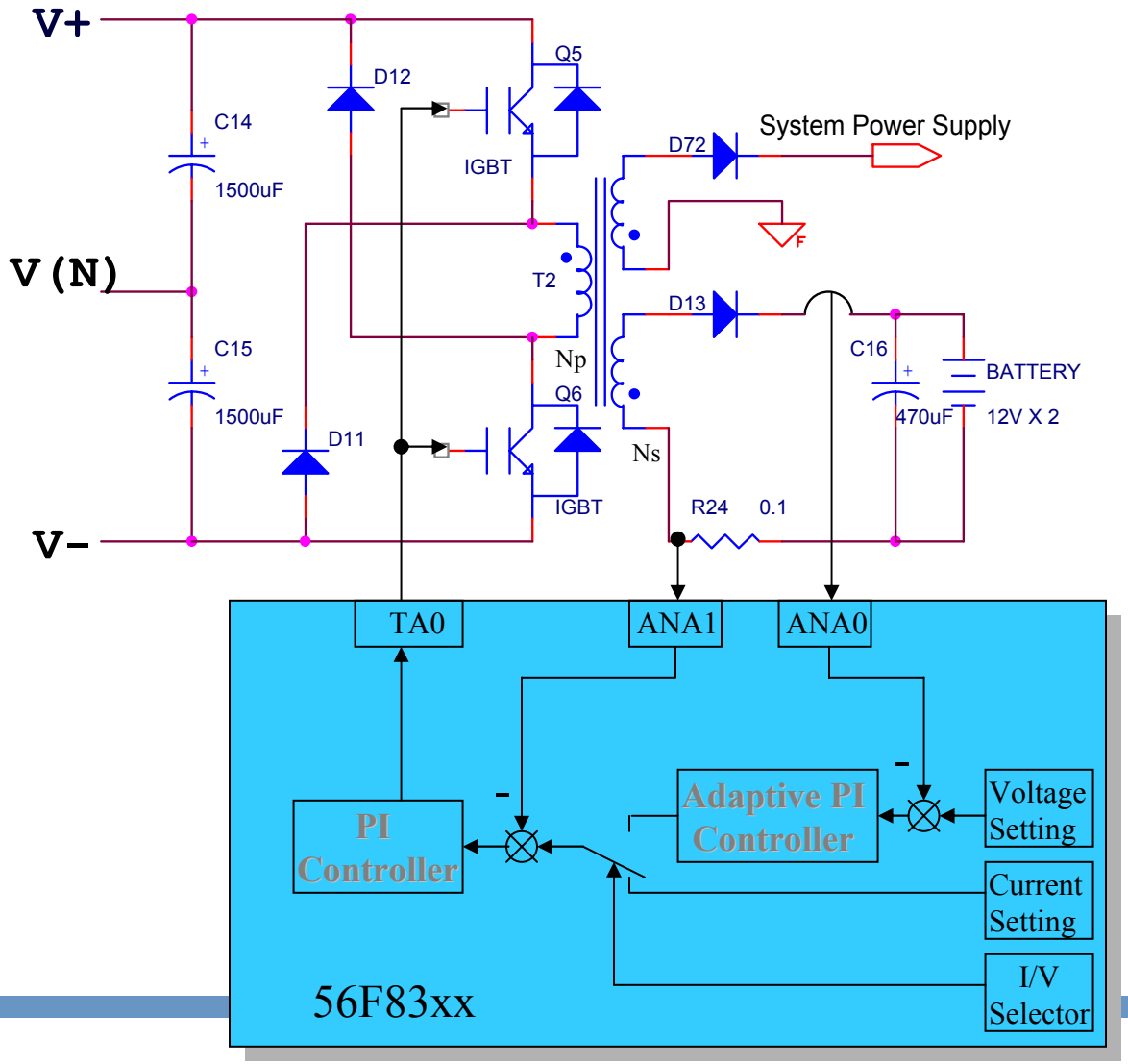
Output Inverter



- Half bridge topology
- Fully controlled by DSP
- 20 KHz switching frequency and sampling rate
- 50 μs control loop for both current and voltage
- Adaptive PID controller for Voltage loop
- Power transistors controlled by two PWM channels in complementary mode
- Three output frequency modes
  - ✓50 Hz;
  - ✓60 Hz;
  - ✓Auto Sensing, which enables output frequency in synchronous with input frequency

Hardware Implementation

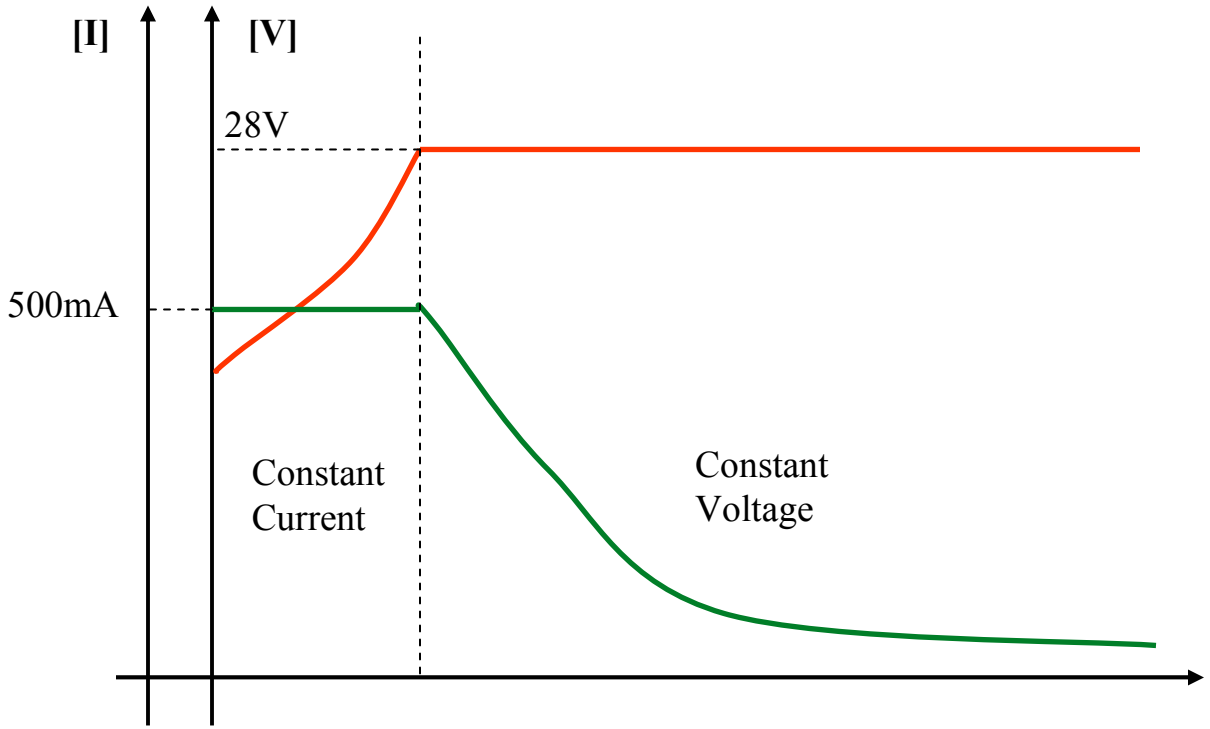
Battery Charger



- **Fully digital controlled Double-Ended Discontinuous Mode Fly back Converter**
  - ✓Lower off-voltage stress applied on Power transistor Q5&Q6
- **Both Power transistors share same control signal**
- **20 KHz switching frequency and sampling rate**
- **PI controller for both current and voltage loop**
- **50 μs Current control loop and 0.8 ms voltage control loop**
- **Output parameters**
  - ✓Output Voltage: 28 Vmax
  - ✓Output Current: 1.0 A max
- **2 State charge scheme**
  - ✓Constant current
  - ✓Constant voltage

Hardware Implementation
Battery Charging Scheme

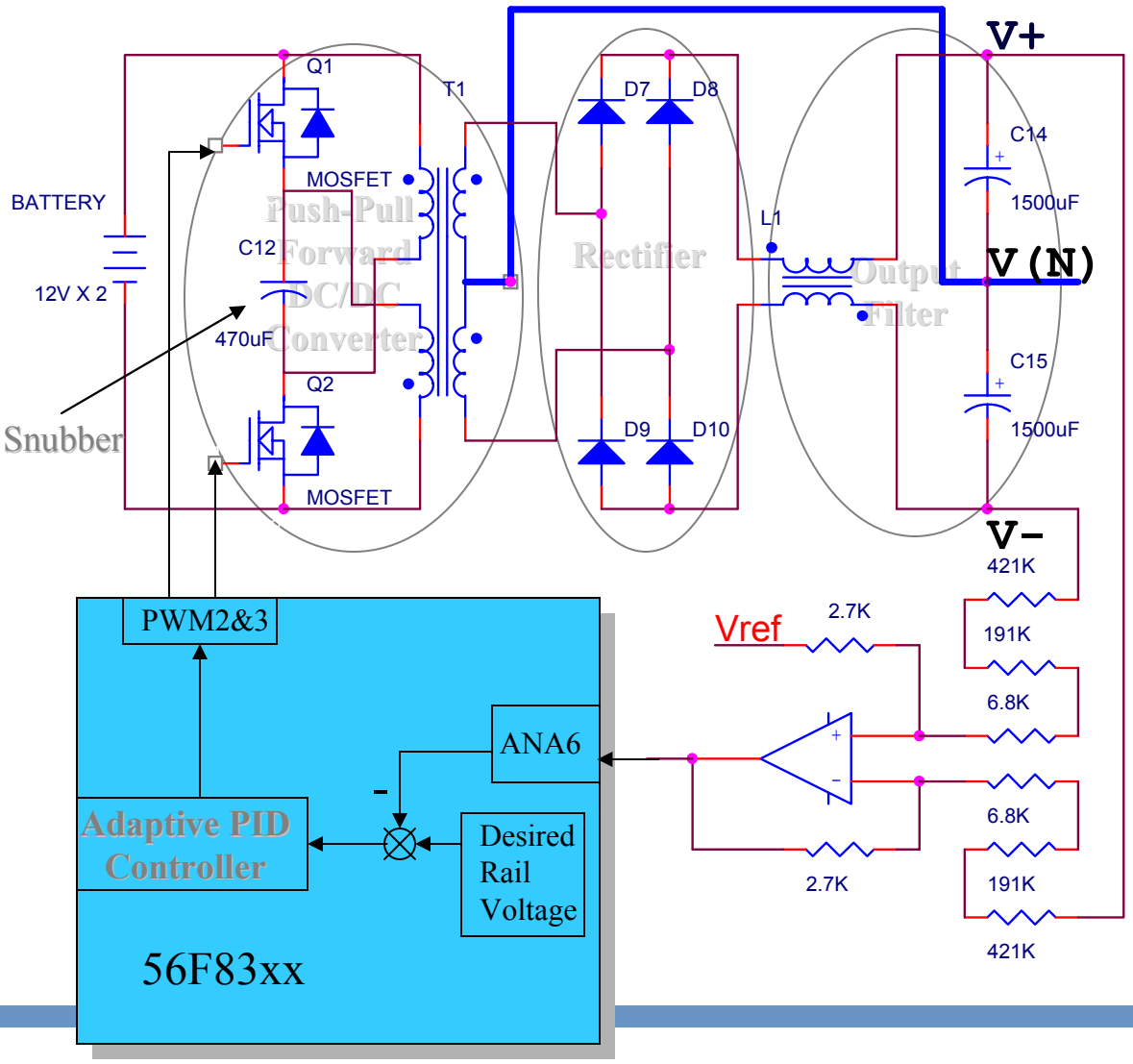
- **2 Step Charging: Constant Current and Constant Voltage**



Battery capacitance is defined as the integral over time of the current supplied to the battery. This information is stored in the system and useful for calculating the time the battery will give power to the system.

Hardware Implementation

Battery Booster



- Fully digital controlled Push-Pull Forward DC/DC Booster
- Convert battery voltage (24 V) to bipolar DC bus voltage (up to +/- 420 V)
- 20 KHz switching frequency and sampling rate
- PID controller for voltage loop with Over current protection
- 0.8 ms control loop
- PWM control signals are a pair of 180° out-of-phase square-wave pulses.
- PWM duty cycle cannot be greater than 50%
- Both PFC and Battery booster share common DC bus voltage measurement sensor
- Output parameters
  - ✓Output Voltage: 420 Vmax
  - ✓Output Current: 500 mA max

Online UPS System with TCP/IP Protocol Agenda

Introduction

Hardware Implementation

UPS Connectivity

Software Implementation

Competitive Differentiators

On-line UPS Connectivity

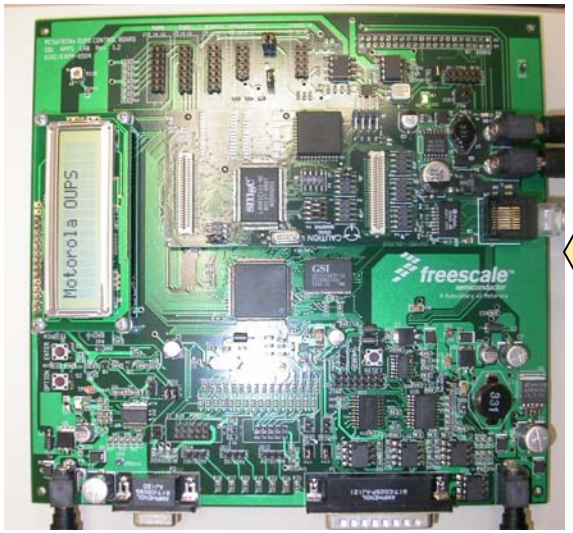
Freescale On-line UPS Solution more than an UPS!!

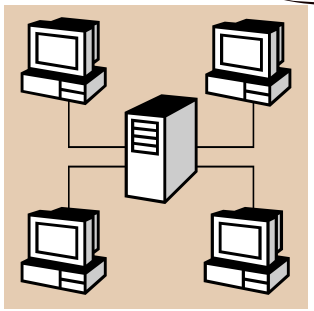
Why keep worrying about physically supervising your System when you can do it REMOTELY?

•The UPS can be connected to an internal network or to Internet:

- **It allows you to monitor the condition of your system remotely using a network**
- **It can send e-mails when there is a malfunction, so you can be sure you are the first to know when there is a problem**
- **A remote database can gather data from several UPS for an automatic monitoring system**
- **The service provider can perform maintenance of the system automatically, remotely and easily**

How does it work?



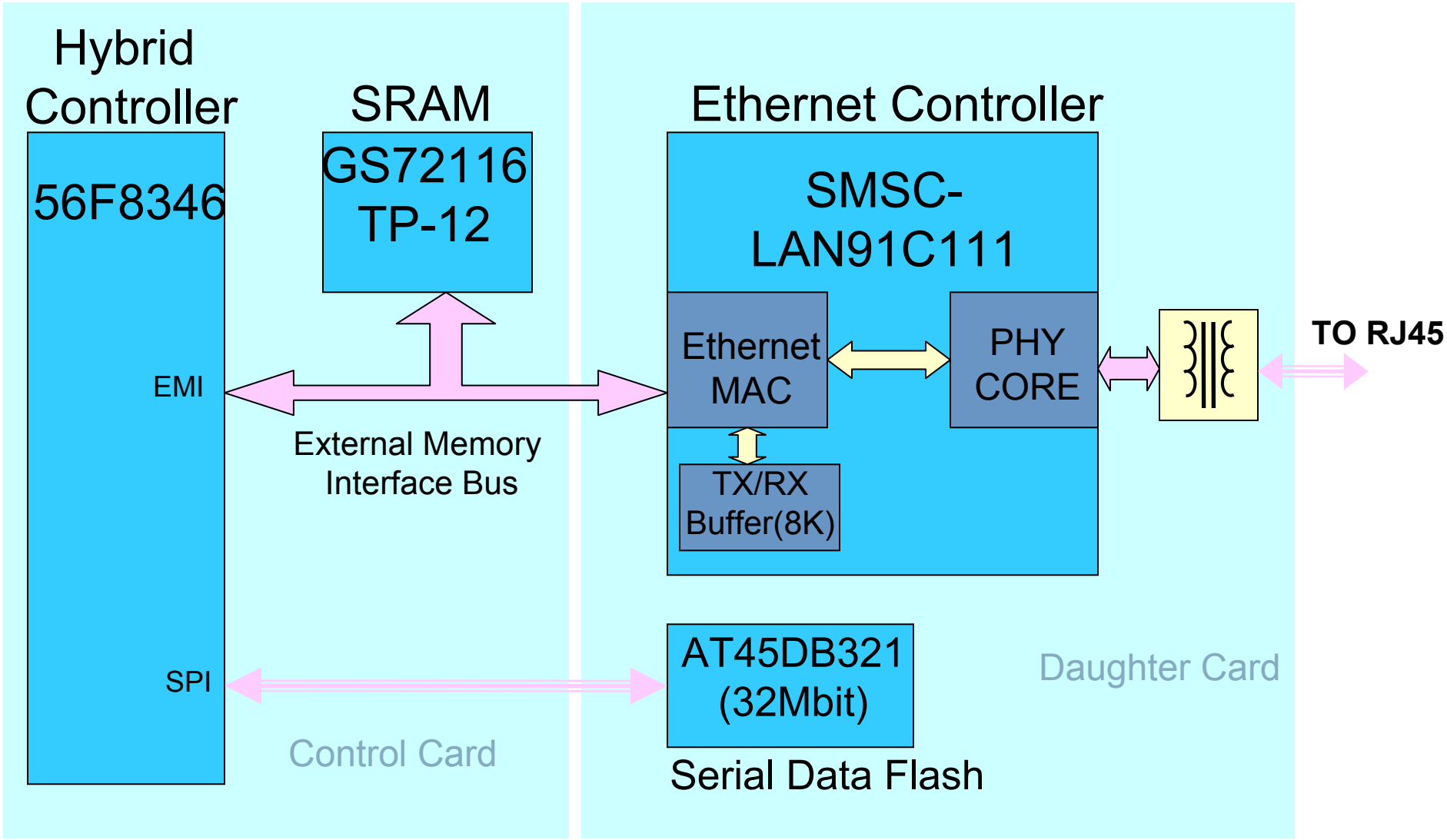


- UPS continuously updates its information (Voltage, Current, Battery charge…)
- If a request is received, it will respond according to the protocol
- If a fail is detected, it will send an email

- Information travels through Ethernet connection to the internal network or Internet

- The user or technical support center can request data, verify status in html pages and receive e-mails in case of failures.
- Servers can automatically receive and analyze this information.

On-line UPS Connectivity Hardware



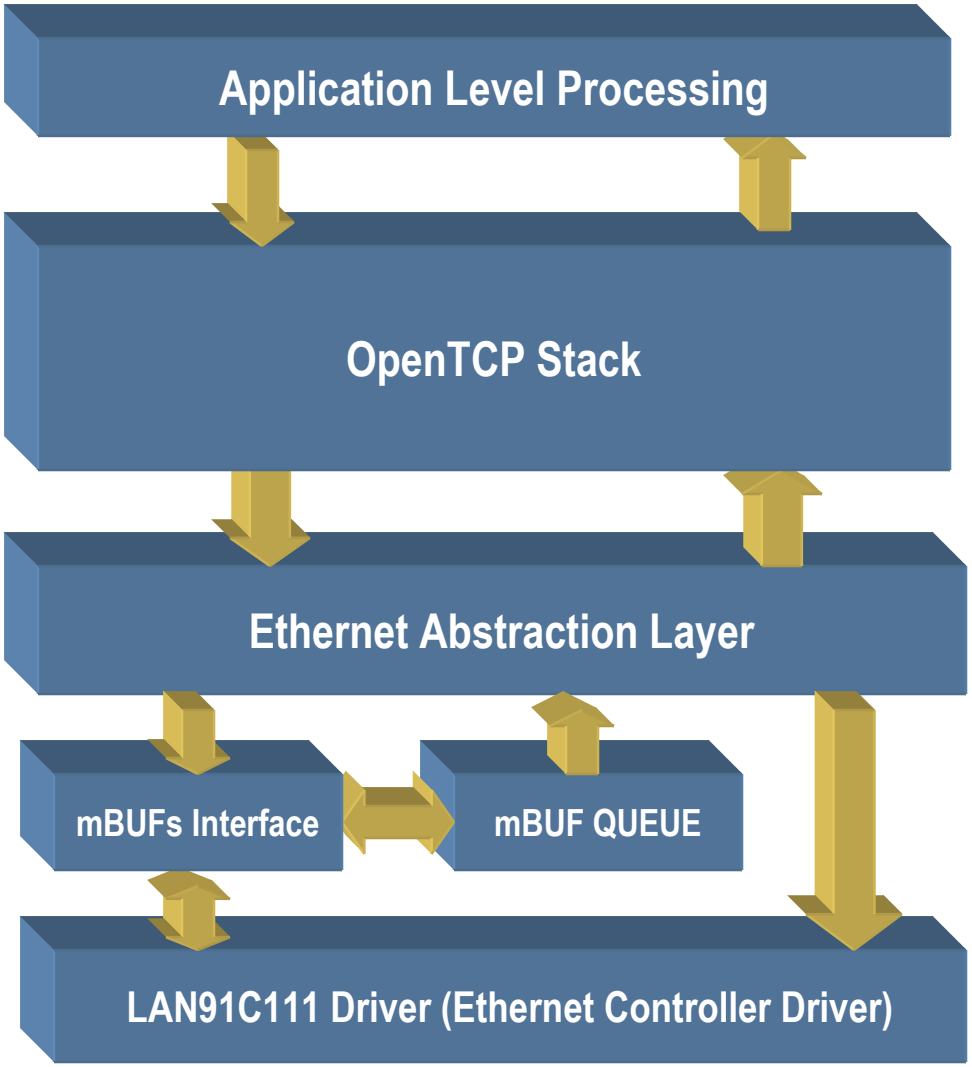
On-line UPS Connectivity Software

UPS uses a world-class, highly-reliable, highly-robust TCP/IP stack:

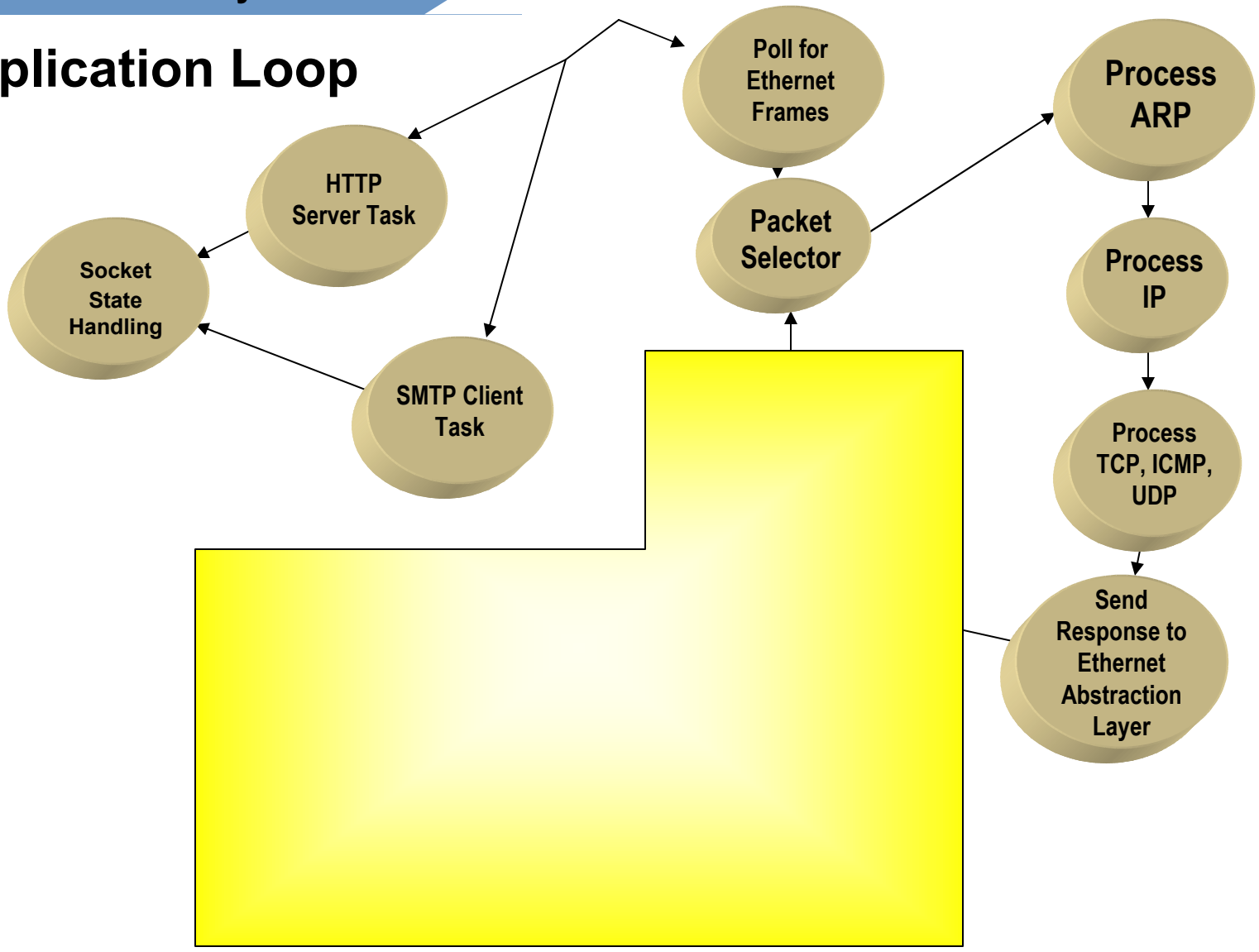
This provides key features to the UPS:

- **Standard software, which can be adapted to the user needs**
- **Support for several application protocols like: TFTP, Telnet, HTTP, SMTP, POP3…**
- **Proven robustness**
- **More information on OpenTCP can be found at http://www.opentcp.org/**

Implementation of OpenTCP for the DSP568F346



Main application Loop



Connectivity Performance

With minimum CPU time the Connectivity Software can:

•Respond ping requests

- **Send HTML pages**
- **Send e-mail messages**

- **And the possibilities are endless!!**

Online UPS System with TCP/IP Protocol Agenda

Introduction

Hardware Implementation

UPS Connectivity

Software Implementation

Competitive Differentiators

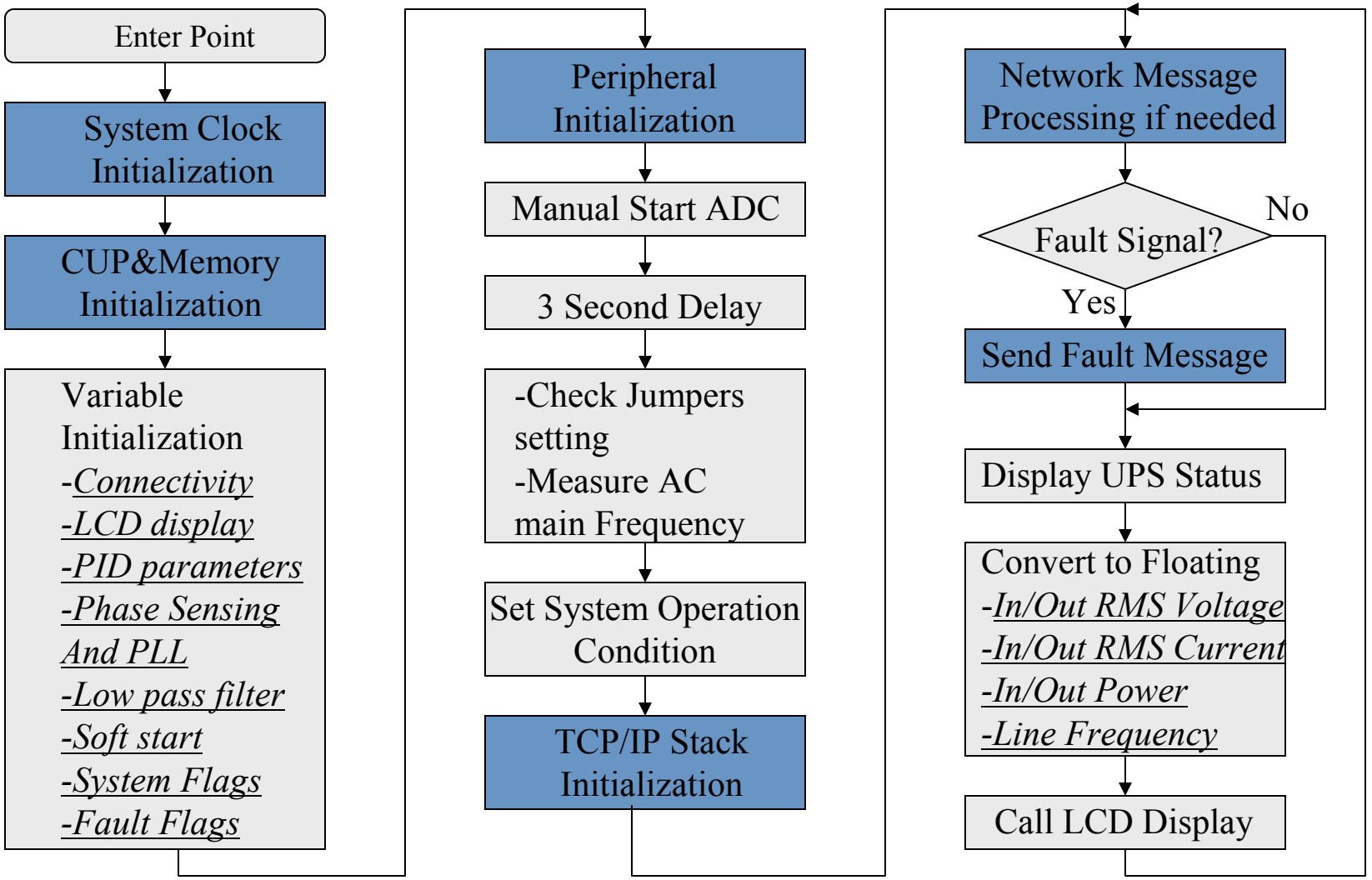
Software Implementation

Software Functions

- ✓ Initialization and Main loop
- ✓ Five UPS event interrupts
  1. ADC End-of-Scan interrupt
  2. Inverter over current interrupt (PWM Fault0)
  3. Rectifier/PFC over current interrupt (PWM Fault1)
  4. Battery booster over current interrupt (PWM Fault2)
  5. 50 ms periodical interrupts
  6. Three Communication & Input event interrupts
  7. SCI interrupt for PC master
  8. Two GPIO input interrupts
- ✓ Software written in C
- ✓ Critical algorithm written in Intrinsic Functions and PESLs and Micro
- ✓ Plug-in TCP/IP communication protocol

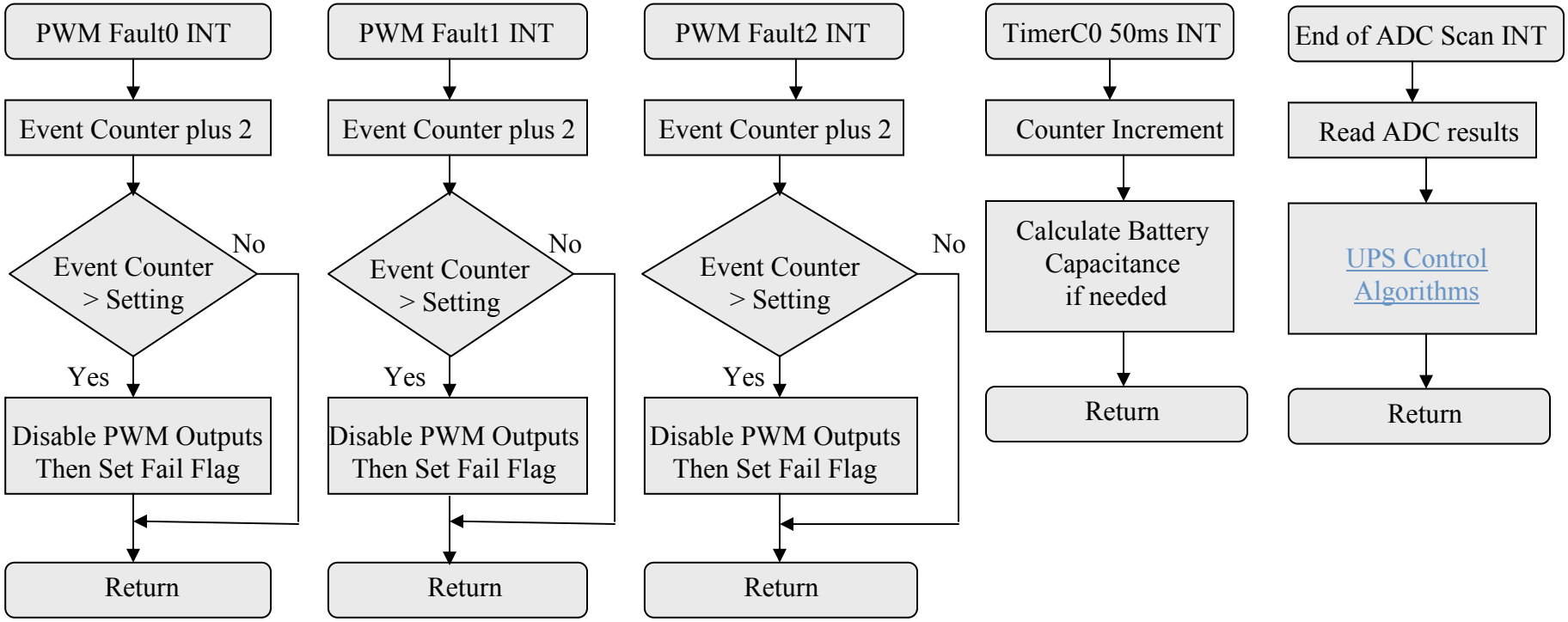
Software Implementation

Software Flowchart – Main



Software Implementation

Software Flowchart - Interrupts



Online UPS System with TCP/IP Protocol Agenda

Introduction

Hardware Implementation

UPS Connectivity

Software Implementation

Competitive Differentiators

Technical Differences For Online UPS Applications Between DSP and MCU

56F83xx Hybrid Controller

- Full digital control system
- Digital controlled direct PFC
  - Predictable switching frequency
  - Less harmonics
- Digital controlled battery charger
  - programmable charge scheme which can contain customer IP for various type batteries and extend battery life.
  - Advanced battery management
- Simple battery booster
- **RS232 , CANBus, TCP/IP protocol**
- input voltage : 120 V version or 220 V version
- Universal input operating frequency 47.5 Hz – 63 Hz
- Has bandwidth for future expansion

• 16-bit Microcontroller

- Mixed digital + analog control
- Analog controlled indirect PFC
  - Unpredictable switching frequency
  - Rich harmonics
- Analog controlled battery charger
  - Constant voltage with current-limit charge scheme which only fit for lead acid battery
  - Battery management inapplicable
- Simple battery booster
- RS232 only
- input voltage : 120 V version or 220 V version
- Universal input operating frequency 45 Hz – 65 Hz
- No bandwidth for future expansion

56800/E Hybrid Controller Roadmap

Features

56850 Series
Telecom/voice processors,
RAM-based, 120 MMACS,
Up to 80KB PRAM,
81–144 pins

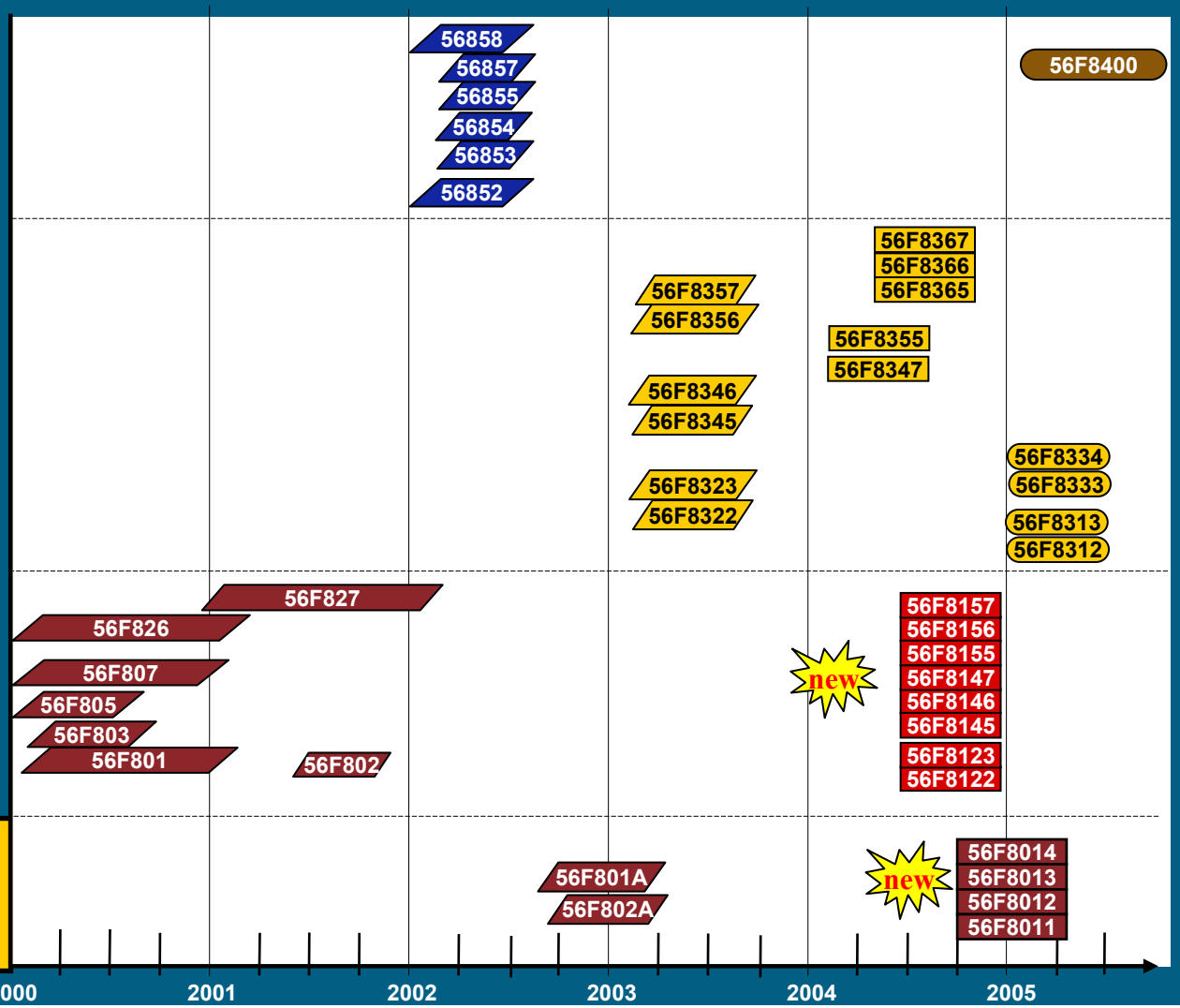
56F8300 Series
Automotive & Industrial,
Flash-based, 60 MMACS,
40-528KB PFlash,
48–160 pins

56F8100 Series
Industrial,
Flash-based, 40 MMACS,
40-528KB PFlash,
48–160 pins

56F820 Series
General Purpose,
Flash-based, 40 MMACS,
64 -130KB PFlash,
100–128 pins

56F8000 Series
Automotive & Industrial,
Flash-based, 32 MMACS,
12-16KB PFlash,
28-32 pins

56F800 Series
Industrial controllers,
Flash-based, 30-40 MMACS,
20-128KB PFlash,
32–160 pins



Proposal
Planning
Execution
Production

0.18µ, 56800E
120 MMACS

0.18µ, 56800E
120 MMACS

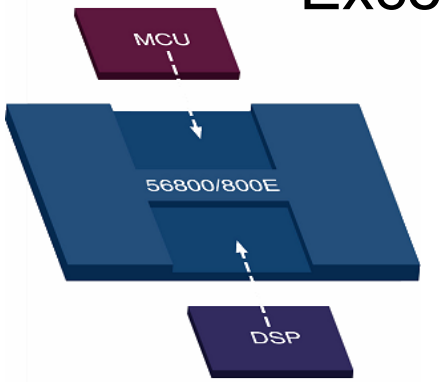
0.25µ, 56800E
60 MMACS

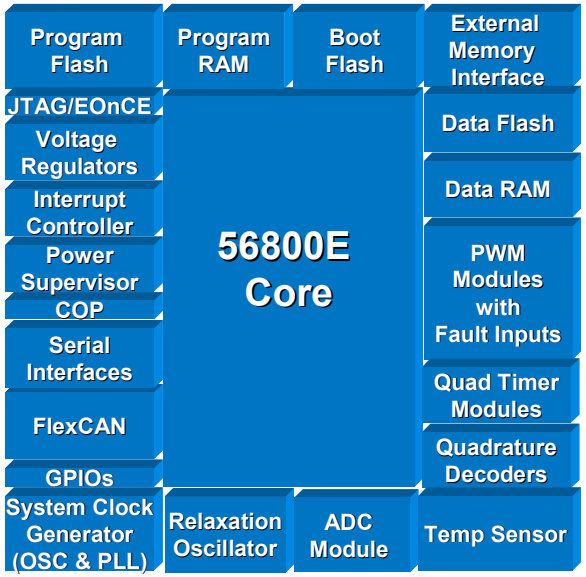
0.25µ, 56800E
40 MMACS

0.25µ, 56800
30/40 MMACS

Launched by Motorola
freescale semiconductor

Exceptional Performance



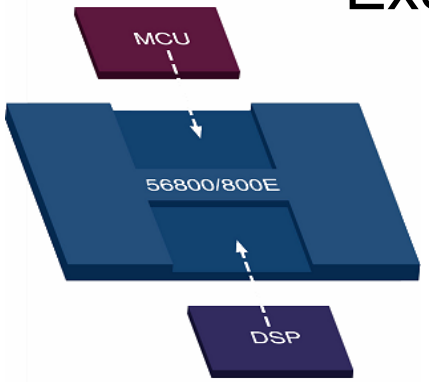


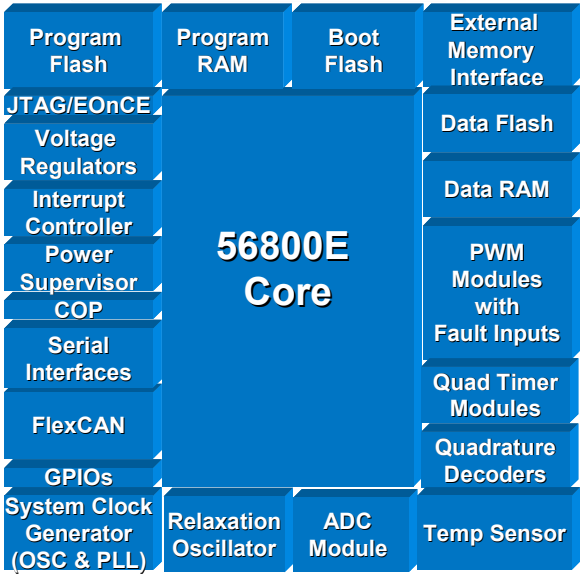
Package: From 48 up to 160 pin LQFP

- Sustained 60 MHz/MIPs processing from Flash
- Superior Code Density and Code Efficiency
- MCU features:
  - **Bit manipulation, 8/16/32bit native data types, fast interrupts enhance control code**
- DSP features:
  - **Dual Harvard Architecture, zero overhead interruptible looping, and circular buffers enhance signal processing**
- Superior 32-bit performance provided by the internal 32-bit-wide buses and registers while providing linear memory space of 4 MB program and 32MB data
- Feature rich peripherals such as 12-bit ADCs, 16-bit PWM, flash security, and multiple serial communication choices (SCI, SPI, CAN).
- Dedicated Interrupts for standard peripheral features increasing real-time performance.

Launched by Motorola freescale semiconductor

Exceptional Reliability





Package: From 48 up to 160 pin LQFP

Industry-Leading high volume, extended temperature, 3rd generation flash.

- **From the company that invented the technology**

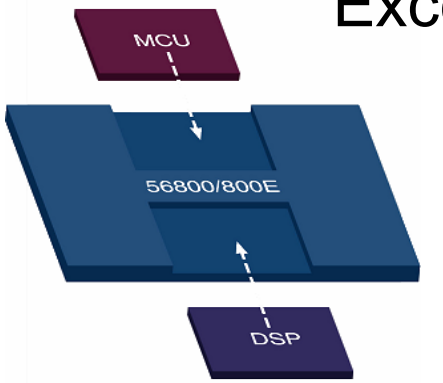
Production Qualified devices meeting the highest design and test specs ensuring proper operation in the harshest environments

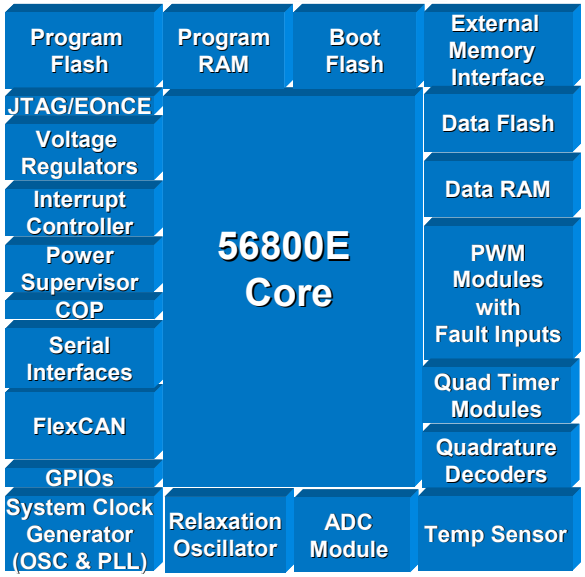
Industry-Leading Safety Features

- **PWM – write protected registers, multiple fault inputs**
- **Power supervisor – POR, Low Voltage Interrupts**
- **OCCS – Loss of clock/lock**
- **Temperature sensor**
- **COP – run-away code recovery**
- **Decoder – zero speed watchdog**
- **Flash – protection and security**

Launched by Motorola freescale semiconductor

Exceptional Integration

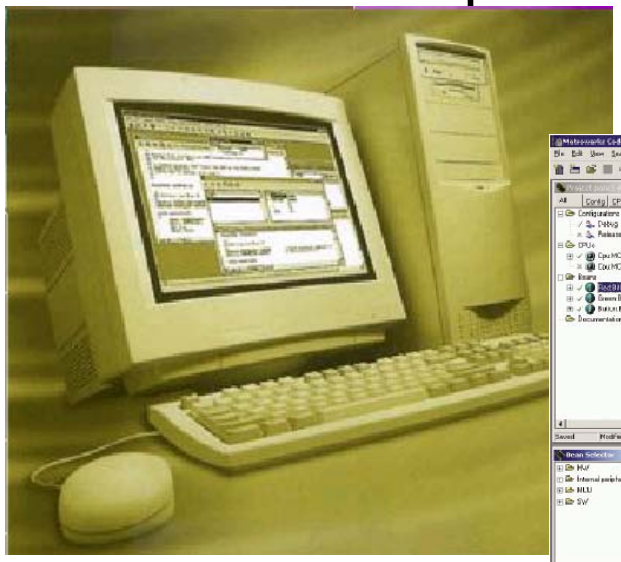


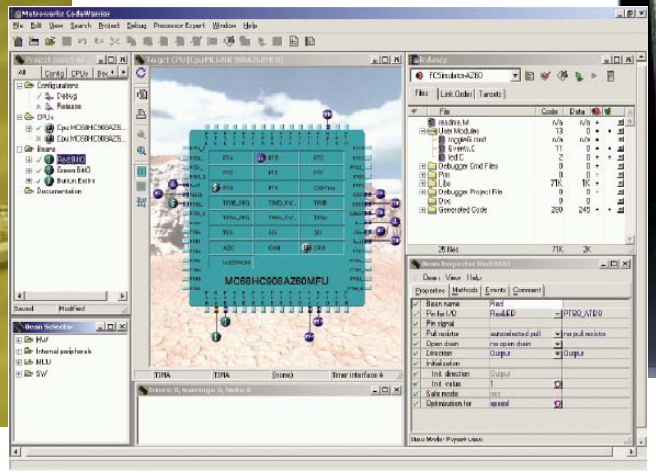


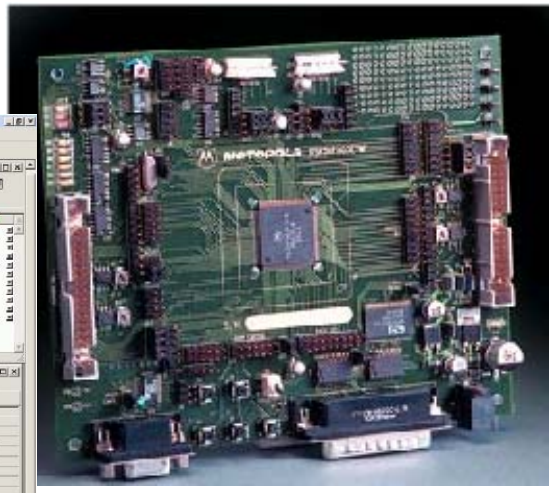
Package: From 48 up to 160 pin LQFP

- Large system cost savings from…
  - **Internal Program and Data Flash**
  - **On-board voltage regulation**
  - **Internal oscillator, factory tuned, highly accurate**
  - **EEPROM emulation using on-chip FLASH**
  - **Glueless EMI and digital I/O**
  - **Independent, highly sophisticated peripherals**
- Broad and expanding product portfolio ensures that you pay for only the features you need today while ensuring a path to your future

The Complete Development Environment







CodeWarrior™ for 56800/E

CodeWarrior for Motorola 56800/E is a windows based visual IDE that includes an optimizing C compiler, assembler and linker, project management system, editor and code navigation system, debugger, simulator, scripting, source control, and third party plug in interface.

Processor Expert™

Processor Expert (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system. PE is fully integrated with the CodeWarrior for 56800/E.

Hardware Tools

The 56800/E solutions are supported with a complete set of evaluation modules which supply all required items for rapid evaluation and software and hardware development. In addition several command converter options exist for customer target system debugger connection.

Launched by Motorola freescale semiconductor

Processor Expert Overview

Processor Expert™

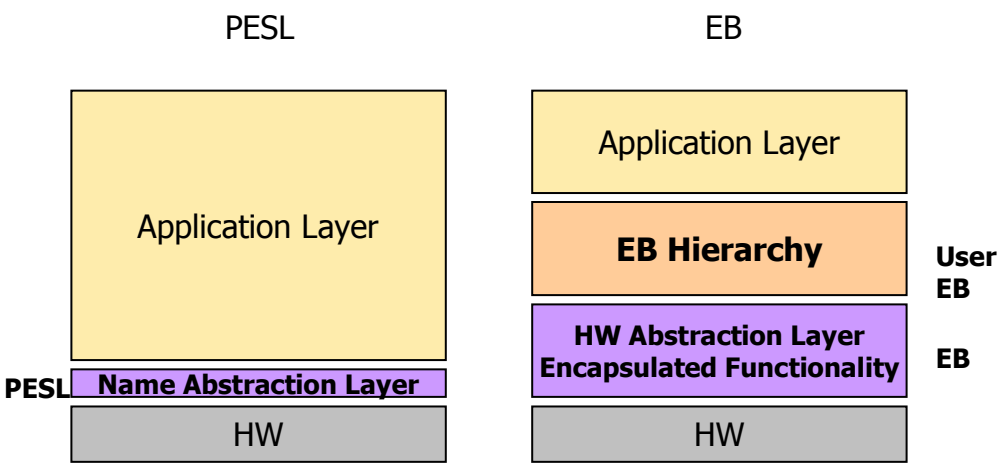
- Supports rapid application development
- Enables component oriented programming
- Provides expert advice if necessary
- Delivers instant functionality of generated code
- Provides tested ready-to-use code

Key Abstraction Technologies

- **PESL**
  - Processor Expert System Library
  - Peripheral oriented
- **EB – an abstraction provider**
  - Embedded Beans
  - Functionality oriented
  - Real *components* for building of an application

How Features of PE are Achieved

- Developed by experienced programmers of embedded systems
- Expert knowledge system is working on the background of PE and checks all the settings
- Provides context help and access to CPU/MCU vendor documentation
- All EB delivered by UNIS are tested according to ISO testing procedures (UNIS is ISO certified company)



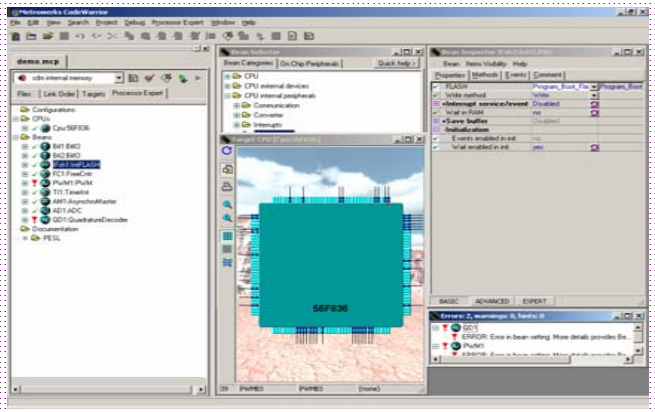
Processor Expert Features

Available across 8/16-bit product lines
Rapid application development

Expert configuration system
Instant functionality of generated code
Two Peripheral programming levels
- Embedded Beans
- PESL

Application Specific Algorithm Libraries
- All SDK algorithm libraries ported

Tested and ready-to-use code



Application Specific Algorithm Libraries

Memory Manager
- Dynamic allocation

Feature Phone Library
- CallerID type 1&2, CallerID Parser, Generic Echo Cancellor

DSP Library
- FIR, IIR, FFT, Auto Correlation, Bit Reversal

Telephony Libraries
- AEC, AGC, Caller ID,
- CAS, CPT, CTG, DTMF
- G165, G168, G711
- G723, G726, G729

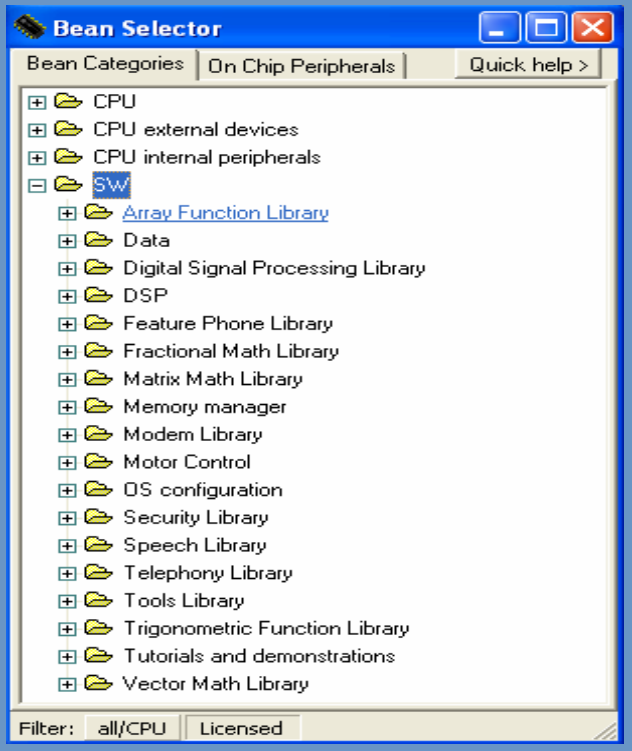
Modem Libraries
- V.8bis, V.21, V.22bis, V.42bis

Security Libraries
- RSA, DES, 3DES,

Motor Control
- BLDC, ACIM, SR motor specific algorithms
- General purpose algorithms

Math Libraries
- Matrix, Fractional, Vector
- Trigonometric

Tools Library
- Cycle Count, FIFO, FileIO, Test



Conclusion

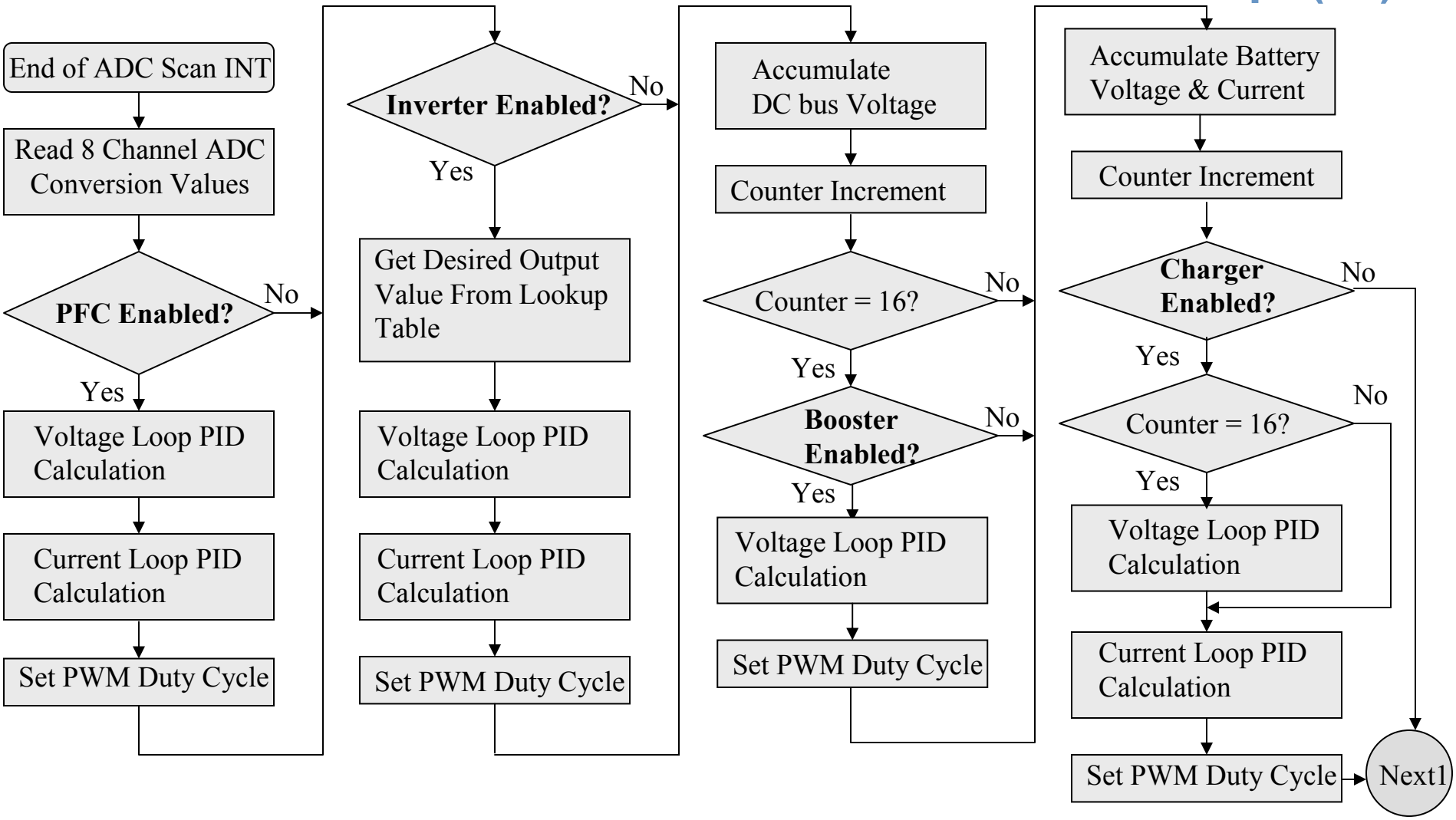
- This reference design demonstrates a complete hardware and software solution for On-line UPS by using Freescale's DSP which simplify circuitry with low component count.

- 56800/E Hybrid controllers are well suited to a broad range of Power Electronics application including UPS; Power supply; Inverter.

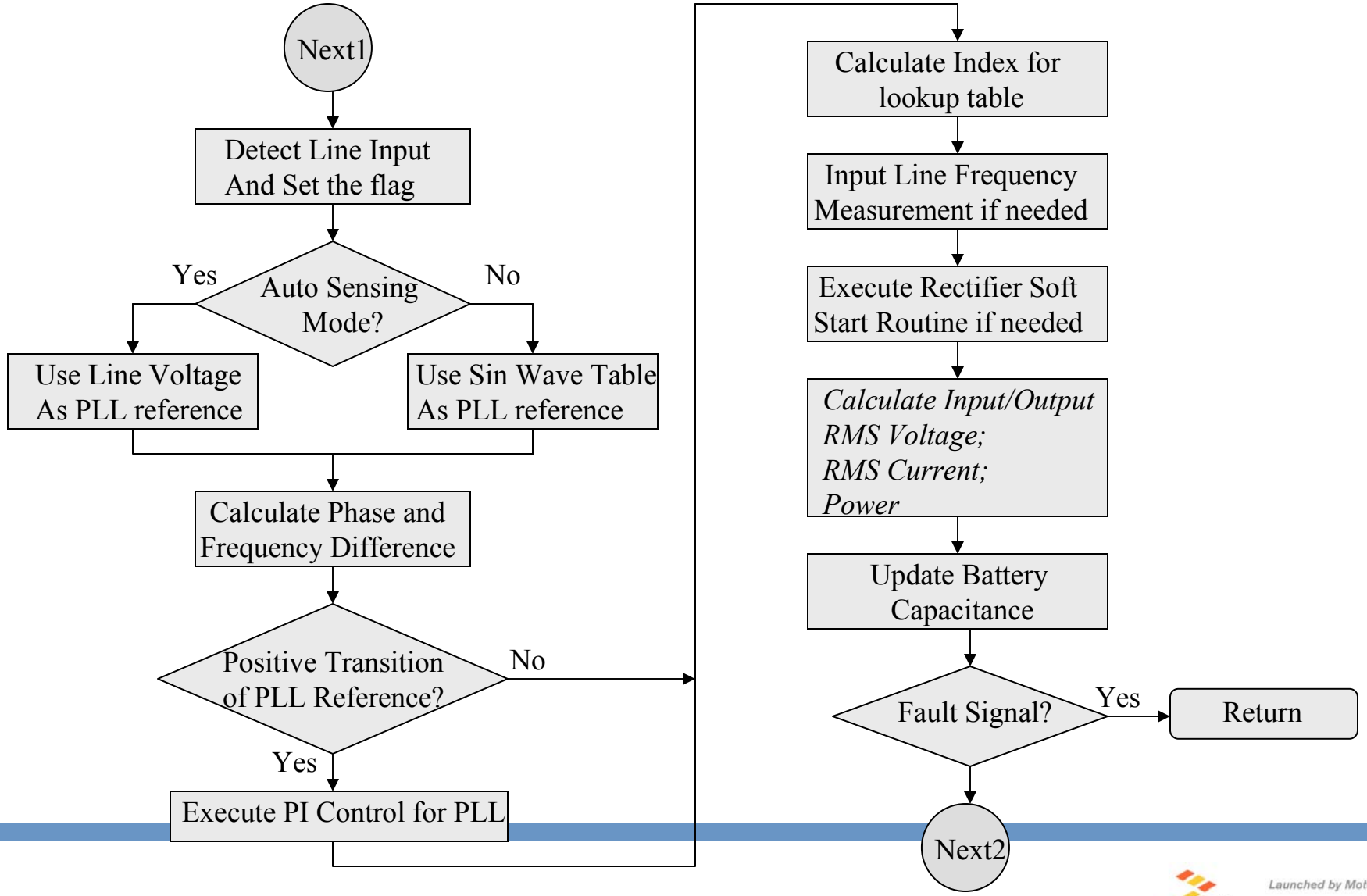
- Very powerful CodeWarrior and Processor Expert development environment accelerates development cycle.

Back Up

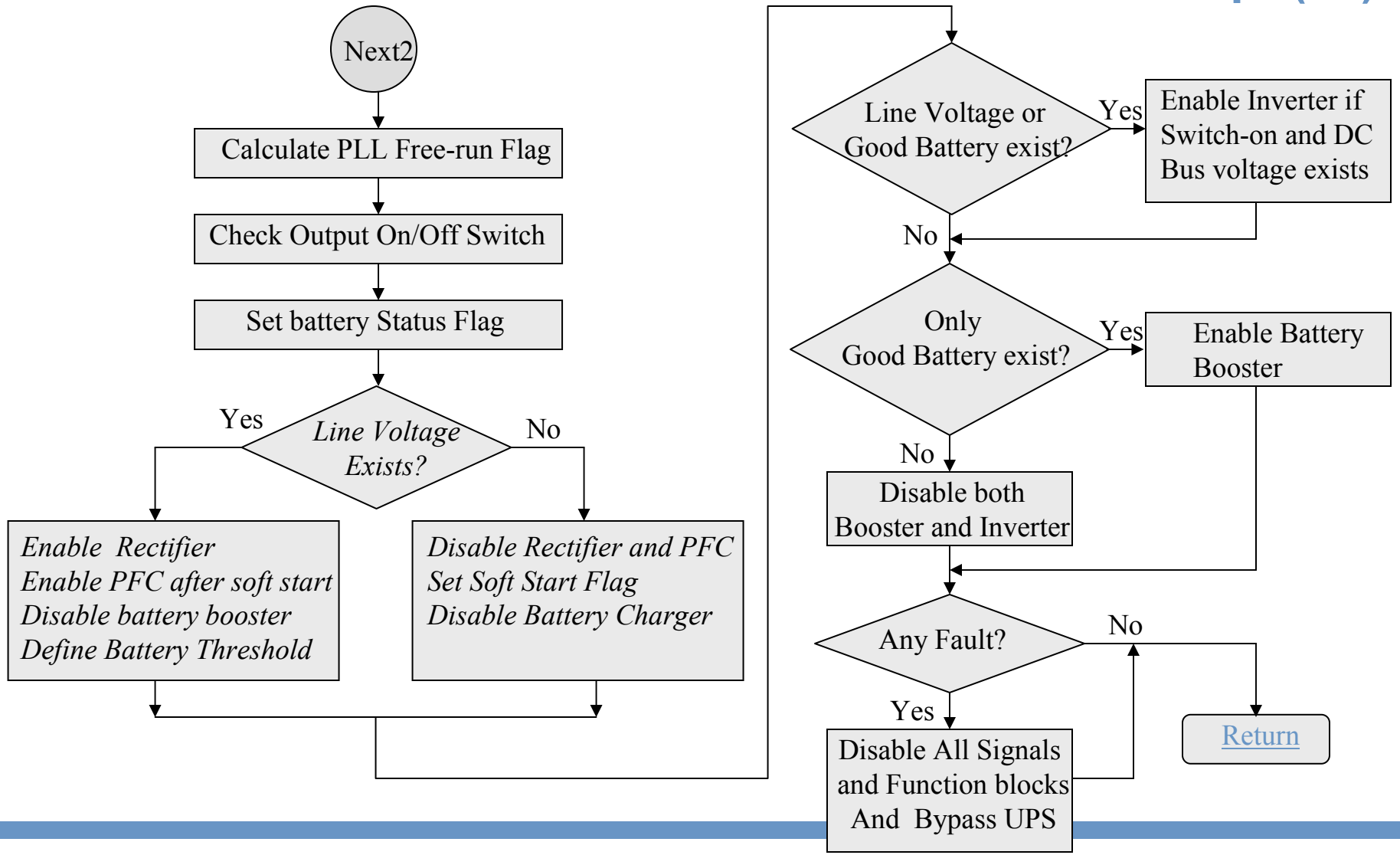
Software Flowchart – ADC Interrupt (1)



Software Flowchart – ADC Interrupt (2)



Software Flowchart – ADC Interrupt (3)



56F8300 Core Differentiators

56F8300	Benefit of 56F8300
✓ More MCU-like general purpose register files that include four 36 bit Data Accumulators and three 16 bit data registers	Improved code density enabling more efficient use of memory and faster execution. Improved signal processing performance.
✓ Complete MCU-like bitwise logic and bit manipulation instruction set	Improved code density and execution speed of control and protocol processing code
✓ Supports two circular buffers with size up to 16K words or double words	Improved signal processing performance. The 56F8300 can provide greater than six times the signal processing power.
✓ Supports native integer and fractional arithmetic with saturation logic	Improved and more flexible signal processing performance. The 56F8300 can provide greater than six times the signal processing power.

56F8300 Core Differentiators

56F8300	Benefit of 56F8300
✓ Support for two zero overhead do-loops.	Improved signal processing performance and flexibility
✓ True single cycle MAC and dual read capability provided by Dual Harvard Architecture.	Improved signal processing performance
✓ Low latency for standard interrupts and support for two fast interrupts	Improved control code performance
✓ Native 8-, 16-, 32-bit data types with bus width support	Improved code density and execution speed of control and protocol processing code and better support for 32 bit processing
✓ True software stack with arbitrary depth and location.	Supports unlimited function calls and nested interrupts

56F8300 Chip Differentiators

56F8300	Benefit of 56F8300
✓ 56F8300 family has very diverse memory size offering both larger and smaller amount of total memory	Pay for just the memory you need now, while enabling further growth through a set of pin and feature compatible devices
✓ Data flash page size at 256 words enables EEPROM emulation using Flash memory.	EEROM emulation using data Flash memory lowers systems cost by eliminating need for external EEPROM.
✓ Family includes devices with highly accurate factory trimmed internal relaxation oscillator.	Lower system cost and higher reliability by eliminating components
✓ Safety features such as loss of clock/lock detection, write once registers on critical PWM registers, and on chip temperature sensor	Improved and fault tolerant performance in safety critical applications. Will pass safety tests such as the cut crystal test.

56F8300 Chip Differentiators

56F8300	Benefit of 56F8300
✓ 56F8300 supports independent peripherals, Quad timer, Quadrature Decoder, PWM module, which are used for embedded control	Customer gets more feature rich peripherals that can be used in a more flexible independent fashion enabling simpler, speedier, and verifiable system/software designs
✓ On-chip voltage regulators, POR, and low voltage detection.	Customer gets simpler less expensive system by the elimination of external components.
✓ Digital I/Os are 5V tolerant which gluelessly interface to the 5V system.	Simplify system by easing use of 5 volt devices and interfaces
✓ ADC offers high performance and excellent resolution, 12 bits and 1.2 usec conversion rate, and has more features such as Signed or Unsigned result; Zero Crossing Detection, Over Limit Detection, Signal Ended or differential inputs, and self calibration.	Better ADC performance enabling more applications with simpler software

56F8300 Chip Differentiators

56F8300	Benefit of 56F8300
✓ 56F8300 is a Flash based device enabling true single chip operation	56F8300 does not require external memory storage to boot from saving on system cost.
✓ 56F8300 has Flash security enabling customers to disable external access to memory	56F8300 provides excellent protection of customer IP
✓ 56F8300 devices supporting external memory interface can access external memory at 60 Mhz	56F8300 external memory interface is very flexible enabling customers to simplify their design and operate at higher performance
✓ Select 56F8300 devices can support two three phase motors	56F8300 offers lower system cost by requiring fewer devices

56F8300 Chip Differentiators

56F8300	Benefit of 56F8300
✓ Flash has excellent endurance of 10,000 worst case and 100,000 typical erase/program cycles	Much greater flexibility using the 56F8300 flash
✓ 56F8300 devices provide data flash enabling dual parallel reads of static tables and dynamic variables	Increased flexibility for software and signal processing performance
✓ Flash doesn't require any special voltages and is fully in-circuit in-field programmable	Much greater flexibility using the 56F8300 flash enabling in field and less costly programming
✓ Boot flash enables custom loaders and field upgrade capability. It can also be used as general program flash	Increased flexibility and safety for in field program upgrades and in circuit factory programming