

# How to do LPDDR4 DQ Swapping in S32G

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# Problem Background

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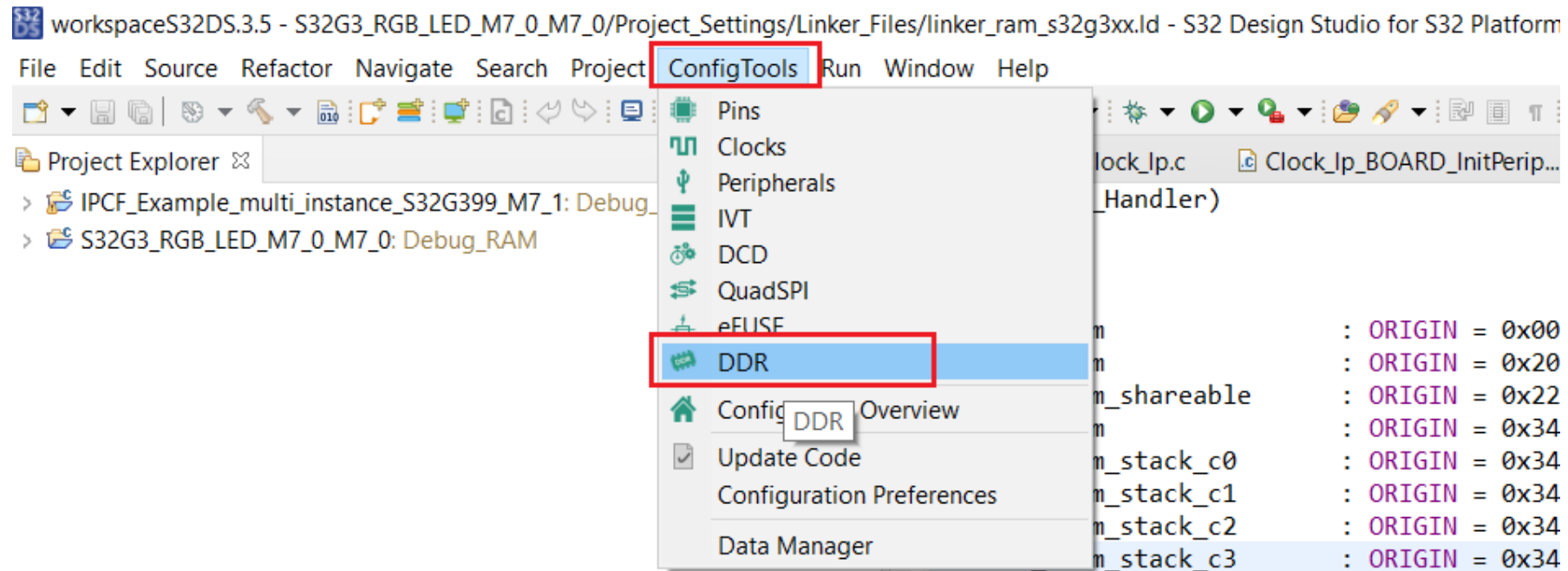
1. Customer report ddr initialization failed issue when running ATF in their board;
2. Suggested them to do LPDDR4 Firmware\_Init\_Test but still failed;
3. They used “MT53E1G32D2FW-046”, the LPDDR4 parameter is the same as “MT53D1024M32D4DT-046” in RDB3;
4. Customer just changed “DQ Swapping” in their board;

# How to change DQ swapping

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You should create new S32G S32DS project firstly, then you can open DDR tool as following:

For example: if you just install “S32DS.3.5.exe”, you should install “SW32G\_S32DS\_3.5\_D2207.zip” and “SW32\_RTD\_4.4\_3.0.4\_DS\_updatesite\_D2207.zip”, then create new S32G project firstly.



# How to change DQ swapping

You can change DQ Swapping sequence as following, please caution that: the fixed upper line means Data Pins in LPDDR4 side, you can just change Data Pins sequence in S32G Side:

Static Refresh Rate [0.25x] no

Per Bank Refresh no

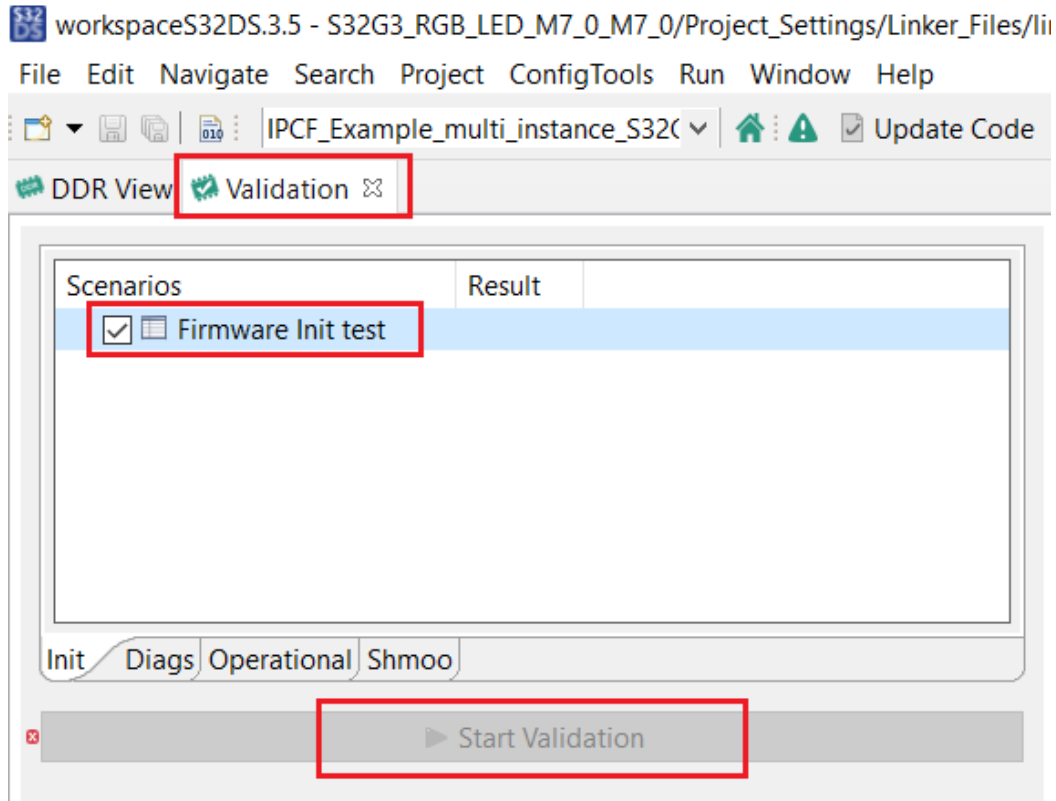
**DQ Swapping**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Problems

# How to change DQ swapping

You can do LPDDR4 Firmware\_Init\_Test, this is basic test, you should confirm this test can be passed in your board, otherwise you should check your “S32G + LPDDR4” related hardware based on hardware design guide:



# How to change DQ swapping

If you encounter LPDDR4 Firmware\_Init\_Test failed issue:

- 1). You should double confirm “DDR View configuration” firstly;
- 2). You can do “phy vref shmoo” and replace the phy quotient default value with the shmoo test result;

The screenshot shows the DDR View software interface. On the left, under 'Scenarios', the 'LPDDR4 Phy Vref' test is selected and highlighted with a red box. Below it, the 'Shmoo' tab is active, and the 'Start Validation' button is also highlighted with a red box. On the right, the 'Results' panel shows a table for 'Optimizing Phy Vref' with a 'Phy Vref Quotient' value of '0' highlighted in a red box. Below this, a 'Summary' table shows 'Phy Init' with 'Run' count 1 and 'Elaps' N/A.

Script	Run	Elaps
Phy Init	1	N/A

## Initial Board Settings

PHY ODT Impedance	60 Ohm
PHY Drive Strength	40 Ohm
PHY Vref Quotient	0x18
PHY Vref	0.206 V
DRAM ODT Impedance	40 Ohm
DRAM Drive Strength	40 Ohm
CA Vref Training	yes



# How to change DQ swapping

If you encounter LPDDR4 Firmware\_Init\_Test failed issue:

3). You can try to lower LPDDR4 Clock Cycle Freq to 800MHz, default is 1600MHz;

## ▼ Device Information

Clock Cycle Freq (MHz)	<input type="text" value="800 MHz"/>
DDR_CLK frequency	400MHz
Density per channel (Gb)	<input type="text" value="8G"/>
Number of ROW Addresses	<input type="text" value="16"/>
Number of Chip Selects used	<input type="text" value="2"/>
Number of Channels	<input type="text" value="2"/>
Number of COLUMN Addresses	<input type="text" value="10"/>
Number of BANK addresses	<input type="text" value="3"/>

The NXP logo is rendered in a bold, white, sans-serif font. The letters 'N', 'X', and 'P' are interconnected, with the 'X' having a distinctive shape where the two vertical strokes are slightly offset. The background is a solid dark blue.

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A large, multi-story office building with a grid of windows is visible in the background, tinted in a dark blue color. A sign on the top right corner of the building displays the NXP logo in green.

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