

S32 DESIGN STUDIO INTRODUCTION

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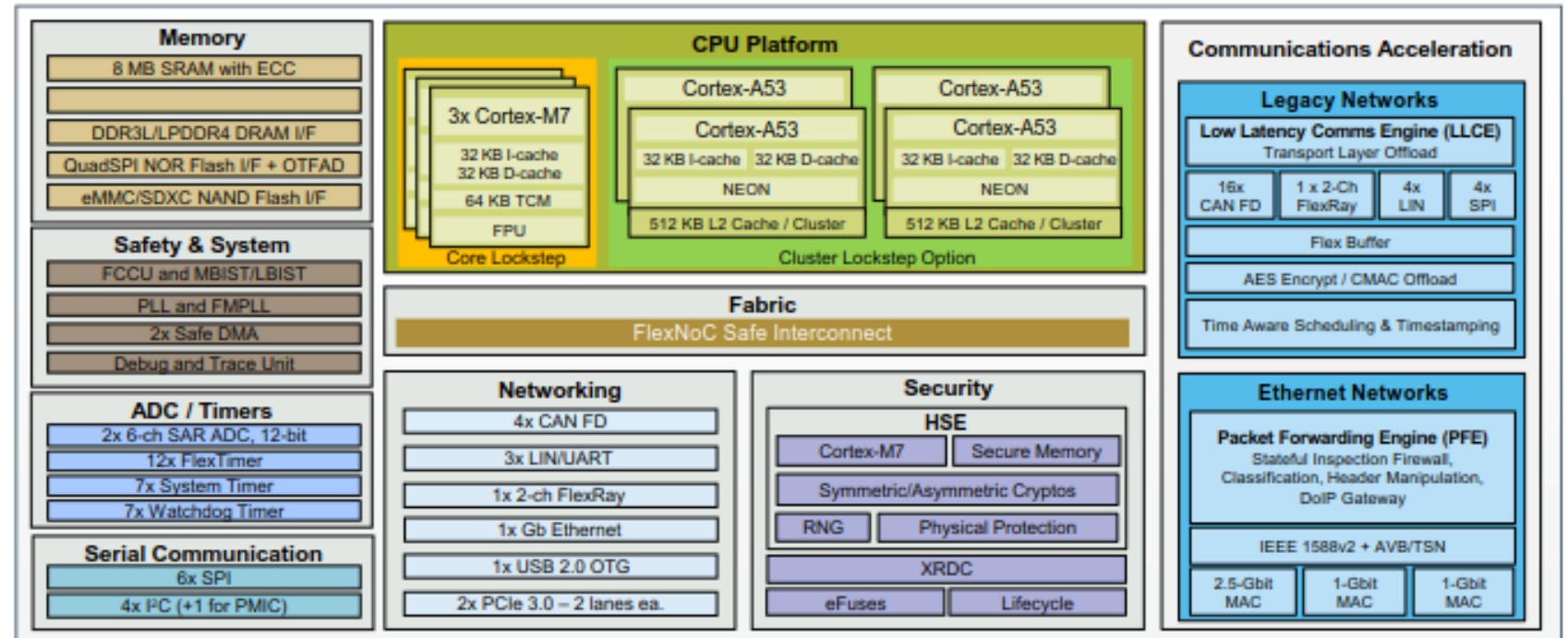


CONFIDENTIAL AND PROPRIETARY



SECURE CONNECTIONS
FOR A SMARTER WORLD

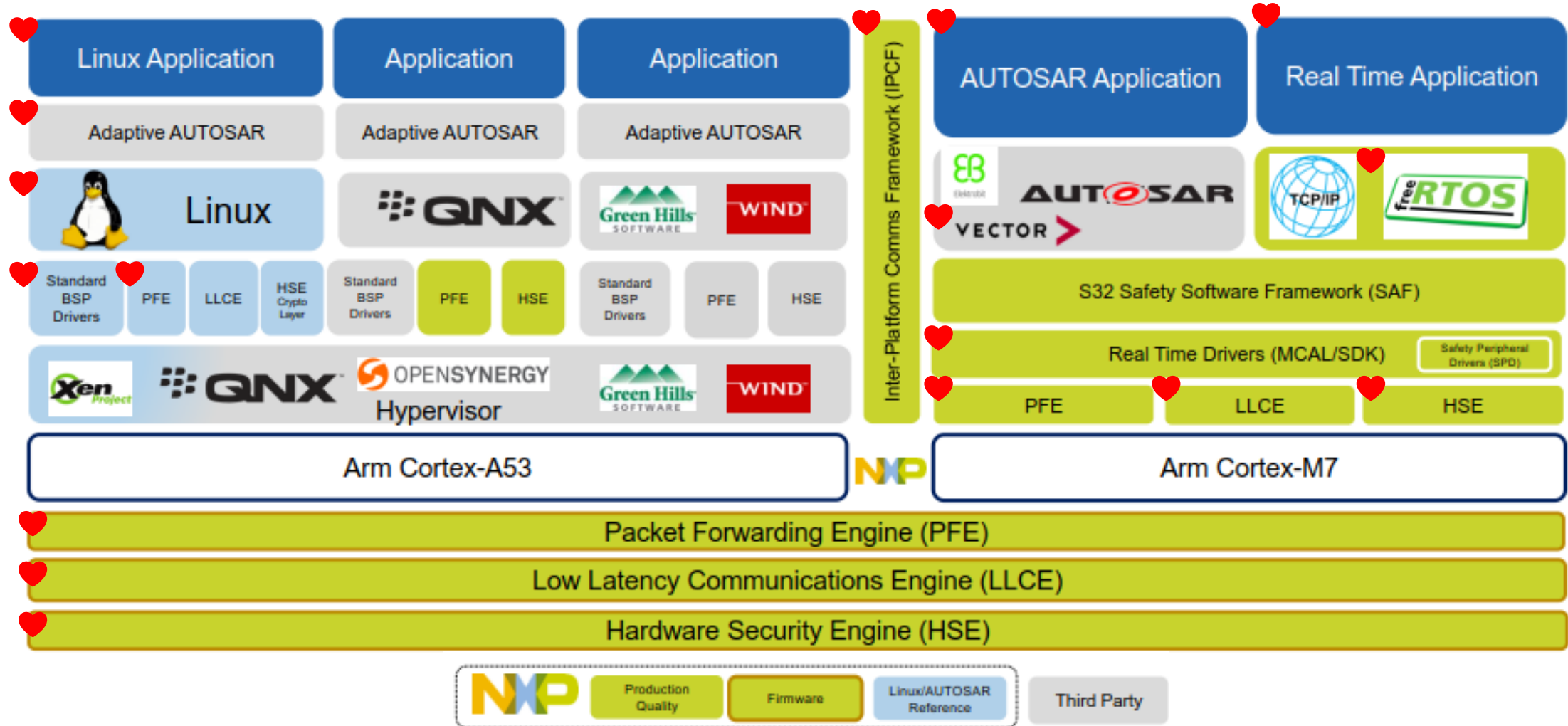
S32G Overview



| | S32G234M | S32G233A | S32G254A | S32G274A |
|-----------------|-----------------------------|-----------------------------|-----------------------------|---------------------------|
| CPU | N/A | Cluster0: Signal Cortex-A53 | | Cluster0: Dual Cortex-A53 |
| | N/A | Cluster1: Signal Cortex-A53 | | Cluster1: Dual Cortex-A53 |
| CPU (Real Time) | 3x Arm Cortex-M7 (lockstep) | 1x Arm Cortex-M7 (lockstep) | 3x Arm Cortex-M7 (lockstep) | |
| Internal RAM | 8MB | 6MB | 8MB | |

Software

Source: pr469773 - S32G Software Offering v7.3 (7.3).pdf

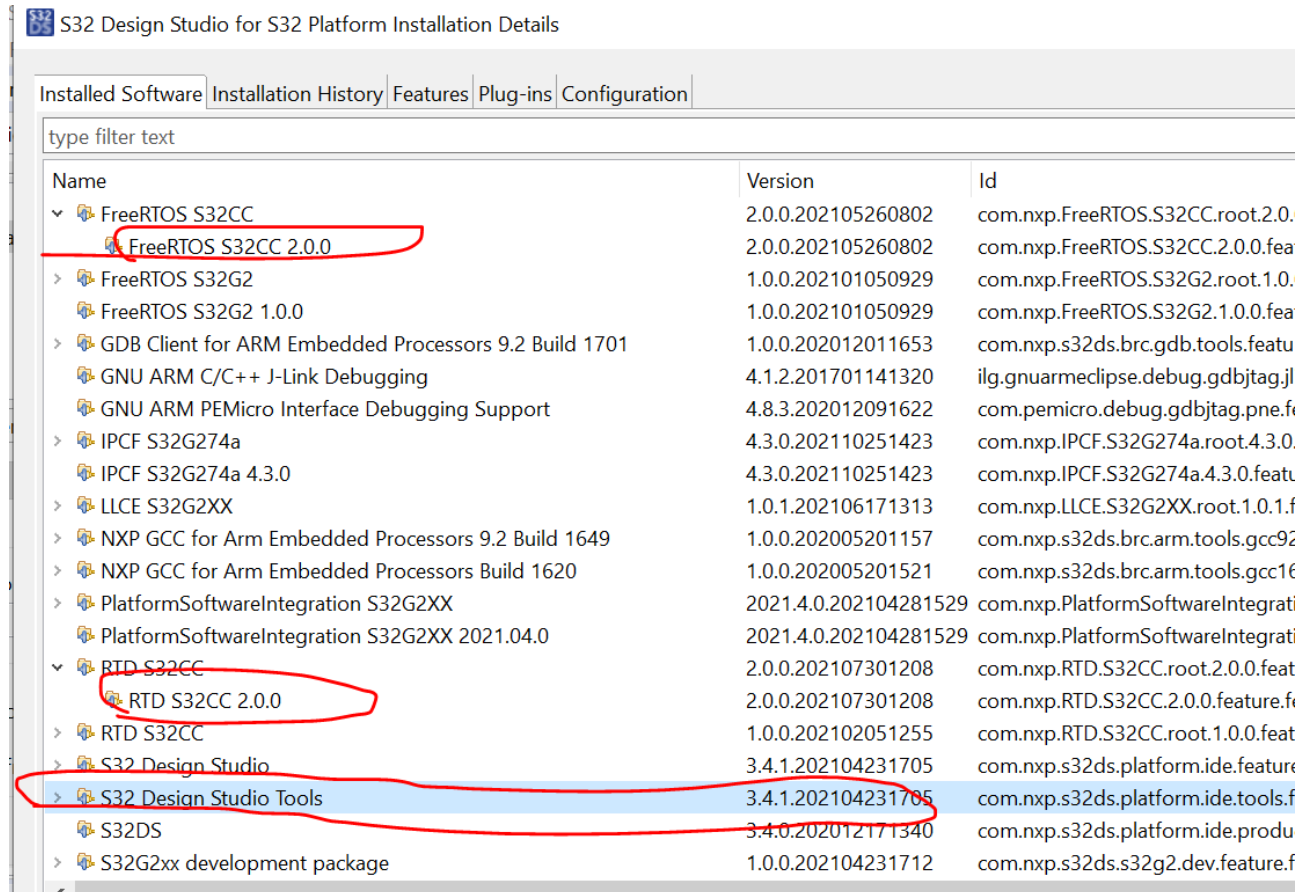


♥ Most GC customers' use case



Development Tool --- S32 Design Studio 3.4

- Get installation package and license from NXP website.
- Packages list in S32DS as following



| Name | Version | Id |
|---|-----------------------|-------------------------------------|
| FreeRTOS S32CC | 2.0.0.202105260802 | com.nxp.FreeRTOS.S32CC.root.2.0. |
| FreeRTOS S32CC 2.0.0 | 2.0.0.202105260802 | com.nxp.FreeRTOS.S32CC.2.0.0.fea |
| FreeRTOS S32G2 | 1.0.0.202101050929 | com.nxp.FreeRTOS.S32G2.root.1.0. |
| FreeRTOS S32G2 1.0.0 | 1.0.0.202101050929 | com.nxp.FreeRTOS.S32G2.1.0.0.fea |
| GDB Client for ARM Embedded Processors 9.2 Build 1701 | 1.0.0.202012011653 | com.nxp.s32ds.brc.gdb.tools.featu |
| GNU ARM C/C++ J-Link Debugging | 4.1.2.201701141320 | ilg.gnuarmedclipse.debug.gdbjtag.jl |
| GNU ARM PEMicro Interface Debugging Support | 4.8.3.202012091622 | com.pemicro.debug.gdbjtag.pne.fi |
| IPCF S32G274a | 4.3.0.202110251423 | com.nxp.IPCF.S32G274a.root.4.3.0. |
| IPCF S32G274a 4.3.0 | 4.3.0.202110251423 | com.nxp.IPCF.S32G274a.4.3.0.featu |
| LLCE S32G2XX | 1.0.1.202106171313 | com.nxp.LLCE.S32G2XX.root.1.0.1.f |
| NXP GCC for Arm Embedded Processors 9.2 Build 1649 | 1.0.0.202005201157 | com.nxp.s32ds.brc.arm.tools.gcc92 |
| NXP GCC for Arm Embedded Processors Build 1620 | 1.0.0.202005201521 | com.nxp.s32ds.brc.arm.tools.gcc16 |
| PlatformSoftwareIntegration S32G2XX | 2021.4.0.202104281529 | com.nxp.PlatformSoftwareIntegrati |
| PlatformSoftwareIntegration S32G2XX 2021.04.0 | 2021.4.0.202104281529 | com.nxp.PlatformSoftwareIntegrati |
| RTD S32CC | 2.0.0.202107301208 | com.nxp.RTD.S32CC.root.2.0.0.featu |
| RTD S32CC 2.0.0 | 2.0.0.202107301208 | com.nxp.RTD.S32CC.2.0.0.feature.fi |
| RTD S32CC | 1.0.0.202102051255 | com.nxp.RTD.S32CC.root.1.0.0.featu |
| S32 Design Studio | 3.4.1.202104231705 | com.nxp.s32ds.platform.ide.feature |
| S32 Design Studio Tools | 3.4.1.202104231705 | com.nxp.s32ds.platform.ide.tools.f |
| S32DS | 3.4.0.202012171340 | com.nxp.s32ds.platform.ide.produ |
| S32G2xx development package | 1.0.0.202104231712 | com.nxp.s32ds.s32g2.dev.feature.f |

Product Information

Automotive SW – S32G2 Standard Software

Your choice contains a suite of products. Please select one of the product lines below.
To register a New Product please click on the button below

[Register](#)

[Automotive SW - S32G2 - AUTOSAR 4.4 MCAL \(ISO26262\)](#)

[Automotive SW - S32G2 - HSE Firmware](#)

[Automotive SW - S32G2 - Real-Time Drivers](#)

[Automotive SW - S32G2 - S32 Design Studio](#)

[Automotive SW - Software Development Kit for Cortex-M](#)

[Automotive SW - Elektrobit Tresos Studio / AUTOSAR Configuration Tool](#)

[Automotive SW - S32G2 - Inter-Platform Communication Framework](#)

[Automotive SW - S32G2 - Linux BSP](#)

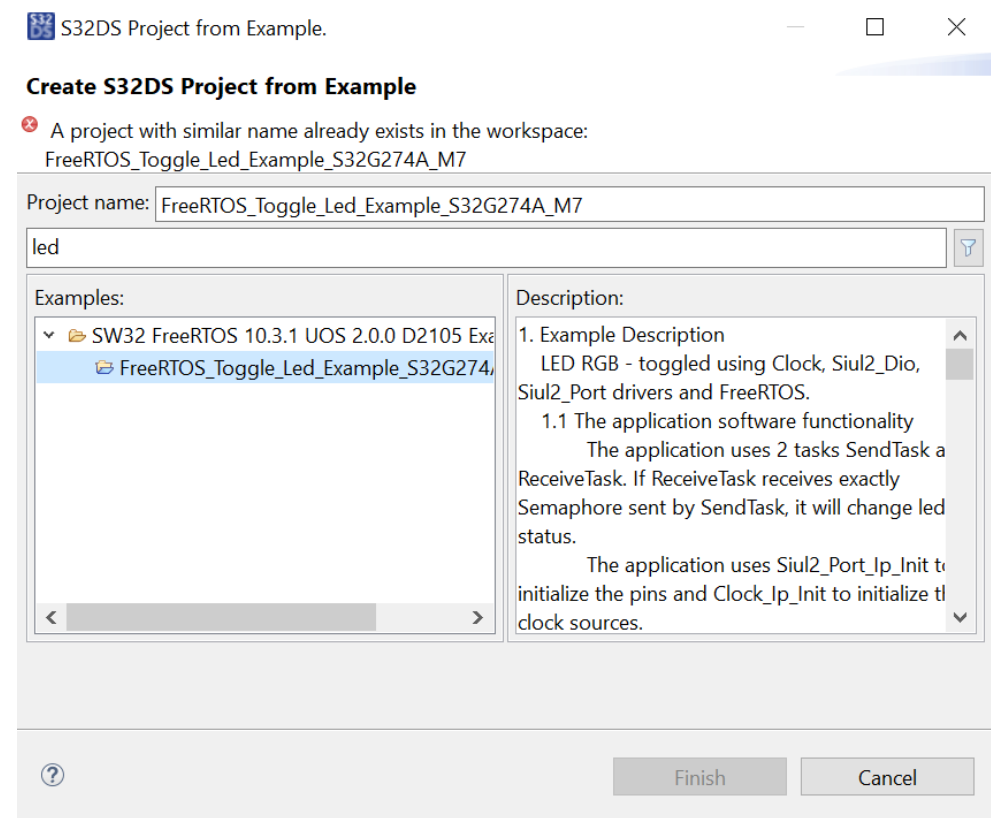
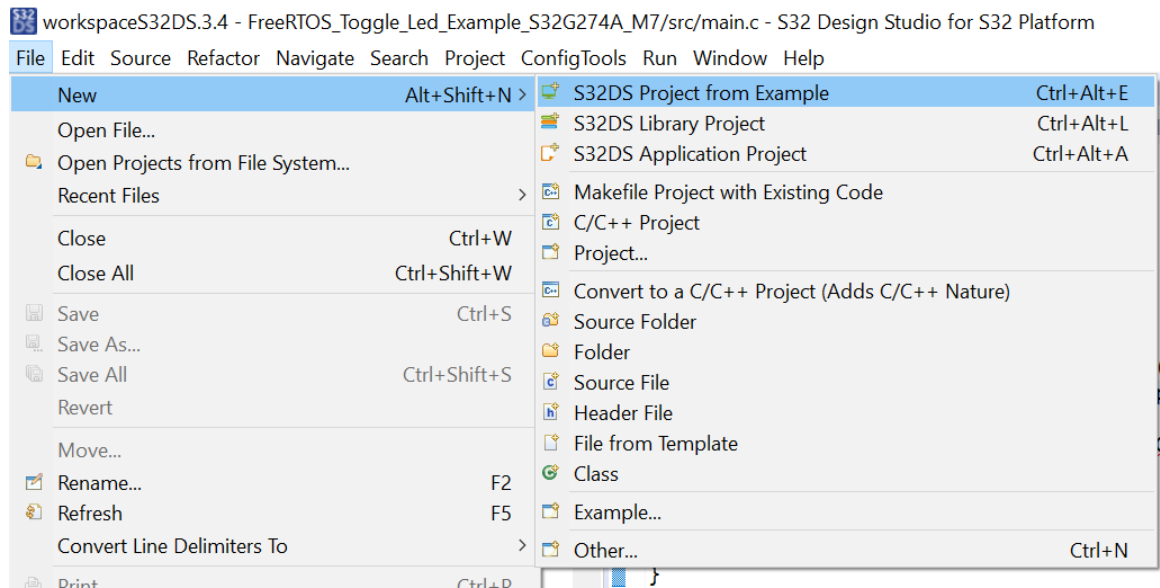
[Automotive SW - S32G2 - LLCE Driver + Firmware](#)

[Automotive SW - S32G2 - PFE Driver + Firmware](#)

Project in S32DS

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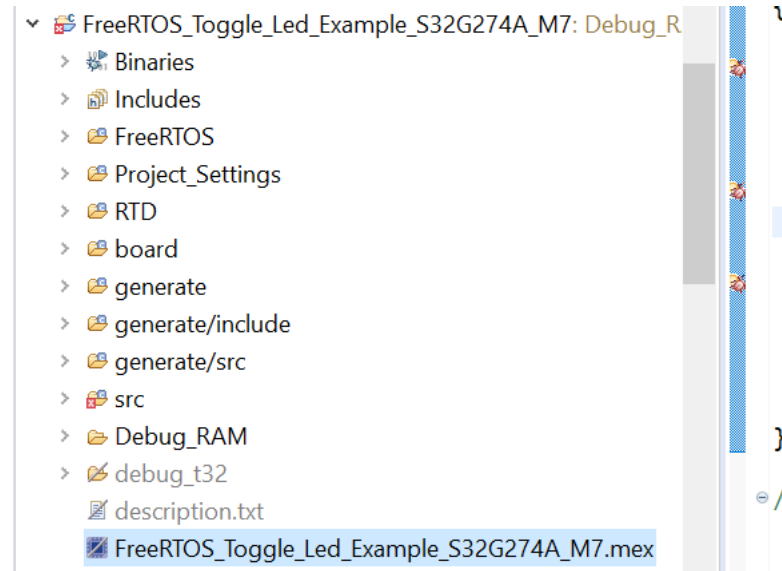
- Create a project from examples
- Such as FreeRTOS_Toggle_Led_Example_S32G274A_M7



Project in S32DS

2/11

- Double click mex file to do configurations



- Pins configuration for PINMUX based on IOMUX excel in RM attachments.

The screenshot displays the S32 Design Studio interface for configuring pins. On the left, a list of peripherals is shown with checkboxes, including ADC_0, CAN_0, CTU, DDR_GPR, FCCU, FXOSC, and I2C_0. The central area features a pin grid for the S32G274A_Rev2_525bga package, with rows labeled A through AC and columns numbered 1 to 25. A blue dot is visible on the grid. On the right, the 'Code Preview' pane shows the configuration code for 'Siul2_Port_Ip_Cfg.h@Cortex-...'. The code includes comments and defines pin labels, such as 'pin_num: Y9, pin_signal: PA_06, lat'. The code is as follows:

```
1 /* clang-format off */
2 /*
3  * TEXT BELOW IS USED AS SETTING FOR 1
4  !!GlobalInfo
5  product: Pins v9.0
6  processor: S32G274A_Rev2
7  package_id: S32G274A_Rev2_525bga
8  mcu_data: PlatformSDK_S32XX_2021_05
9  processor_version: 0.0.0
10 pin_labels:
11 - {pin_num: Y9, pin_signal: PA_06, lat
12   * BE CAREFUL MODIFYING THIS COMMENT -
13   */
14 /* clang-format on */
15
16 #include "Siul2_Port_Ip_Cfg.h"
17
18 /* clang-format off */
19
20 /*
21  * TEXT BELOW IS USED AS SETTING FOR 1
22  BOARD_InitPins:
23   - options: {callFromInitBoot: 'true',
24   - pin list:
```



- Clocks configuration (Be careful of conflicts for different cores and apps)

workspaceS32DS.3.4 - FreeRTOS_loggle_Led_Example_S32G2/4A_M//src/main.c - S32 Design Studio for S32 Platform

File Edit Source Refactor Navigate Search Project ConfigTools Clocks Run Window Help

FreeRTOS_Toggle_Led_Example_S32 Update Code Functional Group BOARD BootClockRUN

Clocks Diagram Clks Table Search elements in di

Run Mode DRUN Clock Development Error Detect Disabled Clock User Mode Support Disabled Clock Disable Ram Wait States Config Disabled

Clock Loops Timeout 50000 Clock Timeout Method OSIF_COUNTER_DUMMY Get Clock Frequency API Disabled

The diagram shows a complex clock tree starting from external clocks (32 kHz Slow IRC, 48 MHz Fast IRC, 40 MHz FXOSC) and internal PLLs (COREPLL, PERIPHPLL). It branches into various system clocks like FIRC, CORE_PLL DFS1/2, and PHIO/PHI1. The right side of the diagram lists the resulting clock names and their frequencies, such as ADC0_CLK (48 MHz), DDR0_CLK (400 MHz), and CORE PLL PHIO (800 MHz).

| Clock Name | Enable | Control | Source |
|--------------|-------------------------------------|---------|--------|
| ADC0_CLK | <input checked="" type="checkbox"/> | | PER... |
| ADC1_CLK | <input checked="" type="checkbox"/> | | PER... |
| CLKOUT0_CLK | <input checked="" type="checkbox"/> | | FXO... |
| CLKOUT1_CLK | <input checked="" type="checkbox"/> | | FXO... |
| CRC0_CLK | <input checked="" type="checkbox"/> | | XBA... |
| CTU0_CLK | <input checked="" type="checkbox"/> | | PER... |
| CTU1_CLK | <input checked="" type="checkbox"/> | | PER... |
| DAPB_CLK | <input checked="" type="checkbox"/> | | COR... |
| DDR0_CLK | <input checked="" type="checkbox"/> | | DDR... |
| DMA0_CLK | <input checked="" type="checkbox"/> | | XBA... |
| DMA1_CLK | <input checked="" type="checkbox"/> | | XBA... |
| DMAMUX0_CLK | <input checked="" type="checkbox"/> | | XBA... |
| DMAMUX1_CLK | <input checked="" type="checkbox"/> | | XBA... |
| DMAMUX2_CLK | <input checked="" type="checkbox"/> | | XBA... |
| DMAMUX3_CLK | <input checked="" type="checkbox"/> | | XBA... |
| DMA_CRC0_CLK | <input checked="" type="checkbox"/> | | XBA... |
| DMA_CRC1_CLK | <input checked="" type="checkbox"/> | | XBA... |
| EIM0_CLK | <input checked="" type="checkbox"/> | | A53... |

Problems

type filter text

| Level | Resource | Issue |
|-------|----------|-------|
|-------|----------|-------|



- Components configuration (Related guides in NXP\S32DS.3.4\S32DS\software\PlatformSDK_S32XX_xxxx)

The screenshot displays the S32 Design Studio interface for a project named 'freertos_1'. The main window shows the 'FreeRTOS configuration [OS]' settings. On the left, a 'Components' sidebar lists categories like MCAL, Drivers, OS, and Middleware, with 'freertos_1' selected under OS. The configuration table includes various parameters such as 'cpu clock [Hz]', 'tick rate [Hz]', and 'max priorities'. On the right, an 'Overview' panel provides general information about the configuration, including hardware details like the processor (S32G274A_Rev2) and SDK version (PlatformSDK_S32XX_2021_05). A 'Peripherals' section shows a USB icon and a 'Generated code' section with 'Update code enabled' checked.

| FreeRTOS configuration | |
|--|-------------------------------------|
| Name: freertos_1 | |
| Mode: General Mode | |
| FreeRTOS configuration | |
| General definitions | |
| cpu clock [Hz] | 400000000 |
| tick rate [Hz] | 1000 |
| max priorities | 5 |
| minimal stack size | 90 |
| max task name len | 10 |
| library max syscall interrupt priority | 1 |
| use 16bit ticks | <input type="checkbox"/> |
| idle should yield | <input checked="" type="checkbox"/> |
| use preemption | <input checked="" type="checkbox"/> |
| num thread local storage pointers | 0 |
| use port optimised task selection | <input type="checkbox"/> |
| use task notifications | <input checked="" type="checkbox"/> |
| use time slicing | <input checked="" type="checkbox"/> |
| use newlib reentrant | <input type="checkbox"/> |
| enable backward compatibility | <input checked="" type="checkbox"/> |
| enable POSIX errno | <input type="checkbox"/> |
| use application task tag | <input type="checkbox"/> |
| record stack high address | <input type="checkbox"/> |



- QSPI configuration for boot progress

workspace532DS.5.4 - FreeRTOS_toggle_Led_Example_S32G274A_m7/stc/main.c - S32 Design Studio for S32 Platform

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FreeRTOS_Toggle_Led_Example_S32G274A_m7/stc/main.c Update Code

QuadSPIView

Flash Port Connection

Port: A

DLL Bypass Mode

DLL in Bypass mode

DLL Auto Update Mode

DLL in Auto Update mode

IPCR Enable Mode

IPCR Trigger

SFLASH Clock Frequency

Clock Frequency [MHz]: 0x0

Import QuadSPI Image

Export QuadSPI Image

QuadSPI Registers

| Register Name | Value | Description |
|---------------|------------|-------------------|
| MCR | 0xf404c | Module Confi... |
| FLSHCR | 0x303 | Flash Memor... |
| BFGENCR | 0x0 | Buffer Generi... |
| DLLCRA | 0x1200000 | DLL Flash Me... |
| PARITYCR | 0x0 | Parity Config... |
| SFACR | 0x800 | Serial Flash M... |
| SMPR | 0x0 | Sampling Reg... |
| DLCR | 0x40ff40ff | Data Learning... |
| SFA1AD | 0x0 | Serial Flash M... |
| SFA2AD | 0x0 | Serial Flash M... |
| DLPR | 0xaa553443 | Data Learn Pa... |
| SFAR | 0x0 | Serial Flash M... |
| TBDR | 0x0 | TX Buffer Dat... |

Command Sequences

Add

| # | Binary Content |
|---|---------------------|
| | No content in table |

Flash Write Data

Add

| # | Address Valid | Configurati... | Valid Addr... | PAD | Compr |
|---|---------------|----------------|---------------|-----|-------|
| | | | | | |

No content in table



Project in S32DS

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- DDR configuration and validation
- DDR code is from validation of Init

workspaceS32DS.3.4 - FreeRTOS_Toggle_Led_Example_S32G274A_M7/src/main.c - S32 Design Studio for S32 Platform

File Edit Source Refactor Navigate Search Project ConfigTools Run Window Help

FreeRTOS_Toggle_Led_Example_S32

Update Code

DDR View Validation

Device Information

| | |
|-----------------------------|---------|
| Clock Cycle Freq (MHz) | 800 MHz |
| DDR_CLK frequency | 400MHz |
| Density per channel (Gb) | 8G |
| Number of ROW Addresses | 16 |
| Number of Chip Selects used | 2 |
| Number of Channels | 2 |
| Number of COLUMN Addresses | 10 |
| Number of BANK addresses | 3 |
| Number of BANKS | 8 |
| Total DRAM density (Gb) | 32 |
| Bus Width | 32 |
| Clock Cycle Time (ns) | 1.25 |

Initial Board Settings

| | |
|--------------------|---------|
| PHY ODT Impedance | 60 Ohm |
| PHY Drive Strength | 40 Ohm |
| PHY Vref Quotient | 0x18 |
| PHY Vref | 0.285 V |

workspaceS32DS.3.4 - FreeRTOS_Toggle_Led_Example_S32G274A_M7/src/main.c - S32 Design Studio for S32 Platform

File Edit Source Refactor Navigate Search Project ConfigTools Run Window Help

FreeRTOS_Toggle_Led_Example_S32

Update Code

DDR View Validation

Scenarios

| Scenarios | Result |
|---|--------|
| <input type="checkbox"/> Firmware Init test | |

Start Validation

Connections:

Select connection type: Serial

Select COM port: COM3

XOSC source frequency: 40 MHz

Results

PHY Test

| | |
|--------------|-------------|
| Pass / Total | Checking... |
| 0 | |

Legend:

Summary

Test results

| | | | |
|-----------------|-----------------|-------------------|------------------|
| Passed 0 (0.0%) | Failed 0 (0.0%) | Queued 1 (100.0%) | Skipped 0 (0.0%) |
|-----------------|-----------------|-------------------|------------------|

| Script | Run | Elapsed ti... | Result | Fail reason |
|----------|-----|---------------|---------|-------------|
| Phy Init | 1 | N/A | Queu... | |

Error capture registers

Script: Phy Init

Run: 1

Problems

type filter text

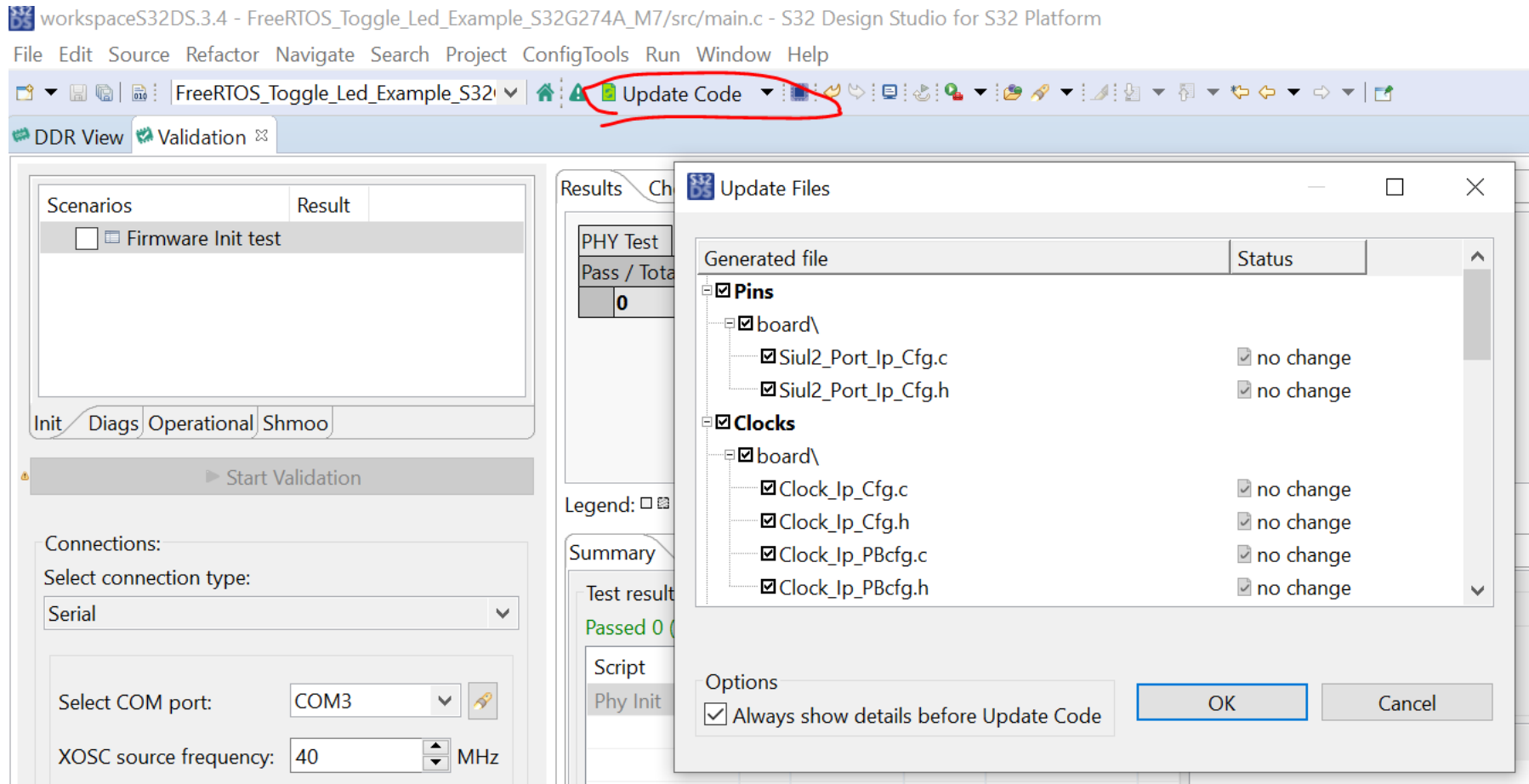
| Level | Resource | Issue | Origin |
|-------|----------|-------|--------|
|-------|----------|-------|--------|



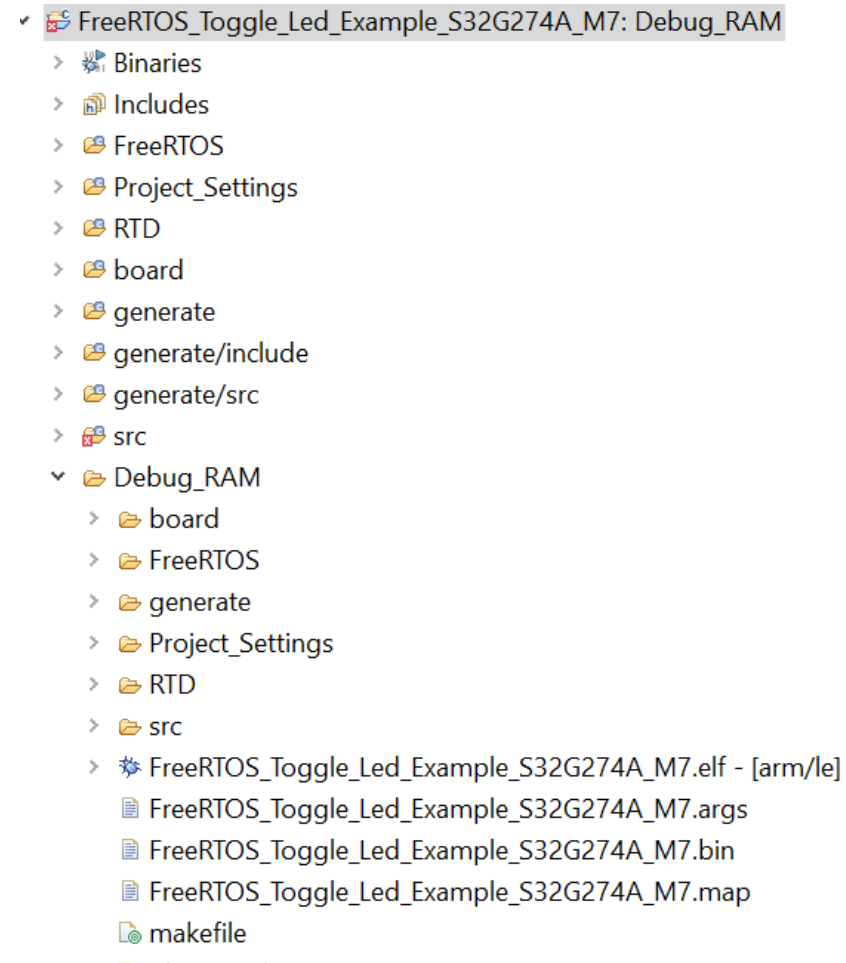
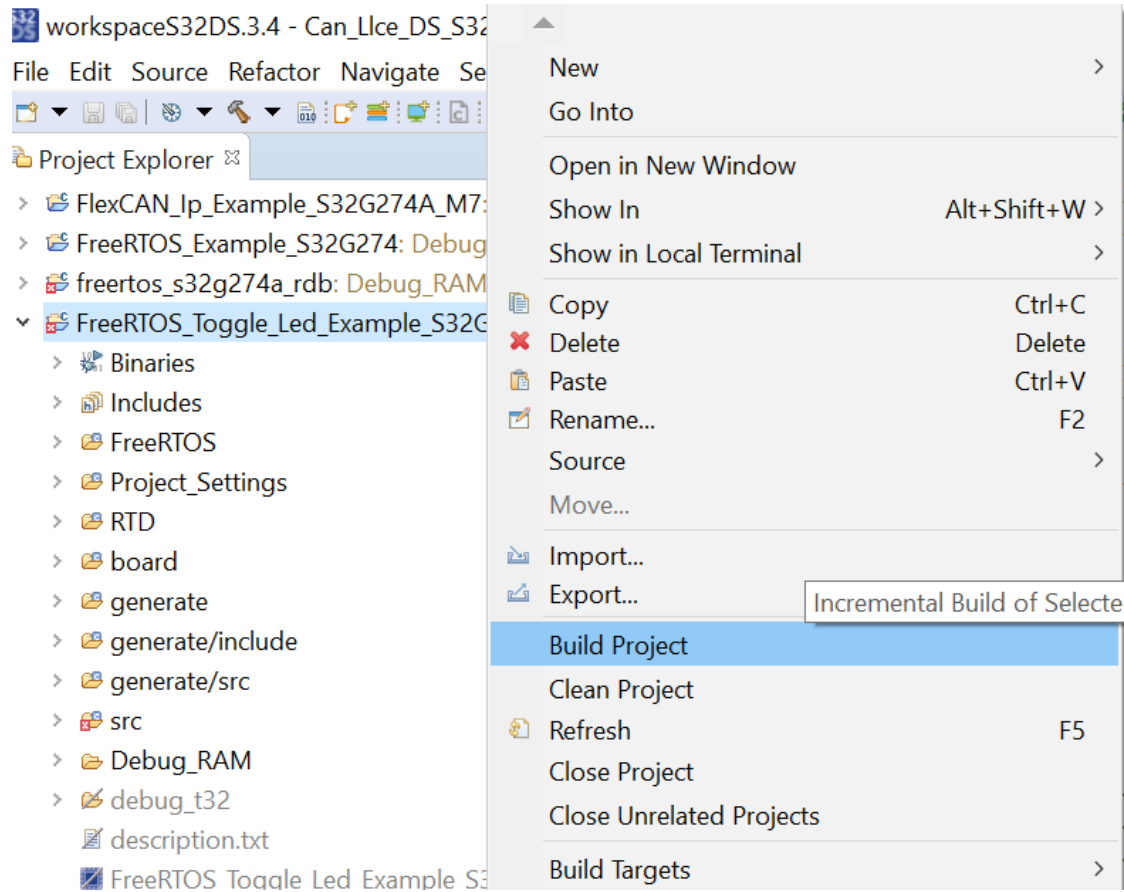
Project in S32DS

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- Update code based on all configurations



- Build project and generate elf/binary image



- IVT configuration for boot

workspaceS32DS.3.4 - FreeRTOS_Toggle_Led_Example_S32G274A_M7/src/main.c - S32 Design Studio for S32 Platform

File Edit Source Refactor Navigate Search Project ConfigTools IVT Run Window Help

FreeRTOS_Toggle_Led_Example_S32 Update Code

IVTView

Boot Configuration

Boot Target: A53_0

BOOTSEQ: Secured boot mode

Boot Target Watchdog

GMAC Generation

ADKP File: N/A

Life Cycle

Life Cycle: Keep existing configuration

Interface selection

Boot device type: QuadSPI Serial Flash

Configure QuadSPI parameters

QuadSPI para...: N/A

IVT Image Address

IVT Image Start Address: 0x0

Automatic Align

Automatic Align Start Address: 0x0

Image Table

On

Self-Test DCD

N/A

Start address: 0x100 Size in bytes: 4

On

Self-Test DCD (backup)

N/A

Start address: 0x108 Size in bytes: 4

On

DCD

N/A

Start address: 0x110 Size in bytes: 4

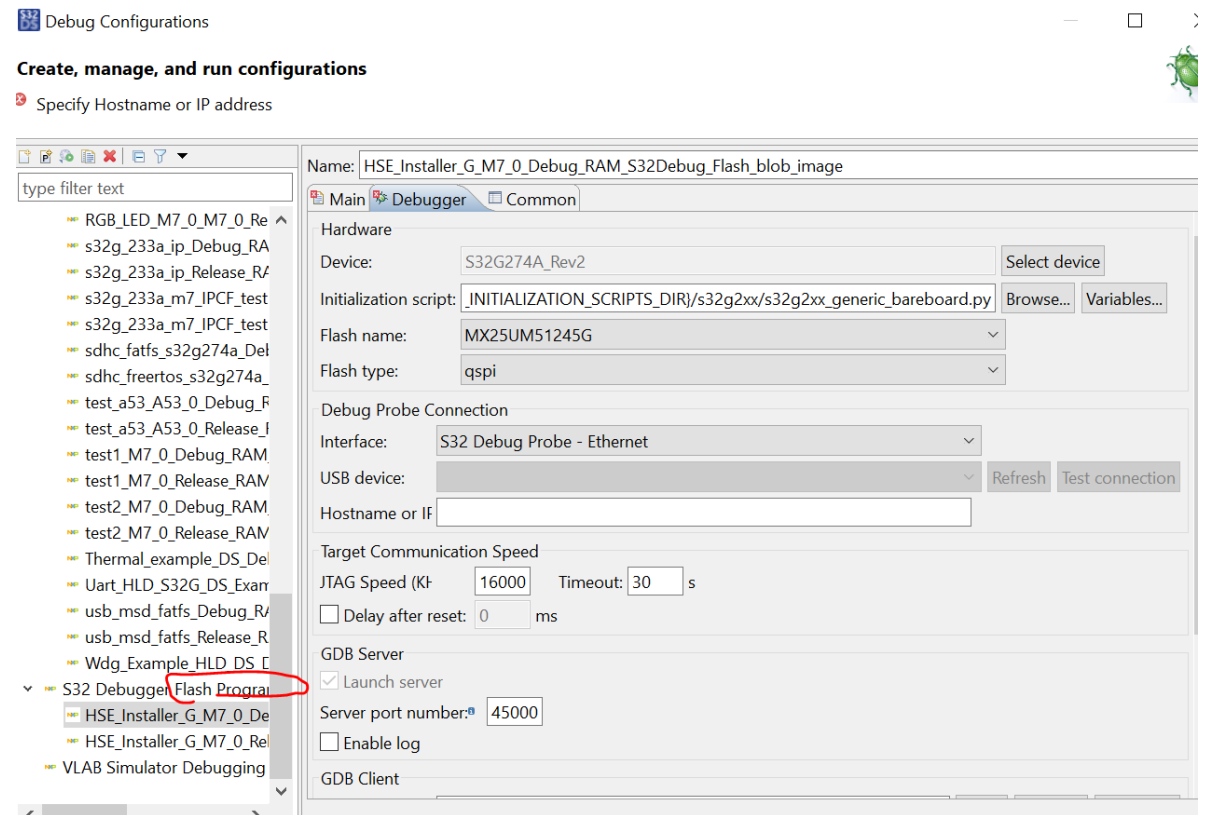
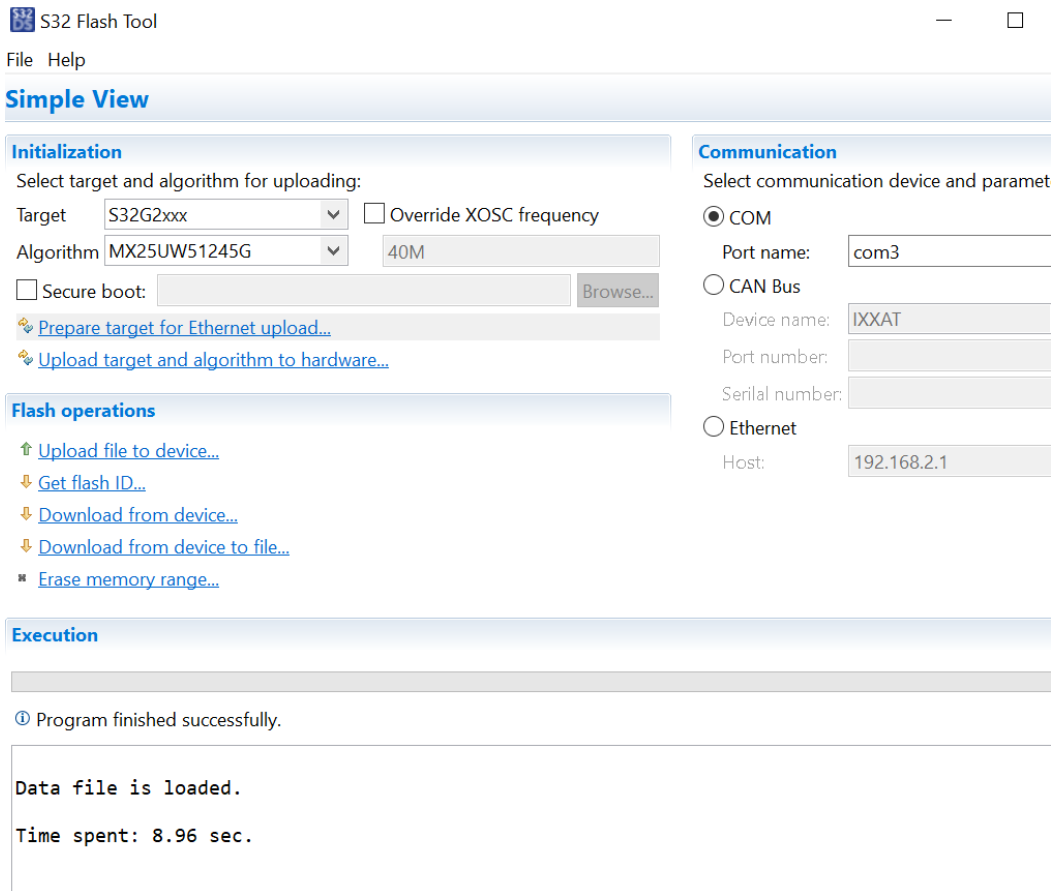
| Start | Memory Layout | End |
|-------|---|-------|
| 0x0 | IVT Image - 256 bytes | 0xff |
| 0x100 | Self-Test DCD - 4 bytes | 0x103 |
| 0x108 | Self-Test DCD (backup) - 4 bytes | 0x10b |
| 0x110 | DCD - 4 bytes | 0x113 |
| 0x118 | DCD (backup) - 4 bytes | 0x11b |
| 0x130 | Application bootloader - 4 bytes | 0x133 |
| 0x138 | Application bootloader (backup) - 4 bytes | 0x13b |
| | 196 bytes | |

Overview Problems

Configuration - General Info



- Program image to qspi flash or SD/EMMC by COM port or Debugger tool
- Ethernet port cannot be supported anymore



- Debug configurations

The screenshot shows the IDE interface. On the left, the Project Explorer displays a project structure for 'FreeRTOS_Toggle_Led'. A context menu is open over the 'FreeRTOS_Toggle_Led' folder, with 'Debug As' selected. Below the menu, a list of hardware components is visible, including '1 Local C/C++ Application' and '2 S32DS C/C++ Application'. The main editor area shows a list of hardware components with their IDs and frequencies, such as 'PFEMAC1_EXT_RX.outFr' and 'QSPI0_CLK.outFreq, va'.

The screenshot shows the 'Debug Configurations' dialog box. The title bar reads 'Debug Configurations'. The main area is titled 'Create, manage, and run configurations'. The configuration name is 'FreeRTOS_Toggle_Led_Example_S32G274A_M7_Debug_RAM_S32Debug'. The hardware section shows 'Device: S32G274A_Rev2' and 'Core: M7_0'. The 'Initial core' checkbox is checked. The 'Debug Probe Connection' section shows 'Interface: S32 Debug Probe - USB' and 'USB device: 00:04:9f:06:bb:be - S32 Debug Probe'. The 'Target Communication Speed' section shows 'JTAG Speed (KHz): 16000' and 'Timeout: 30 s'. The 'GDB Server' section shows 'Launch server' checked and 'Server port number: 4500'. The 'GDB Client' section shows 'Executable: \${S32DS_GDB_ARM32_PY}'. The 'Debug' button is highlighted.

The screenshot shows the 'Secure debugging' settings dialog box. The 'Enable secure debugging' checkbox is checked. The 'Debugging type' dropdown menu is open, showing 'Password' selected. Other options include 'Challenge & Response'. The 'Clear data stored' button is visible. The 'Revert' and 'Apply' buttons are at the bottom.



Debug in S32DS

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- Launch Debug session

workspaceS32DS.3.4 - FreeRTOS_Toggle_Led_Example_S32G274A_M7/src/main.c - S32 Design Studio for S32 Platform

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Debug Project Explorer

FreeRTOS_Toggle_Led_Example_S32G274A_M7_Debug

FreeRTOS_Toggle_Led_Example_S32G274A_M7.elf [

Thread #1 1 [core: 0] (Suspended : Breakpoint)

main() at main.c:468 0x345001b4

C:/NXP/S32DS.3.4/S32DS/tools/gdb-arm/arm32-e

S32 Debugger

Semihosting

```
main.c bootloader_m... Bootloader.c BootloaderR... main.c main.c
/* Details the startup initialization sequence is the following.
 * - startup asm routine
 * - main()
 */
int main(void)
{
#if 0
/* Initialize Clock */
Clock_Ip_StatusType Status_Init_Clock = CLOCK_IP_ERROR;
Status_Init_Clock = Clock_Ip_Init(Mcu_aClockConfigPB);

if (Status_Init_Clock != CLOCK_IP_SUCCESS)
{
while(1); /* Error during initialization. */
}
#endif
/* Initialize all pins using the Port driver */
Siul2_Port_Ip_PortStatusType Status_Init_Port = SIUL2_PORT_ERROR;
Status_Init_Port = Siul2_Port_Ip_Init(NUM_OF_CONFIGURED_PINS0, g_pin_mux_I

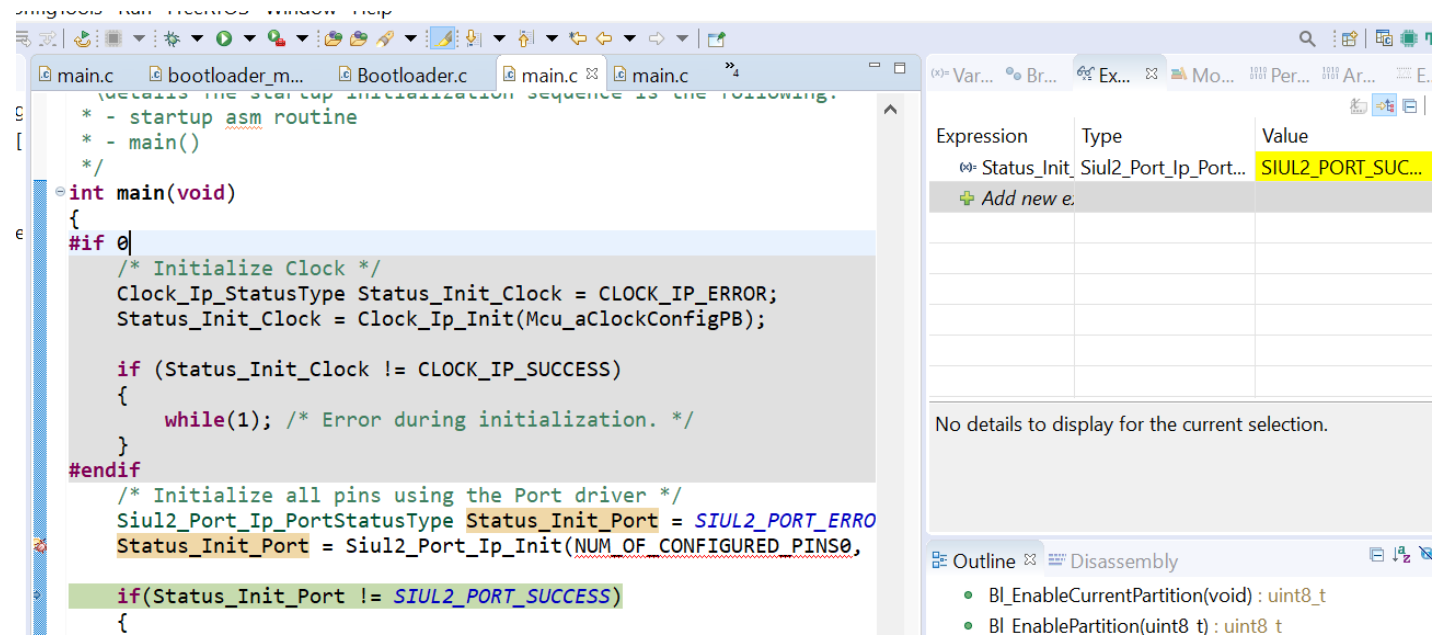
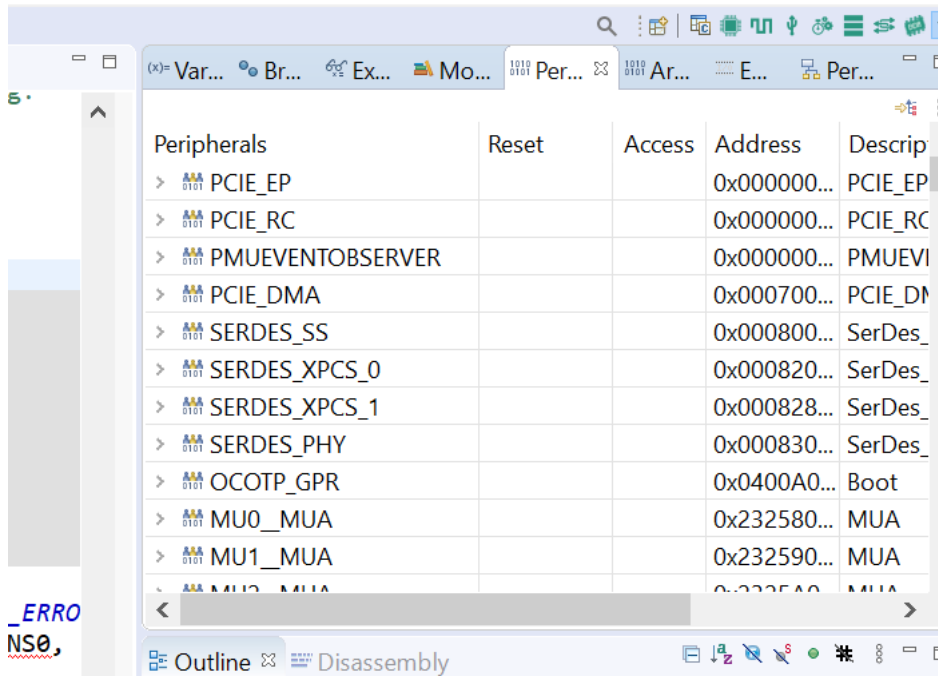
if(Status_Init_Port != SIUL2_PORT_SUCCESS)
{
while(1); /* Error during initialization. */
}

vSemaphoreCreateBinary(sem_handle);
```

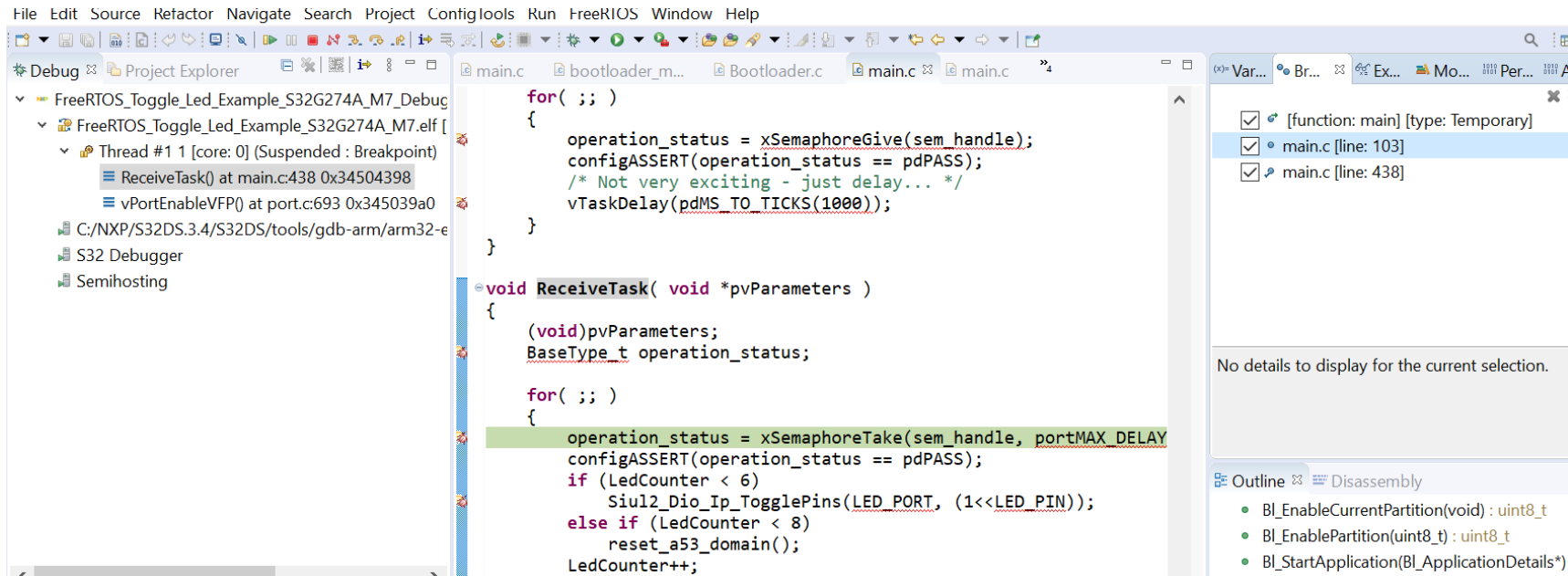
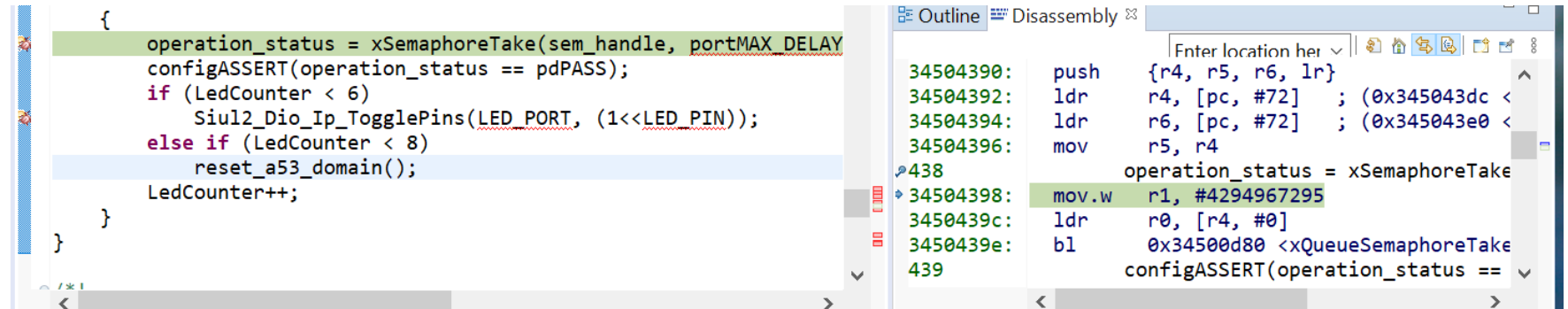
Debug in S32DS

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- Registers and Expressions

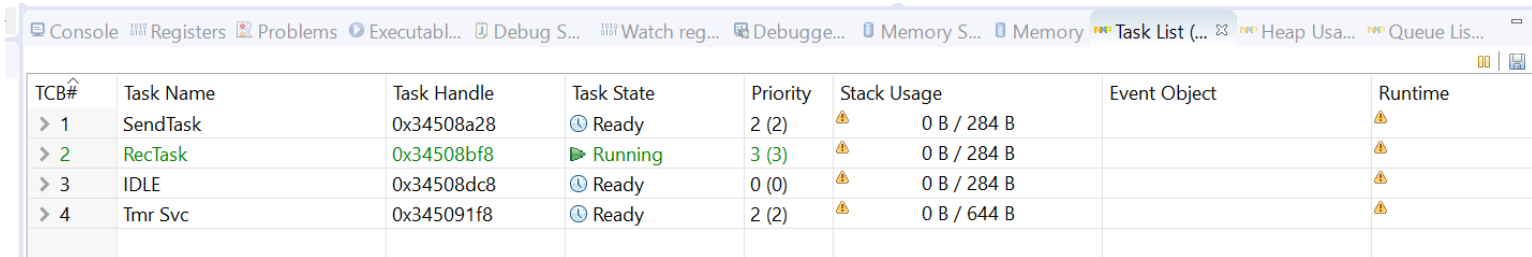


- Breakpoints and Disassembly

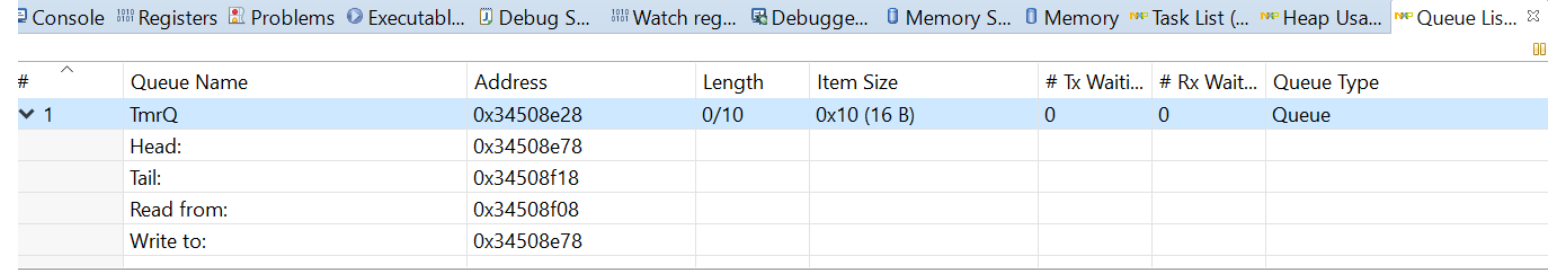


Debug in S32DS

- OS (Free RTOS) awareness

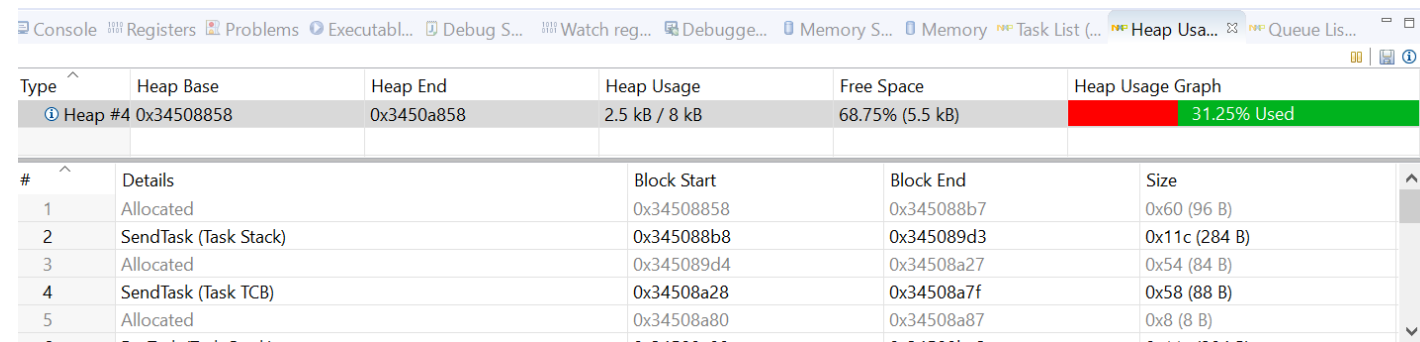


| TCB# | Task Name | Task Handle | Task State | Priority | Stack Usage | Event Object | Runtime |
|------|-----------|-------------|------------|----------|-------------|--------------|---------|
| > 1 | SendTask | 0x34508a28 | Ready | 2 (2) | 0 B / 284 B | | |
| > 2 | RecTask | 0x34508bf8 | Running | 3 (3) | 0 B / 284 B | | |
| > 3 | IDLE | 0x34508dc8 | Ready | 0 (0) | 0 B / 284 B | | |
| > 4 | Tmr Svc | 0x345091f8 | Ready | 2 (2) | 0 B / 644 B | | |



| # | Queue Name | Address | Length | Item Size | # Tx Waiti... | # Rx Wait... | Queue Type |
|---|------------|------------|--------|-------------|---------------|--------------|------------|
| 1 | TmrQ | 0x34508e28 | 0/10 | 0x10 (16 B) | 0 | 0 | Queue |

Head: 0x34508e78
Tail: 0x34508f18
Read from: 0x34508f08
Write to: 0x34508e78



| Type | Heap Base | Heap End | Heap Usage | Free Space | Heap Usage Graph |
|---------|------------|------------|---------------|-----------------|------------------|
| Heap #4 | 0x34508858 | 0x3450a858 | 2.5 kB / 8 kB | 68.75% (5.5 kB) | 31.25% Used |

| # | Details | Block Start | Block End | Size |
|---|-----------------------|-------------|------------|---------------|
| 1 | Allocated | 0x34508858 | 0x345088b7 | 0x60 (96 B) |
| 2 | SendTask (Task Stack) | 0x345088b8 | 0x345089d3 | 0x11c (284 B) |
| 3 | Allocated | 0x345089d4 | 0x34508a27 | 0x54 (84 B) |
| 4 | SendTask (Task TCB) | 0x34508a28 | 0x34508a7f | 0x58 (88 B) |
| 5 | Allocated | 0x34508a80 | 0x34508a87 | 0x8 (8 B) |



Other Resources

- DS basic guide in C:\NXP\S32DS.3.4\S32DS\help\pdf
- DS howto guide in C:\NXP\S32DS.3.4\S32DS\help\resources\howto
- DS video guide in C:\NXP\S32DS.3.4\S32DS\help\resources\video



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