NXP Semiconductors
Application Note

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S12VR Hardware Design Guidelines

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Contents

1 Introduction

This document lists the required external components and shows how they should be connected to use the MC9S12VR family of S12 MagniV microcontrollers in any application. It also lists recommended external components that can be used to extend the use cases of the MCU. Finally, it provides a printed-circuit board (PCB) design recommendation section, with layout and routing recommendations that should increment immunity against electromagnetic coupling and reduce electromagnetic emissions.

2 Power Management

The power and ground pins are described in subsequent sections.

2.1 VSUP – Main Power Supply Pin

VSUP is the 12 V/18 V supply voltage pin for the on chip voltage regulator. This is the voltage supply input from which the voltage regulator generates the on chip voltage supplies. It must be protected externally against a reverse battery connection, as seen in Figure 2.

The designer could choose to add Bulk/Bypass capacitor as a charge tank to provide power when losing battery. The value of this capacitor depends on the current consumption and the amount of time the MCU needs to perform house-keeping activities before shutting down.

2.2 VSUPHS — Voltage Supply Pin for High-Side Drivers

VSUPHS is the 12 V/18 V shared supply voltage pin for the high-side drivers.

2.3 Digital I/O and Analog Supplies

2.3.1 VDDX, VSSX — Pad Supply Pins

VDDX is the supply domain for the digital Pads. VDDX1 and VDDX2 are the 5 V power supply output for the I/O drivers. This voltage is generated by the on chip voltage regulator. Bypass requirements on VDDX1 and VDDX2 pins depend on how heavily the MCU pins are loaded. All VDDX pins are connected together internally. An off-chip stability and decoupling capacitor between VDDX and VSSX are required. This supply domain is monitored by the Low Voltage Reset circuit. VDDX1 and VDDX2 have to be connected externally to VDDA pin.

2.3.2 VDDA, VSSA — Regulator Reference Supply Pins

VDDA and VSSA pins are used to supply the analog parts of the regulator. Internal precision reference circuits are supplied from these signals. An off-chip decoupling capacitor between VDDA and VSSA is required and can improve the quality of this supply. VDDA has to be connected externally to VDDX.

NOTE

All GROUND pins of the microcontroller (VSSX1, VSSX2, VSS, VSSA, LGND and LSGND) must be connected together.

2.3.3 VSENSE — Supply (Battery) Voltage Sense Pin

This pin can be connected to the supply (Battery) line for voltage measurements. The voltage present at this input is scaled down by an internal voltage divider, and can be routed to the internal ADC. The pin itself is protected against reverse battery connections. To protect the pin from external fast transients, an external resistor (RVSENSE_R) is needed for protection.

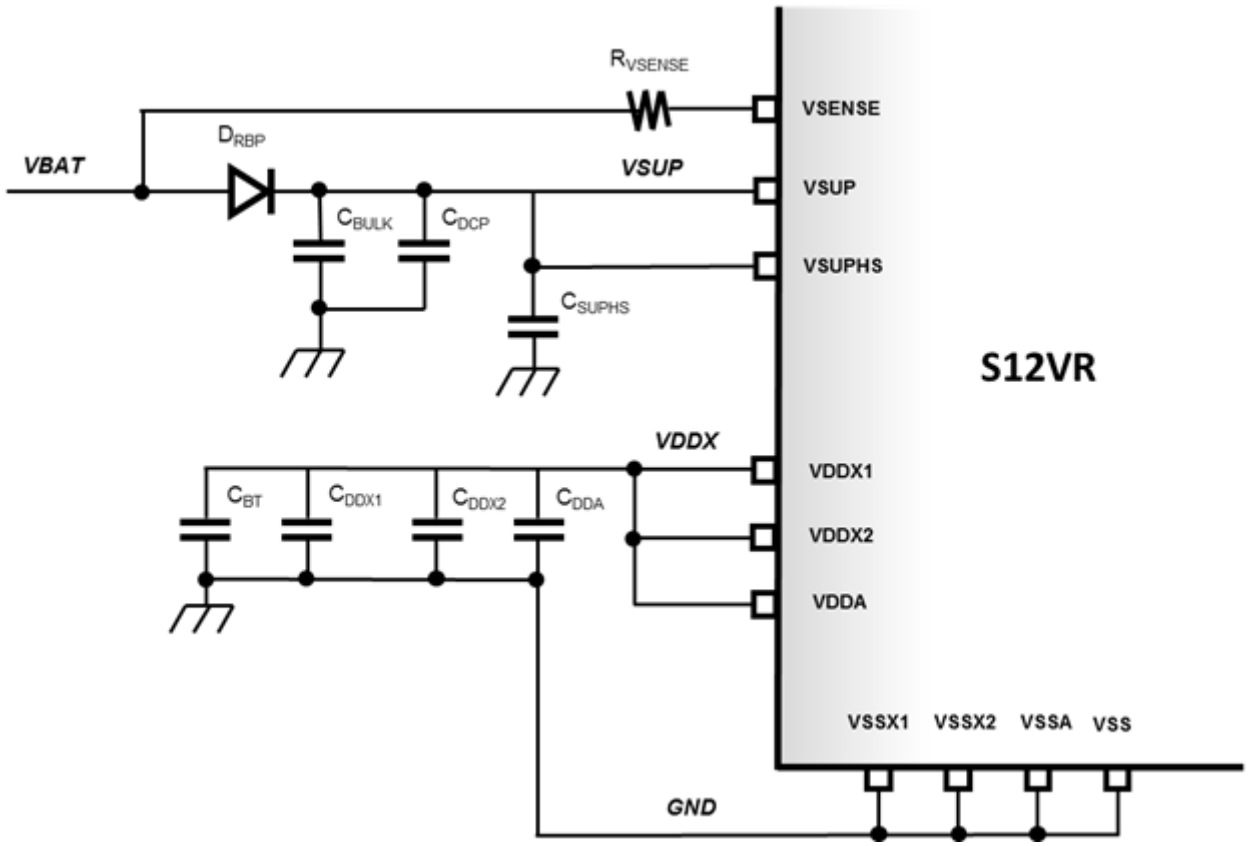


Figure 1. S12ZVR power supply pins

Table 1. Component description and recommended values for VDDX/VDDA

Symbol	Characteristic	Value
D_{RBP}	Reverse Current/Battery diode Protection	
C_{BULK}	Bulk/Bypass capacitor	
C_{DCP}	Decoupling Capacitor	
C_{SUPHS}	Decoupling/Bypass Capacitor	
R_{VSENSE}	Metal Film resistor	10 kΩ
C_{BT}	Stability Capacitor. X7R Ceramic or Tantalum	4.7 µF – 10 µF
$CD_{DX1,2}$	Decoupling Capacitor for VDDX. X7R Ceramic	100 nF - 220 nF
C_{DDA}	Decoupling Capacitor for VDDA. X7R Ceramic	100 nF - 220 nF

3 Programming Interface

3.1 BKGD

The background debug controller (BDC) is a single-wire, background debug system implemented in on chip hardware for minimal CPU intervention. The device BKGD pin interfaces directly to the BDC. The S12VR maintains the standard S12 serial interface protocol but introduces an enhanced handshake protocol and enhanced BDC command set to support the linear instruction set family of S12 devices and offer easier, more flexible internal resource access over the BDC serial interface. The BKGD signal is used as a pseudo-open-drain signal for the background debug communication. The BKGD signal has an internal pull-up device.

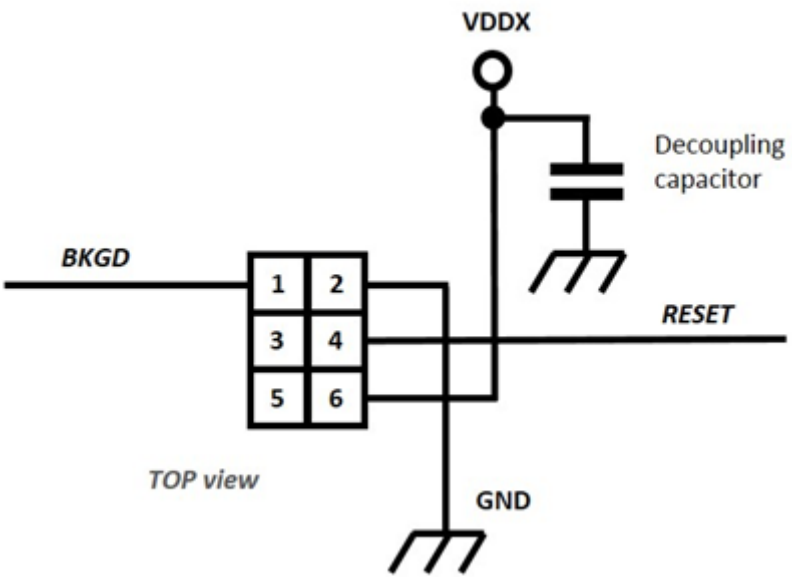


Figure 2. Debug connector configuration

3.2 RESET

The RESET signal is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The RESET pin has an internal pull-up device.

Upon detection of any reset source, an internal circuit drives the RESET pin low for 512 PLLCLK cycles. After 512 PLLCLK cycles the RESET pin is released. The internal reset of the MCU remains asserted while the reset generator completes the 768 PLLCLK cycles long reset sequence. In case the RESET pin is externally driven low for more than these 768 PLLCLK cycles (External Reset), the internal reset remains asserted longer.

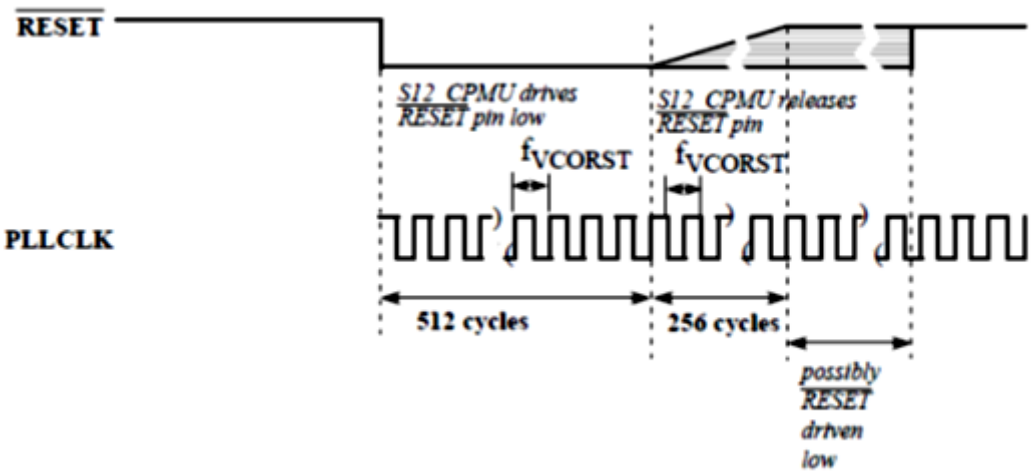


Figure 3. Debug connector configuration

In prototype designs, it is common to add a push-button to manually force a reset. In this case, the designer could choose to add a debounce capacitor to this button. In the event of an internal reset event, the MCU forces the RESET pin low and up again so that other circuits connected to this pin are reset as well. This reset pulse must last less than 24 µs. The debounce capacitance on the reset line must ensure that this timing constraint is met. Capacitors smaller than 10 pF are recommended.

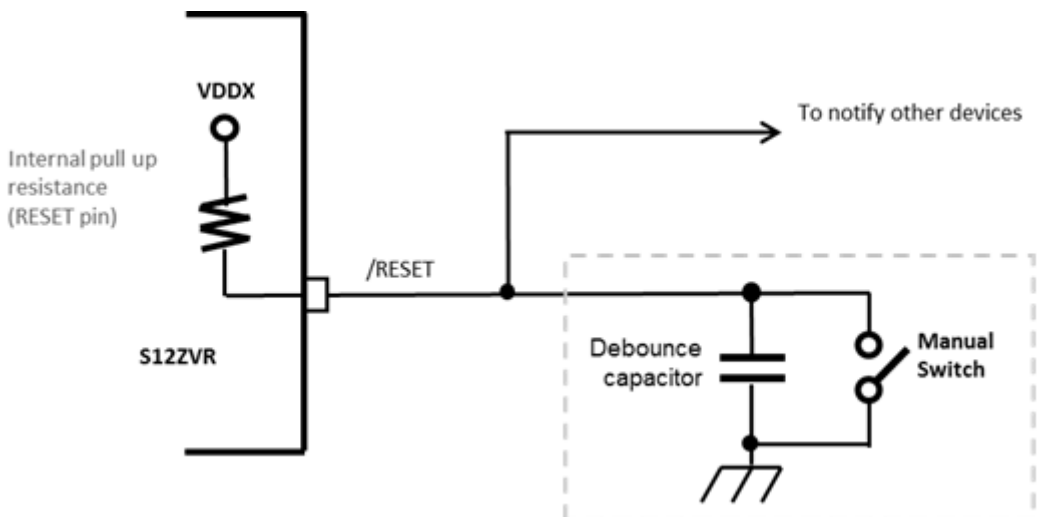


Figure 4. Debug connector configuration

3.3 TEST Pin

This pin should always be grounded in all applications.

4 Clock Circuitry

The S12VR devices have an internal 1 MHz internal RC oscillator with +/-1.3% accuracy over rated temperature range. There is an alternative to add an external resonator or crystal, for higher and tighter tolerance frequencies. The S12VR includes an oscillator control module capable of supporting either Loop Controlled Pierce (LCP) or Full Swing Pierce (FSP) oscillator configurations. The oscillation mode is selectable by software.

4.1 EXTAL and XTAL

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. If XOSCLCP is enabled, the MCU internal OSCCLK_LCP is derived from the EXTAL input frequency. If OSCE=0, the EXTAL pin is pulled down by an internal resistor of approximately 200 kΩ and the XTAL pin is pulled down by an internal resistor of approximately 700 kΩ.

The pierce oscillator provides a robust, low-noise and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators. S12VR supports crystals or resonators from 4 MHz to 20 MHz. The Input Capacitance of the EXTAL, XTAL pins is 7 pF.

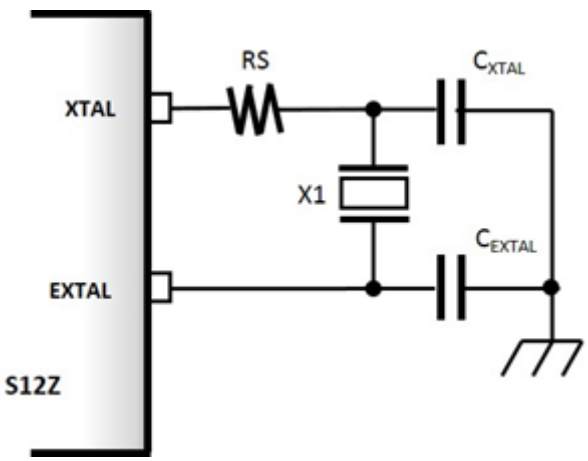


Figure 5. Debug connector configuration

Table 2. Components of the oscillator circuit

Symbol	Description
R_S	Bias Resistor
X_1	Quartz Crystal / Ceramic Resonator
C_{XTAL}	Stabilizing Capacitor
C_{EXTAL}	Stabilizing Capacitor

The load capacitors are dependent on the specifications of the crystal and on the board capacitance. It is recommended to have the crystal manufacturer evaluate the crystal on the PCB.

4.2 Suggestions for the PCB Layout of Oscillator Circuit

The crystal oscillator is an analog circuit and must be designed carefully and according to analog-board layout rules:

- External feedback resistor [Rf] is not needed because it's already integrated.

- It is recommended to send the PCB to the crystal manufacturer to determine the negative oscillation margin as well as the optimum regarding CXTAL and CEXTAL capacitors. The data sheet includes recommendations for the tank capacitors CXTAL and CEXTAL. These values together with the expected PCB, pin, etc. stray capacity values should be used as a starting point.
- Signal traces between the S12VR pins, the crystal and, the external capacitors must be as short as possible, without using any via. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI. The capacitance of the signal traces must be considered when dimensioning the load capacitors.
- Guard the crystal traces with ground traces (guard ring). This ground guard ring must be clean ground. This means that no current from and to other devices should be flowing through the guard ring. This guard ring should be connected to VSSx of the S12VR with a short trace. Never connect the ground guard ring to any other ground signal on the board. Also avoid implementing ground loops.
- The main oscillation loop current is flowing between the crystal and the load capacitors. This signal path (crystal to CEXTAL to CXTAL to crystal) should be kept as short as possible and should have a symmetric layout. Hence, both capacitor's ground connections should always be as close together as possible.

The following figure shows the recommended placement and routing for the oscillator layout.

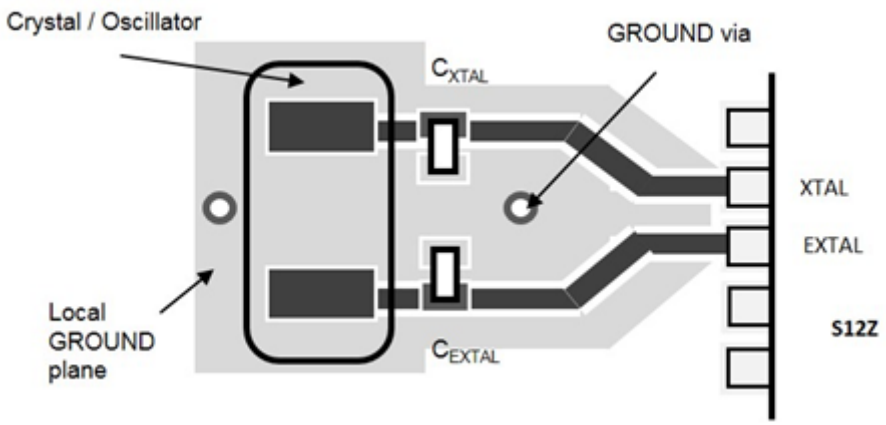


Figure 6. Suggested Crystal Oscillator Layout

5 High Voltage Inputs (HVI)

The high-voltage input (HVI) on port L has the following features:

- Input voltage proof up to VHVI
- Digital input function with pin interrupt and wakeup from stop capability
- Analog input function with selectable divider ratio routable to ADC channel. Optional direct input bypassing voltage divider and impedance converter. Capable to wake-up from stop (pin interrupts in run mode not available). Open input detection.

The connection of an external pull device on a high-voltage input can be validated by using the built-in pull functionality of the HVI. Depending on the application type, an external pull down circuit can be detected with the internal pull-up device whereas an external pull-up circuit can be detected with the internal pull down device which is part of the input voltage divider.

Note that the following procedures make use of a function that overrides the automatic disable mechanism of the digital input buffer when using the HVI in analog mode. Make sure to switch off the override function when using the HVI in analog mode after the check has been completed.

An external resistor REXT_HVI must be always connected to the high-voltage inputs to protect the device pins from fast transients and to achieve the specified pin input divider ratios when using the HVI in analog mode.

5.1 External Pulldown Device

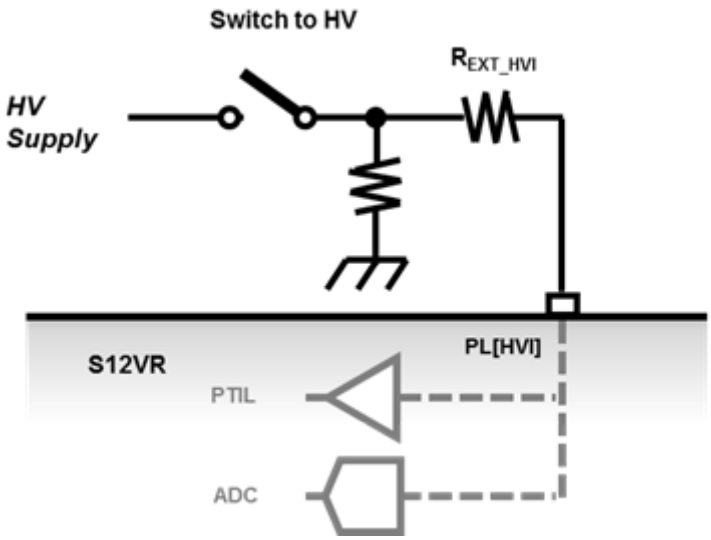


Figure 7. Digital Input Read with Pull-up Enabled

5.2 External Pullup Device

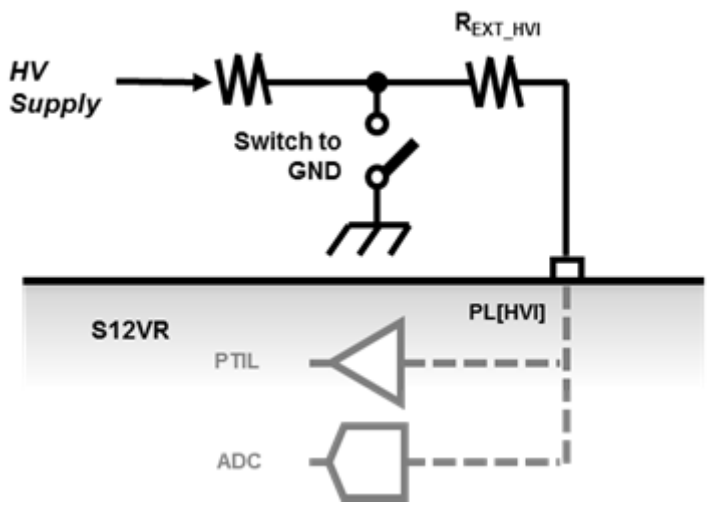


Figure 8. Digital Input Read with Pull-down Enabled

6 High-Side Drivers

The HSDRV module provides two high-side drivers typically used to drive LED or resistive loads. The nominal current high-side drivers can operate is 50 mA, so the resistive load must consider that specification. The incandescent or halogen lamp is not considered here as a possible load.

NOTE

On mask set 2N05E, high-side drivers cannot drive capacitive loads. Doing so could activate the overcurrent shutdown circuitry. Mask set 0N59H includes an overcurrent fault mask logic. This can mask faults that last less than 10 µs after the High Side Driver is activated, thus masking the overcurrent associated with small capacitors connected at the pin.

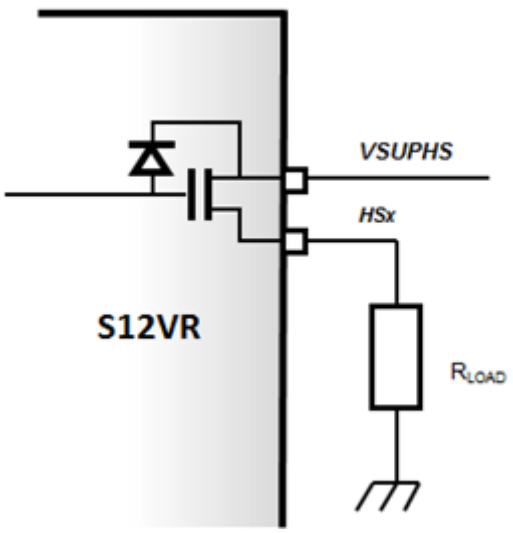


Figure 9. High side driver

7 Low-Side Drivers

The LSDRV module includes two independent low side drivers with common current sink. Each driver has the following features:

- Selectable gate control of low-side switches: LSDRx register bits, PWM or timer channels. See PIM chapter in the reference manual for routing options.
- Open-load detection while enabled – While driver off: selectable high-load resistance open-load detection.
- Over-current protection with shutdown

Low-side drivers drive coils up to 450 mH at a 10 kHz frequency; a reverse battery protection is required. Thus, the other end of the coil can be connected to the VSUP pin, which should also be protected by a diode. Pin LSGND must be connected to the same ground as the voltage regulator.

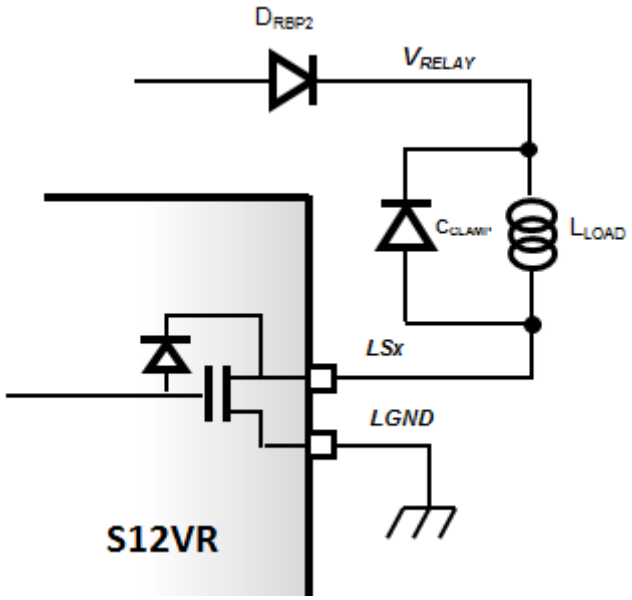


Figure 10. Debug connector configuration

Table 3. Component description for LSx pins

Symbol	Characteristic	Value
D_{RBP2}	Reverse Current/Battery diode Protection	
D_{CLAMP}	Clamp diode Protection	

8 LIN Interface Circuit

The Local Interconnect Network (LIN) is a serial communication protocol, designed to support automotive networks. As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required.

The LIN Physical Layer module includes the following distinctive features:

- Compliant with LIN Physical Layer 2.2 specification
- Compliant with the SAE J2602-2 LIN standard
- Standby mode with glitch-filtered wake-up
- Slew rate selection optimized for the baud rates: 10.4 Kbit/s, 20 Kbit/s and Fast Mode (up to 250 Kbit/s)
- Switchable 34 kΩ/330 kΩ pull up resistors (in shutdown mode, 330 kΩ only)
- Current limitation for LIN Bus pin falling edge
- Overcurrent protection
- LIN TxD-dominant timeout feature monitoring the LPTxD signal

The LIN transmitter is a low-side MOSFET with current limitation and overcurrent transmitter shutdown. A selectable internal pull up resistor with a serial diode structure is integrated, so no external pull up components are required for the application in a slave node. To be used as a master node, an external resistor of 1 kΩ must be placed in parallel between VLINSUP and the LIN Bus pin, with a diode between VLINSUP and the resistor. The fall time from recessive to dominant and the rise time from dominant to recessive is selectable and controlled to guarantee communication quality and reduce EMC emissions. The symmetry between both slopes is guaranteed.

Typical applications for LIN include switches, actuators (e.g., window lift and door lock modules), body control electronics for occupant comfort (e.g., door, steering wheel, seat and mirror modules), motors, and sensors (e.g., in climate control, lighting, rain sensors, smart wipers, intelligent alternators and switch panels).

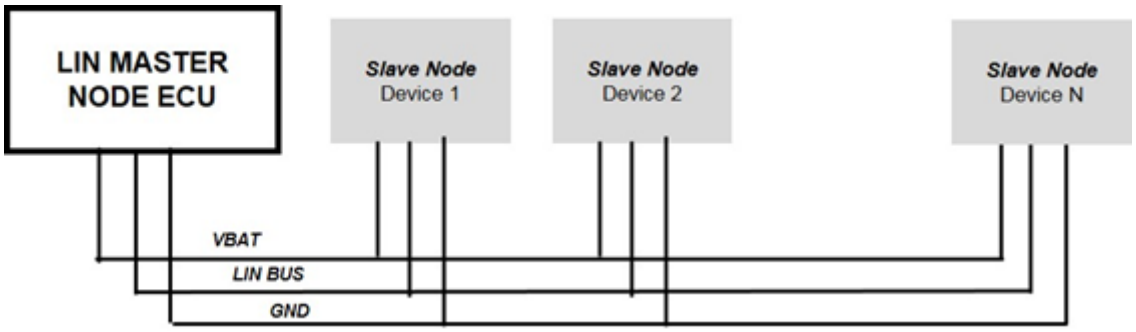


Figure 11. LIN bus topology

The LIN bus topology utilizes a single master and multiple nodes, as shown below. Connecting application modules to the vehicle network makes them accessible for diagnostics and service.

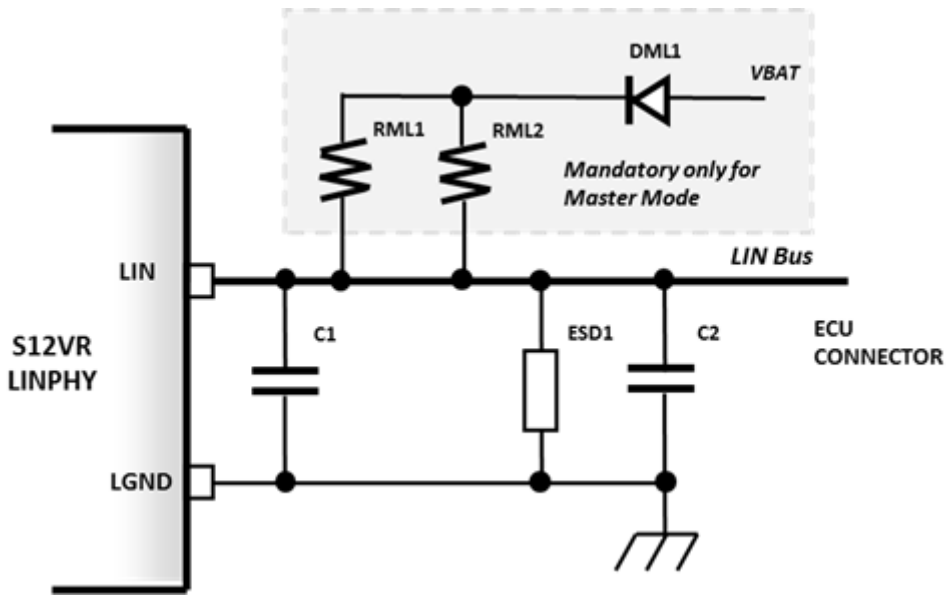


Figure 12. Circuit diagram for LIN Interface

8.1 LIN Components Data

Table 4. LIN components

Reference	Part	Mounting	Remark
DMLIN	Diode	Mandatory only for master ECU	Reverse Polarity protection from LIN to VSUP.
RML1 and RML2	Resistor: 2 kΩ Power Loss: 250 mW Tolerance: 1%	Mandatory only for Master ECU	For Master ECU: If more than 2 resistors are used in parallel, the values have to be chosen in a way

Table continues on the next page...

Table 4. LIN components (continued)

Reference	Part	Mounting	Remark
	Package Size: 1206 Requirement: Min Power rating of the complete master termination has to be ≥ 500 mW		that the overall resistance RM of 1 kΩ and the minimum power loss of the complete master termination has to be fulfilled. For Slave ECU: RMLIN1 and RMLIN2 are not needed on the PCB layout
C1	Capacitor: Slave ECU: typically 220 pF Master ECU: from 560 pF up to approximately ten times that value in the slave node [CSLAVE], so that the total line capacitance is less dependent on the number of slave nodes. Tolerance: 10% Package Size: 0805 Voltage: ≥50 V	Mandatory	The value of the master node has to be chosen in a way that the LIN specification is fulfilled.
C2	Capacitor: Package Size: 0805	Optional	Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.
ESD1	ESD Protection Package Size: 0603 -0805	Optional	Layout pad for an additional ESD protection part. Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.

9 Unused Pins

Unused digital pins can be left floating. To reduce power consumption, it is recommended that these unused digital pins are configured as inputs and have the internal pull resistor enabled. This will decrease current consumption and susceptibility to external electromagnetic noise. ADC unused pins should be grounded to reduce leakage currents. The EXTAL and XTAL pins default reset condition is to have pull-downs enabled. These pins should be connected to ground if not used.

The voltage regulator controller pin BCTL should be left unconnected if not used, and the VDDX voltage regulator must be configured to operate with the internal power transistor by setting the appropriate register (CPMUVREGCTL register, bit EXTXON = 0, bit INTXON = 1). If the VDDC regulator is not used, the VDDC pin must be shorted with VDDX, and the BCTLC pin must be left unconnected.

10 General Board Layout Guidelines

10.1 Traces Recommendations

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in the figure below.

Figure 13. Poor and correct way of bending traces in right angles

To minimize crosstalk, not only between two signals on one layer but also between adjacent layers, route them 90° to each other.

Complex boards need to use vias while routing; you have to be careful when using them. These add additional capacitance and inductance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. While using differential signals, use vias in both traces or compensate the delay in the other trace.

10.2 Grounding

Grounding techniques apply to both multi-layer and single-layer PCBs. The objective of grounding techniques is to minimize the ground impedance and thus to reduce the potential of the ground loop from circuit back to the supply.

- Route high-speed signals above a solid and unbroken ground plane.
- Do not split the ground plane into separate planes for analog, digital, and power pins. A single and continuous ground plane is recommended.
- There should be no floating metal/shape of any kind near any area close to the microcontroller pins. Fill copper in the unused area of signal planes and connect these coppers to the ground plane through vias.

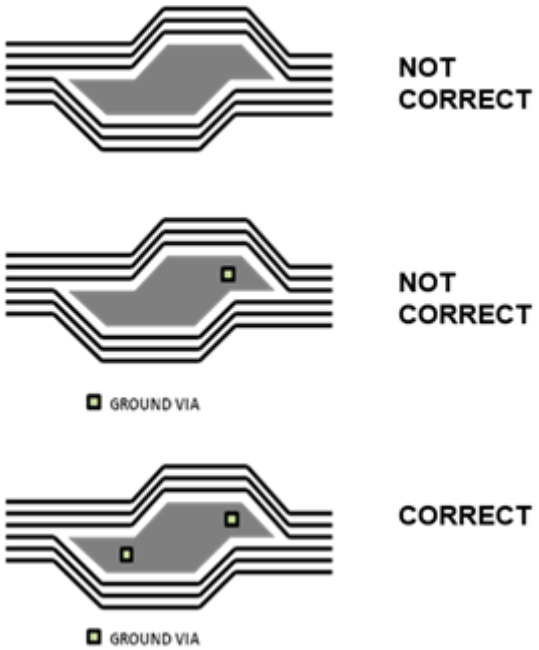
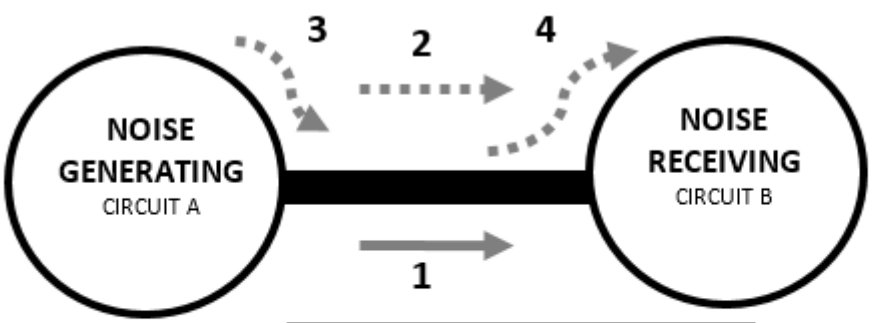


Figure 14. Eliminating floating metal/shape

10.3 EMI/EMC and ESD Considerations for Layout

These considerations are important for all system and board designs. Though the theory behind this is well explained, each board and system experiences this in its own way. There are many PCB and component related variables involved.

This application note does not go into the electromagnetic theory or explain the whys of different techniques used to combat the effects, but it considers the effects and solutions most recommended as applied to CMOS circuits. EMI is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby. Studying EMC for your system allows testing the ability of your system to operate successfully counteracting the effects of unplanned electromagnetic disturbances coming from the devices and systems around it. The electromagnetic noise or disturbances travels via two media: conduction and radiation.



	Propagation path
1	Conductor
2	Air
3	Air to Conductor
4	Conductor to Air

Figure 15. Electromagnetic noise propagation

The design considerations narrow down to:

- The radiated and conducted EMI from your board should be lower than the allowed levels by the standards you are following.
- The ability of your board to operate successfully counteracting the radiated and conducted electromagnetic energy (EMC) from other systems around it.

The EMI sources for a system consists of several components such as PCB, connectors, cables, etc. The PCB plays a major role in radiating the high frequency noise. At higher frequencies and fast-switching currents and voltages, the PCB traces become effective antennas radiating electromagnetic energy; e.g., a large loop of signal and corresponding ground. The five main sources of radiation are: digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast switching clocks, external buses, PWM signals are used as control outputs and in switching power supplies. The power supply is another major contributor to EMI. RF signals can propagate from one section of the board to another building up EMI. Switching power supplies radiate the energy which can fail the EMI test. This is a huge subject and there are many books, articles and white papers detailing the theory behind it and the design criteria to combat its effects.

Every board or system is different as far as EMI/EMC and ESD issues are concerned, requiring its own solution.

However, the common guidelines to reduce an unwanted generation of electromagnetic energy are as shown below:

- Ensure that the power supply is rated for the application and optimized with decoupling capacitors.
- Provide adequate filter capacitors on the power supply source. The bulk/bypass and decoupling capacitors should have low equivalent series inductance (ESL).
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias.
- Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.

11 References

- MC9S12VR-Family Reference Manual, see nxp.com

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