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Revisions			
Rev	Description	Date	Approved
A	Original Release	9/10/09	T.Q
A1	DNP R315.Install R316	11/19/09	T.Q
	Remove R160		
	Pull up U29.1/4		
	DNP R32.Install R34		
	DNP R70.Install R74		
	DNP R51.Install R63		
	Change relay power to 5V Add protect diode		
	Change 25M crystal due to height limit Add 4.7k pull up on LGPL4 Change C72/C73 to 8pf		
B	Release for pilot	12/01/09	T.Q
B1	Fixed wrong symbol of part 480-75983	02/02/10	T.Q
	Changed power input from ATX to PD45		
	Added +3.3V DC-DC output		
	Reassigned RJ45 UART pin order		

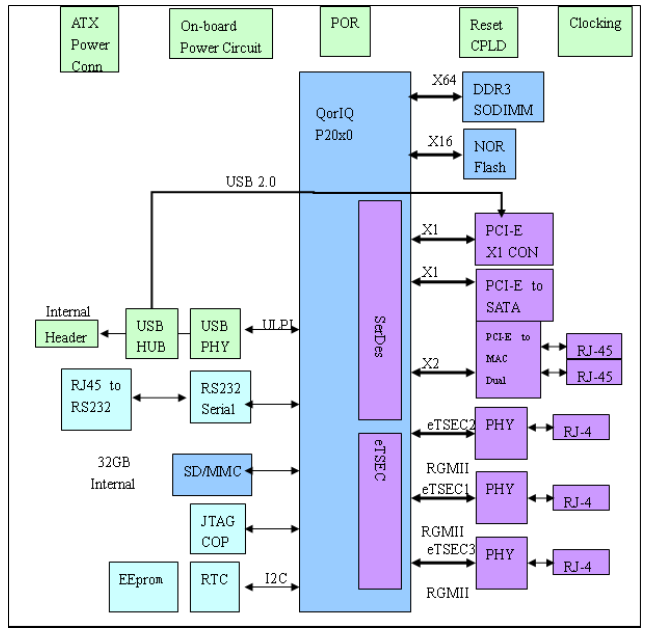
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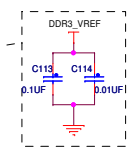
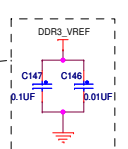
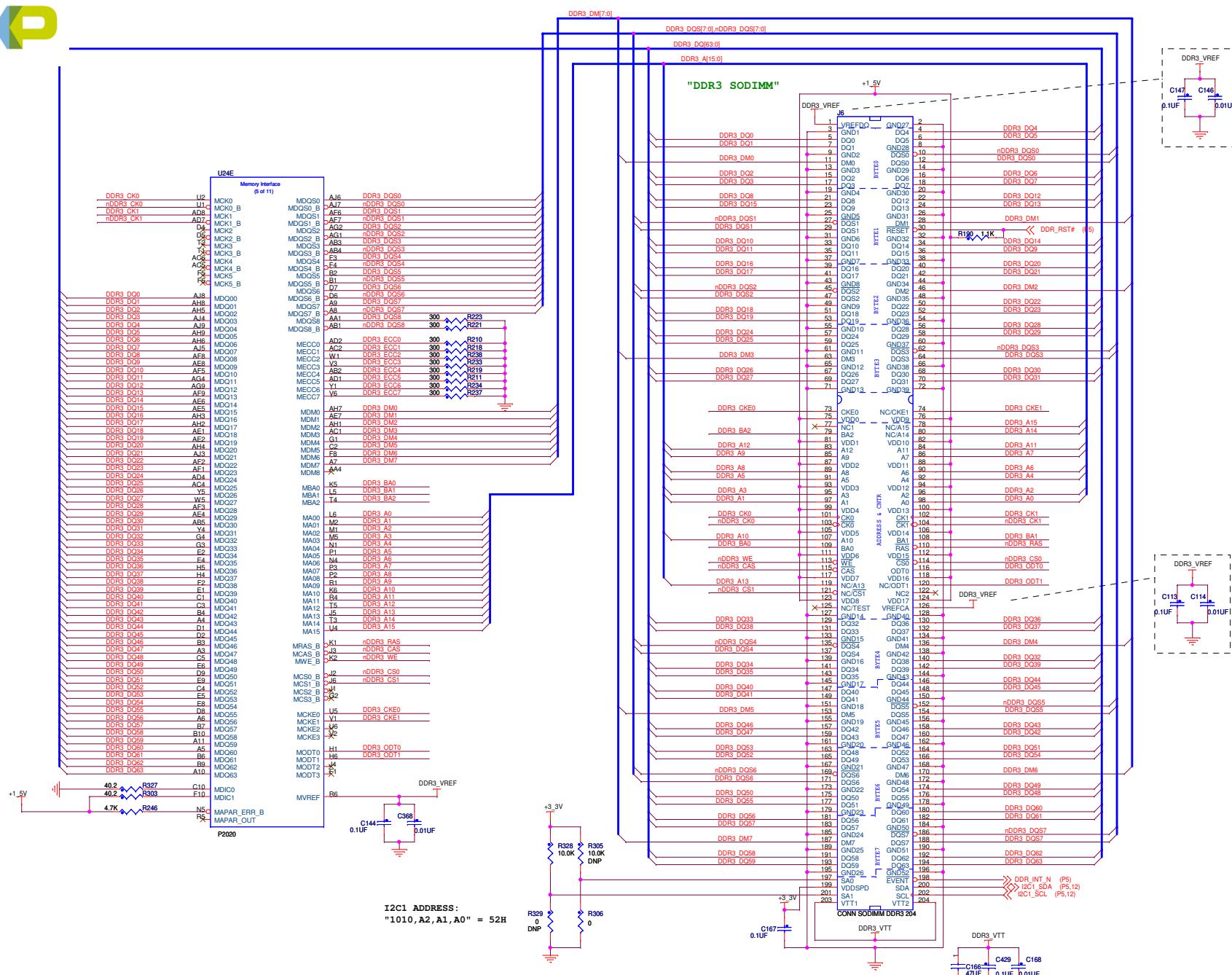
	SECURE-1000	SECURE-2000	SECURE-4000
CPU	QorIQ P2010E 800 MHz	QorIQ P2020E 800 MHz	QorIQ P2020E 1.2 GHz

		Networking & Multimedia Group 6501 William Cannon Drive West Austin, TX 78758-6598	
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Drawing Title: P2020SECURE-4000/2000/1000		Drawn by: <DrawnBy>	
Page Title: COVER PAGE		Approved: <Approver>	
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All polarized capacitors are aluminum electrolytic

- Interrupted lines coded with the same letter or letter combinations are electrically connected.
- Device type number is for reference only. The number varies with the manufacturer.
- Special signal usage:
 _B Denotes - Active-Low Signal
 <> or [] Denotes - Vectored Signals
- Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.





I2C1 ADDRESS:
"1010,A2,A1,A0" = 52H

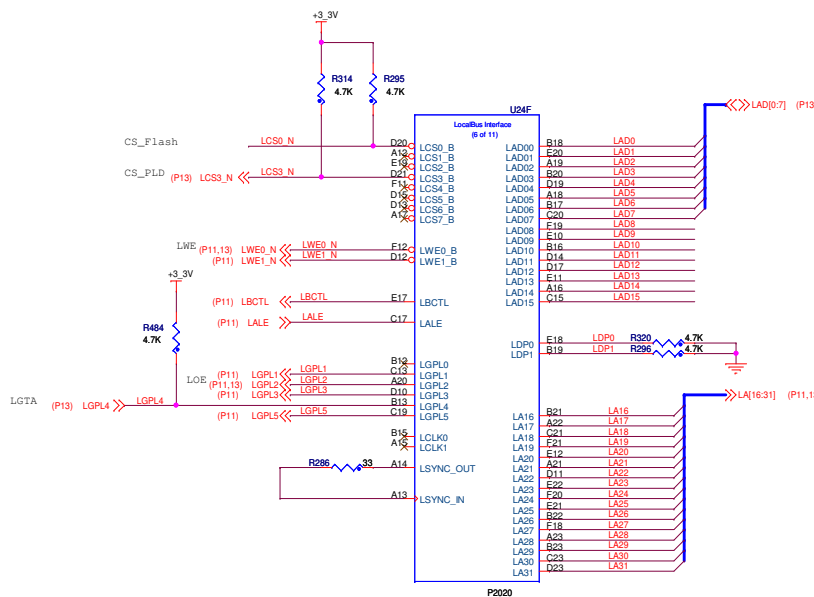
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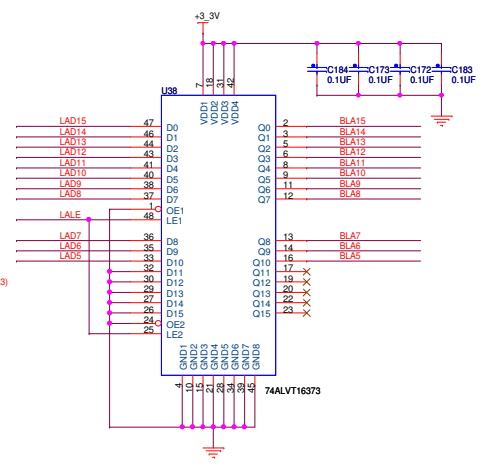
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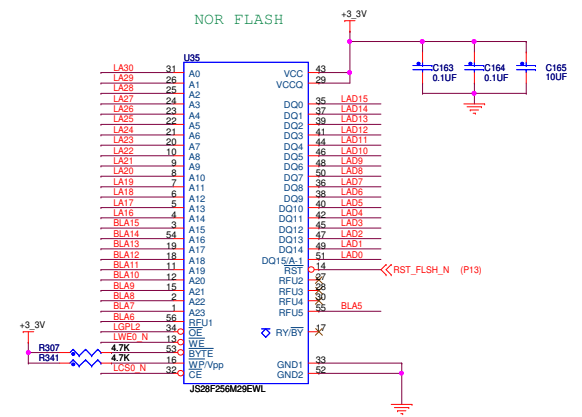
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LOCAL BUS INTERFACE
ADDRESS - LATCH



NOR FLASH



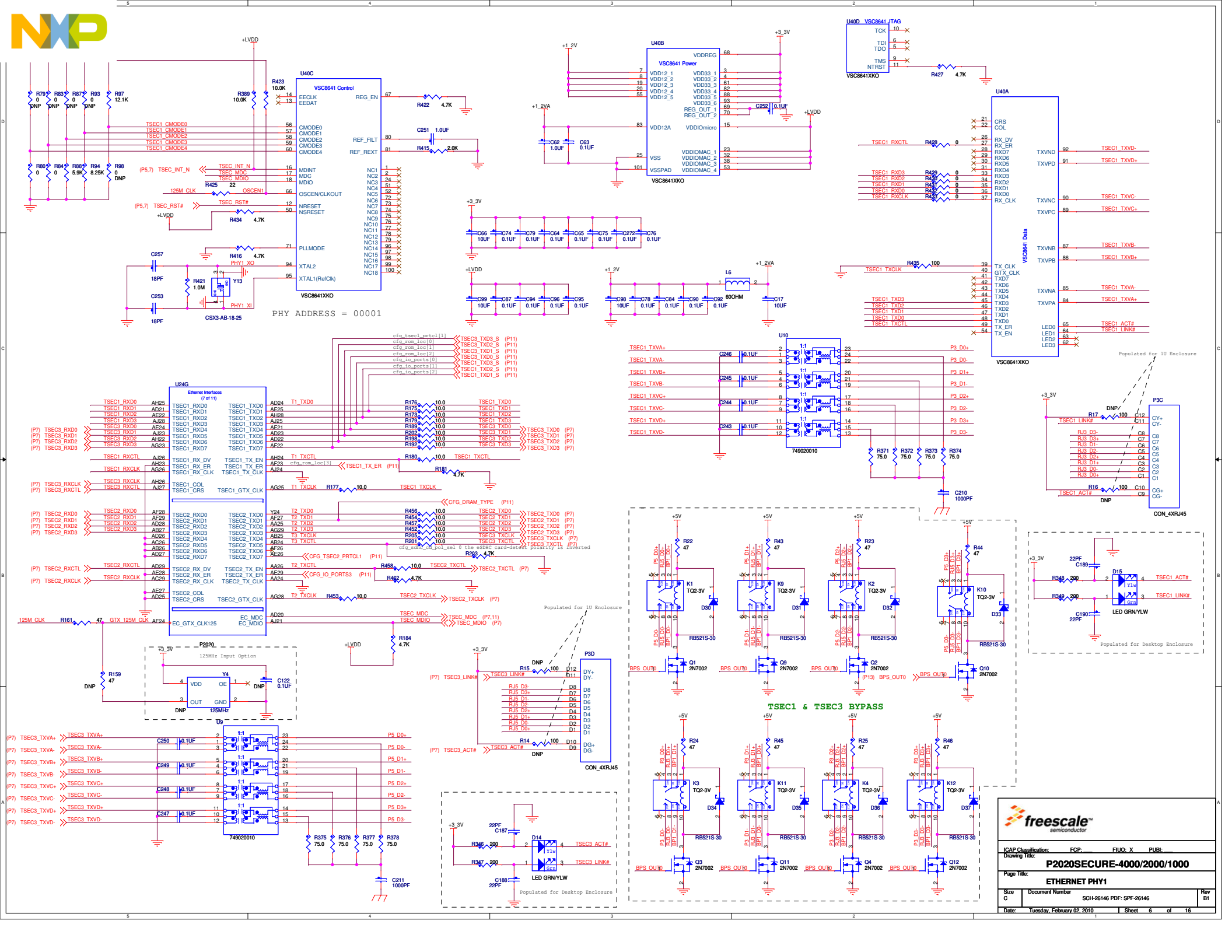
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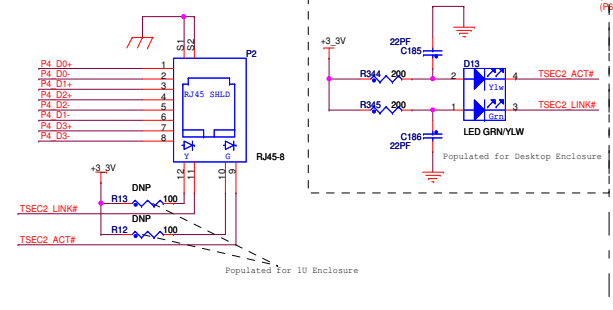
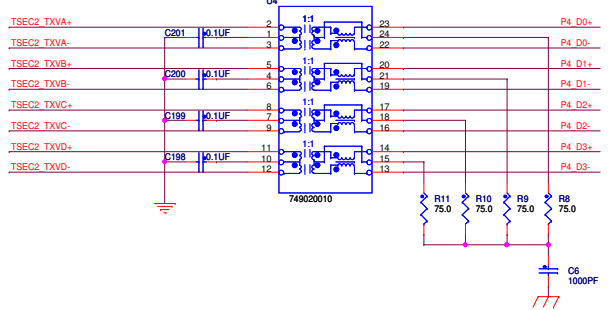
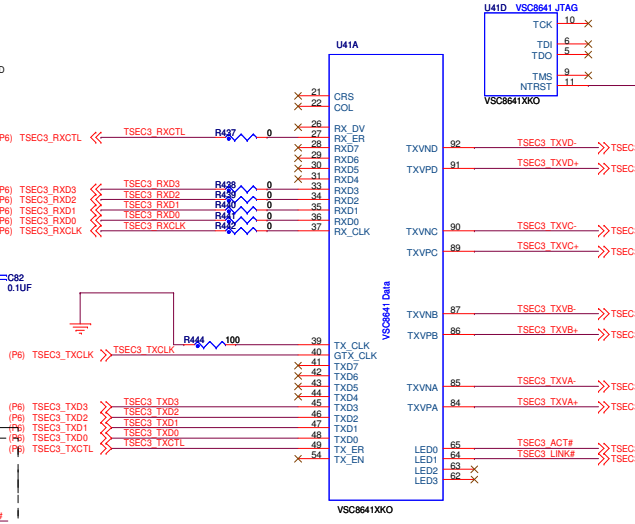
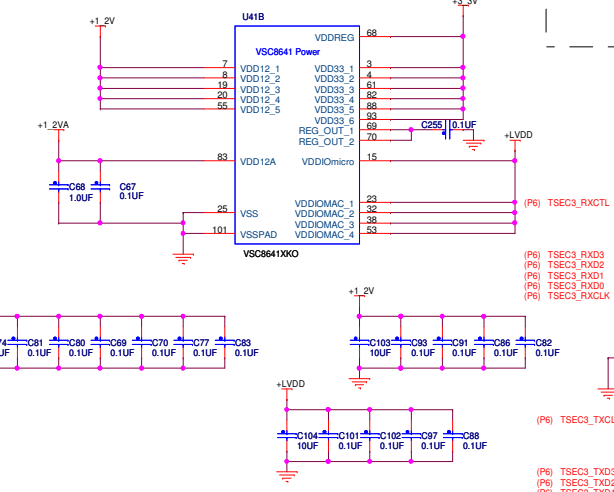
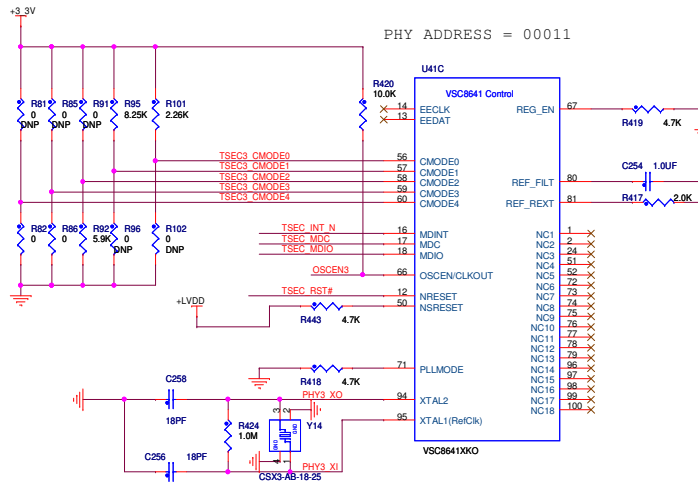
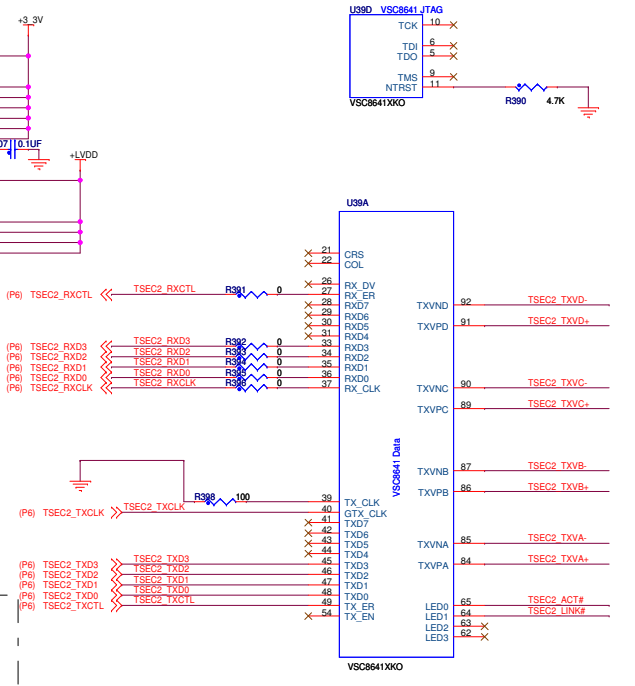
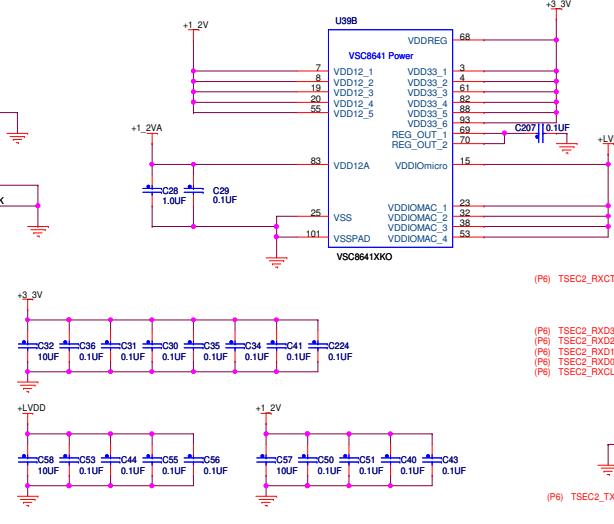
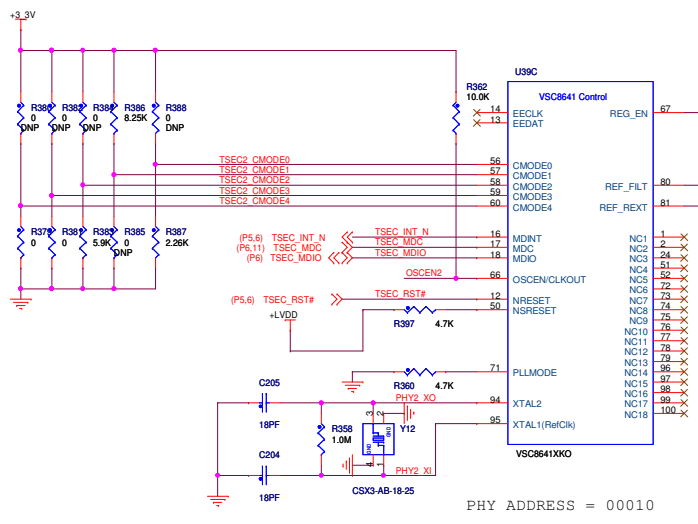
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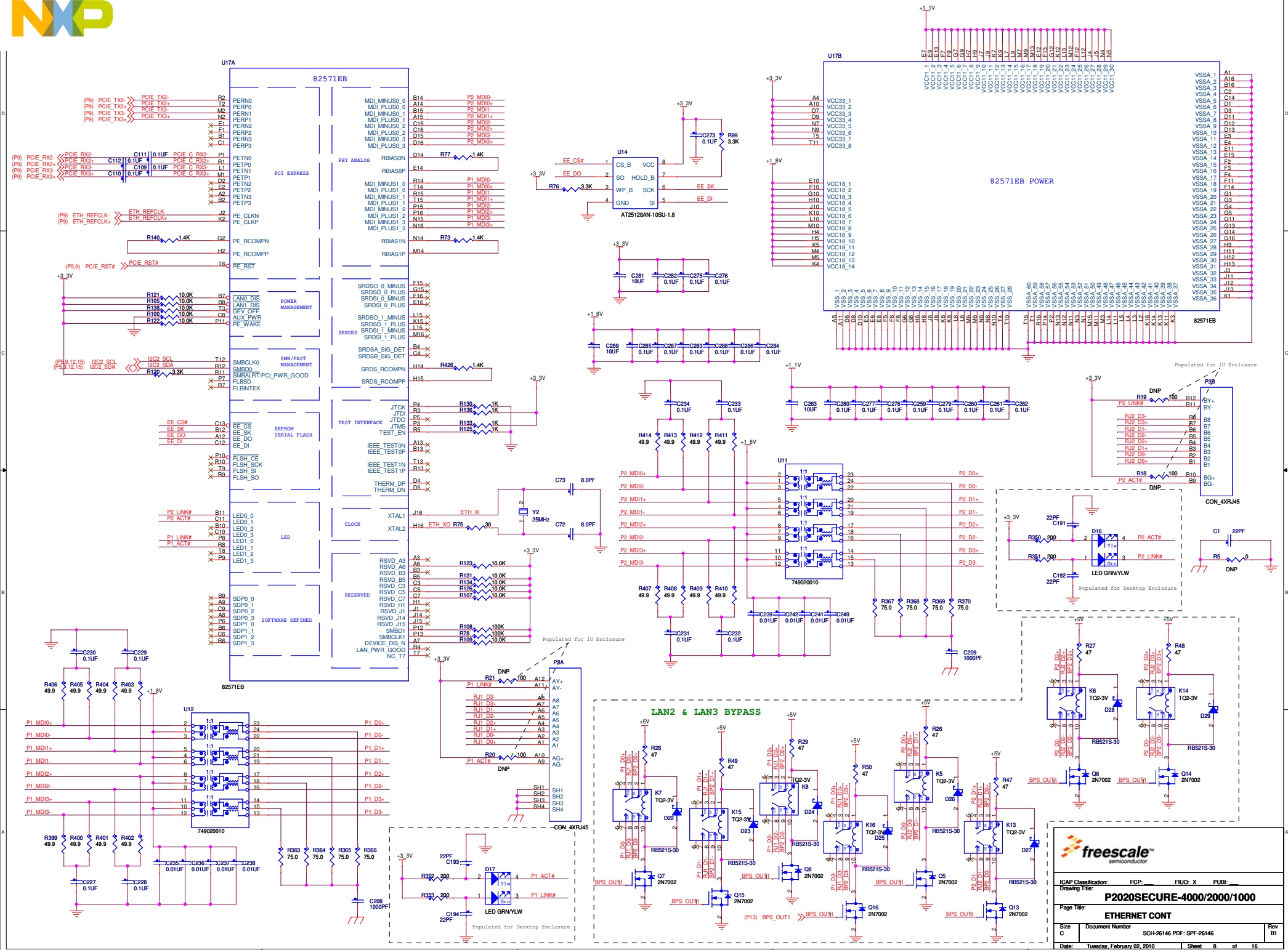
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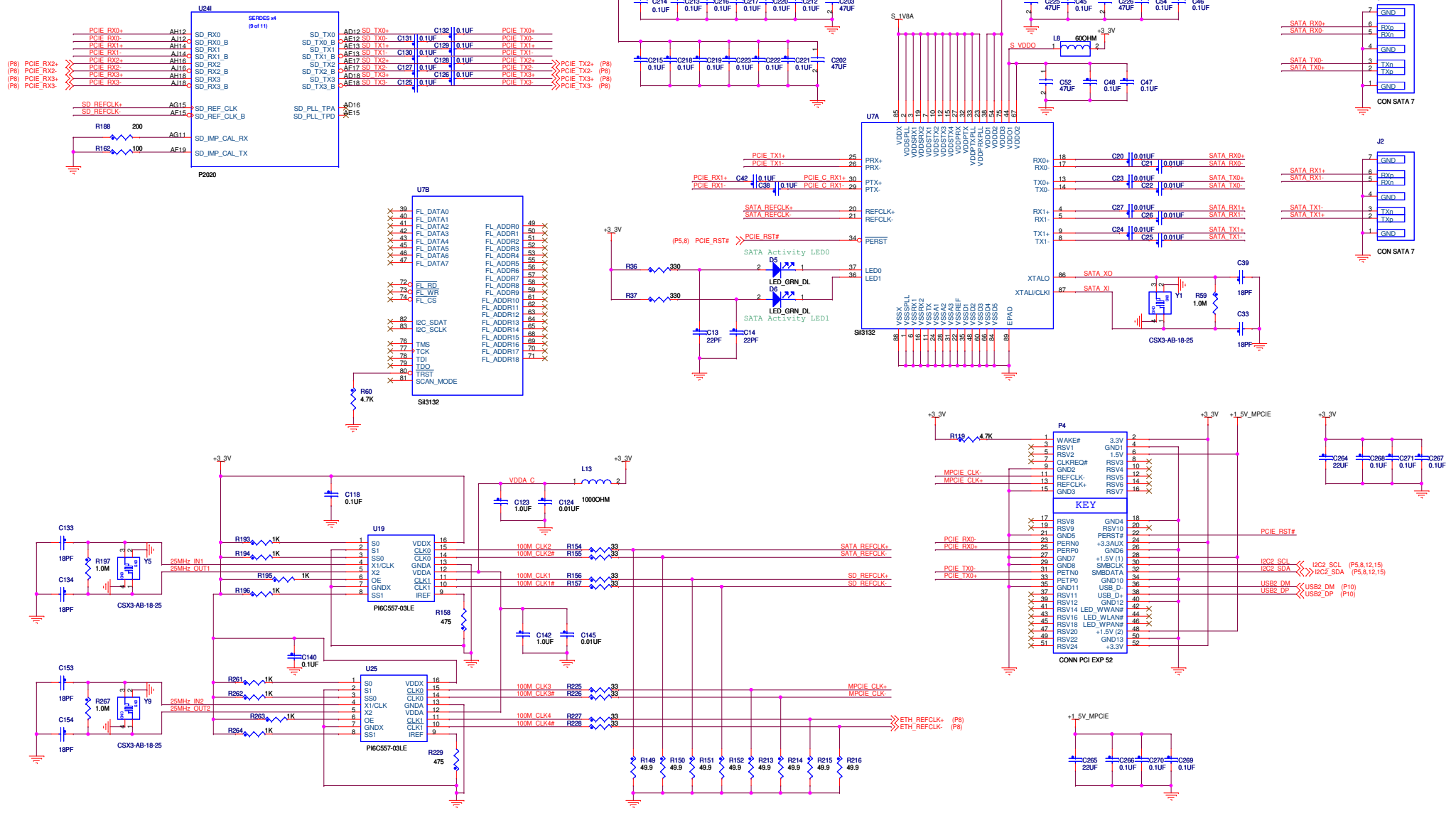
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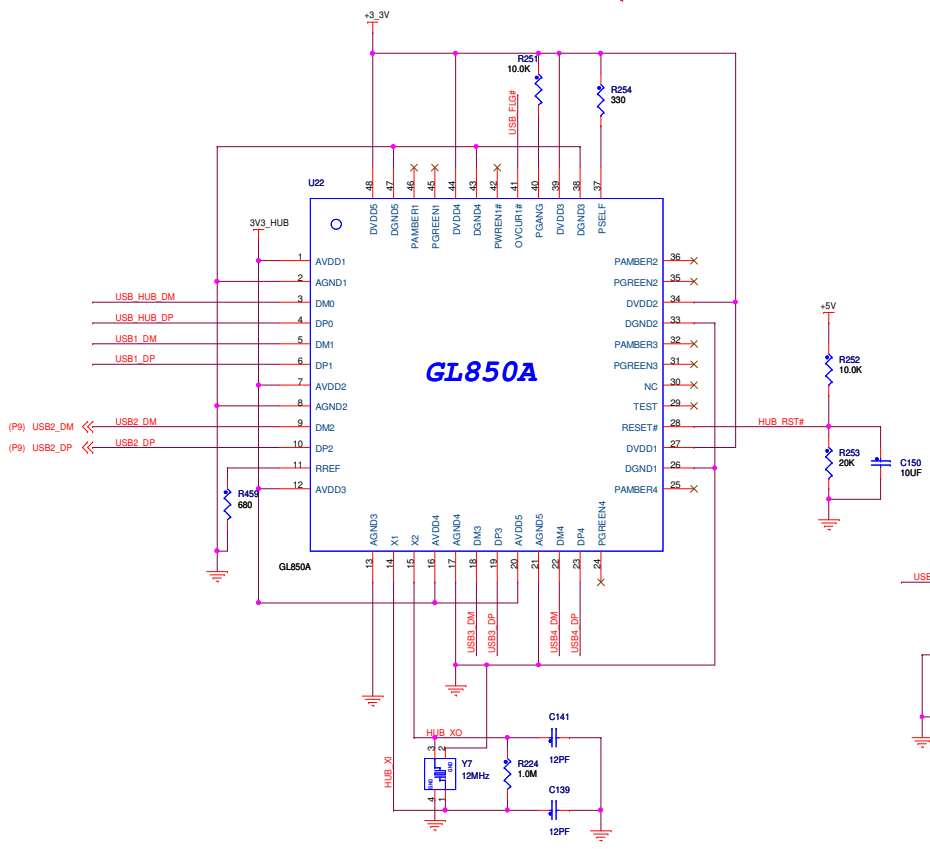
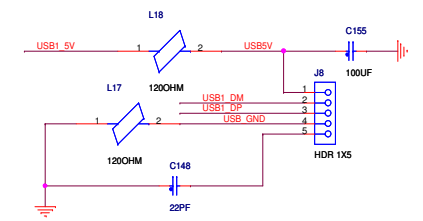
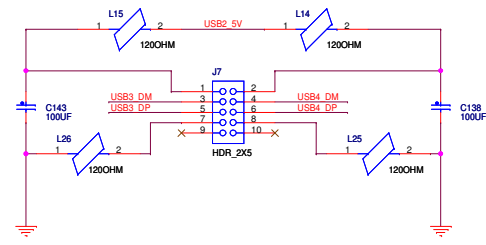
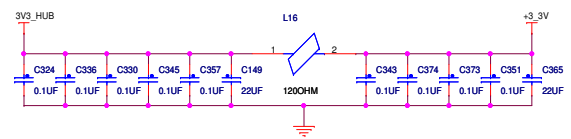
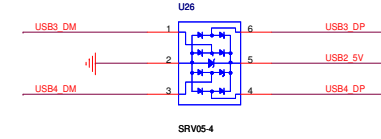
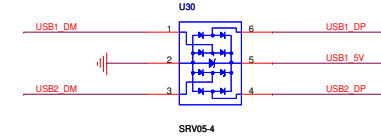
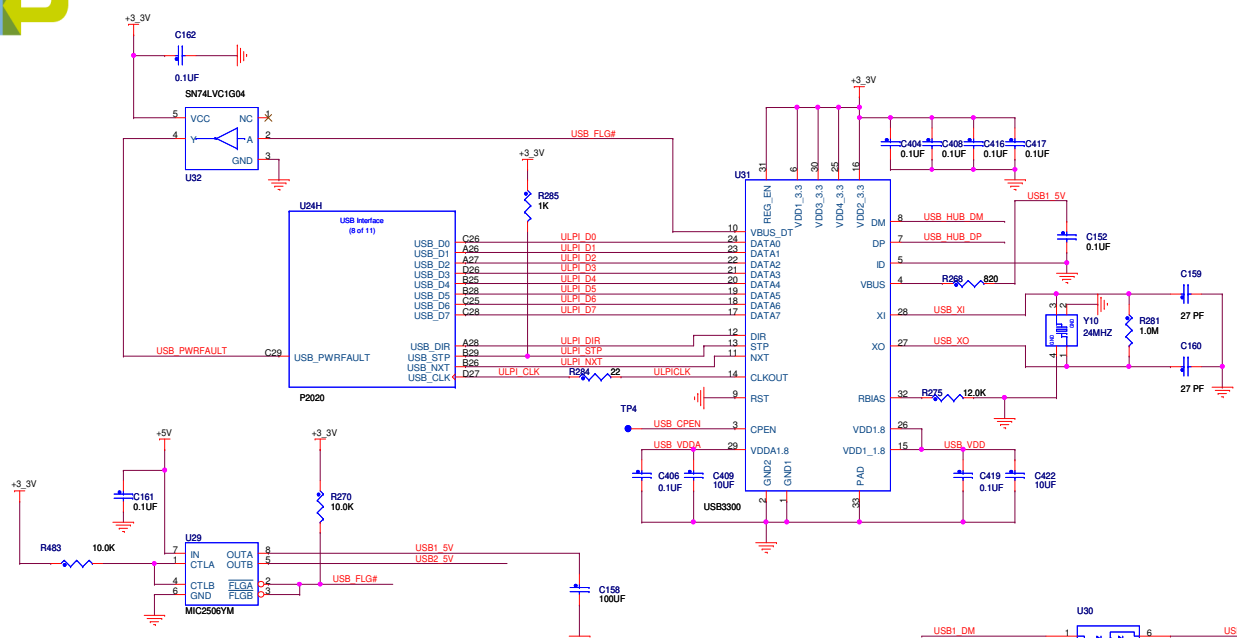
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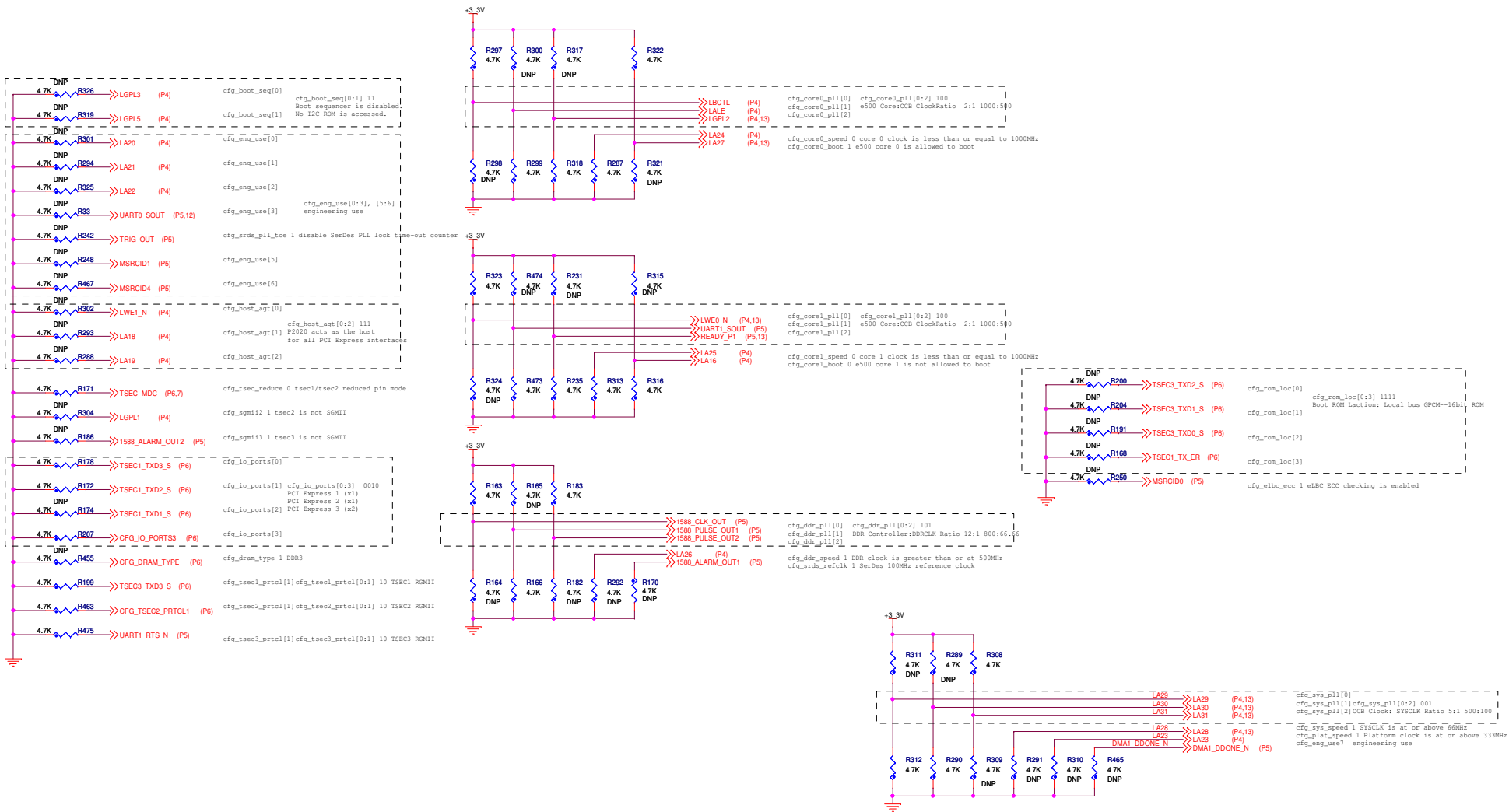
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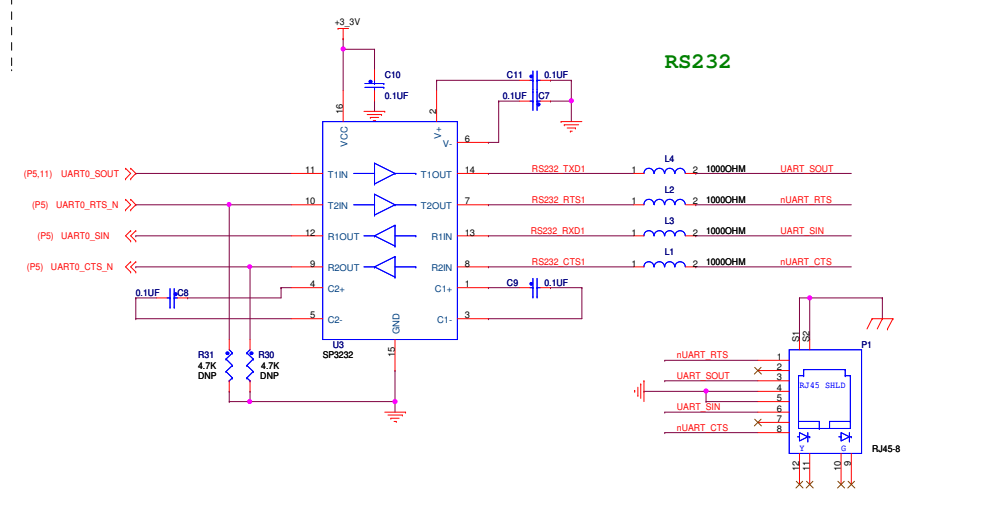
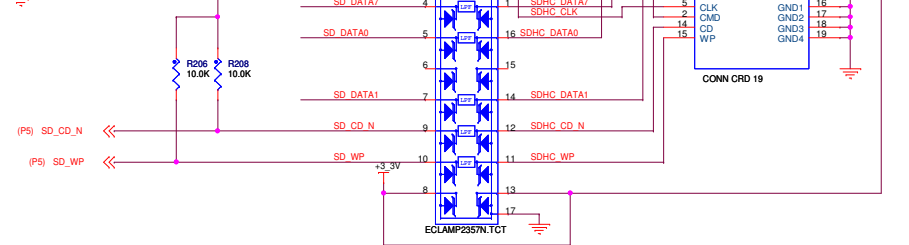
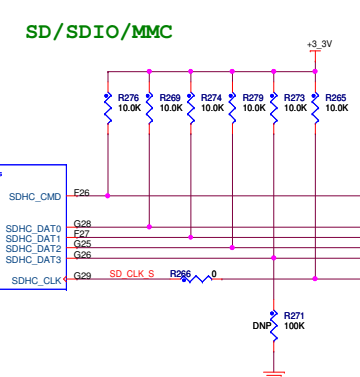
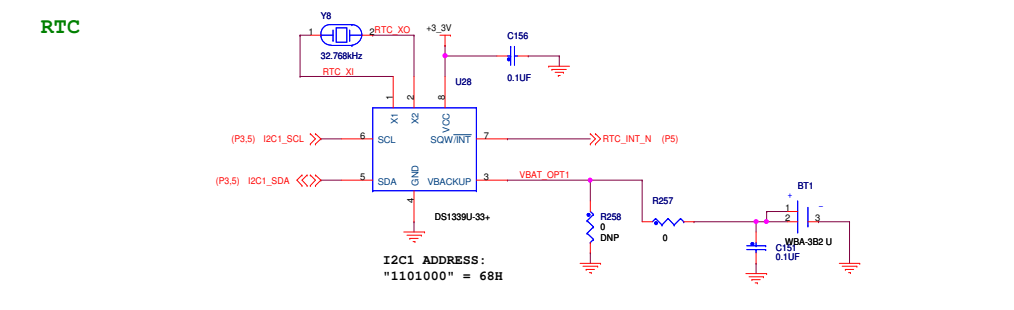
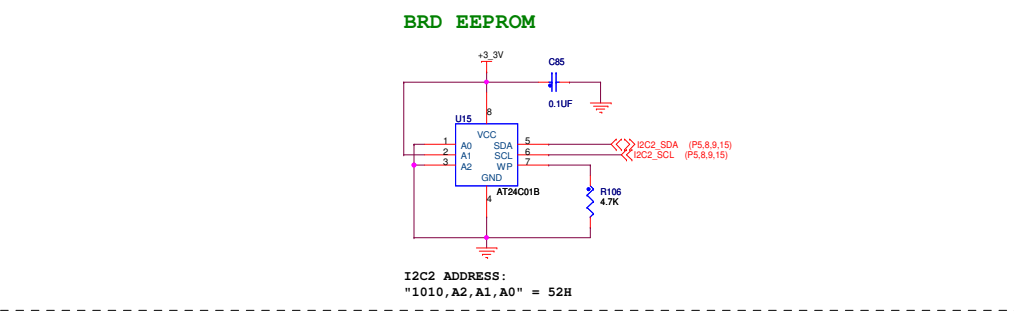
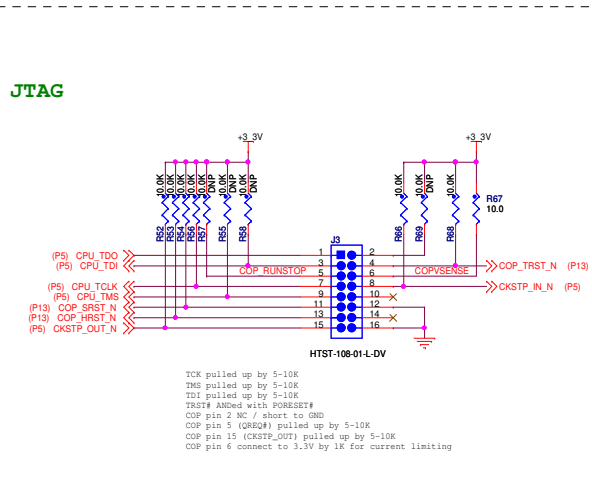
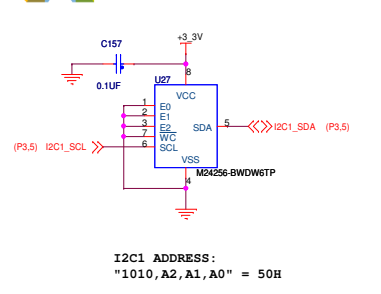
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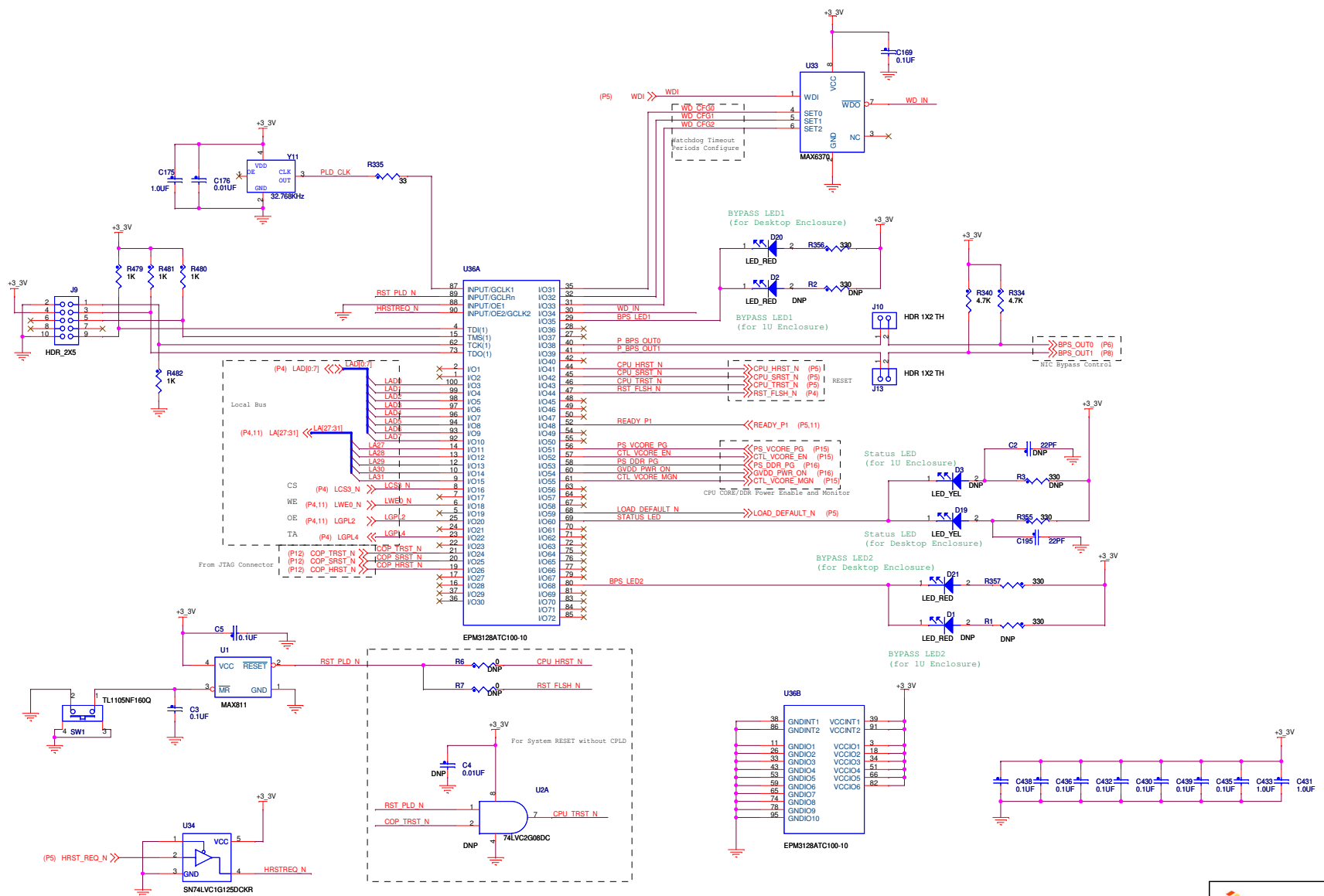
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POR Configuration Options







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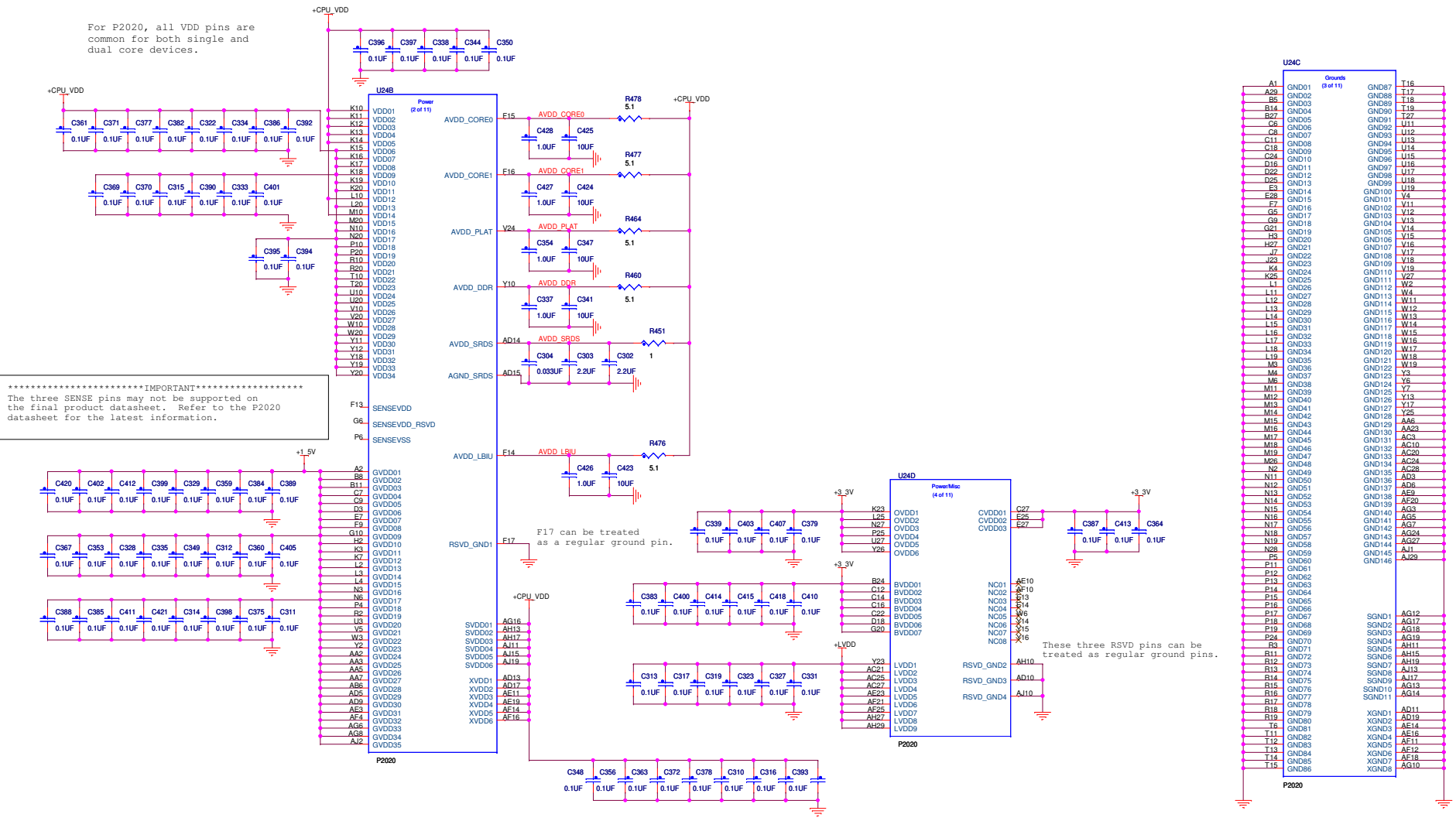
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For P2020, all VDD pins are common for both single and dual core devices.



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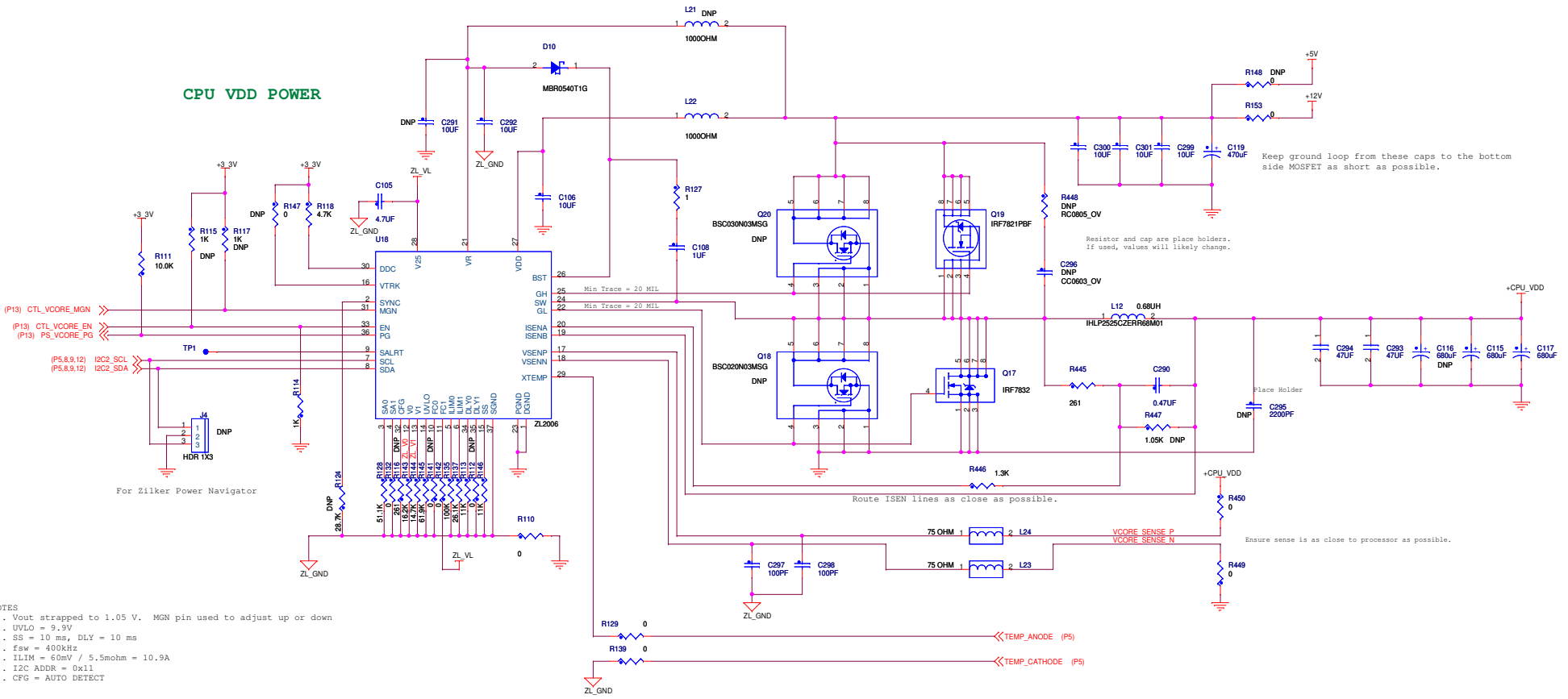
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CPU VDD POWER



- NOTES
- 1). Vout strapped to 1.05 V. MGN pin used to adjust up or down
 - 2). UVLO = 9.9V
 - 3). SS = 10 ms, DLY = 10 ms
 - 4). Fsw = 400kHz
 - 5). I LIM = 60mV / 5.5mohm = 10.9A
 - 6). I2C ADDR = 0x11
 - 7). CFG = AUTO DETECT

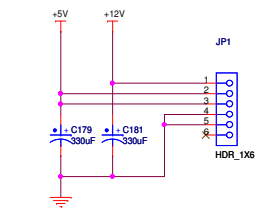
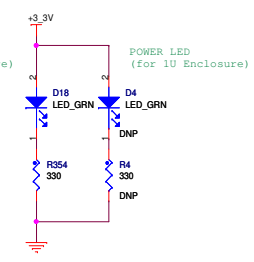
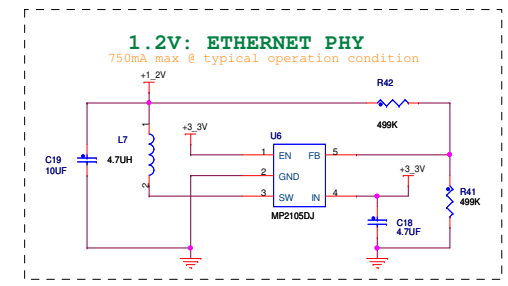
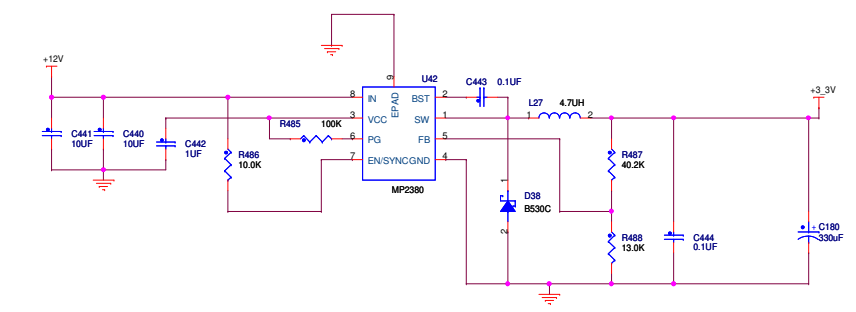
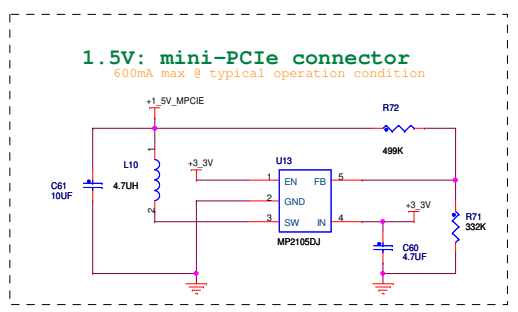
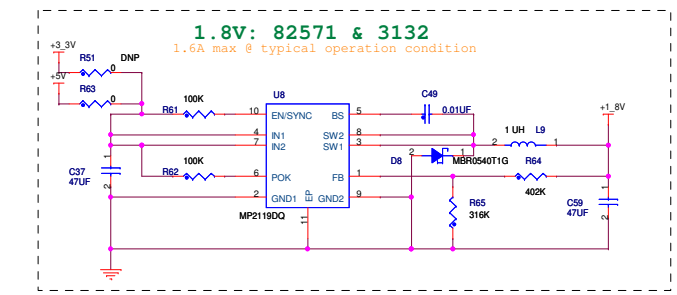
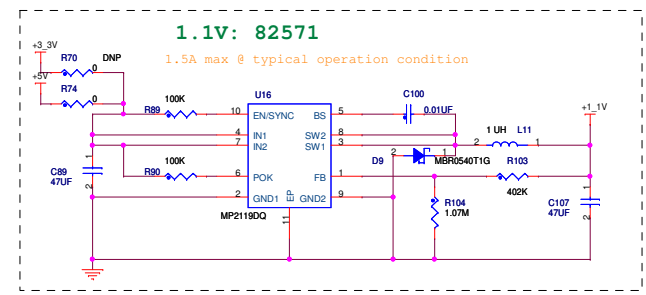
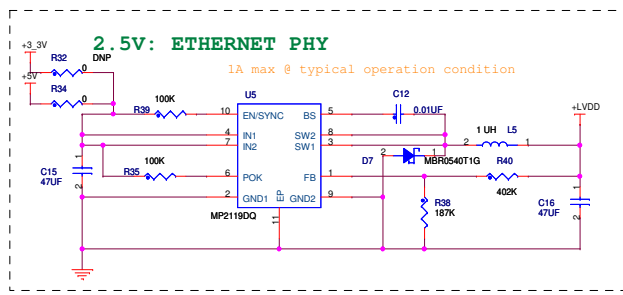
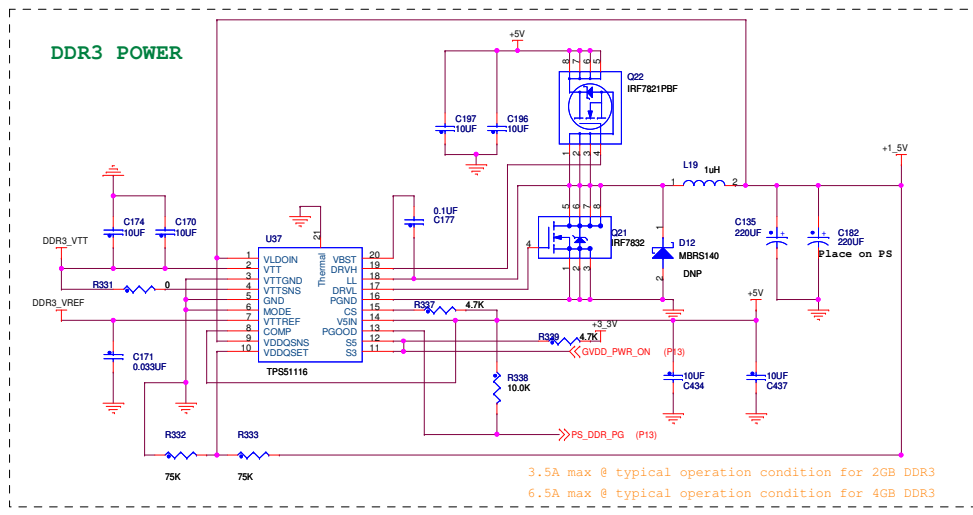
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Page Title: **POWER SUPPLY (CPU)**

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