Direct PFC Using the MC56F8013

Devices Supported:

MC56F80xx

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Chapter 1
Introduction

Chapter 2
Control Theory

Chapter 3
System Concept

Chapter 4
Hardware Implementation

Chapter 5
Software Implementation

Chapter 6
PFC Incorporation into Motor Control Applications

Chapter 7
Measured Results

Chapter 8
Application Setup

Appendix A
Schematic, Parts List, and Layouts

Appendix B
Glossary of Abbreviations

Chapter 1
Introduction

1.1 Introduction

This document describes the design of an average current mode control for power factor correction (PFC) on Freescale's MC56F8013 digital signal controller (DSC). Although the application is written for the MC56F8013, it can be ported into the other members of the DSC MC56F80xx family according to the application requirements. The presented implementation represents a fully digital solution. Fast current and slow voltage loops are implemented digitally using the DSC. This means that the voltage (outer) control loop is performed digitally by the DSC, and the PFC power switch is controlled directly by the DSC PWM output. Therefore, it is called direct PFC. The direct PFC algorithm works in an average current control continuous conduction mode (CCM).

The use of the direct control approach requires more DSC resources than the indirect solution, where the PWM is generated by external hardware circuitry. On the other hand, it is possible to generate a pure current sine wave drawn from the line and obtain the ideal ohmic load character at the input. Another advantage of this concept is a constant transistor switching frequency, which reduces noise. You can achieve better sytem dynamcis using direct PFC. Also, you do not need a synchronization signal from the line voltage and fewer passive components are needed compared to indirect PFC. The solution is cost-effective. The example of PFC implementation into a 3ph AC induction vector control drive with single shunt current sensing is desribed in Chapter 6, "PFC Incorporation into Motor Control Applications".

This control approach is suitable for medium and higher power applications. The DSC performance enables the concurrent operation of the PFC and motor control applications.

1.2 Freescale Controller Advantages and Features

The Freescale MC56F80xx family is well suited for control of switch mode power supplies (SMPS) and motor control, combining the DSP's calculation capability with the MCU's controller features on a single chip. These hybrid controllers offer many dedicated peripherals such as pulse width modulation (PWM) modules, analogue-to-digital converters (ADC), timers, communication peripherals (SCI, SPI, I^2C), and on-board flash and RAM.

The MC56F80xx family members provide the following peripheral blocks:

- One PWM module with PWM outputs, fault inputs, fault-tolerant design with dead time insertion, supporting center-aligned, and edge-aligned modes
- 12-bit ADC, supporting two simultaneous conversions; ADC and PWM modules can be synchronized
- One dedicated 16-bit general purpose quad timer module

- One serial peripheral interface (SPI)
- One serial communications interface (SCI) with LIN slave functionality
- One inter-integrated circuit (I^2C) port
- On-board 3.3 V to 2.5 V voltage regulator for powering internal logic and memories
- Integrated power-on reset and low-voltage interrupt module
- All pins multiplexed with general purpose input/output (GPIO) pins
- Computer operating properly (COP) watchdog timer
- External reset input pin for hardware reset
- JTAG/On-Chip Emulation (OnCE™) module for unobtrusive, processor-speed-independent debugging
- Phase-locked loop (PLL) based frequency synthesizer for the hybrid controller core clock, with on-chip relaxation oscillator

Table 1-1. Memory Configuration

Memory Type	MC56F8013
Program flash	16 Kbyte
Unified data/program ram	4 Kbyte

The SMPS and motor control benefit greatly from the flexible PWM module, fast ADC, and quad timer module.

The PWM offers flexibility in its configuration, enabling efficient three-phase motor control. The PWM module is capable of generating asymmetric PWM duty cycles in center-aligned configuration. The PWM reload SYNC signal can be generated to provide synchronization with other modules (Quadtimers, ADC).

The PWM block has the following features:

- Three complementary PWM signal pairs, six independent PWM signals (or a combination)
- Complementary channel operation features
- Independent top and bottom dead time insertion
- Separate top and bottom pulse width correction via current status inputs or software
- Separate top and bottom polarity control
- Edge-aligned or center-aligned PWM reference signals
- 15-bit resolution
- Half-cycle reload capability
- Integral reload rates from one to sixteen periods
- Mask/swap capability
- Individual, software-controlled PWM output
- Programmable fault protection
- Polarity control
- 10mA or 16mA current sink capability on PWM pins

- Write-protectable registers

The ADC module has the following features:

- 12-bit resolution
- Dual ADCs per module; three input channels per ADC
- Maximum ADC clock frequency of 5.33 MHz with a 187 ns period
- Sampling rate of up to 1.78 million samples per second
- Single conversion time of 8.5 ADC clock cycles (8.5 x 187 ns = 1.59 µs)
- Additional conversion time of six ADC clock cycles (6 x 187 ns = 1.125 µs)
- Eight conversions in 26.5 ADC clock cycles (26.5 x 187 ns = 4.97 µs) using parallel mode
- Ability to use the SYNC input signal to synchronize with the PWM (if the integration allows the PWM to trigger a timer channel connected to the SYNC input)
- Ability to sequentially scan and store up to eight measurements
- Ability to scan and store up to four measurements on each of two ADCs operating simultaneously and in parallel
- Ability to scan and store up to four measurements on each of two ADCs operating asynchronously to each other in parallel
- Interrupt generating capabilities at the end of a scan when an out-of-range limit is exceeded and on a zero crossing
- Optional sample correction by subtracting a pre-programmed offset value
- Signed or unsigned results
- Single-ended or differential inputs
- PWM outputs with hysteresis for three of the analogue inputs

The application uses the ADC block in simultaneous mode scan. It is synchronized to the Quadrature timer 3. This configuration allows the simultaneous conversion of the required analogue values for the input current, input voltage, and output voltage within the required time.

The Quadrature timer is an extremely flexible module, providing all required services relating to time events. It has the following features:

Four 16-bit counters/timers

Count up/down

Counters are cascadable

Programmable count modulus

Maximum count rate equal to the peripheral clock/2, when counting external events

Maximum count rate equal to the peripheral clock/1, when using internal clocks

Count once or repeatedly

Counters are preloadable

Counters can share available input pins

Each counter has a separate prescaler

Each counter has a capture and compare capability

The application uses two channels of the quad timer for:

- One channel for generating PWM
- One channel for synchronization PWM to ADC

Chapter 2
Control Theory

2.1 PFC Average Current Control Mode Theory

The control structure is divided into two loops: an inner current control and an outer voltage control loop as shown in Figure 2-1. The outer voltage control loop is implemented via software in the microcontroller and keeps a constant voltage on the DC bus. The voltage control loop utilizes a PI controller, and the output defines the amplitude required for the PFC current. The PFC control algorithm provides a sinusoidal input current without phase shift to the input voltage through dedicated PFC hardware controlled by the MCU.

The hardware incorporates an input bridge rectifier DB, PFC inductance L, PFC diode D, and PFC switch Q. These analogue quantities are sensed – rectified input voltage, input current, and DC-bus voltage. The input current is controlled using the PFC switch to achieve the desired input current and the desired level of the DC-bus voltage (U_{REQ}).

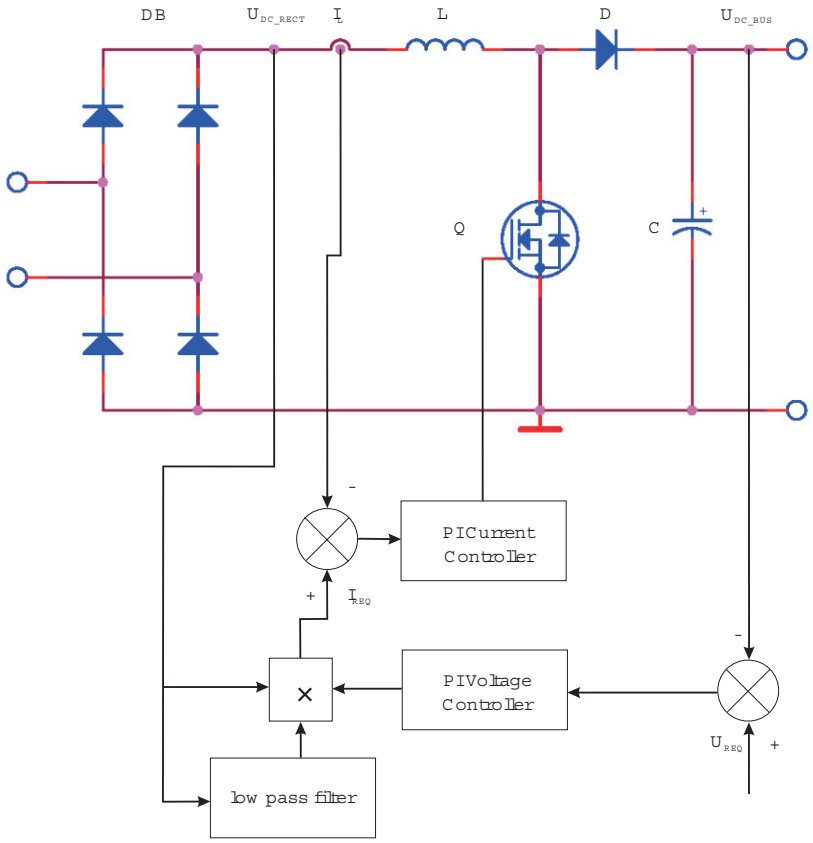

Figure 2-1. Average Mode Control Block Diagram

The inner current loop is implemented via software as with the outer loop, and employs the PI controller to maintain the sinusoidal input current by directly controlling the PFC transistor. The input to the PI controller is the difference between the current reference, $I_{REQ,}$ and the actual current, I_L. The sinusoidal waveform of I_{REQ} is derived from the shape of the input voltage $U_{DC\ RECT}$, as shown in Figure 2-1. The final current reference, I_{REQ}, is acquired by multiplying a rectified input voltage waveform by the output of the voltage controller. The current PI controller's output generates a signal, D, corresponding to the duty cycle of a boost converter in an open loop, expressed as

Eqn. 2-1

$$D = \frac{V_{DCBUS} - V_{DCRECT}}{V_{DCBUS}}$$

where:

$V_{DC\ BUS}$ = DC bus voltage
$V_{DC\ RECT}$ = rectified input voltage
D = duty cycle of PFC transistor

The resultant signal, D, defines the duty cycle of the PFC transistor. The bandwidth of the current PI controller has to be set above 8 kHz to get a sufficient response. Therefore, the current PI controller algorithm has to be executed at least once every 60 µs, which puts a lower-limit requirement on the performance of the DSC. The DSC performance requirement for the voltage control loop is low. The bandwidth of the voltage control loop is set below 20 Hz. Therefore, the DSC performance is not a limiting factor in this part of the PFC algorithm.

Chapter 3
System Concept

3.1 System Specification

The dedicated PFC hardware is designed as part of the whole system. The PFC board together with the power stage and controller board form one compact system to drive a three-phase AC/BLDC motors, including PFC control. This chapter describes the PFC part. PFC incorporation into a single shunt vector control is described in Chapter 6, “PFC Incorporation into Motor Control Applications”.

The application meets the following performance specifications:

- Hardware used:
  - MC56F8013/23 controller board
  - PFC board
  - 3ph AC/BLDC high voltage power stage board
- Control technique incorporating:
  - Inner current loop
  - Outer voltage loop
  - Current reference generation
  - RMS input voltage calculation
- FreeMASTER software monitor
  - FreeMASTER software graphical control page (required output voltage, actual output voltage, actual input current, actual input voltage control and system status)
  - FreeMASTER software voltage scope (observes input voltage, output voltage, input current, duty cycle, and RMS input voltage)
  - FreeMASTER software current recorder (observes actual and desired current, duty cycle)
  - FreeMASTER software start-up recorder (required and actual output voltage)
- Fault protection:
  - DC-bus over-voltage and under-voltage
  - Over-current protection
  - Input voltage over-voltage and under-voltage

3.2 PFC Characteristics

Table 3-1 provides the basic characteristic of the stand-alone PFC at 25°C and a 385V DC-bus voltage.

Table 3-1. PFC Characteristics

Parameter	Value	Unit
Input AC Voltage at 50Hz	230	V
Input AC Current	5	A
DC bus Voltage	385	V
Output Power	750	W
Power Factor at max. Load	0.99	-
THD	4.46	%

3.3 Application Description

A system concept can be seen in Figure 3-1. The system incorporates the following hardware boards:

- PFC board
- 3ph AC/BLDC high voltage power stage board
- MC56F8013/23 controller board

The MC56F8013/23 controller board executes the control algorithm. According to feedback signals, it generates a PWM signal for the PFC MOSFET transistor switching.

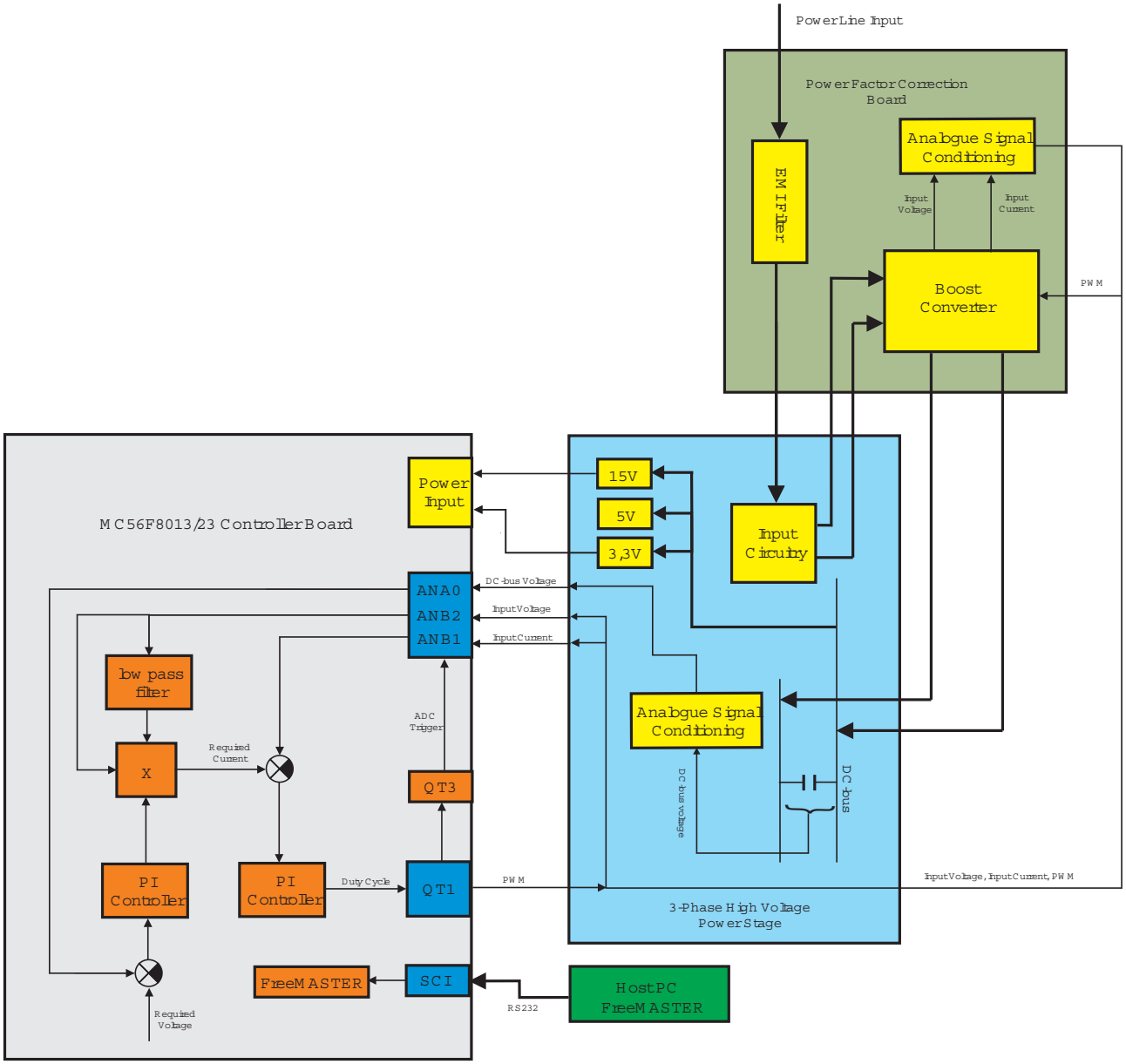

Figure 3-1. System Concept

3.4 Power Factor Correction

The power factor correction application provides the sinusoidal input current by controlling the PFC switch. In the control loop, the actual DC-bus voltage is compared with the desired one. The control error is processed by the PI (proportional-integral) controller, which generates the amplitude of the reference current. Input rectified voltage is multiplied by the input rectified RMS voltage and by the output of the voltage controller. This multiplied value is the reference current. This reference current is compared to the actual one sensed on the shunt resistor. The difference between them is then processed in the PI current controller. The output from this controller is the PWM signal for quad timer 1, which directly switches the PFC transistor.

3.5 Software Specification

The software is written in C. The software specifications are listed in Table 3-2. A useful feature of this application is the ability to debug software via the JTAG interface. The real-time debugging can be performed in Metrowerks as well.

Table 3-2. Software Specification

Control Algorithm	Average current control
	Inner current loop
	Outer voltage loop
Target Processor	MC56F80xx
Language	C with some code written in assembler
Compiler	Metrowerks ANSI-C/C++ Compiler DSP for 56800 r. 7.0

3.6 Hardware Specification

The board and its interconnections are mentioned in Chapter 8, “Application Setup”.

The hardware operates on 230 V AC power. For other desired application parameters, the EMI filter, PFC inductance, PFC switch, shunt resistor, and driver circuitry components should be changed. Other components and the board layout remain the same.

3.7 Application Monitoring

The dedicated Freescale software tool FreeMASTER is used for real-time debugging and for demonstration of the application. The state of the application is scanned periodically and all variables are represented in FreeMASTER.

There are four main pages that simplify application tuning. The input current, input voltage, and DC-bus voltage are sampled with the ADC. The ADC sampling is triggered by QuadTimer channel 2 and synchronized to the PWM signal generated by Quad Timer 1.

Based on feedback signals, the PFC algorithm is performed as described in Section 2.1, “PFC Average Current Control Mode Theory”. Two independent control loops are executed to achieve the desired behaviour.

The PWM signal is disabled and the fault state is displayed in the case of over-voltage, under-voltage, or over-current.

Chapter 4
Hardware Implementation

4.1 Introduction

This chapter describes the design of the application hardware. As mentioned, the hardware incorporates three parts:

- MC56F8013/23 controller board
- PFC board
- 3ph AC/BLDC high voltage power stage board

Although the power stage is mainly dedicated to motor control, it contains important components for PFC as well. Unfortunately, not all the necessary PFC components are present there, so a dedicated PFC board needs to be connected.

This chapter focuses on the unique PFC board used for this application design, because the MC56F8013/23 controller board and 3ph AC/BLDC high voltage power stage board are described in detail in the dedicated user's manuals.

The block diagram is described in Figure 3-1.

4.2 PFC board overview

As described in Chapter 2, "Control Theory," the PFC hardware incorporates an EMI filter, input rectifier, PFC inductance, PFC switch, and PFC diode. Their designs are described in this chapter. The design of the other components, such as the DC-bus capacitors, input capacitor C1, fuse, varistor, thermistor, current sensing circuitry, diode D2, input voltage sensing circuitry, and output voltage sensing circuitry is not mentioned here because they are part of the 3ph AC/BLD C high voltage power stage board, rather than the PFC itself.

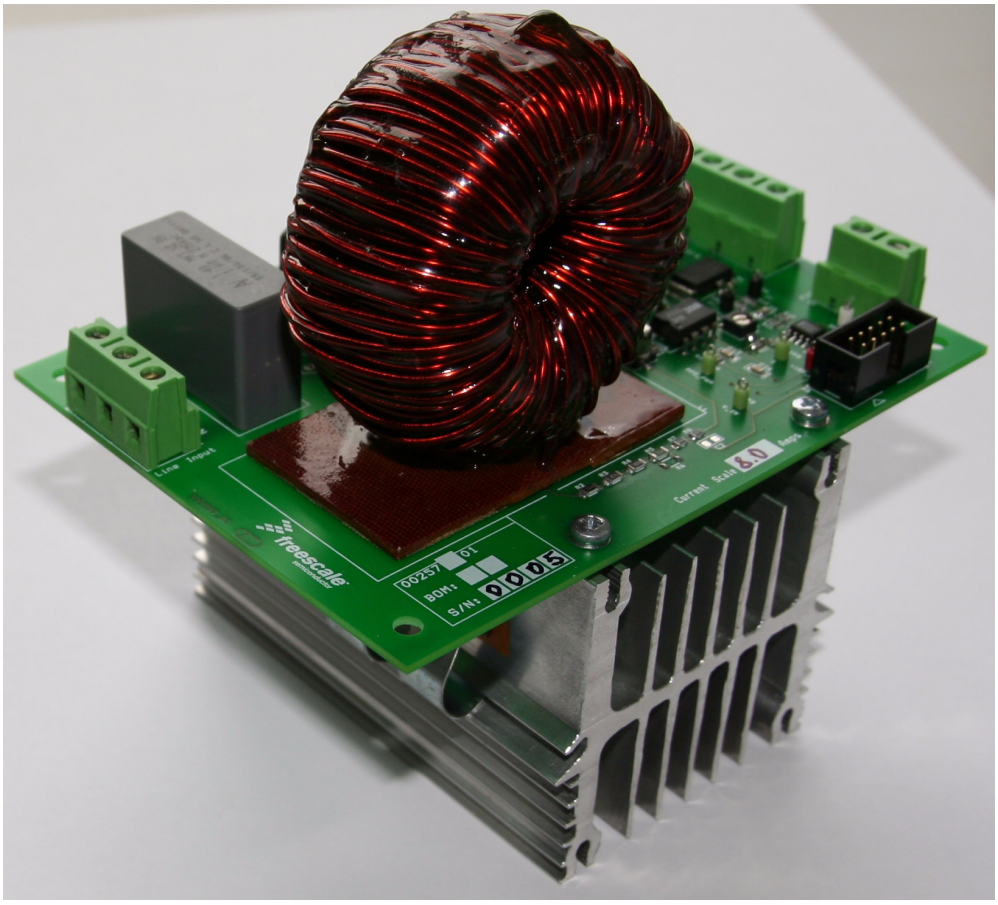

Figure 4-1. PFC Board

4.3 System components

The PFC hardware is shown in the block diagram in Figure 3-1. It incorporates the PFC board, controller board, and power stage board. The PFC board contains three major parts:

- EMI filter
- boost converter
- MOSFET driver

A detailed design description of the individual parts follows. The reference design includes the PCB design files and bill of materials (BOM).

4.3.1 PFC board

4.3.1.1 Design of the PFC Inductance

For design of the PFC inductance dedicated software, “Inductor Design Software 2005” from Micrometals, Inc. was used and the proposed core samples were ordered. Output parameters from this software were used for inductor manufacturing. A suitable core, T200-30B, was selected. Using the

Micrometals software, you need to fill-in input parameters for the inductor calculation. One of these parameters is the inductance, which can be calculated using the formula below.

$$L = \frac{\sqrt{2} \cdot V_{IN} \cdot D}{f_s \cdot \Delta i} \quad \textit{Eqn. 4-1}$$

V_{IN} - input voltage rms value

D - duty cycle, see equation below

f_s - switching frequency

Δi - current ripple is 20% of the current peak

$$\Delta i = 0.2 \cdot \frac{\sqrt{2} \cdot P_{IN}}{V_{IN}} \quad \textit{Eqn. 4-2}$$

P_{in} - input power

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad \textit{Eqn. 4-3}$$

V_{out} - output voltage

All the parameters are filled-in according to the required design parameters. For our particular design, $R_{dc,max} = 1\Omega$, $I_{max} = 5.1A$, $V_{in} = 230V$, $V_{out} = 385V$, frequency = 32kHz.

4.3.1.2 Design of the PFC switch and its driver

For design of the power MOSFET, the method for calculating an equivalent flat-topped current was selected. Output power is 750 W and nominal AC line voltage is 230 V. With a minimum rectified DC voltage of 272 V, peak flat-topped current, I_{pft} , is calculated using the following formula.

$$I_{pft} = \frac{D_{MAX}}{\eta} \cdot \frac{P_{OUT}}{V_{MIN(RECT)}} \quad \textit{Eqn. 4-4}$$

where:

P_{OUT} - output power

$V_{MIN(RECT)}$ - minimum rectified DC voltage

D_{MAX} - maximum duty cycle

η - converter efficiency

The MOSFET-ON voltage should be 2 percent of the minimum supply voltage:

$$V_{ON} = 0.02 \cdot V_{MIN(RECT)} = I_{pft} \cdot r_{ds(on)100} \quad \textit{Eqn. 4-5}$$

The $r_{ds(on)100}$ value at 100°C is 1.6 times its value at 25°C.

$$r_{ds(on)25} = \frac{r_{ds(on)100}}{1.6} \quad \textit{Eqn. 4-6}$$

The power MOSFET transistor should meet this requirement. Although switching frequency is 32 kHz, the MOSFET from Infineon was selected because it has a low $r_{ds(on)}$ value. Therefore, conduction losses are lower and the whole PFC efficiency higher. For selection of the power switch, the avalanche save

operation area characteristic should be evaluated as well. Finally, according to these requirements, the SPP20N60S5 was selected.

The MOSFET transistor is driven using driver IR2121. This driver has current detection and a limiting loop to limit the driven transistor current. The protection circuitry detects over-current in the driven transistor and limits the gate drive voltage. Cycle-by-cycle shutdown is programmed by an external capacitor, which directly controls the time interval between detection of the over-current limiting condition and the latched shutdown.

4.3.1.3 Design of the PFC diode

The diode selection is based on reverse voltage, forward current, and the switching speed. The diode selection in this design is critical. A diode with a fast recovery characteristic is important. The HFA08TB60S was selected as the most suitable with a reverse recovery time of 18 ns, a continuous forward current of 8 A and a reverse voltage of 600 V.

4.3.1.4 Design of the EMI filter

There are many suitable EMI filters available from many companies, but selecting a proper filter is important for system performance. Because the theory is quite in-depth, this document does not go into detail of the EMI filter design. You can find some theory and practical designs of EMI filters in various documentations. In this design, a discrete EMI filter has been calculated. It consists of one choke and four capacitors (see Figure 4-2). You can calculate the EMI filter, but the real behaviour of the entire system can behave differently, mainly at higher frequencies.Therefore, you should measure these parameters in a real application and then modify the components to achieve a better performance on EMI interference.

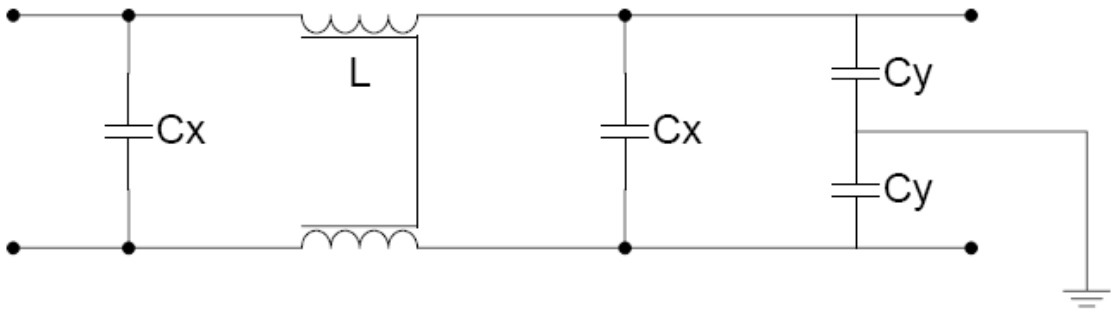

Figure 4-2. EMI filter

The first step is to measure common-mode and differential-mode noise without a filter. Then, determine the common-mode and differential-mode attenuation requirements from the measured noise and the conducted EMI limits specified by the CISPR international standard, or by those standards that you have to meet. Next, determine the filter corner frequencies, $f_{r,cm}$ and $f_{r,cm}$, for the common-mode and differential-mode filters. Common-mode components are L_{cm} and C_y. C_y is selected first and should have a value between 2.2 nF and 33 nF, then L_{cm} is calculated. For calculating common-mode inductance, L_{cm} ,the equation below should be used.

$$L_{Cm} = \left(\frac{1}{2\pi \cdot f_{r,cm}}\right)^2 \cdot \frac{1}{2 \cdot C_y} \qquad \textit{Eqn. 4-7}$$

As a differential-mode inductance, L_{dm}, the leakage inductance of common-mode inductance was utilized. According to C_{x1} and C_{x2} values, use the equation below.

$$C_{x1} = C_{x2} = \left(\frac{1}{2\pi \cdot f_{r,\,dm}}\right)^2 \cdot \frac{1}{L_{dm}} \qquad \textit{Eqn. 4-8}$$

After the parameters of all the components are known, the EMI filter can be tested and noises measured to see if the limits meet the standards. At high frequencies, it is hard to predict filter behaviour, so testing is an important part of verification. If the EMI filter does not meet the limits, modifications should be made or the PCB rearranged.

Chapter 5
Software Implementation

5.1 General

The whole application is controlled by the DSC MC56F8013. This low-cost digital signal controller offers many important features and peripherals to this kind of application. The quad timer and ADC are the most important peripherals used in this application. The ADC is used for sensing analogue quantities and the quad timer for timing the control algorithm, ADC sampling synchronization and control signal generation.

The entire PFC algorithm is implemented in one interrupt routine generated from the quadrature timer (QT1) (31.25 µs). This routine is called every 31.25 µs, corresponding to 32 kHz. Such a frequency is high enough to generate the proper current shape and doesn't load the DSC core more than necessary. The current loop is executed on every interrupt, as shown in Figure 5-2. The current controller utilizes a recursive algorithm for fast execution time.

Quad timer, channel 2, is used as a synchronization signal between A/D converter B and the PWM signal generated by QT1. The A/D converter B synchronization signal (scan start) is executed at the midpoint of the on-time PWM signal to measure an average inductor current. The ADC reads the input current and input voltage in one sequence using A/D converter B, and in another sequence, converts the output voltage using A/D converter A.

An overview of all sensed quantities can be seen in Table 5-1. Input current is sensed every QT1 interrupt, 31.25µs, and input voltage and output voltage is sensed every fourth QT1 interrupt, 125 µs. All quantities are sensed at the midpoint of the duty cycle (see Figure 5-1).

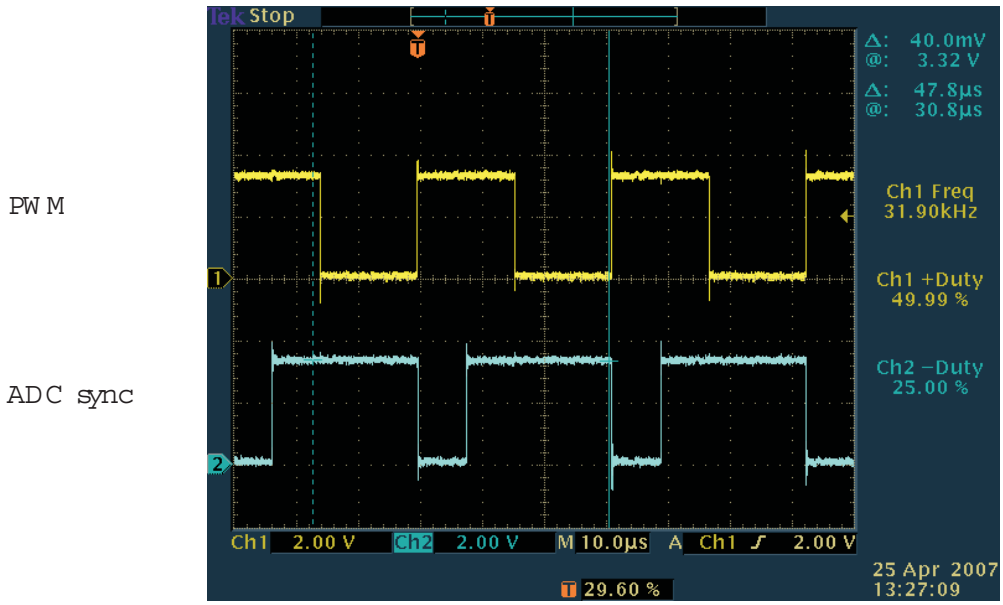

Figure 5-1. ADC synchronization

RMS input voltage is gained by filtering the input voltage by a 10 Hz low-pass filter.

The switching frequency of the PFC transistor is set to 32 kHz. This constant switching frequency of the PFC transistor simplifies the design of the input filter. The result of the current controller defines the duty cycle of the PFC transistor.

Table 5-1. Overview of Sensed Quantities

Quantity	Type of Conversion	Conversion Period
V_{OUT}	slow	125 µs
I_{IN}	fast	31.25µs
V_{IN}	slow	125 µs

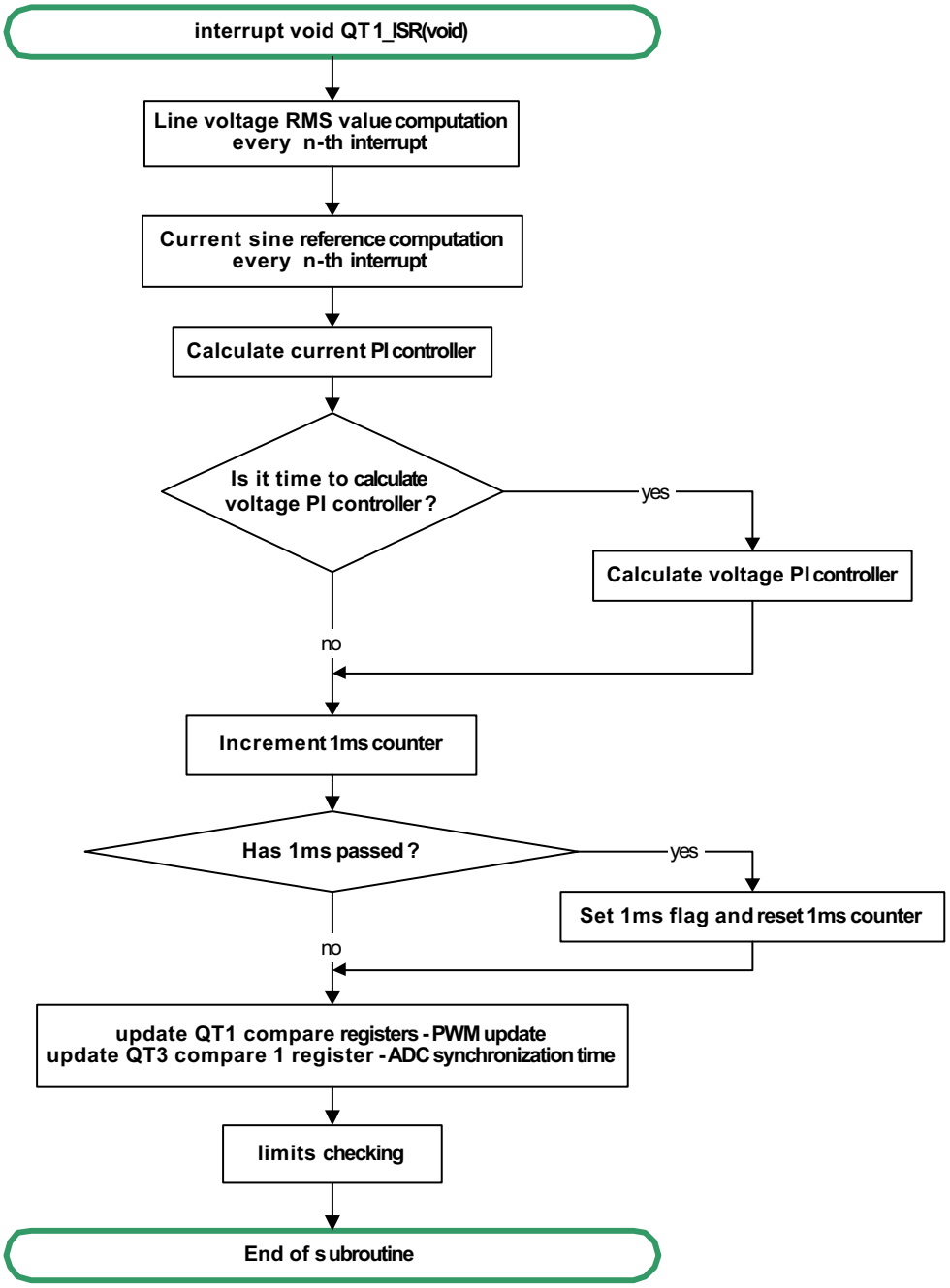

Figure 5-2. QT1 Interrupt Service Routine

5.2 MCU Loading and PFC Routine Execution Times

The execution times of the PFC routine were measured by oscilloscope. The results can be seen in Figure 5-3. The total estimated MCU load is 61%. The execution times of each routine can be seen in Table 5-2, and the code sizes in Table 5-3.

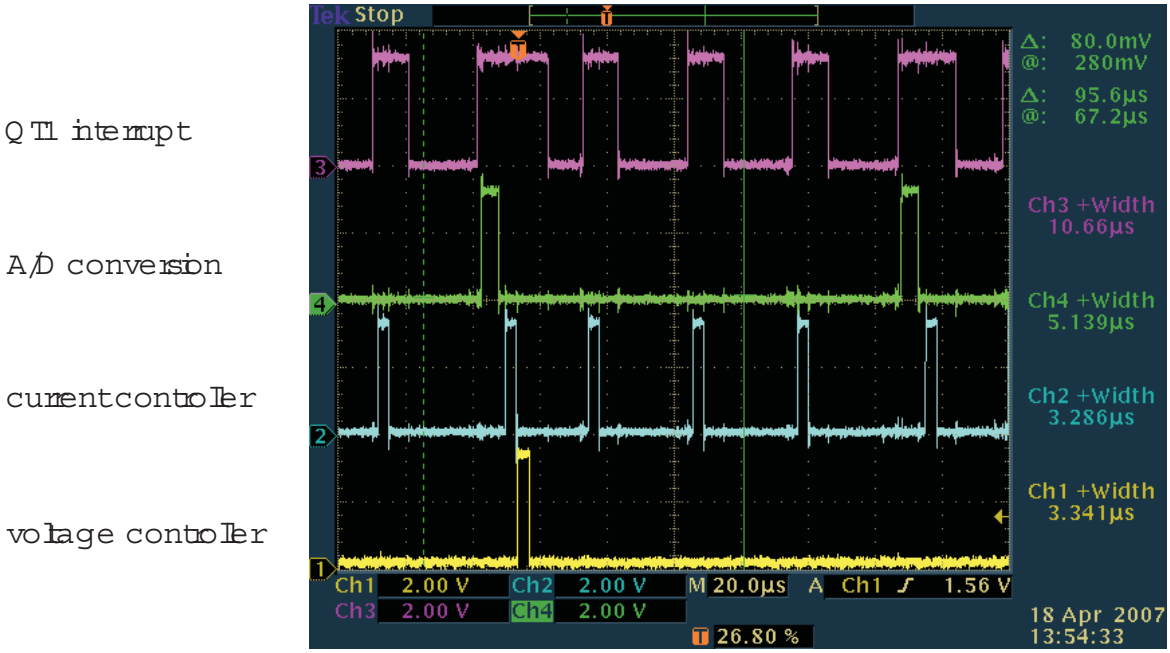

Figure 5-3. CPU Load

Table 5-2. Execution Time of Periodic Interrupts

Name	Execution Period	Execution Time
QT1 Interrupt	31.25 µs	19.1 µs
A/D conversion time	31.25 µs	2.7 µs
Current controller	31.25 µs	3.3 µs
Voltage controller	53 ms	3.3 µs

Table 5-3. Size of Application Code in PFC section

Memory Type	Size in Bytes	Available on MC56F8013
Flash	6248	16kB
RAM	62	4kB
Stack	256	

Chapter 6
PFC Incorporation into Motor Control Applications

6.1 General

PFC can be incorporated as a part of every system supplied from AC power. This chapter describes the implementation of PFC into a 3ph AC induction vector control drive with single shunt current sensing.

System concept can be seen in Figure 6-2.

In this chapter, the motor control application described uses an AC induction motor with a tachogenerator. If you would like to use a motor with an encoder sensor, the MC56F8013 does not have enough timer channels for encoder processing. You would need to use a device with more timers, such as the MC56F8037. Porting of the presented MC56F8013 software to the MC56F8037 is straightforward.

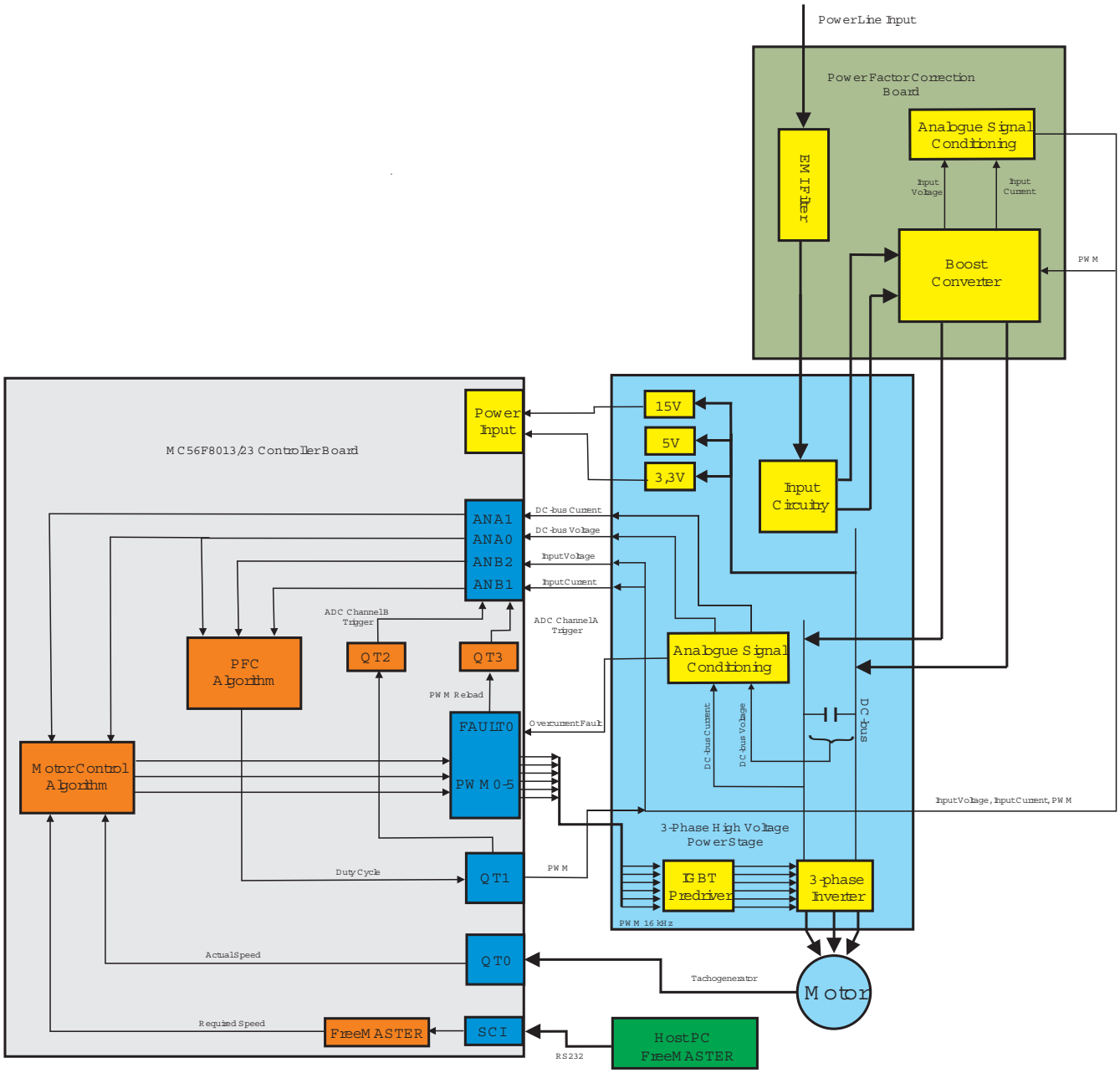

Figure 6-1. System Concept

The system consists of three boards: power factor correction board, 3ph AC/BLDC high voltage power stage board and the MC56F8013/23 controller board. Hardware and software implementations are described in the following sections.

6.2 Hardware Overview

There is no need for any additional hardware to implement control of the ACIM. Configuration is the same as for standalone PFC purposes. A suitable motor must be connected.

6.3 Software Overview

The application software is interrupt driven running in real time. There are three periodic interrupt service routines executing the major motor control and PFC tasks (see Figure 6-2).

- The Timer 3 interrupt service routine performs a fast current control loop and PFC tasks. It is executed when a third DC-bus current sample is read, with a 125µs period.
- The PWM reload interrupt service routine performs a fast current control loop and PFC tasks. It is executed every PWM half-reload, with a 31.25µs period.
- The ADC Channel A End of Scan interrupt service routine reads the DC-bus current samples. It is executed for three consecutive sample readings within one PWM cycle.

There is also the non-periodical interrupt service routine.

The PWM fault interrupt service routine is executed on an over-current event to manage an over-current fault condition. It is executed only if the fault condition occurs.

The background loop is executed in the application power line. It manages non-critical time tasks, such as the application state machine and FreeMASTER communication polling.

The PWM module is configured to run in center-aligned mode with counter modulo CMOD equaling 800, corresponding to a switching frequency of 16 kHz on a 32 MHz bus clock (PWM cycle period = 62.5 µs). The PWM_half_reload_sync signal is generated every PWM half-cycle with a 31.25 µs period. The PWM_half_reload_sync is connected to the secondary input pin#3, a signal to the TMR module. An output from TMR channel 3 is connected to the SYNC0 signal, which is used to trigger the ADC Channel A. TMR channel 3 is configured in triggered count mode. A connection link between the PWM module, TMR module, and the ADC module enables defining the exact multiple time instants of ADC sampling, which are synchronized to the generated PWM signal.

ADC channel A is started for the third time after 31.25 µs and the third DC-bus current sample is read. Simultaneously, the Timer 3 interrupt is executed. After the third current sample has been read, the Timer 3 ISR is interrupted and the ADC Channel A End of Scan ISR is executed. When this ISR has finished, the Timer 3 ISR continues processing.

The fast current control loop is executed in the PWM reload ISR, which is synchronized to the PWM_half_reload_sync signal. Prior to the PWM reload ISR being executed, three ADC samples of the DC-bus current are taken and processed by the ADC Channel A End of Scan ISR.

The timing diagram in Figure 6-2 shows how a triple triggered ADC conversion is performed. The events are executed in the following steps:

1. A PWM counter reaches zero. A PWM half-reload occurs. Values stored in the PWM value registers (VAL0-5) are applied to the PWM outputs. The PWM reload flag (PWMF) is set to one and pending. The PWM half-reload interrupt is disabled at the beginning of every PWM reload cycle. A signal to PWM_half_reload_sync is generated by the PWM module.
2. The TMR channel 3 count is triggered by the PWM_half_reload_sync signal, which is connected to its secondary source input. The timer starts counting up from zero.
3. A compare on Compare 1 register (COMP1) occurs. An output (OFLAG) of TMR ch. 3 is set to one. The value from the Comparator Load 1 register (CMPLD1) is loaded into the COMP1 register.

4. A rising edge on the SYNC0 input of the ADC module starts an ADC conversion.
5. The ADC conversion finishes. The ADC End of Scan 1 flag (EOSI1) is set.
6. The ADC end-of-scan ISR is entered. The interrupt is processed as a fast interrupt with a priority level 2. The value from the Result 0 (RSLT0) register is stored in a buffer. A new value stored in a timing table is loaded into the CMPLD1 register of TMR ch. 3. An output (OFLAG) of TMR ch. 3 is forced to zero. The EOSI1 flag is cleared.
7. A second compare on Compare 1 (COMP1) occurs. Steps three to six are repeated. The Timer 3 interrupt is enabled.
8. A third compare on Compare 1 (COMP1) occurs. Timer 3 Interrupt routine is executed and ADC channel A starts a conversion. The resultant value is read by the ADC End of Scan ISR that interrupts the Timer 3 ISR because of a higher priority. Before the ADC EOS ISR exits, the ADC EOS Interrupt is disabled. The Timer 3 ISR then performs part of the routines for the fast current control loop. PWM_half_reload is enabled.
9. A PWM half reload is executed every 31.25 µs. The two ISRs (ADC EOS, Timer 3) perform the remainder of the current control algorithm and the PFC. When finished, the new values are stored in the PWM value registers (VAL0-5). The TMR ch. 3 registers COMP1 and CMPLD1 are loaded with these new values and the counter is reset.
10. Execute the PFC algorithm.

When a new PWM Reload event occurs, the sequence restarts at the first step.

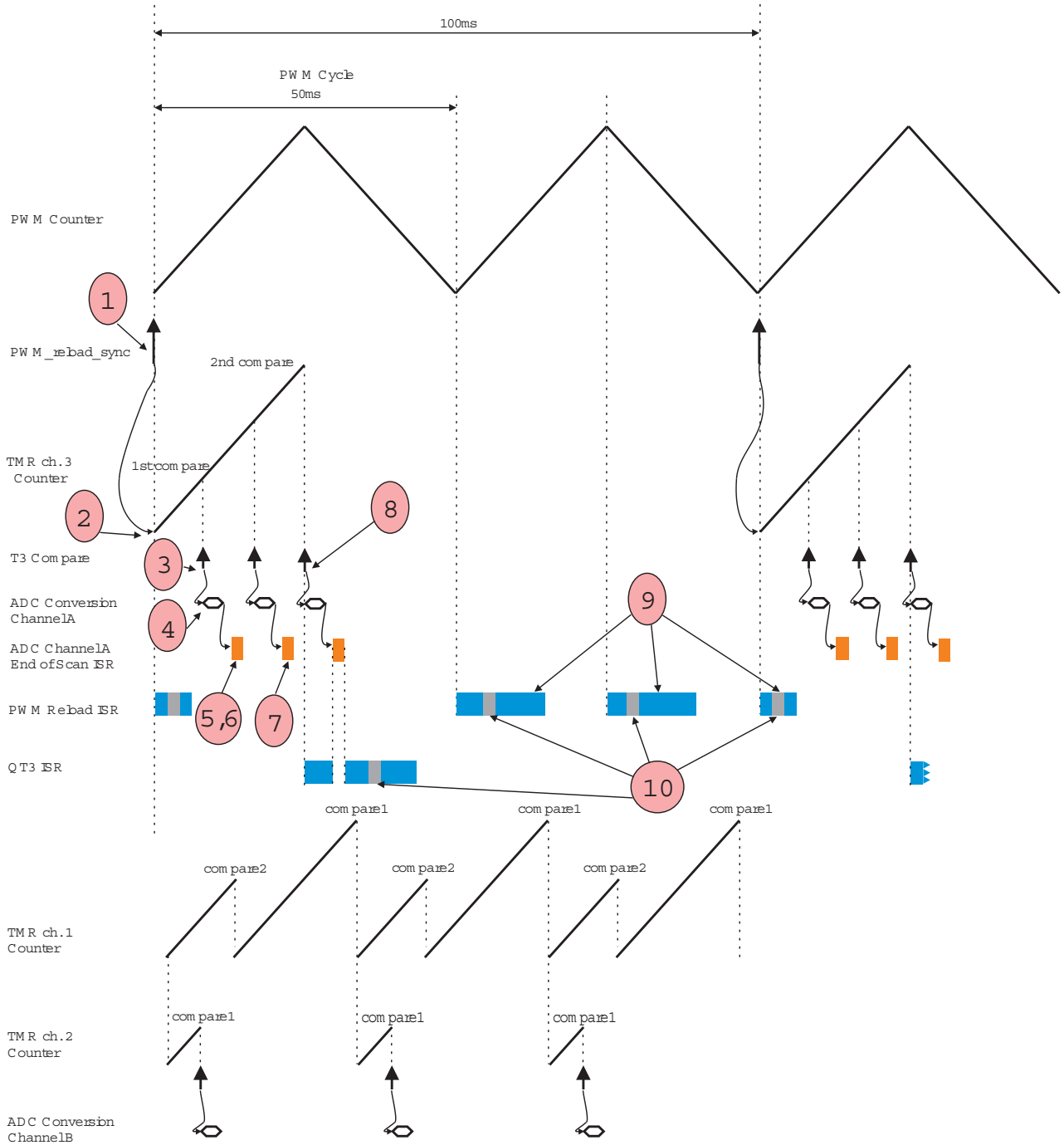

Figure 6-2. Application Interrupts and Timing

6.4 Freescale Semiconductor Support

The software listing for the integrated PFC/ACIM single shunt vector control application is not part of this reference design. However, the application source code can be provided under specific business conditions. For more information, contact your Freescale representative.

Chapter 7
Measured Results

7.1 General

The average current mode control of the power factor correction has been tested in the 3ph AC induction vector control drive with single shunt current sensing reference design described in Chapter 6, “PFC Incorporation into Motor Control Applications”. The results can be seen in Figure 7-1 and Figure 7-2. Figure 7-1 shows the input current and voltage at full load. Figure 7-2 details current harmonics that were measured at full-load. From this figure, it can be seen that the application meets IEC 61000-3-2 on full load. Total harmonic distortion is 4.46% and the power factor is 0.99.

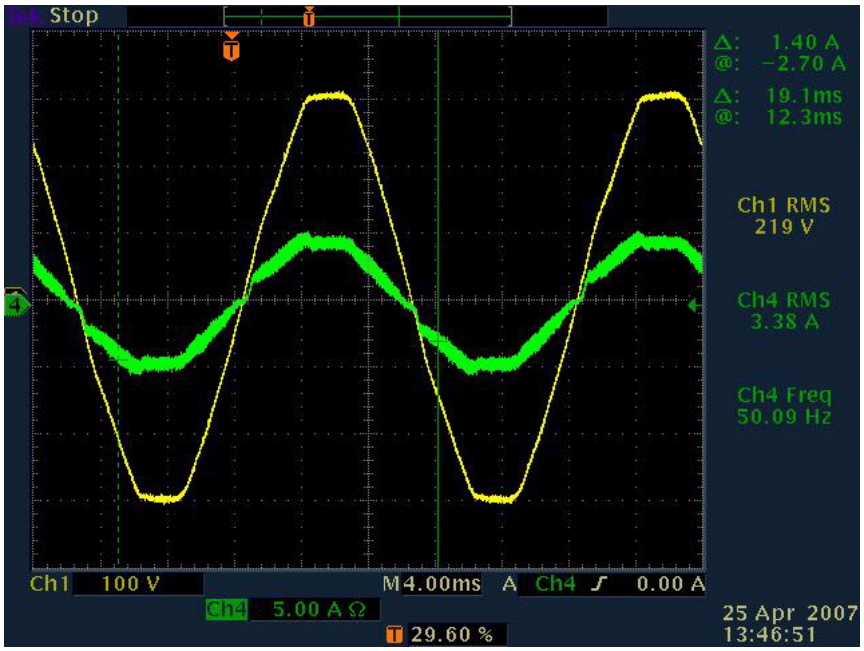

Figure 7-1. Input Current and Voltage at maximum load

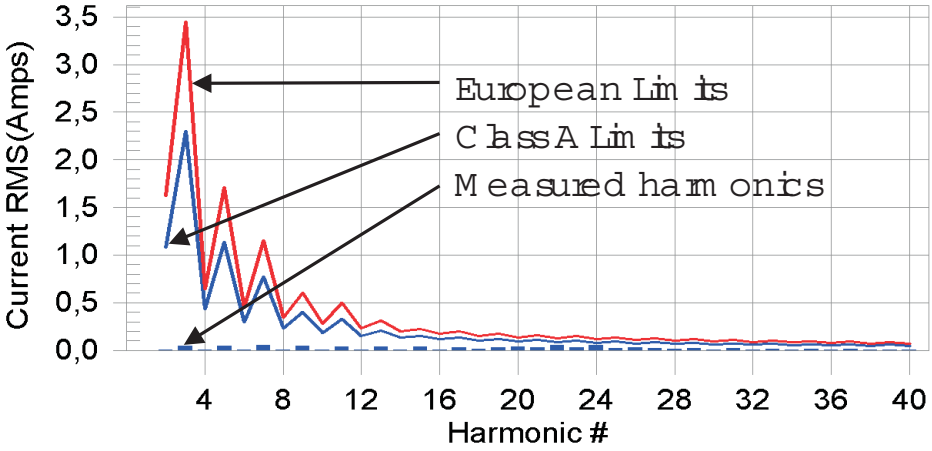

Figure 7-2. Measured harmonics

Chapter 8
Application Setup

8.1 General

As described earlier, the motor control applications are targeted at the MC56F8013 device. The concept of the motor control drive incorporates the following hardware components:

- MC56F8013/23 controller board
- PFC board
- 3ph AC/BLDC high voltage power stage board
- AC induction motor

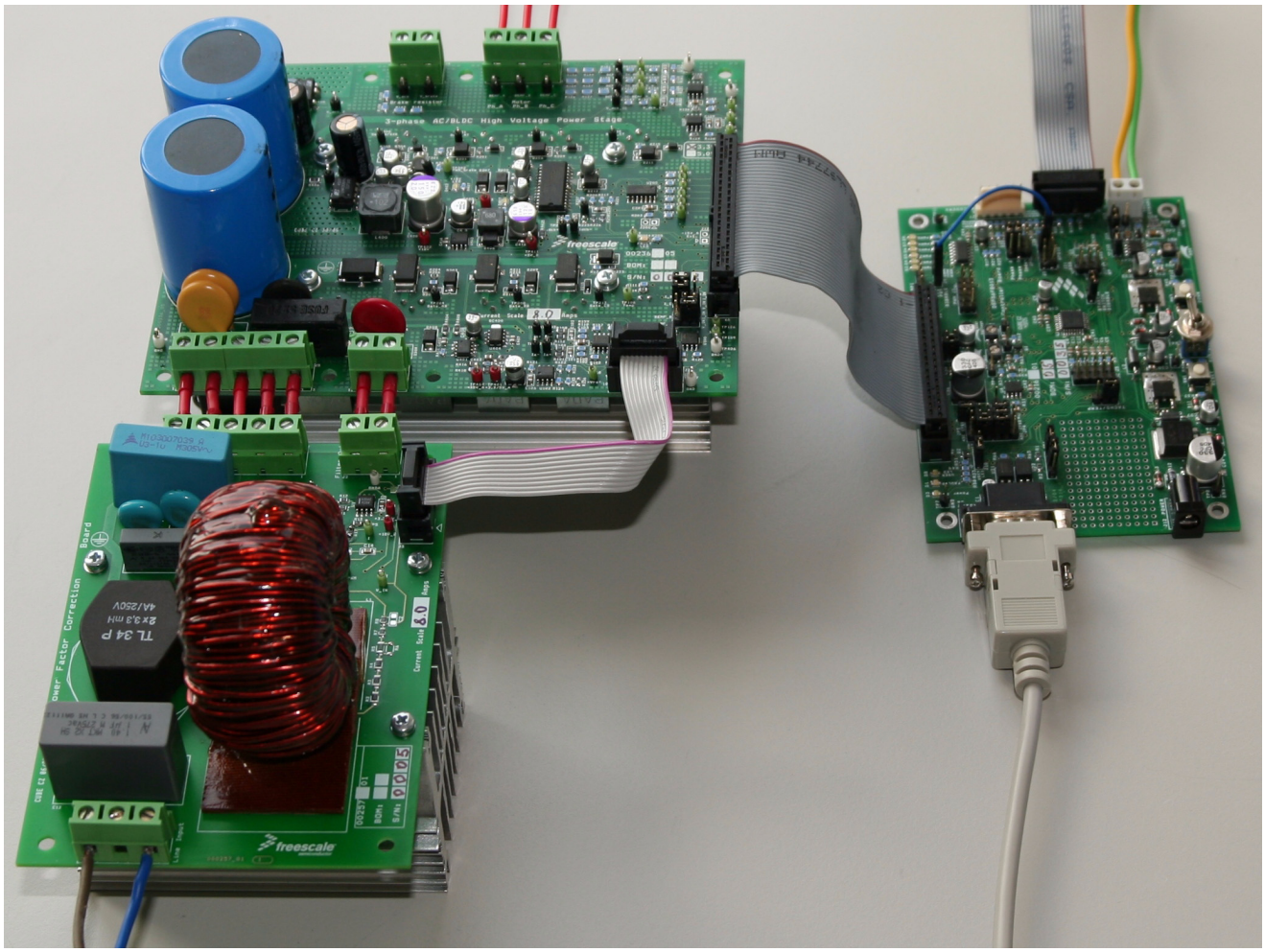

Figure 8-1. Demo Application Setup

8.2 MC56F8013 Controller Board Setup

Prior to the MC56F8013/23 controller board being connected to the power-stage, it needs to be configured for correct operation. Also, the demo application code has to be programmed into the flash memory first. For the MC56F8013/23 controller board configuration, follow these steps:

1. Set the jumper configurations on the MC56F8013/23 Controller Board as shown in the table:

Table 8-1. MC56F8013/23 Controller Board Jumper Setting[1]

Jumper	Setting	Description
JP1	2-3	SCI Bi-Wire Configuration
JP4	1-2, 4-5, 7-8	ADC CFG2 Configuration (motor phase-current sensing)
JP5	5-6, 8-9	ADC CFG1 Configuration (motor phase-current sensing)
J16	1-2	+5V Power Supply from UNI-3 connector
J18	1-2	+15V Power Supply from UNI-3 connector

[1] Other Jumpers are set to OPEN

2. Interconnect pin 6 from the J2 pinhead with pin 1 of the J9 pinhead, because Quad Timer 1 is used for PWM generation.
3. Connect a tachogenerator to the connector J13.
4. Connect a +12V power supply to the J12 power connector on the MC56F8013/23 Controller Board.
5. Set the Over-Voltage Thresholds.
6. Trimpot R29 sets the over-voltage threshold. Use a voltmeter to measure the threshold level at test-point TP3. Turn the R29 trimpot to set the threshold level. The voltage level on TP3 should be >3.2V.
7. Connect the parallel JTAG Command Converter or the USB-TAP to the host PC and to the J4 header on the MC56F8013/23 Controller board.
8. Compile your project and program it into the device.
9. Disconnect the +12V power supply from the J12 power connector on the MC56F8013/23 Controller Board.
10. Unplug the JTAG Command Converter or the USB-TAP from the J4 header on the MC56F8013/23 Controller board.

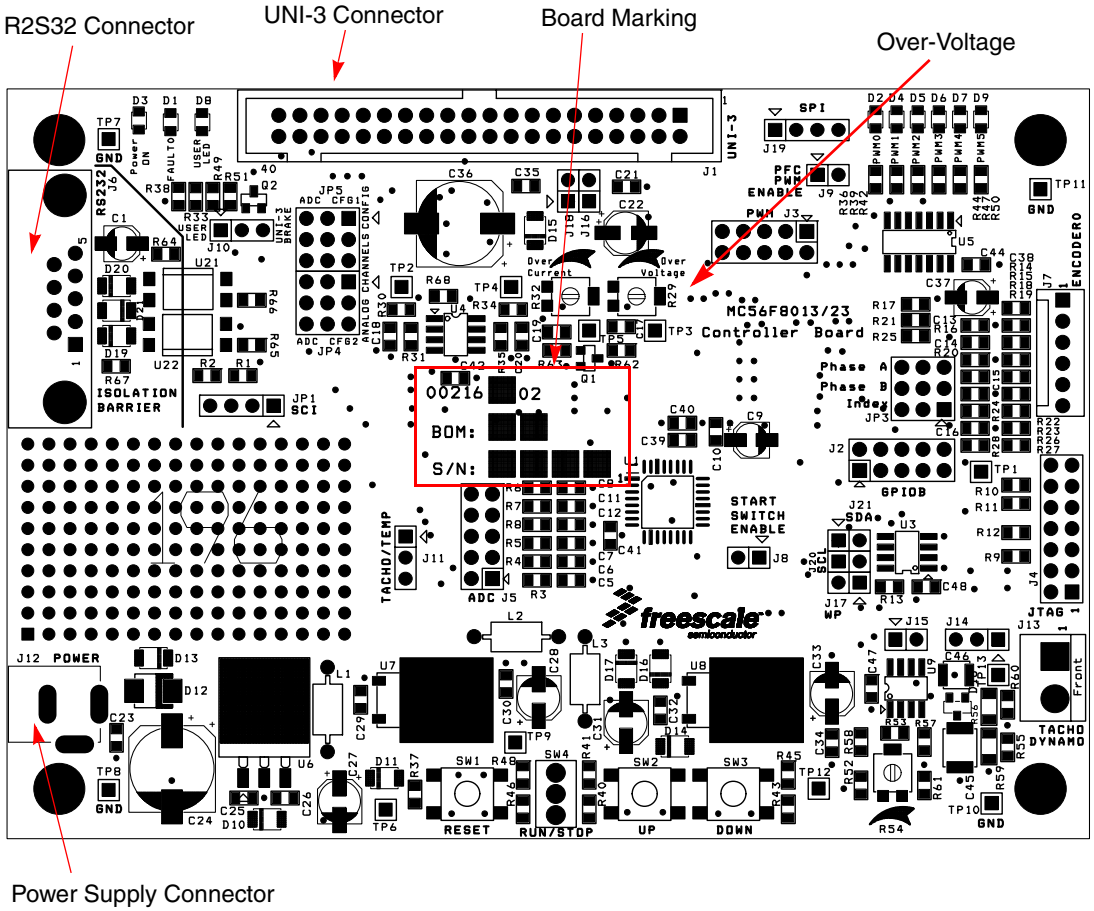

Figure 8-2. MC56F8013/23 Controller Board View

8.3 Power Stage Board Setup

For the power stage board configuration, follow these steps:

1. Set the jumper on pinhead J3 between pins 3 – 5 and 4 – 6.
2. Connect the AC Induction Motor to the connector J6.

8.4 PFC Board Setup

The PFC board is interconnected to the power stage board. Connectors J2, J3, and J4 on the PFC board are connected to connectors J9, J11, and J5 on the power stage board. These power connectors should be interconnected by a power wire. PFC control and sensing signals are available on the PFC control connector J5, which is connected to the J2 connector on the power stage board. The AC power is connected to the J1 connector.

When all the boards are configured, they can be interconnected, and the whole demo hardware set-up can be built. The complete application set-up is shown in Figure 8-3. A 230 V AC power supply to terminals J1 on the PFC board can be applied and the FreeMASTER control page can be run.

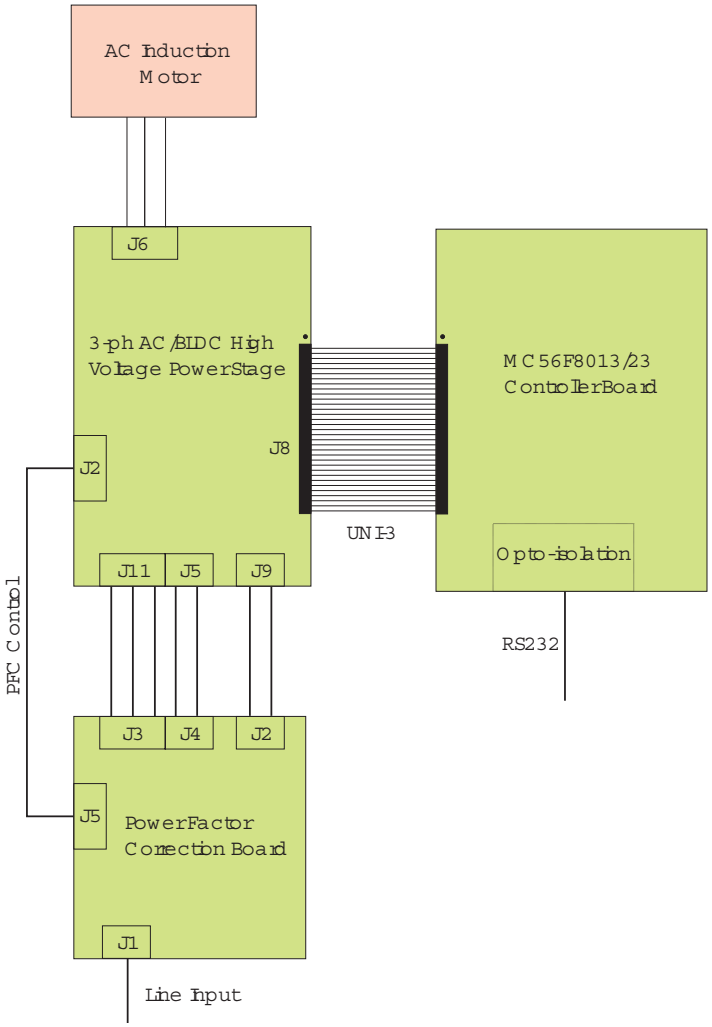

Figure 8-3. Demo Application Connection Overview

CAUTION

There is a risk of electric shock. The PFC Board, MC56F8013/23 Controller Board, and the 3ph AC/BLDC high voltage power stage board are connected to high voltage. The only safe mode of control is by remotely controlling the application using the host PC running the FreeMASTER application. The RS232 port is the only interface that provides galvanic isolation.

CAUTION

The JTAG connector does not provide galvanic isolation. The demo hardware set-up has to be disconnected from high-voltage if a JTAG connection is required. To debug the application or to download code to the device flash memory using JTAG, use a low-voltage +12 V power supply connected to the J12 connector on the MC56F8013/23 controller board.

Appendix A
Schematic, Parts List, and Layouts

A.1 Schematic

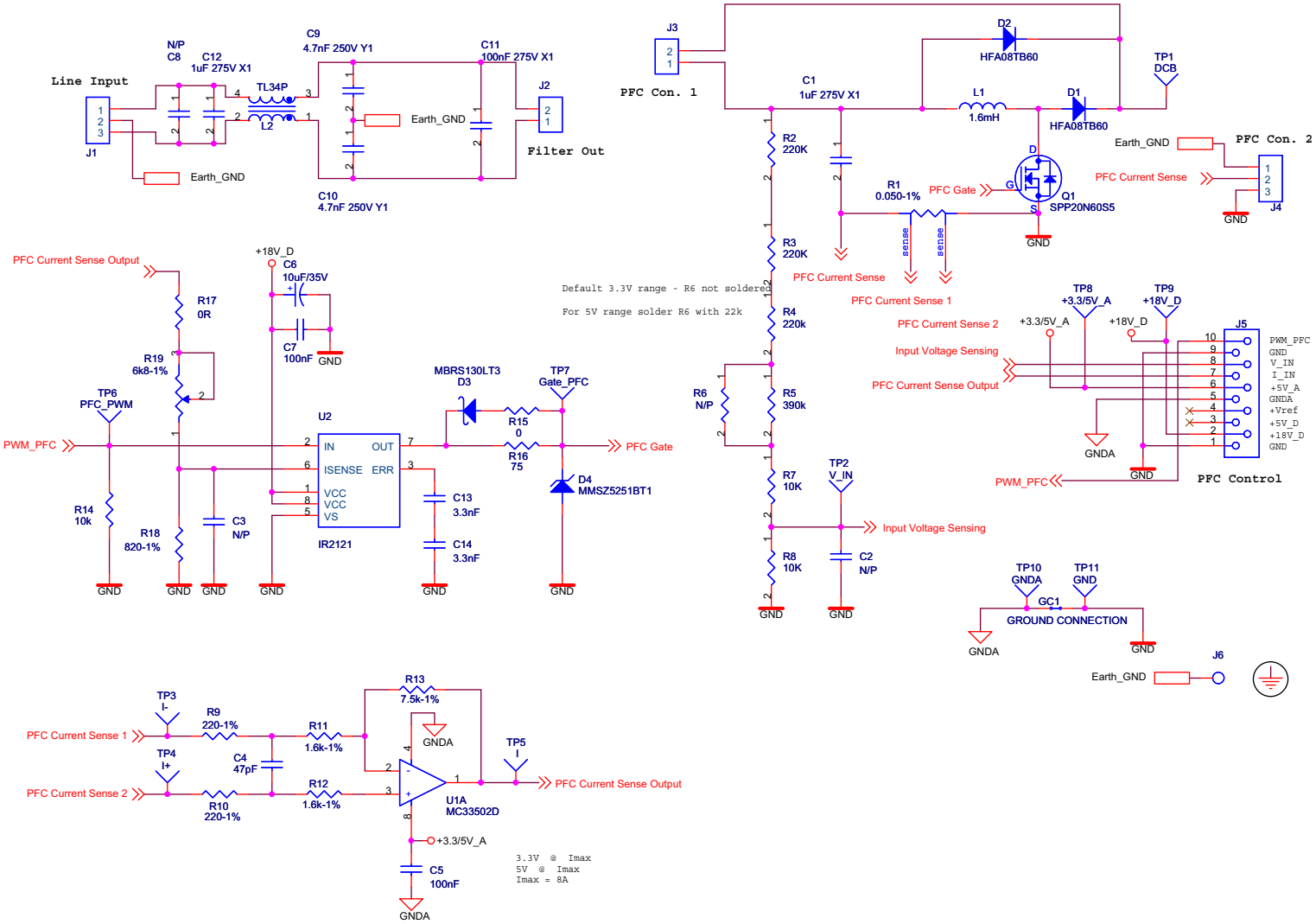

Figure A-1. PFC Schematic

A.2 Parts List

Table A-1. Printed Circuit Board Parts List

Designators	Quantity	Description	Manufactures	Part Number
C1	1	1 μF/ 275V X1	Any Acceptable	—
C2	1	N/P	—	—
C3	1	N/P	—	—
C4	1	47 pF size 0805	Any Acceptable	—
C5, C7, C13, C14	4	100 nF size 0805	Any Acceptable	—
C6	1	10 μF/ 35V size C	Any Acceptable	—
C8	1	N/P	—	—
C9, C10	2	4.7 nF/ 275V Y1	Any Acceptable	—
C11	1	100 nF/ 275V X1	Any Acceptable	—
C12	1	1 μF/ 275V X1	Any Acceptable	—
D1, D2	2	8A/600V Ultrafast Rectifier TO220	International Rectifier	HFA08TB60
D3	1	1A/30V Schottky Rectifier size SMB	On Semiconductor	MBRS130LT3
D4	1	20V Zener Diode SOD-123	On Semiconductor	MMSZ5250BT1
GC1	1	Ground connection	—	—
J1, J4	2	CON/TOP 1.5 GS 3/90	Camden Electronics	CTB0110/3
J2, J3	2	CON/TOP 1.5 GS 2/90	Camden Electronics	CTB0110/2
J5	1	CON/10	Any Acceptable	MLW10G
J6	1	Ground connection	—	—
L1	1	1.6mH/5.1A	Customs	—
L2	1	2x3.3mH 4A/250V Current Compensated Toroid Choke	Tesla Blatna	TL34P
Q1	1	20A/600V MOSFET TO-220	Infineon Technologies	SPP20N60S5
R1	1	50 mΩ Resistor 1% size 4723	Isabellenhütte	SMV-R050-1.0
R2, R3, R4	3	220kΩ Resistor size 1206	Any Acceptable	—
R5	1	390kΩ Resistor size 1206	Any Acceptable	—
R6	1	N/P	—	—
R7, R8, R14	3	10kΩ Resistor size 0805	Any Acceptable	—

Table A-1. Printed Circuit Board Parts List (continued)

Designators	Quantity	Description	Manufactures	Part Number
R9, R10	2	220Ω Resistor 1% size 0805	Any Acceptable	—
R11, R12	2	1.6kΩ Resistor 1% size 0805	Any Acceptable	—
R13	1	7.5kΩ Resistor 1% size 0805	Any Acceptable	—
R15	1	0Ω Resistor size 0805	Any Acceptable	—
R16	1	75Ω Resistor size 0805	Any Acceptable	—
R17	1	0Ω Resistor size 0805	Any Acceptable	—
R18	1	820Ω Resistor 1% size 0805	Any Acceptable	—
R19	1	10kΩ Trimmer 1% size 4315	Any Acceptable	—
TP1, TP3, TP4, TP7	4	Test Point Black 1mm	Any Acceptable	—
TP2, TP5, TP6	3	Test Point Green 1mm	Any Acceptable	—
TP8, TP9	2	Test Point Red 1mm	Any Acceptable	—
TP10, TP11	2	Test Point White 1mm	Any Acceptable	—
U1	1	MC33502D/SOIC-8	Freescale	MC33502D
U2	1	IR2121/DIP-8	International Rectifier	IR2121

A.3 Layouts

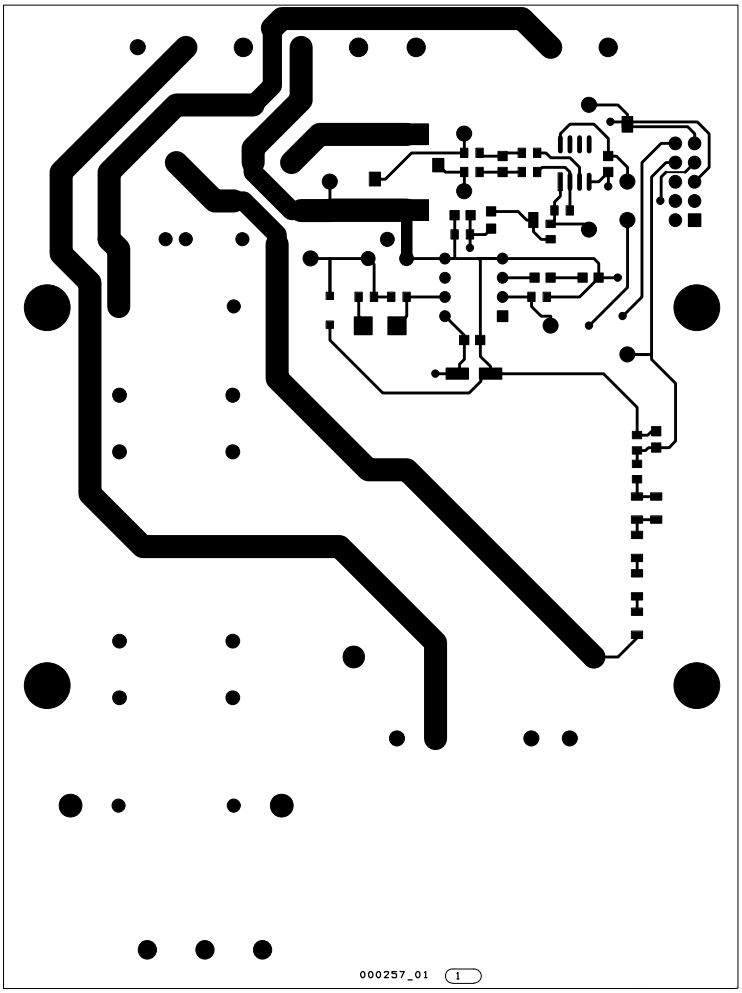

Figure A-2. PFC Board Top Layer

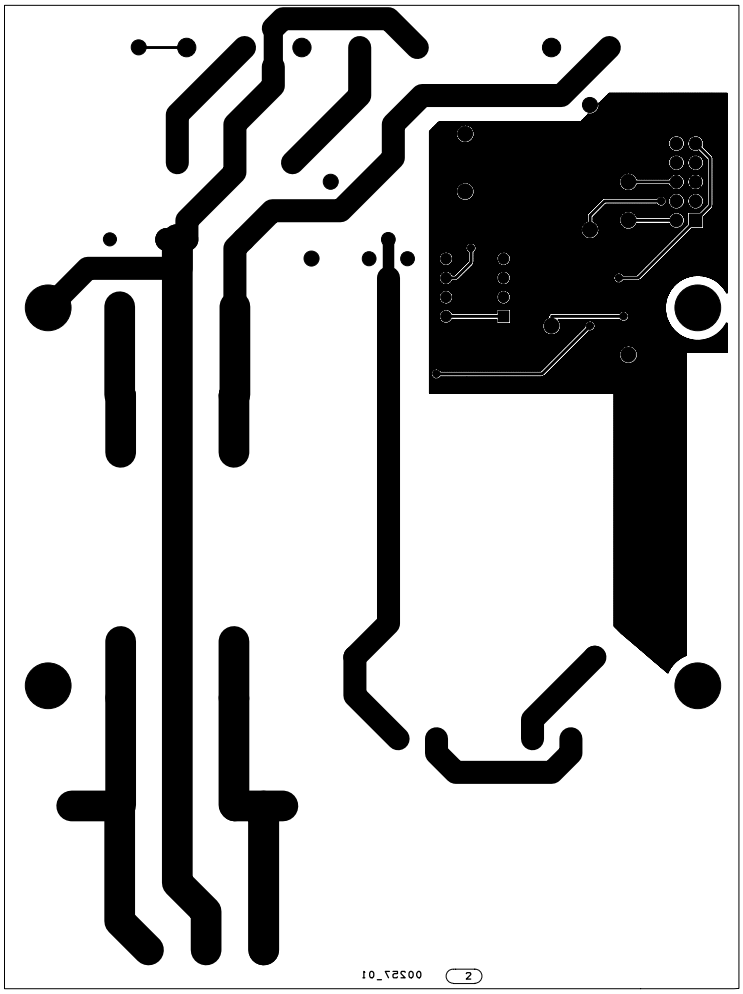

Figure A-3. PFC Board Bottom Layer

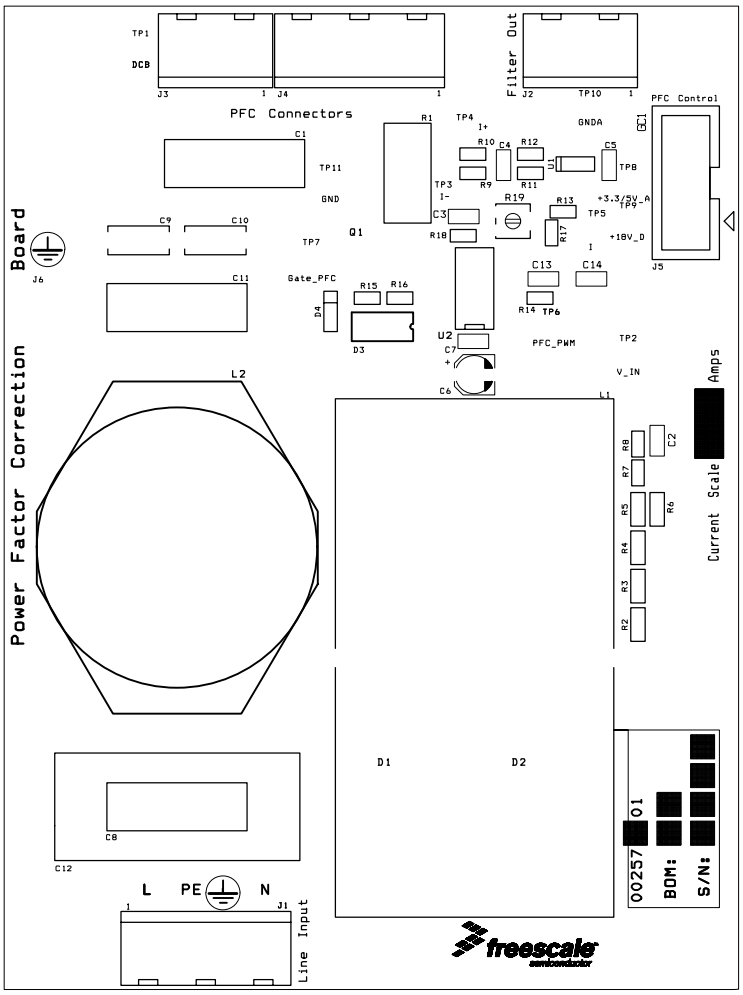

Figure A-4. PFC Board Silkscreen Top Layer

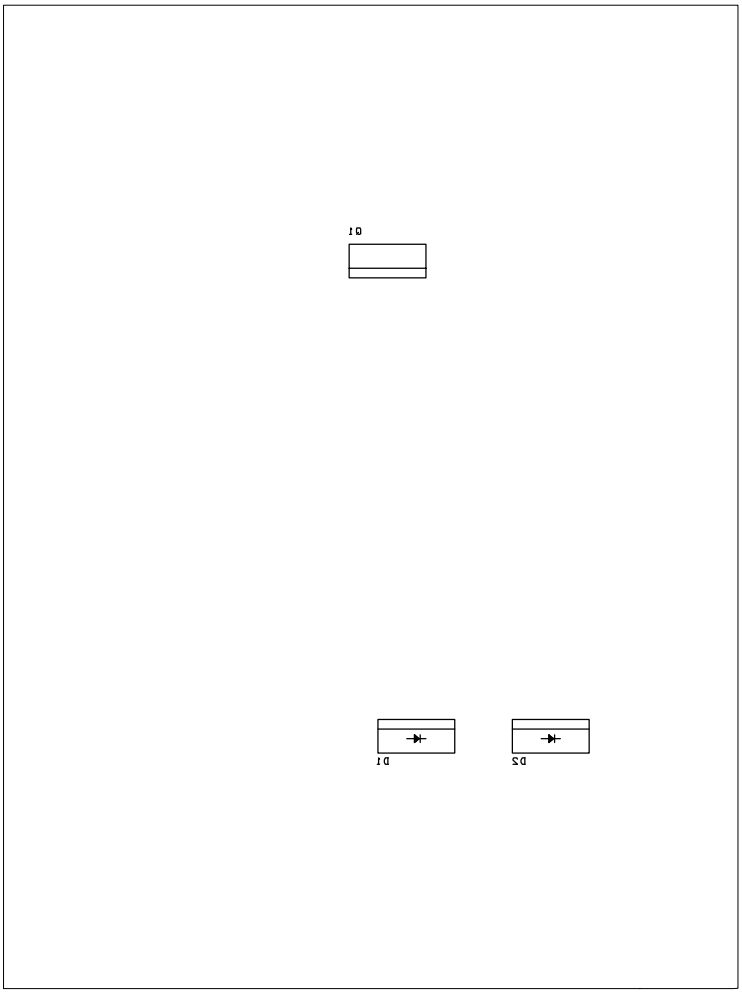

Figure A-5. PFC Board Silkscreen Bottom Layer

Appendix B
Glossary of Abbreviations

AC — alternating current

ACIM — AC induction motor

ADC — analogue-to-digital converter

BLDC — brushless direct current (motor)

CCM — continuous conduction mode

DC — direct current

DSC — digital signal controller

MC56F80xx — a Freescale family of 16-bit DSCs dedicated to motor control

GPIO — general purpose input/output

I/O — input/output interfaces between a computer system and the external world. A CPU reads an input to sense the level of an external signal and writes to an output to change the level of an external signal

JTAG — Joint test action group: acronym commonly used to refer to an interface allowing on-chip emulation and programming

LED — light emitting diode

PI controller — proportional-integral controller

PLL — phase locked loop

PFC — power factor correction

PWM — pulse width modulation

Quad timer — a module with four 16-bit timers

reset — to force a device to a known condition

SCI — serial communication interface module: a module that supports asynchronous communication

SPI — serial peripheral interface module: a module that supports synchronous communication

SMPS — switch mode power supply

THD — total harmonic distortion