



MC56F8006 Controller Daughter Board for BLDC/PMSM Motor Control Drive

Users Manual

MC56F8006DBUM

Rev. 0
05/2009

freescale.com



Table of Contents

Chapter 1 Board Overview

| | | |
|-----|---|---|
| 1.1 | MC56F8006 Controller Daughter Board for BLDC/PMSM Motor Control Drive Outline | 7 |
| 1.2 | About this Manual | 7 |
| 1.3 | Setup Guide | 8 |
| 1.4 | Board Description | 8 |

Chapter 2 Pin Description

| | | |
|-------|---|----|
| 2.1 | Introduction | 9 |
| 2.2 | Signal Descriptions | 9 |
| 2.2.1 | Configuration Header J1 | 9 |
| 2.2.2 | ADC Configuration Headers J5, J6 | 10 |
| 2.2.3 | JTAG Header J3 | 10 |
| 2.2.4 | Daughter Board Connectors J3 and J4 | 11 |

Appendix A. MC56F8006 Controller Daughter Board for BLDC/PMSM Motor Control Drive Schematics

Appendix B. Bill of Materials

Appendix C. MC56F8006 Controller Daughter Board for BLDC/PMSM Motor Control Drive Layouts



MC56F8006 Controller Daughter Board for BLDC/PMSM Motor Control Drive

Users Manual

by:Lukas Osmancik
Freescale Semiconductor
Czech System Center

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify that you have the latest information available, refer to www.freescale.com

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

| Date | Revision Level | Description | Page Number(s) |
|---------|----------------|-----------------|----------------|
| 01/2009 | 0 | Initial release | N/A |

Chapter 1

Board Overview

1.1 MC56F8006 Controller Daughter Board for BLDC/PMSM Motor Control Drive Outline

Freescale's MC56F8006 Controller Daughter Board for BLDC/PMSM Motor Control Drive, together with a 3-phase BLDC/PMSM Motor Control Drive board, create a single unit for developing BLDC/PMSM motor-control applications.

The daughter board is connected via two connectors to the 3-phase BLDC/PMSM Motor Control Drive board. All necessary signals are available to allow a variety of algorithms to control the 3-phase PMSM and BLDC motors.

Figure 1-1 is an illustration of the controller daughter board.

1.2 About this Manual

Key items are in the following locations in this manual:

- Setup instructions — [1.3 Setup Guide](#).
- Schematics — [Appendix A. MC56F8006 Controller Daughter Board for BLDC/PMSM Motor Control Drive Schematics](#).
- Pin assignments — [Chapter 2 Pin Description](#)
- Pin-by-pin description — [2.2 Signal Descriptions](#).



Figure 1-1 MC56F8006 Controller Daughter Board

1.3 Setup Guide

Setup and connections for the MC56F8006 Controller Daughter Board for BLDC/PMSM Motor Control Drive are straightforward. The controller daughter board plugs into the main board via two 20-pin daughter board connectors. The system can be powered by a 12 to 24 V DC power supply. For safety reasons, and ease of making measurements, use a regulated DC supply. Limit power supply to under five amps.

Place jumpers to route the required signals to the controller. For jumper settings, visit chapter [2.2.1 Configuration Header J1](#) and [2.2.2 ADC Configuration Headers J5, J6](#).

A step-by-step setup procedure for the main board is available in the *3-phase BLDC/PMSM Motor Control Drive User Manual*.

WARNING

Check the power supply voltage before plugging in the Controller Daughter Board. If an input voltage higher than 24 V is applied, the controller daughter board can be damaged.

1.4 Board Description

The Controller Daughter Board is populated with an MC56F8013 or MC56F8023 digital signal controller (DSC). All the necessary signals are available on two 20-pin Rib-cage connectors, J6 and J7. Headers J1, J2, J4, and J5 are configuration headers and are used for board configuration. For more details, see [2.2.1 Configuration Header J1](#) and [2.2.2 ADC Configuration Headers J5, J6](#). JTAG header J3 is used for uploading the program onto the controller.

Board schematic is available in [Appendix A. MC56F8006 Controller Daughter Board for BLDC/PMSM Motor Control Drive Schematics](#).

Chapter 2

Pin Description

2.1 Introduction

Inputs and outputs are located on seven connectors and headers available on the board:

- Configuration header J1
- ADC configuration headers J5, J6
- JTAG header J2
- Two 20-pin daughter board connectors J3, J4

Pin descriptions for each connector and header are identified in the following information. [Figure 2-1](#) shows the pin assignments for the daughter board connectors J3 and J4. [Table 2-5](#) and [Table 2-6](#) show the signal descriptions. Several configuration headers are used because the MC56F8006 controller in the LQFP32 package doesn't have enough pins.

2.2 Signal Descriptions

Pin descriptions are identified in this subsection.

2.2.1 Configuration Header J1

Configuration header J1 serves for connecting the ENCODER Index/Hall sensor phase C signal or the RxD signal for SCI communication to the controller GPIOB6 pin. [Table 2-1](#) shows the jumper settings for the selected function.

Table 2-1 Configuration Header J1

| Pins shorted | Signal Name | Description |
|--------------|-------------|---|
| 1–2 | ENC_Index | ENCODER Index or Hall sensors Phase C input |
| 2–3 | RxD | RxD signal for SCI communication |

2.2.2 ADC Configuration Headers J5, J6

Table 2-2 and Table 2-3 show the ADC Configuration Headers pin description. Header J5 selects, if the BEMF voltages or phase currents are routed to the controller ADC inputs. Header J6 selects, if the DC-bus current or phase currents are routed to the controller ADC input.

Table 2-2 ADC Configuration Header J5 — Signal Descriptions

| Header # | Pins shorted | Signal Name | Description |
|----------|--------------|--------------|---|
| 5 | 1–2 | I_sense_A | Analog-sense signal that measures current in phase A. |
| | 3–4 | BEMF_sense_A | Analog-sense signal that measures phase A back-EMF. |
| | 5–6 | I_sense_B | Analog-sense signal that measures current in phase B. |
| | 7–8 | BEMF_sense_B | Analog-sense signal that measures phase B back-EMF. |
| | 9–10 | I_sense_C | Analog-sense signal that measures current in phase C. |
| | 11–12 | BEMF_sense_C | Analog-sense signal that measures phase C back-EMF. |

Table 2-3 ADC Configuration Header J6 — Signal Descriptions

| Header # | Pins shorted | Signal Name | Description |
|----------|--------------|-------------|--|
| 6 | 1–2 | I_sense_DCB | Analog-sense signal that measures current in phase DC-bus. |
| | 2–3 | I_sense_A | Analog-sense signal that measures current in phase A. |

2.2.3 JTAG Header J3

This serves for updating the software for the MC56F8006 controller. Signals are described in Table 2-4.

Table 2-4 JTAG Header J2 — Signal Descriptions

| Pin # | Signal Name | Description |
|-------|-------------|-------------------------|
| 1 | TDI | Test data input signal |
| 2 | GND | Digital ground |
| 3 | TDO | Test data output signal |
| 4 | GND | Digital ground |
| 5 | TCK | Test clock input signal |
| 6 | GND | Digital ground |

Table 2-4 JTAG Header J2 — Signal Descriptions (Continued)

| Pin # | Signal Name | Description |
|-------|-------------|----------------------------------|
| 7 | No Connect | |
| 8 | No Connect | |
| 9 | /RESET | $\overline{\text{RESET}}$ signal |
| 10 | TMS | Test mode select input signal |
| 11 | +3.3V | Digital +3.3 V power supply |
| 12 | No Connect | |
| 13 | No Connect | |
| 14 | No Connect | |

2.2.4 Daughter Board Connectors J3 and J4

Signal inputs and outputs for interconnection with the 3-phase BLDC/PMSM LV Motor Control Drive are situated on two 20-pin connectors, located on the board's bottom-side. [Figure 2-1](#) shows the pin assignments. This figure shows the physical layout of the connectors, assuming that the board is oriented upside down (bottom is up). [Table 2-5](#) and [Table 2-6](#) contain the lists of signal descriptions for connectors J6 and J7.

Table 2-5 Daughter Board Connector J3 — Signal Descriptions

| Pin # | Signal Name | Description |
|-------|-------------|---|
| 1 | GND | Digital and power ground |
| 2 | +3.3V | Digital +3.3 V power supply |
| 3 | NC | |
| 4 | NC | |
| 5 | PWM_AT | Gate-drive signal for the top half-bridge of phase A. A logic low turns on phase A's top switch. |
| 6 | PWM_AB | Gate-drive signal for the bottom half-bridge of phase A. A logic high turns phase A's bottom switch on. |
| 7 | PWM_BT | Gate-drive signal for the top half-bridge of phase B. A logic low turns on phase B's top switch. |
| 8 | PWM_BB | Gate-drive signal for the bottom half-bridge of phase B. A logic high turns phase B's bottom switch on. |
| 9 | PWM_CT | Gate-drive signal for the top half-bridge of phase C. A logic low turns on phase C's top switch. |
| 10 | PWM_CB | Gate-drive signal for the bottom half-bridge of phase C. A logic high turns phase C's bottom switch on. |
| 11 | OC | Overcurrent signal from the 3-phase bridge driver |

Table 2-5 Daughter Board Connector J3 — Signal Descriptions (Continued)

| Pin # | Signal Name | Description |
|-------|-------------------|--|
| 12 | INT | Interrupt signal from the 3-phase bridge driver |
| 13 | TxD | TxD signal between JM60 and the Controller Daughter Board |
| 14 | RxD | RxD signal between JM60 and the Controller Daughter Board |
| 15 | TOGGLE_SWITCH_ON1 | Toggle switch input (switch in position ON1) on the BLDC drive |
| 16 | TOGGLE_SWITCH_ON2 | Toggle switch input (switch in position ON2) on the BLDC drive |
| 17 | UP_SWITCH | UP switch input |
| 18 | DOWN_SWITCH | DOWN switch input |
| 19 | USER_LED | USER LED signal |
| 20 | /RESET | $\overline{\text{RESET}}$ signal |

Table 2-6 Daughter Board Connector J4 — Signal Descriptions

| Pin # | Signal Name | Description |
|-------|---------------|--|
| 1 | GNDA | Analog power supply ground |
| 2 | +3.3VA | Analog +3.3 V power supply |
| 3 | I_sense_A | Analog-sense signal that measures current in phase A. It is scaled at 50 V per amp of DC-bus current. |
| 4 | I_sense_B | Analog-sense that measures current in phase B. It is scaled at 0.563 V per amp of DC-bus current. |
| 5 | I_sense_C | Analog-sense signal that measures current in phase C. It is scaled at 0.563 V per amp of DC-bus current. |
| 6 | BEMF_sense_A | Analog-sense signal that measures phase A back-EMF. It is scaled at 8.09 mV per volt of DC-bus voltage. |
| 7 | BEMF_sense_B | Analog-sense signal that measures phase B back-EMF. It is scaled at 8.09 mV per volt of DC-bus voltage. |
| 8 | BEMF_sense_C | Analog-sense signal that measures phase C back-EMF. It is scaled at 8.09 mV per volt of DC-bus voltage. |
| 9 | V_sense_DCB | Analog-sense signal that measures bus voltage. It is scaled at 8.09 V per volt of DC-bus voltage. |
| 10 | V_sense_DCB/2 | Analog-sense signal that measures bus voltage. It is scaled at 8.09 V per volt of DC-bus voltage. |
| 11 | I_sense_DCB | Analog-sense signal that measures bus current. It is scaled at 8.09 V per amp of DC-bus current. |
| 12 | ENC_PhaseA | Encoder or Hall sensor Phase A input pin logic |

Table 2-6 Daughter Board Connector J4 — Signal Descriptions (Continued)

| Pin # | Signal Name | Description |
|-------|-------------|---|
| 13 | ENC_PhaseB | Encoder or Hall sensor Phase B input pin logic |
| 14 | ENC_Index | Encoder Index or Hall sensor Phase C input pin logic |
| 15 | DRV_EN | 3-phase bridge gate driver enable signal |
| 16 | /SS | SPI pin chip select pin for the 3-phase bridge driver |
| 17 | MOSI | SPI pin Master Out Slave In pin for the 3-phase bridge driver |
| 18 | SCLK | SPI pin Clock Source pin Input for the 3-phase bridge driver |
| 19 | MISO | SPI pin Master In Slave Out pin for the 3-phase bridge driver |
| 20 | GND | Digital and power ground |

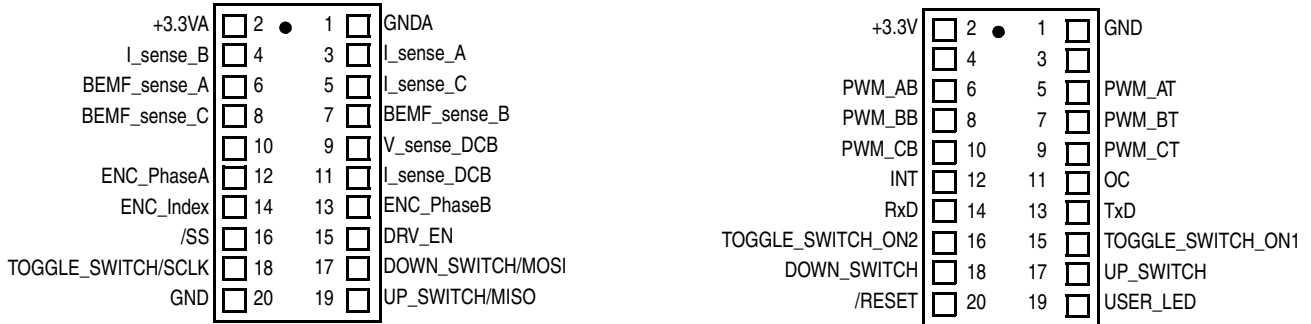


Figure 2-1 J3 and J4 Connector Physical View on Daughter Board



Appendix A. MC56F8006 Controller Daughter Board for BLDC/PMSM Motor Control Drive Schematics

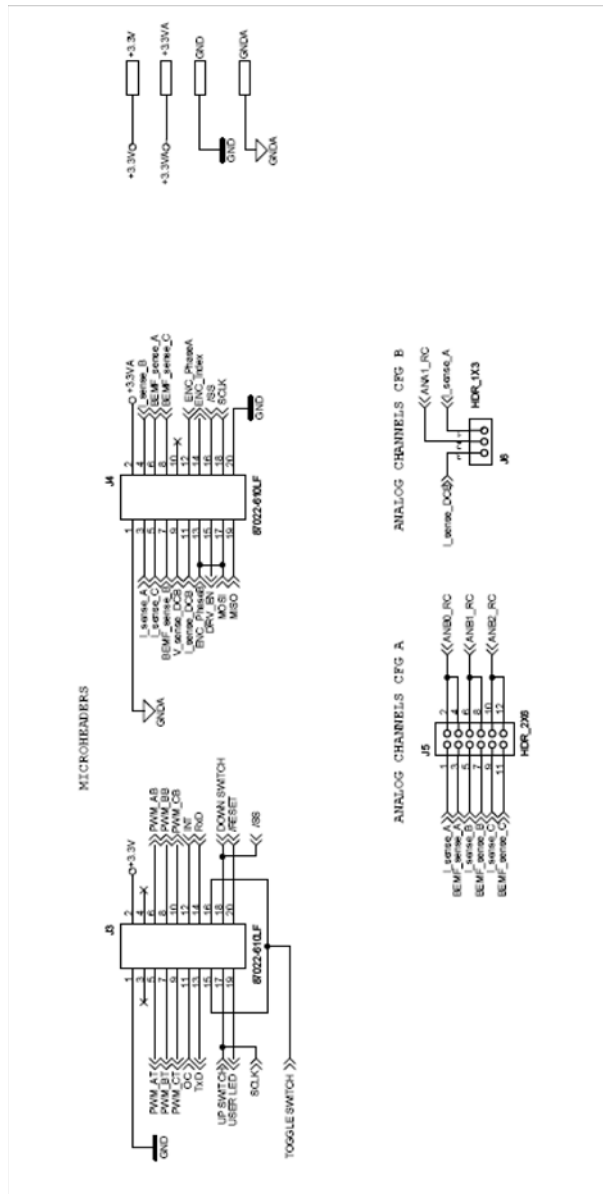


Figure A-1 Daughter Board Connectors and Headers

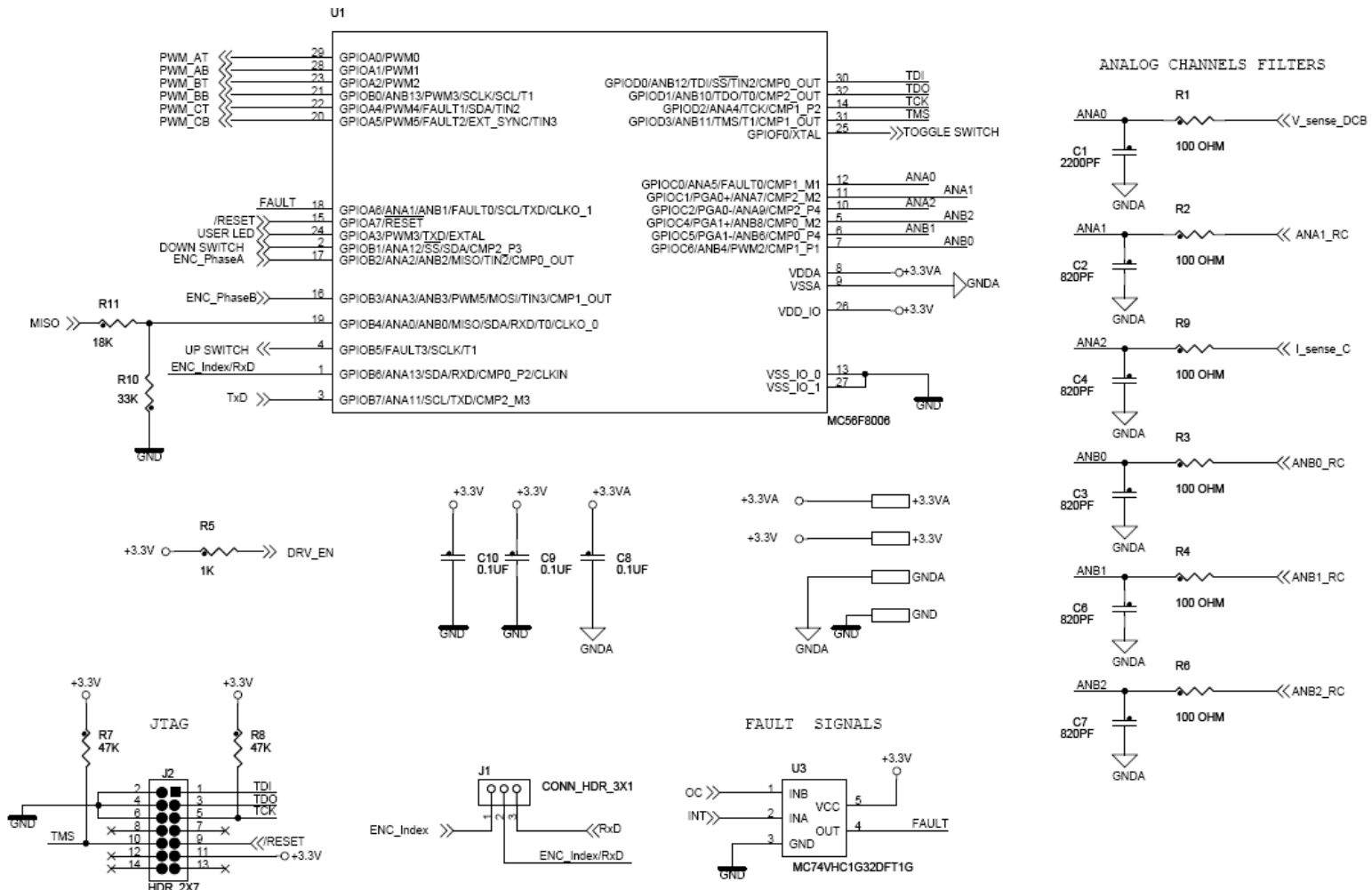


Figure A-2 Controller and Headers

Appendix B. Bill of Materials

Table B-1 Parts List

| DESIGNATORS | QUANTITY | DESCRIPTION | MANUFACTURER | PART NUMBER |
|-----------------------|----------|--|----------------------------|------------------|
| C2,C2,C4,C6,C7 | 5 | 820 pF/6.3 V size 0805 | ANY ACCEPTABLE | — |
| C1 | 1 | 2200 pF/ 6.3 V size 0805 | ANY ACCEPTABLE | — |
| C8,C9,C10 | 3 | 100 nF/6.3 V size 0805 | ANY ACCEPTABLE | — |
| J1,J6 | 2 | HDR 3x1 | MOLEX | 09-65-2038 |
| J2 | 1 | HDR 2x7 | TYCO ELECTRONICS | 4-103322-2 |
| J3,J4 | 2 | 87022-610 | FCI | 87022-610LF |
| J5 | 1 | HDR 2x6 | TYCO ELECTRONICS | |
| R1,R2,R3,R4,R6, R9 | 6 | 100 Ω Resistor 1/8 W 1 % size 0805 | ANY ACCEPTABLE | — |
| R5 | 1 | 1 k Ω Resistor 1/8 W size 0805 | ANY ACCEPTABLE | — |
| R7,R8 | 2 | 47 k Ω Resistor 1/8 W size 0805 | ANY ACCEPTABLE | — |
| R10 | 1 | 33 k Ω Resistor 1/8 W size 0805 | ANY ACCEPTABLE | — |
| R11 | 1 | 18 k Ω Resistor 1/8 W size 0805 | ANY ACCEPTABLE | — |
| U1 | 1 | digital signal controller/LQFP-32 | FREESCALE SEMICONDUCTOR | MC56F8006VLC |
| U2 | 1 | two-input OR gate | ON SEMICONDUCTOR | MC74VHC1G32DFT1G |

Appendix C. MC56F8006 Controller Daughter Board for BLDC/PMSM Motor Control Drive Layouts

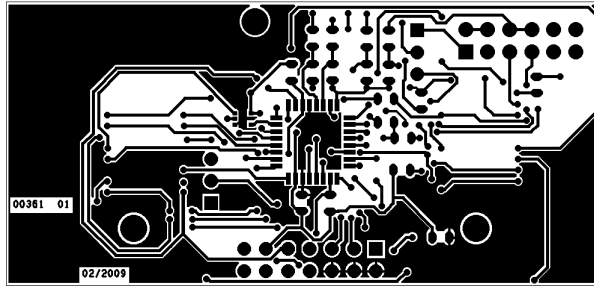


Figure C-1 Board Top Layer

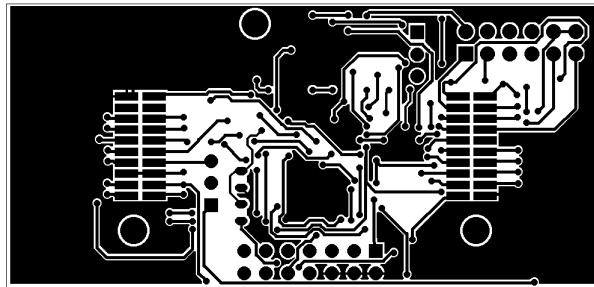


Figure C-2 Board Top Layer

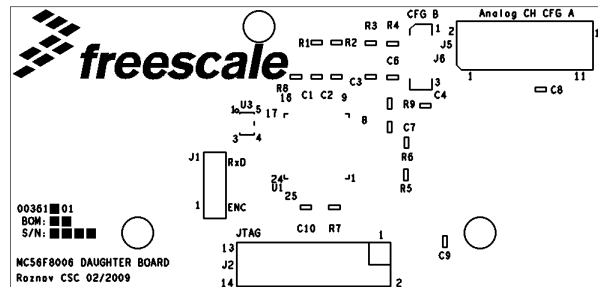


Figure C-3 Board Top Layer



How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.



Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. The ARM POWERED logo is a registered trademark of ARM Limited. ARM7TDMI-S is a trademark of ARM Limited. Java and all other Java-based marks are trademarks or registered trademarks of Sun Microsystems, Inc. in the U.S. and other countries. The Bluetooth trademarks are owned by their proprietor and used by Freescale Semiconductor, Inc. under license.

© Freescale Semiconductor, Inc. 2004. All rights reserved.