Design of a Digital AC/DC SMPS using the 56F8323 Device

Designer Reference Manual

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16-bit Digital Signal Controllers

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
08/2005	0	Initial release	N/A

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About This Document

This manual describes the use of a 56F8323 device in an SMPS application.

Audience

This manual targets design engineers interested in developing a digital AC/DC SMPS application.

Organization

This User's Manual consists of the following sections:

- **Chapter 1, Hardware Design of a Power Factor Correction System,** explains system and hardware designs for a PFC system.
- **Chapter 2, Hardware Design of a DC/DC Converter System,** provides system and hardware designs for the application's DC/DC system.
- **Chapter 3, Controller Board Hardware Architecture,** contains a detailed explanation of the controller board's hardware design.
- **Chapter 4, Communication Interface Board Hardware Architecture,** details the hardware architecture of the communication interface board.
- **Chapter 5, Control Strategy Design,** describes control strategies for the application's PFC and DC/DC systems.
- **Chapter 6, Software System Design—PWM Control Strategy,** explains design of the PWM and DC/DC software systems.
- **Chapter 7, Software Architecture,** details the application's software architecture.
- **Chapter 8, Flow Chart of Software System Design,** illustrates the software system design.
- **Appendix A, Schematics,** contains schematics for the digital AC/DC SMPS application.
- **Appendix B, SMPS Bill of Materials,** lists all parts used in the application.

Conventions

This document uses the following notational conventions:

Typeface, Symbol or Term	Meaning	Examples
`Courier Monospaced Type`	Code examples	`//Process command for line flash`
Italic	Directory names, project names, calls, functions, statements, procedures, routines, arguments, file names, applications, variables, directives, code snippets in text	...and contains these core directories: *applications* contains applications software... ...CodeWarrior project, *3des.mcp* is... ...the *pConfig* argument.... ...defined in the C header file, *aec.h*....
Bold	Reference sources, paths, emphasis	...refer to the **Targeting DSP56F83xx Platform** manual.... ...see: **C:\Program Files\Freescale\help\tutorials**
Blue Text	Linkable on-line	...refer to Chapter 7, License....
Number	Any number is considered a positive value, unless preceded by a minus symbol to signify a negative value	3V -10 DES^{-1}
ALL CAPITAL LETTERS	# defines/ defined constants	# define INCLUDE_STACK_CHECK
Brackets [...]	Function keys	...by pressing function key [F7]
Quotation marks, “...”	Returned messages	...the message, “Test Passed” is displayed.... ...if unsuccessful for any reason, it will return “NULL”...

Definitions, Acronyms, and Abbreviations

The following list defines the acronyms and abbreviations used in this document. As this template develops, this list will be generated from the document. As we develop more group resources, these acronyms will be easily defined from a common acronym dictionary. Please note that while the acronyms are in solid caps, terms in the definition should be initial capped ONLY IF they are trademarked names or proper nouns.

IC	Integrated Circuit
LC	Inductor Capacitance
PI	Proportional-Integral
PSFB	Phase Shifted Full Bridge
RMS	Root Mean Square
SMPS	Switch Mode Power Supply
ZCS	Zero Current Switch
ZVS	Zero Voltage Switch
ZVT	Zero Voltage Transition

References

The following sources were used to produce this book; we recommend that you have a copy of these references:

1. *DSP56800E Reference Manual,* DSP56800ERM, Freescale Semiconductor, Inc.
2. *56F8300 Peripheral User Manual*, MC56F8300UM, Freescale Semiconductor, Inc.
3. *56F8323 Data Sheet*, MC56F8323, Freescale Semiconductor, Inc.
4. *Implementing a Digital AC/DC Switched-Mode Power Supply using a 56F8300 Digital Signal Controller*, AN3115, Freescale Semiconductor, Inc.

Chapter 1
Hardware Design of a Power Factor Correction System

1.1 Requirements

This section provides the hardware design for the Power Factor Correction (PFC) system. Specifications and performance include:

Input voltage:	85~265V AC
Input frequency:	45~65Hz
Rating output voltage:	370V, voltage range: 350—390V
Rating output power:	500W
Switch frequency:	100K
Power factor:	>95%
Efficiency:	>90%

1.2 System Design

The main circuit consists of two single-switch PFC circuits operated in interleaved mode; see **Figure 1-1**. The circuit is composed of Q_1/Q_2, D_1/D_2, L_1/L_2 and filter capacitance C and includes an EMI filter, input relay and full-wave rectifier. In addition, two assistant switches, Q_3/Q_4, and their assistant network are introduced to realize the Zero Voltage Switch (ZVS) of two main switches.

In the PFC module system, the 56F8323 samples voltage signal, V_{rect}, from the full-wave rectifier; input current, I_{in}; and output voltage, V_{bus}. The outer voltage loop, G1, insures that the output voltage is constant. The output of the voltage loop determines the reference shape of the current loop, which guarantees the input current is a sine wave. The input voltage sample not only determines the input current's crossing point, but at the same time, the input feed forward voltage also accelerates the system response speed when input changes. The speed of the inner current loop, G2, is more rapid. It compares the current sample with current reference, extracts the duty parameters through the current-loop PI regulator, and sends control signals through PWM0—2, achieving the aim of PFC and stabilizing the output voltage.

Zero Voltage Transition (ZVT) technology can realize the ZVS of the main switch and the Zero Current Switch (ZCS) of the boost diode, reducing di/dt of the diode and consequently reducing switch loss and the system's EMI. The operating theory is to realize the ZVS of the main switch, paralleling capacitance in its drain-source, and thus limiting the switch's dv/dt. Before the main switch operates, it releases the charge on capacitance to zero through an assistant circuit, realizing the ZVS of the main switch. The assistant circuit operates a short time before the main switch turns on.

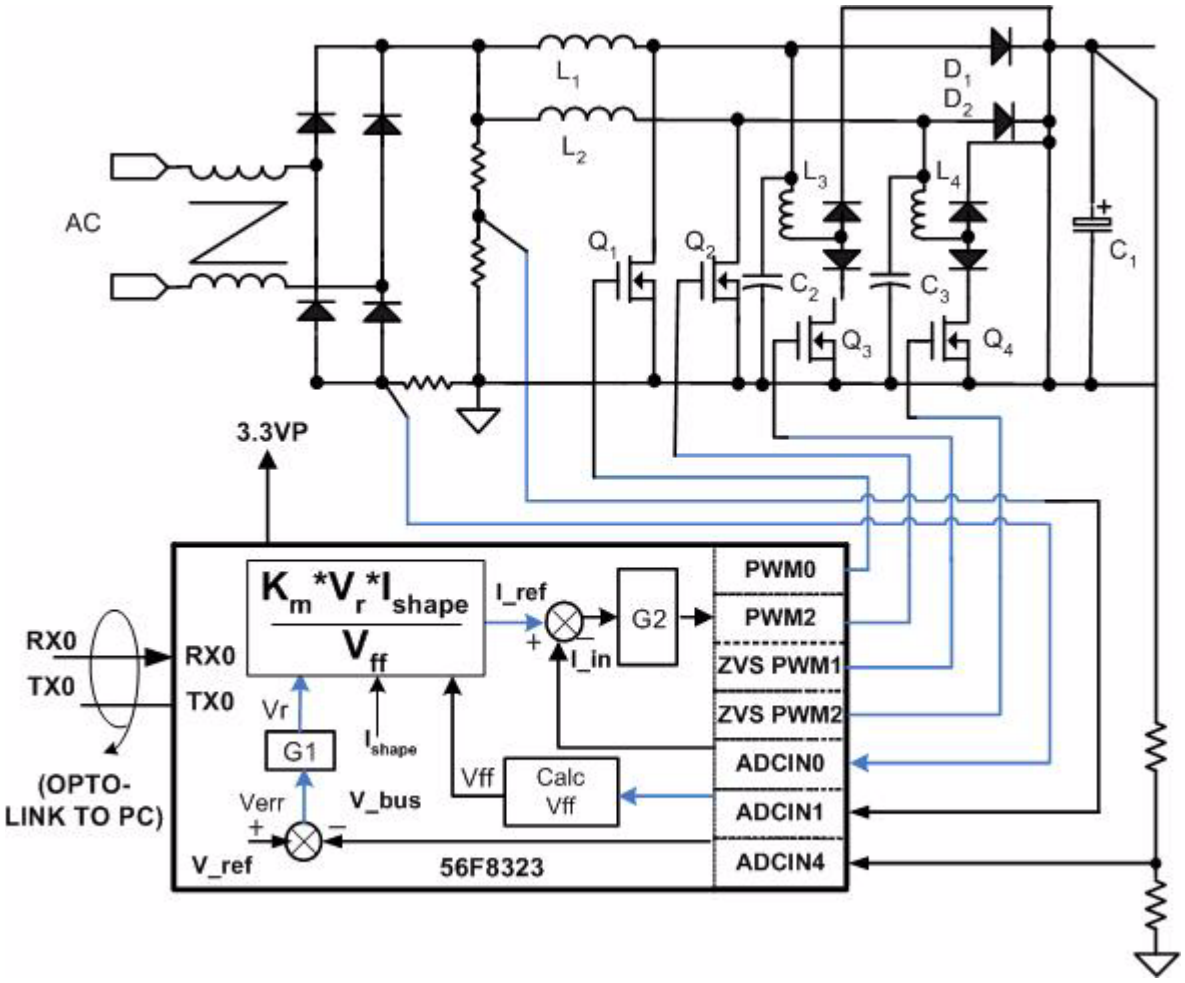


Figure 1-1. PFC Configuration Diagram

1.3 Main Power Circuit Hardware Design

The topology of the main circuit is a double-boost circuit with interleaving and paralleling. The switch period and duty ratio of the two switches are equal, but conduct time is interlaced. Three signals, input current (I_i), input voltage (V_i), and output bus voltage (V_{bus}), are sampled and sent to the 56F8323.

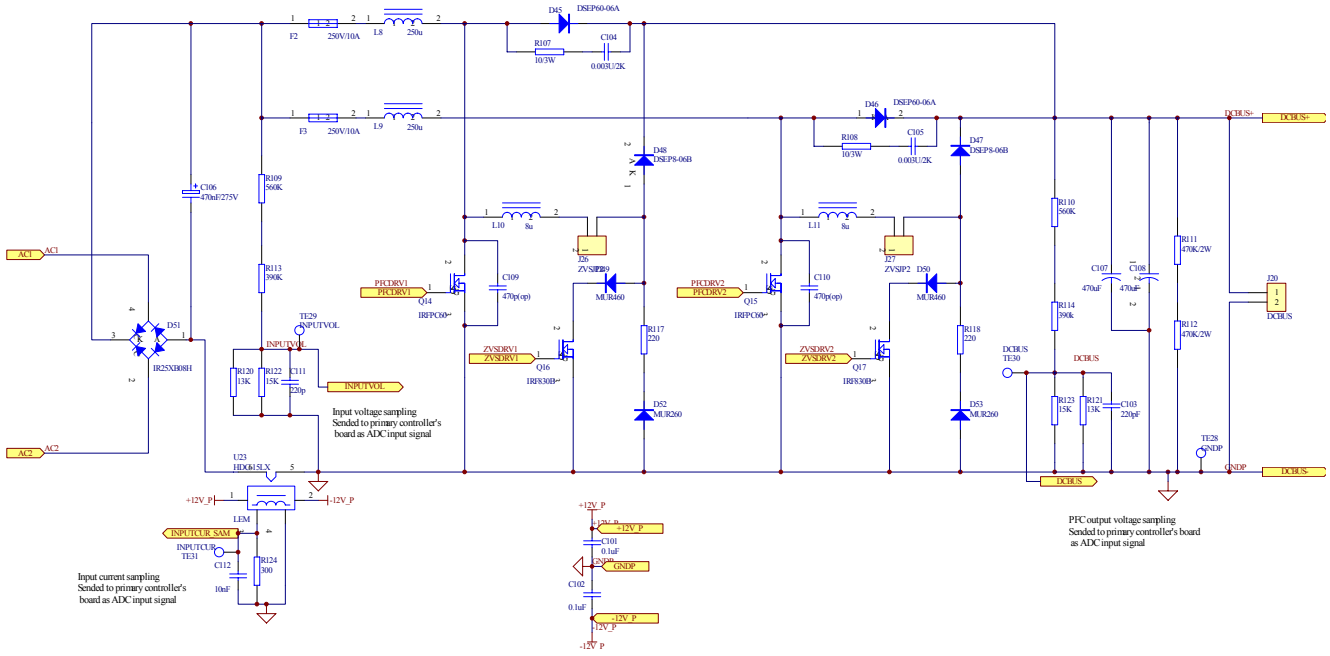


Figure 1-2. PFC Main Circuit

1.3.1 Inductor Selection

Maximum peak line current:

$$I_{pk(\max)} = \frac{\sqrt{2} \times P_O}{\eta V_{in(\min)}} = \frac{\sqrt{2} \times 500}{0.9 \times 85} = 9.24A$$

Eqn. 1-1

Ripple current:

$$\Delta I_L = 20\% I_{pk} = 0.2 \times 9.24 = 3.7A$$

Eqn. 1-2

Determine the duty factor at I_{pk}, where $I_{in(peak)}$ is the peak of the rectified line voltage.

$$D = \frac{V_o - V_{in(peak)}}{V_o} = \frac{380 - \sqrt{2} \times 85}{380} = 0.68$$

Eqn. 1-3

Inductance calculation; f_s is the switching frequency.

$$L = \frac{V_{in} \times D}{fs \times \Delta I} = \frac{\sqrt{2} \times 85 \times 0.68}{100000 \times 3.7} = 221\ \mu H$$

Eqn. 1-4

Round up to 250µH.

1.3.2 Output Capacitor

Output filter inductor can be calculated as follows:

$$C = \frac{2 \times P_O \times \Delta t}{V_{O(\max)}^2 - V_{O(\min)}^2} \qquad \textit{Eqn. 1-5}$$

P_o = 500W

$V_{o(min)}$ = 380 x (1-10%) = 342V

$V_{o(max)}$ = 380 x (1 +10%) = 418V

Δt = 50ms

According to **Equation 1-5**, C = 866μH.

Select the output capacitor to be C = 940μH.

Two 470μH / 450V electrolytic capacitors, connected in parallel, are chosen.

1.3.3 Main Switch

The voltage limit of the main switch is:

$$V_{CEM(S)} > 1.5 V_{cem(S)} = 1.5 V_{in\,(max)} = 1.5 \times 380 = 570 V \qquad \textit{Eqn. 1-6}$$

The circuit limit of the main switch is calculated by RMS value:

$$I_{CEM\,(S)} > 1.5 I_{L(\max)} = 1.5 \times \frac{\sqrt{2} \cdot P_o}{\eta \cdot V_{in(\min)}} = 1.5 \times \frac{\sqrt{2} \cdot 500}{0.9 \times 85} = 13.86\,A \qquad \textit{Eqn. 1-7}$$

Select main switch Q_{400}—Q_{401} to be the MOSFET IRFPC60LC.

Parameters are:

- V_{DSS} = 600V
- I_D = 16A
- $R_{DS(on)tye}$ = 0.4Ω
- TO-247AC package

1.3.4 Output Diode

The voltage limit of the output diode is:

$$V_{CEM(S)} > 1.5 V_{cem(S)} = 1.5 V_{in\,(max)} = 1.5 \times 380 = 570 V \qquad \textit{Eqn. 1-8}$$

The circuit limit of the output diode is calculated by RMS value:

$$I_{CEM(S)} > 1.5 I_{L(\max)} = 1.5 \times \frac{\sqrt{2} \cdot P_o}{\eta \cdot V_{in}(\min)} = 1.5 \times \frac{\sqrt{2} \cdot 500}{0.9 \times 85} = 13.86\,A$$

Eqn. 1-9

Select output diode D_{400}—D_{402} to be FRED DSEP60-06A.

Parameters are:

- V_{RRM} = 600V
- I_{FAVM} = 60A
- t_{rr} = 35nS
- TO-247AD package

1.3.5 Inductor Design

As shown in **Section 1.3.1**, L = 250μH.

Select B_m = 0.3T.

Select magnetic core to be E133, with an effective area of 118mm^2.

Inductor winding can be calculated as follows:

$$N = \frac{LI_{L(\max)}}{A_e B_m} = 38.2$$

Eqn. 1-10

Select N = 38

The gap is:

$$\delta = \frac{\mu_o N^2 A_e}{L} = \frac{1.25 \times 10^{-6} \times 38^2 \times 118 \times 10^{-6}}{250 \times 10^{-6}} = 0.85mm$$

Eqn. 1-11

When work frequency of inductance is 150kHz, the penetrate depth of copper lead is:

$$\Lambda = \sqrt{\frac{2}{2\pi f_s \mu \gamma}} = \sqrt{\frac{1}{3.14 \times 100 \times 10^3 \times 1.25 \times 10^{-6} \times 58 \times 10^6}} = 0.209mm$$

Eqn. 1-12

Where:

γ is the electric conductive ratio of lead

μ is the magnetic conductive ratio of lead

A copper lead with a diameter less than 0.42mm can be selected.

In this case, a high intensity lead with a 0.33mm diameter has an effective area of 0.0855mm2.

Selecting circuit density to be J = 3.5A / mm^2, the area of leads is:

$$S = \frac{3.84}{3.5} = 1.1mm^2$$

Thirteen leads with a 0.33mm diameter must be used.

$$Kc = \frac{38 \times 13 \times 0.0855}{132} = 0.32 << 0.35 \qquad \textit{Eqn. 1-13}$$

1.4 Drive Circuit Hardware Design

A simple and reliable gate drive circuit based on a current-limiting, single-channel driver, IC IR2125, is used, shown in **Figure 1-3**.

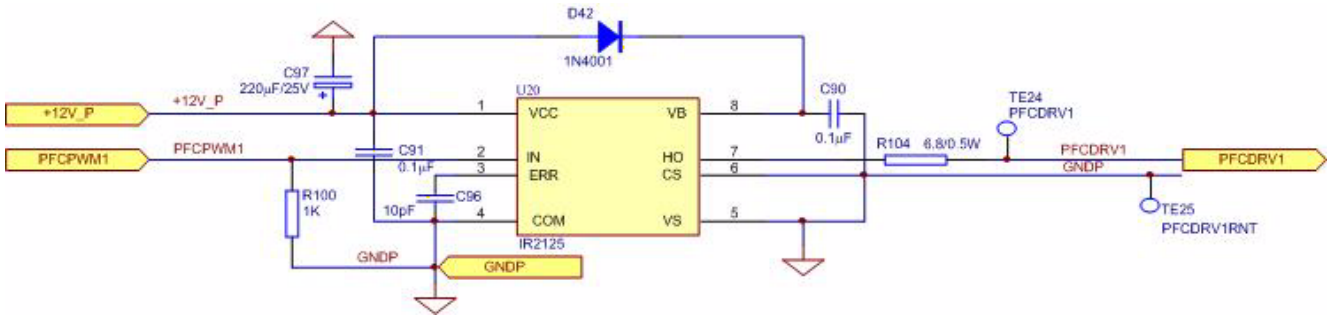


Figure 1-3. PFC Drive Circuit

1.5 Sample Circuit Hardware Design

The sample circuit of three signals, input current, (I_i), input voltage (V_i), and output bus voltage (V_{bus}), is shown in **Figure 1-4**. A simple voltage divider is used for the input voltage sample and the bus voltage sample. A current LEM HDC-15LX is used for the input current sample.

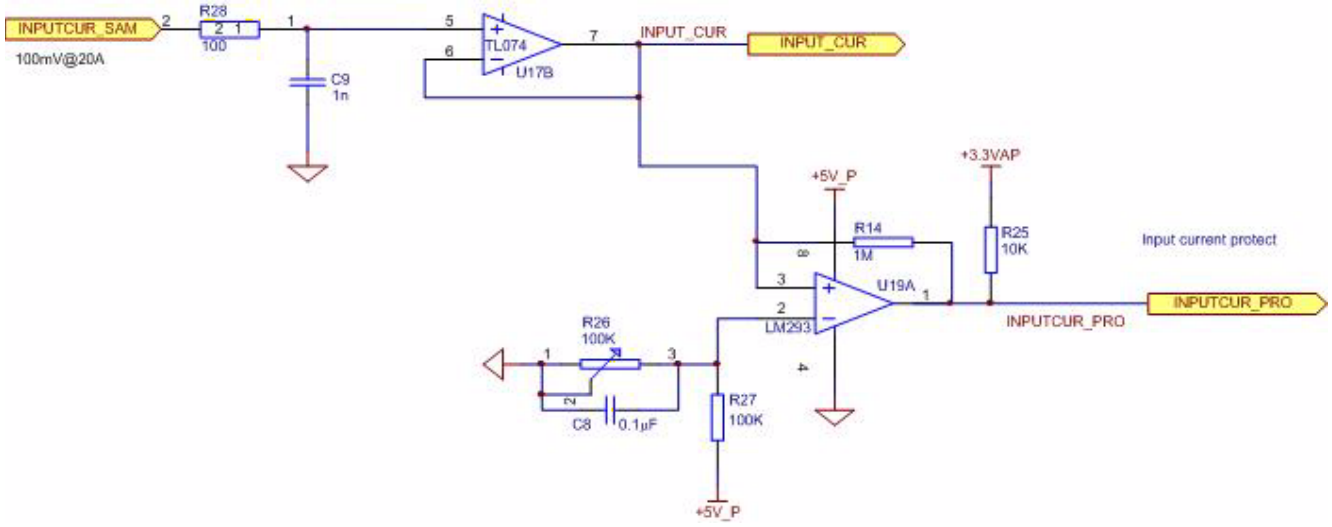


Figure 1-4. PFC Sampling Circuit

1.6 Controller Interface

The entire PFC is controlled by one 56F8323 device, which provides a complete digital solution for high-frequency Power Factor Correction. The interface between the PFC and the controller is shown in **Table 1-1**.

Table 1-1. Interface Description with the Controller (Connected to J1 of Controller)

Pin #	Name	Description	Pin#	Name	Description
J17-1A	GND_A	Analog ground	J17-1B	GND_A	Analog ground
J17-2A			J17-2B		
J17-3A	DCBUS	ADC channel #4, PFC output voltage sample	J17-3B		
J17-4A	INPUT_VOL	ADC channel #0, PFC input voltage sample	J17-4B	INPUT_CUR	ADC channel #1, PFC input current sample
J17-5A	GND_A	Analog ground	J17-5B	GND_A	Analog ground
J17-6A	GND_A	Analog ground	J17-6B	GND_A	Analog ground
J17-7A	+3.3VA	+3.3V analog power	J17-7B	+3.3VA	+3.3V analog power
J17-8A	GND_A	Analog ground	J17-8B	GND_A	Analog ground
J17-9A	GND_A	Analog ground	J17-9B	GND_A	Analog ground
J17-10A	RXD1	SCI1 receive data input	J17-10B	RXD1	SCI1 receive data input
J17-11A	TXD1	SCI1 transmit data output	J17-11B	TXD1	SCI1 transmit data output

Table 1-1. Interface Description with the Controller (Continued) (Connected to J1 of Controller)

Pin #	Name	Description	Pin#	Name	Description
J17-12A	GND_D	Digital ground	J17-12B	GND_D	Digital ground
J17-13A	GND_D	Digital ground	J17-13B	GND_D	Digital ground
J17-14A	AC_RELAY	Input relay control signal	J17-14B	AC_RELAY	Input relay control signal
J17-15A	GND_D	Digital ground	J17-15B	GND_D	Digital ground
J17-16A	NOP		J17-16B	NOP	
J17-17A	NOP		J17-17B	NOP	
J17-18A	NOP		J17-18B	NOP	
J17-19A	NOP		J17-19B	NOP	
J17-20A	PFCPWM2	PWM output for PFC control	J17-20B	PFCPWM2	PWM output for PFC control
J17-21A	PFCPWM1	PWM output for PFC control	J17-21B	PFCPWM1	PWM output for PFC control
J17-22A	GND_D	Digital ground	J17-22B	GND_D	Digital ground
J17-23A	INPUTVOL_FRQ	Input voltage frequency	J17-23B	INPUTVOL_FRQ	Input voltage frequency
J17-24A	PONSIGNAL	Input IO port, tests the power-on signal	J17-24B	PONSIGNAL	Input IO port, tests the power-on signal
J17-25A	GND_D	Digital ground	J17-25B	GND_D	Digital ground
J17-26A	NOP		J17-26B	NOP	
J17-27A	INPUTCUR_PRO	FAULTA1, masks PWM output if PFC input is overcurrent	J17-27B	INPUTCUR_PRO	FAULTA1, masks PWM output if PFC input is overcurrent
J17-28A	GND_D	Digital ground	J17-28B	GND_D	Digital ground
J17-29A	NOP		J17-29B	NOP	
J17-30A	GND_D	Digital ground	J17-30B	GND_D	Digital ground
J17-31A	GND_D	Digital ground	J17-31B	GND_D	Digital ground
J17-32A	+5V_DSP	+5V digital power	J17-32B	+5V_DSP	+5V digital power

Chapter 2
Hardware Design of a DC/DC Converter System

2.1 Requirements

This section contains information about the design of the DC/DC converter system. Specifications and performance include:

Input voltage:	300~380V DC output by PFC
Output voltage:	48V, precision: 3%, ripple: 500mV
Rating output power:	500W
Switch frequency:	150K

2.2 System Design

A phase-shifted, full-bridge DC/DC converter combines the advantages of quasi-resonant technology and traditional PWM technology. It has fixed frequency, utilizes Inductor Capacitance (LC) resonant energy to realize the main switches' ZVS, then utilizes PWM technology to transfer energy. Its advantages include control, limited switching loss, and high reliability. In addition, this system adopts a current doubler with a synchronous rectifier rather than a traditional full-wave rectifier, which adds several advantages, such as limited duty loss, no reverse recovery and less difference required to realize ZVS between two legs.

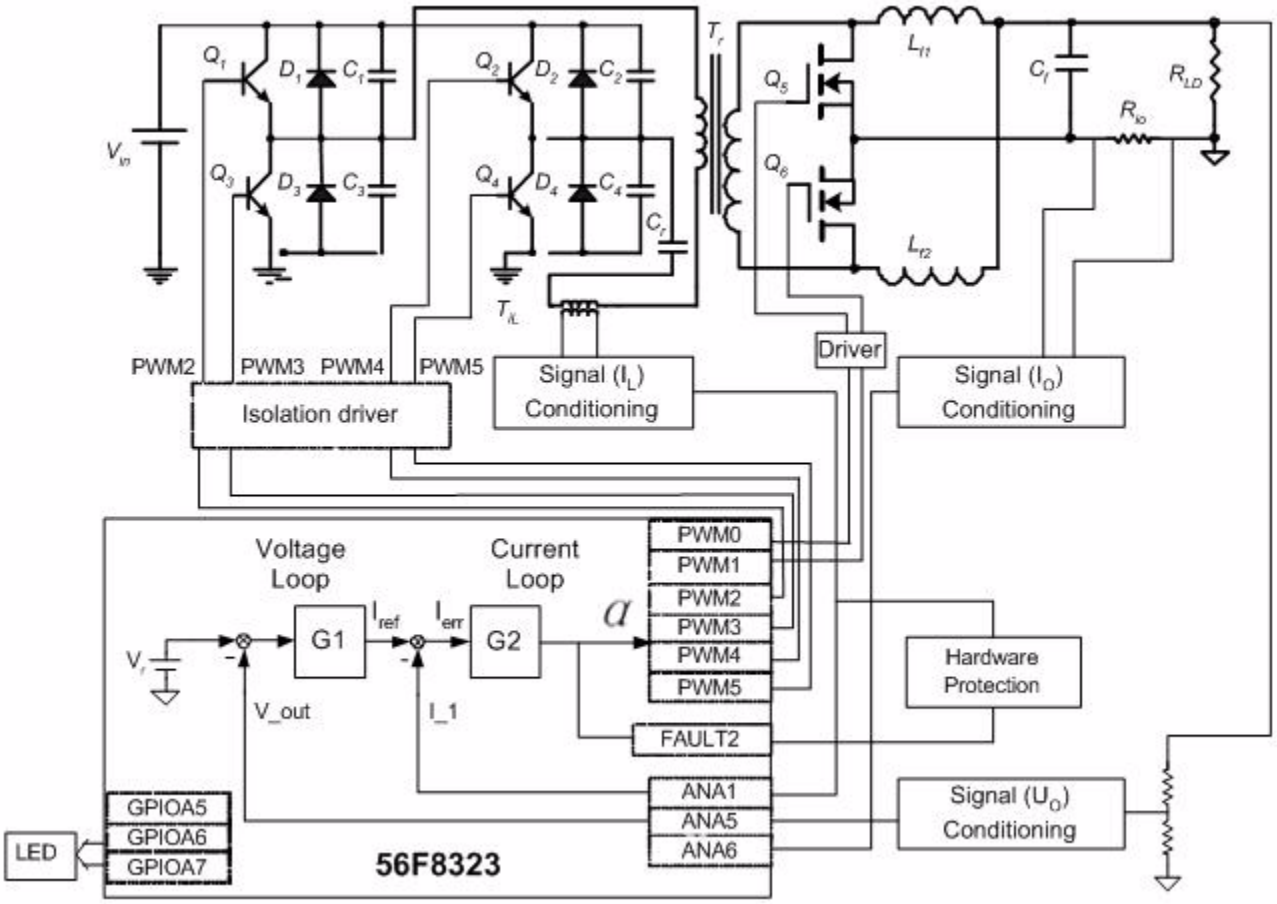


Figure 2-1. DC/DC System Design

2.3 Main Circuit Hardware Design

The DC/DC system design is shown in **Figure 2-2**. The topology of the main circuit is a phase-shifted, full-bridge converter, including four MOSFET (Q_1—Q_4), a transformer (T_r), capacitance (C_r) to prevent saturation of the transformer, secondary synchronous rectifier (Q_5 and Q_6), filter inductors (L_{f1} and L_{f2}) and output filter capacitance (C_f). Three signals, inductance current (I_L), output voltage (V_o), and output current (I_o), are sampled and sent to the 56F8323 device.

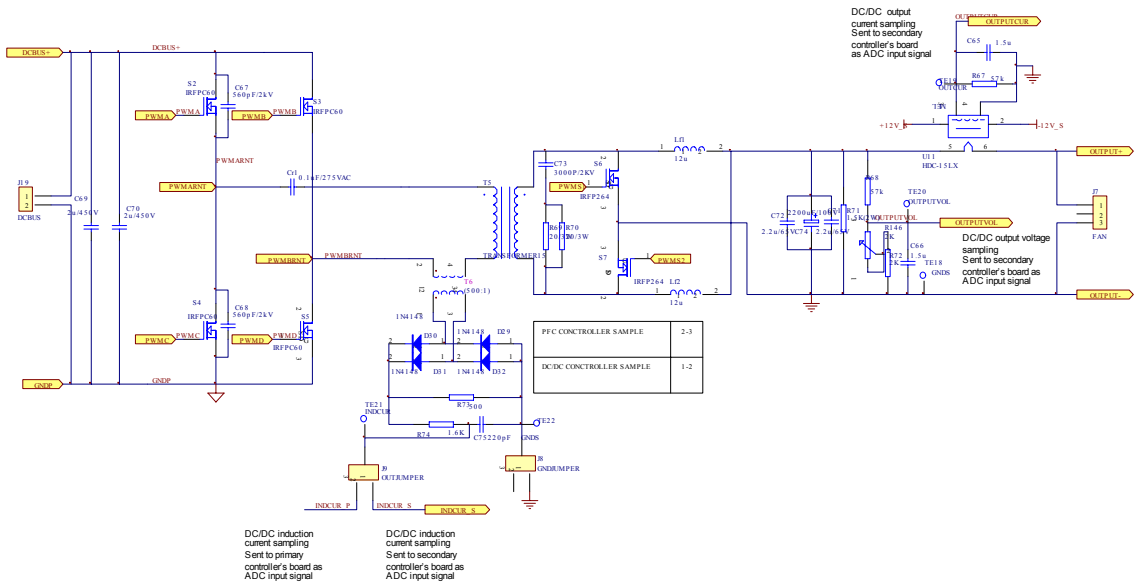


Figure 2-2. DC/DC Main Circuit

2.3.1 Main Switch

The voltage stress of the main switch is:

$$V_{CEM(S)} > 1.5V_{cem(S)} = 1.5V_{in\,(max)} = 1.5 \times 380 = 570V \qquad \textit{Eqn. 2-1}$$

The main switch's current stress is calculated by RMS value:

$$I_{CEM\,(S)} > 4I_{cem(s)} = 4 \times \frac{P_{o(\max)}}{\eta V_{in(\min)}} = 4 \times \frac{500}{0.9 \times 300} = 7.4A \qquad \textit{Eqn. 2-2}$$

Select switch S_1—S_4 to be MOSFET IRFPC60LC.

Parameters are:

- V_{DSS} = 600V
- I_D = 16A
- $R_{DS(on)tye}$ = 0.4Ω
- TO-247 AC package

2.3.2 Transformer's Turns Ratio

Taking into account the duty ratio loss of the secondary side, select the secondary side's maximum duty ratio to be 0.85. The secondary side's minimum voltage can then be calculated as follows:

$$V_{\text{sec(min)}} = \frac{V_{o\,(\max)} + V_D + V_{Lf}}{D_{\text{sec(max)}}} = \frac{52 + 1.5 + 0.5}{0.8} = 67.5V$$

Eqn. 2-3

Where:

$V_{o(max)}$ is the maximum output voltage

V_D is the output diode's forward voltage

V_{Lf} is the output filter inductor's voltage drop

The transformer's turns ratio is:

$$n = \frac{300}{67.5} = 4.4$$

Select the transformer's turns ration to be n = 4.

2.3.3 Resonance Inductor

In order that the zero voltage switch of the lag bridge be achieved, **Equation 2-4** must be satisfied:

$$\frac{1}{2} L_r I^2 = \frac{4}{3} C_{DS} V_{in}^2$$

Eqn. 2-4

Where:

L_r is the resonance inductor

I is the primary circuit current when the switch of the lag bridge is closed

C_{DS} is the drain to source capacitance of MOSFET

The factors below should be considered when resonance indicator, L_r, is selected:

- In order that zero voltage switch is sure to properly handle V_{in}, V_{in} should be calculated by $V_{in(max)}$
- The zero voltage switch occurs when the load is beyond 0.7 of full load
- When the load circuit is 1.04A (10% of full load circuit), the circuit of inductor L_f is in critical current mode, so pulse current Δi_{Lf} is 2.08A

When load is 0.7 of full load:

$$I = \frac{0.7 I_{o\,(\max)} + \Delta i_{Lf} / 2}{n} = \frac{0.7 \times 10.4 + 1.04}{4} = 2.08A$$

Eqn. 2-5

The drain to source capacitance of IRFBC30 is C_{DS} = 360pF.

$V_{in(max)}$ = 380V

According to **Equation 2-4**, L_r = 30μH.

2.3.4 Transformer

2.3.4.1 Number of Turns

If magnetic core is selected to be EI40 and the maximum magnetic flux density is determined to be B_m = 0.10T, then the turns of the secondary side W_{sec} can be calculated as follows:

$$W_{\text{sec}} = \frac{V_{\text{sec(min)}} \bullet D_{\text{sec(max)}}}{4 f_s A_e B_m}$$

Eqn. 2-6

Where:

The effective area of magnetic core is A_e = 138mm^2

$D_{sec(max)}$ = 1 - 0.15 = 0.85

$$V_{\text{sec(min)}} = \frac{V_{in(\text{min})}}{n} = \frac{300}{4} = 75V$$

According to **Equation 2-5**, W_{sec} = 6.2

If the secondary side's number of turns is selected to be W_{sec} = 6, the primary side's number of turns is W_p = 24.

2.3.4.2 Lead Diameter and the Primary Winding's Number of Leads

When transformer's PWM frequency is 150kHz, the penetration depth of the copper lead is:

$$\Lambda = \sqrt{\frac{2}{2\pi f_s \mu \gamma}} = \sqrt{\frac{1}{3.14 \times 150 \times 10^3 \times 1.25 \times 10^{-6} \times 58 \times 10^6}} = 0.171mm$$

Eqn. 2-7

Where:

γ is the electric conductive ratio of lead

μ is the magnetic conductive ratio of lead

A copper lead with a diameter smaller than 0.34mm can be selected. In this case, high-intensity lead with a 0.33mm diameter is selected; the effective area is 0.0855mm^2.

The primary winding's maximum circuit is:

$$I_{p(\max)} = \frac{P_{o(\max)}}{\eta_{tr} V_{in(\text{min})}}$$

Eqn. 2-8

If the transformer's maximum output power is $P_{o(maximal)}$ = 500W, suppose that the efficiency of the transformer is n_{tr} = 0.98. According to **Equation 2-8**, $I_{p(max)}$ = 2.04A; select circuit density to be J = 3.5A/mm^2 and the primary side's area of leads is:

$$S_p = \frac{2.04}{3.5} = 0.583mm^2$$

Seven leads with a 0.33mm diameter must be used.

2.3.4.3 The Secondary Winding's Number of Leads

There are two secondary windings which compose a double half-wave commutator, so the maximum RMS current of the secondary side is:

$$I_{s\,(max)} = 10.4 \Big/ \sqrt{2} = 7.35A$$

If the circuit density is selected to be J = 3.5A/mm^2, the secondary side's effective area of leads is:

$$S_S = \frac{7.35}{3.5} = 2.1mm^2$$

Twenty-five leads with a 0.33mm diameter must be used.

2.3.4.4 Check the Window's Filling Factor

The window area of EI40 is S_c = 155.4mm^2, so the window's filling factor is:

$$Kc = \frac{24 \times 7 \times 0.0855 + 2 \times 6 \times 25 \times 0.0855}{155.4} = 0.26$$

Eqn. 2-9

2.3.5 Resonance Inductor Design

As shown in **Section 2.3.3**, L_r = 30μH.

The maximum current of L_r is:

$$I_{Lr(\max)} = \frac{I_{o(\max)} + \frac{1}{2}\Delta I_{\max}}{n} = \frac{10.4 + \frac{1}{2} \times 2.08}{4} = 2.86A$$

Eqn. 2-10

Select the magnetic core to be EE25, with an effective area of 42.2mm^2.

Select the gap length to be δ = 1.2mm.

The value of the resonance inductor winding can be calculated as follows:

$$N = \sqrt{\frac{L \cdot \delta}{\mu \cdot Ae}} = 26.06$$

Eqn. 2-11

Select N = 26.

Check the maximum magnetic flux density:

$$Bm = \frac{\mu N \, \mathrm{Im}\, ax\sqrt{2}}{\delta} = 0.096T < 0.2T$$

Eqn. 2-12

Since the circuit of the resonance inductor is equivalent to the circuit of the transformer's primary side, the diameter of the lead and the number of windings can be selected to be the same as the transformer's primary side. According to **Section 2.3.4**, seven leads with a 0.33mm diameter can be used. Finally, check the window's fulfilling ratio as follows:

$$Kc = \frac{26 \times 7 \times 0.0855}{81.94} = 0.19 << 0.35$$

Eqn. 2-13

2.3.6 Output Filter Inductor Design

The output filter inductor can be calculated by the following formula:

$$L_f = \frac{V_{o(\min)}}{2 \times (2 f_s) \bullet (10\% I_{o(\max)})} [1 - \frac{V_{o(\min)}}{\frac{V_{in(\max)}}{n} - V_{Lf} - V_D}]$$

Eqn. 2-14

Where:

$V_{o(min)}$ = 35V

$I_{o(max)}$ = 10.4A

$V_{in(max)}$ = 380V

N = 4

V_{Lf} = 0.5V

V_D = 1.5V

According to **Equation 2-14**, L_f = 35μH.

The maximum circuit of L_f is:

$$I_{Lf(\max)} = I_{o(\max)} + \frac{1}{2}\Delta I_{\max} = 10.4 + \frac{1}{2} \times 2.08 = 11.44A$$

Eqn. 2-15

Select magnetic core to be Ei30.

Select the maximum magnetic flux density B_m = 0.40T.

The turns of the output filter inductor can be calculated as follows:

$$N = \frac{L_r I_{Lr(\max)}}{A_e B_m} = \frac{35 \times 11.44}{111 \times 0.4} = 9.5$$

Eqn. 2-16

If N = 10, the gap is:

$$\delta = \frac{\mu_o N^2 A_e}{L_r} = \frac{1.25\times10^{-6}\times10^2\times111\times10^{-6}}{35\times10^{-6}} = 0.3mm$$

Eqn. 2-17

The maximum RMS circuit of the output filter inductor is 10.4A.

Select the circuit density to be J = 3.5A/mm^2, and the winding's area of leads is:

$$S_{Lf} = \frac{10.4}{3.5} = 2.97mm^2$$

Thirty-five leads with a 0.33mm diameter must be used.

The effective area of EI30 is S_c = 132mm^2.

Finally, check the window's fulfilling ratio as follows:

$$Kc = \frac{13\times35\times0.0855}{132} = 0.295 < 0.35$$

Eqn. 2-18

2.3.7 Output Filter Capacitor

One 2200μF/100V output filter capacitor is used.

2.3.8 Output Diode

The output diode's voltage limit is:

$$V_{cem(DR)} = 2V_{in(\max)} / n = 2\times380/4 = 190V$$

Eqn. 2-19

The diode's maximum circuit is:

$$I_{DR(\max)} = I_{o(\max)} + \frac{1}{2}\Delta I_{Lf} = 10.4 + \frac{1}{2}\times1.04 = 10.9A$$

Eqn. 2-20

An ultrafast recovery diode, 60CTQ150, produced by IR Corporation, has been selected for this application.

Parameters are:

- $I_{F(AV)}$ = 60A
- V_{RRM} = 400V
- V_{fm} = 0.93V

2.4 Sample Circuit Hardware Design

The output voltage sample circuit is composed of a simple voltage divider and a voltage follower circuit, shown in **Figure 2-3**.

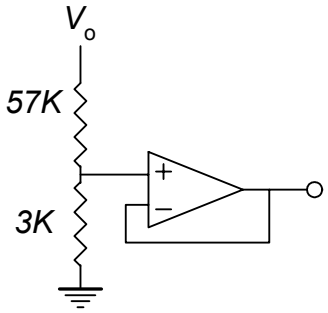


Figure 2-3. Output Voltage Sample Circuit

As the resonance inductance current i_L is an AC quantity, one current transformer can be used for the inductance current sample. The inductance current sample circuit is shown in **Figure 2-4**. Ds_1~Ds_4 compose a full-bridge rectifier. Rs_1 is a sample resistor. Rs_2 is used for current limiting.

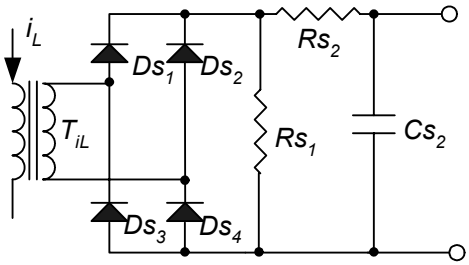


Figure 2-4. Inductance Current Sample Circuit

The output current can be sensed by a current LEM HDC-15LX.

2.5 Drive Circuit Hardware Design

A simple and reliable isolated gate drive circuit is used for each MOSFET, shown in **Figure 2-5**. Only one +12V DC power supply is needed for the four driver circuits.

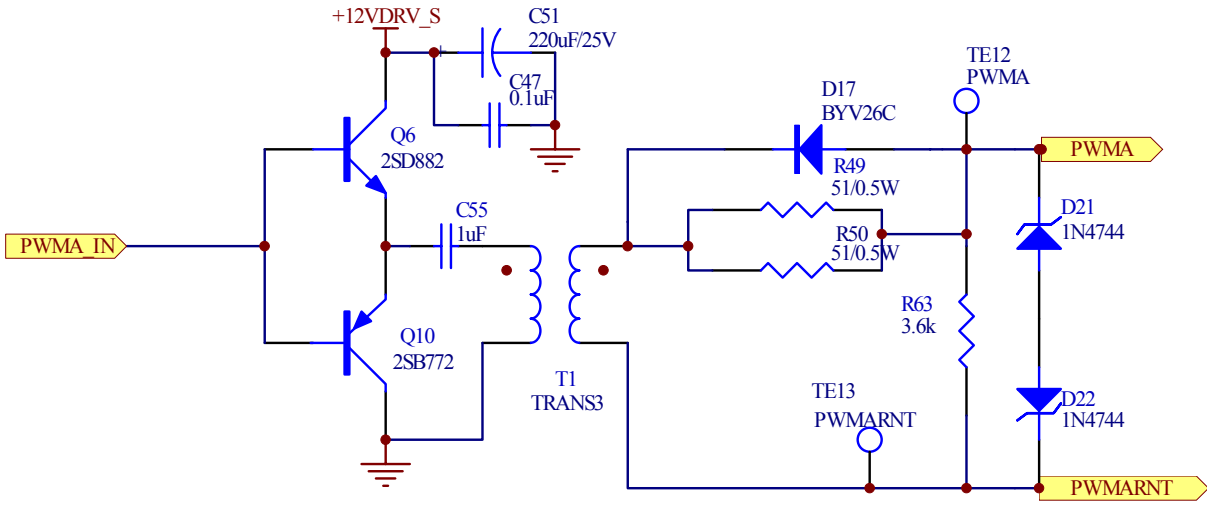


Figure 2-5. Output Voltage Driver Circuit

2.6 Optocoupler Isolation Drive Circuit Hardware Design

Transformer isolation is a convenient solution for the 50% duty signal output. When the duty signal varies, optocoupler isolation is a suitable solution. The HCPL2611 optocoupler is used for isolation and the TC4420 is a special driver IC for MOSFET.

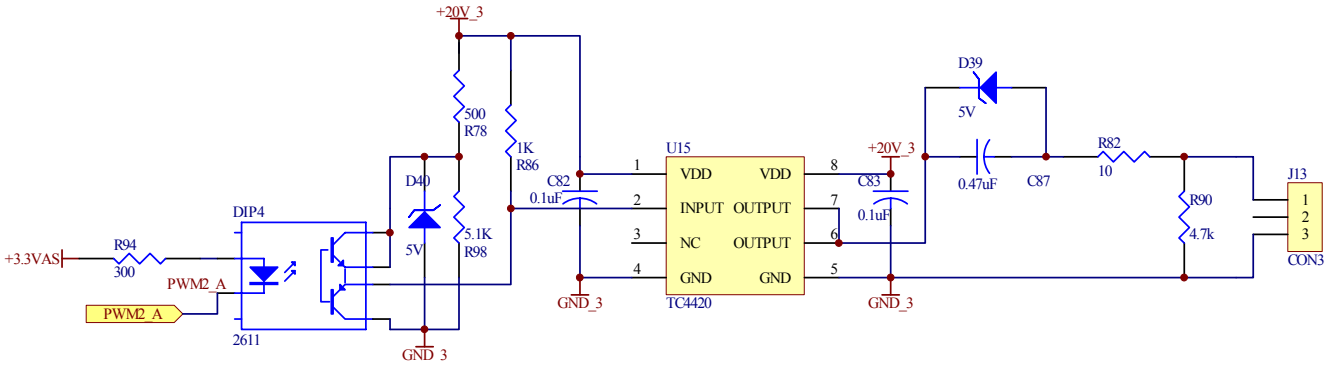


Figure 2-6. Output Voltage Driver Circuit

2.7 Controller Interface

All DC/DC conversion is controlled by one chip, the 56F8323, which provides a full digital solution for high-frequency DC/DC conversion. The interface between the PFC power system and the controller is shown in Table 2-1.

Table 2-1. Interface Description with the Controller (Connected to J1 of Controller)

Pin #	Name	Description	Pin#	Name	Description
J16-1A	GND_A	Analog ground	J16-1B	GND_A	Analog ground
J16-2A	OUTPUT_CUR	ADC channel #6, DC/DC output current sample	J16-2B	OUTPUT_VOL	ADC channel #5, DC/DC output voltage sample
J16-3A			J16-3B	IND_CUR	ADC channel #2, DC/DC induction current sample
J16-4A			J16-4B		
J16-5A	GND_A	Analog ground	J16-5B	GND_A	Analog ground
J16-6A	GND_A	Analog ground	J16-6B	GND_A	Analog ground
J16-7A	+3.3VA	+3.3V analog power	J16-7B	+3.3VA	+3.3V analog power
J16-8A	GND_A	Analog ground	J16-8B	GND_A	Analog ground
J16-9A	GND_A	Analog ground	J16-9B	GND_A	Analog ground
J16-10A	RXD1	SCI1 receive data input	J16-10B	RXD1	SCI1 receive data input
J16-11A	TXD1	SCI1 transmit data output	J16-11B	TXD1	SCI1 transmit data output
J16-12A	GND_D	Digital ground	J16-12B	GND_D	Digital ground
J16-13A	GND_D	Digital ground	J16-13B	GND_D	Digital ground
J16-14A			J16-14B		
J16-15A	GND_D	Digital ground	J16-15B	GND_D	Digital ground
J16-16A	PWM4_S	PWM output for DC/DC control	J16-16B	PWM4_S	PWM output for DC/DC control
J16-17A	PWM3_S	PWM output for DC/DC control	J16-17B	PWM3_S	PWM output for DC/DC control
J16-18A	PWM2_S	PWM output for DC/DC control	J16-18B	PWM2_S	PWM output for DC/DC control
J16-19A	PWM1_S	PWM output for DC/DC control	J16-19B	PWM1_S	PWM output for DC/DC control
J16-20A	PWM6_S	PWM output for synchronized control	J16-20B		
J16-21A	PWM5_S	PWM output for synchronized control	J16-21B		
J16-22A	GND_D	Digital ground	J16-22B	GND_D	Digital ground

Table 2-1. Interface Description with the Controller (Continued) (Connected to J1 of Controller)

Pin #	Name	Description	Pin#	Name	Description
J16-23A			J16-23B		
J16-24A			J16-24B		
J16-25A	GND_D	Digital ground	J16-25B	GND_D	Digital ground
J16-26A	INDCUR_PRO	FAULTA2, masks PWM output if DC/DC inductance is overcurrent	J16-26B	INDCUR_PRO	FAULTA2, masks PWM output if DC/DC inductance is overcurrent
J16-27A			J16-27B		
J16-28A	GND_D	Digital ground	J16-28B	GND_D	Digital ground
J16-29A			J16-29B		
J16-30A	GND_D	Digital ground	J16-30B	GND_D	Digital ground
J16-31A	GND_D	Digital ground	J16-31B	GND_D	Digital ground
J16-32A	+5V_DSP	+5V digital power	J16-32B	+5V_DSP	+5V digital power

Chapter 3
Controller Board Hardware Architecture

3.1 Introduction

The system consists of two parts: a Power Factor Correction (PFC) circuit and a DC/DC conversion circuit. The controller's boards used to control these two subsystems are the same. This section details the hardware design of the controller's board.

The controller board comprises these components:

- Control system circuit
- CPU circuit
- ADC circuit
- Power supply circuit
- DAC circuit
- LED display circuit
- Signals output interface

3.2 Control System Circuit

The system circuit shows the connection between key components and the pin-out arrangement.

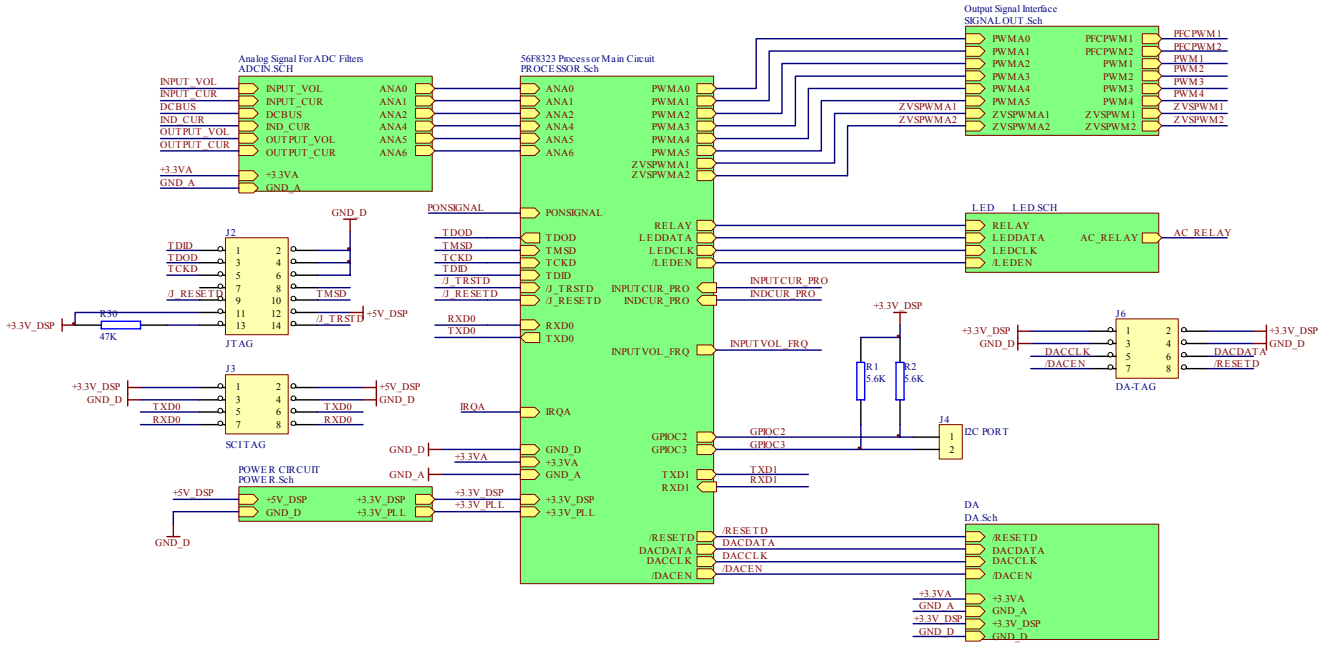


Figure 3-1. Connection Between Subsystems

Table 3-1. Controller Board Pin-Out Description (Connected to J16 and J17 of the Power Board)

Pin #	Name	Description	Pin#	Name	Description
J1-1A	GND_A	Analog ground	J1-1B	GND_A	Analog ground
J1-2A	OUTPUT_CUR	ADC channel #6, DC/DC output current sample	J1-2B	OUTPUT_VOL	ADC channel #5, DC/DC output voltage sample
J1-3A	DCBUS	ADC channel #4, PFC output voltage sample	J1-3B	IND_CUR	ADC channel #2, DC/DC induction current sample
J1-4A	INPUT_VOL	ADC channel #0, PFC input voltage sample	J1-4B	INPUT_CUR	ADC channel #1, PFC input current sample
J1-5A	GND_A	Analog ground	J1-5B	GND_A	Analog ground
J1-6A	GND_A	Analog ground	J1-6B	GND_A	Analog ground
J1-7A	+3.3VA	+3.3V analog power	J1-7B	+3.3VA	+3.3V analog power
J1-8A	GND_A	Analog ground	J1-8B	GND_A	Analog ground
J1-9A	GND_A	Analog ground	J1-9B	GND_A	Analog ground
J1-10A	RXD1	SCI1 receive data input	J1-10B	RXD1	SCI1 receive data input
J1-11A	TXD1	SCI1 transmit data output	J1-11B	TXD1	SCI1 transmit data output
J1-12A	GND_D	Digital ground	J1-12B	GND_D	Digital ground
J1-13A	GND_D	Digital ground	J1-13B	GND_D	Digital ground
J1-14A	AC_RELAY	Input relay control signal	J1-14B	AC_RELAY	Input relay control signal
J1-15A	GND_D	Digital ground	J1-15B	GND_D	Digital ground
J1-16A	PWM4	PWM output for DC/DC control	J1-16B	PWM4	PWM output for DC/DC control
J1-17A	PWM3	PWM output for DC/DC control	J1-17B	PWM3	PWM output for DC/DC control
J1-18A	PWM2	PWM output for DC/DC control	J1-18B	PWM2	PWM output for DC/DC control
J1-19A	PWM1	PWM output for DC/DC control	J1-19B	PWM1	PWM output for DC/DC control
J1-20A	PFCPWM2	PWM output for PFC control	J1-20B	ZVSPWM2	PWM output for synchronized control
J1-21A	PFCPWM1	PWM output for PFC control	J1-21B	ZVSPWM1	PWM output for synchronized control
J1-22A	GND_D	Digital ground	J1-22B	GND_D	Digital ground
J1-23A	INPUTVOL_FRQ	Input voltage frequency	J1-23B	INPUTVOL_FRQ	Input voltage frequency
J1-24A	PONSIGNAL	Input IO port, tests the power-on signal	J1-24B	PONSIGNAL	Input IO port, tests the power-on signal
J1-25A	GND_D	Digital ground	J1-25B	GND_D	Digital ground

Table 3-1. Controller Board Pin-Out Description (Continued) (Connected to J16 and J17 of the Power Board)

Pin #	Name	Description	Pin#	Name	Description
J1-26A	INDCUR_PRO	FAULTA2, masks PWM output if DC/DC inductance is overcurrent	J1-26B	INDCUR_PRO	FAULTA2, masks PWM output if DC/DC inductance is overcurrent
J1-27A	INPUTCUR_PRO	FAULTA1, masks PWM output if PFC input is overcurrent	J1-27B	INPUTCUR_PRO	FAULTA1, masks PWM output if PFC input is overcurrent
J1-28A	GND_D	Digital ground	J1-28B	GND_D	Digital ground
J1-29A	IRQA	External interrupt request A	J1-29B	IRQA	External interrupt request A
J1-30A	GND_D	Digital ground	J1-30B	GND_D	Digital ground
J1-31A	GND_D	Digital ground	J1-31B	GND_D	Digital ground
J1-32A	+5V_DSP	+5V digital power	J1-32B	+5V_DSP	+5V digital power

Table 3-2. JTAG Interface Pin-Out Description (Connected to J204 of the Communication Board)

Pin #	Name	Description	Pin#	Name	Description
J2-1	TDID	Test Data Input	J2-2	GND_D	Digital ground
J2-3	TDOD	Test Data Output	J2-4	GND_D	Digital ground
J2-5	TCKD	Test Clock Input	J2-6	GND_D	Digital ground
J2-7	NOP		J2-8	NOP	
J2-9	/J_RESETD	Reset	J2-10	TMSD	Test Mode Select Input
J2-11	+3.3V_DSP	+3.3V digital power	J2-12	+5V_DSP	+5V digital power
J2-13	PULLUP	+3.3V Pull-up pin	J2-14	/J_TRSTD	Test Reset

Table 3-3. SCI Interface Pin-Out Description (Connected to J201 of the Communication Board)

Pin #	Name	Description	Pin#	Name	Description
J3-1	+3.3V_DSP	+3.3V digital power	J3-2	+5V_DSP	+5V digital power
J3-3	GND_D	Digital ground	J3-4	GND_D	Digital ground
J3-5	TXD0	SCI0 transmit data output	J3-6	TXD0	SCI0 transmit data output
J3-7	RXD0	SCI0 receive data output	J3-8	RXD0	SCI0 receive data output

Table 3-4. DAC Debug Interface Pin-Out Description (Debug purpose only)

Pin #	Name	Description	Pin#	Name	Description
J3-1	+3.3V_DSP	+3.3V digital power	J3-2	+5V_DSP	+5V digital power
J3-3	GND_D	Digital ground	J3-4	GND_D	Digital ground
J3-5	DACCLK	DAC clock signal	J3-6	DACDATA	DAC data signal
J3-7	/DACEN	DAC enable signal	J3-8	/RESETD	DAC reset signal

3.3 CPU Circuit

This circuit shows the signal connections around the controller.

PWMA0 and PWMA1 are used for PFC control; PWMA2, PWMA3, PWMA4 and PWMA5 are used for DC/DC control. FAULTA1 and FAULTA2 are used for hardware protection. If the current through PFC input inductance is too large, FAULTA1 will be high, which indicates than an overcurrent fault has occurred, and the PWM outputs will be masked. If the current through DC/DC primary side inductance is too large, FAULTA2 will be high and the PWM outputs will be masked.

ANA0, ANA1, ANA2, ANA4, ANA5 and ANA6 are used to sample analog signals. ANA7 is used for ADC test.

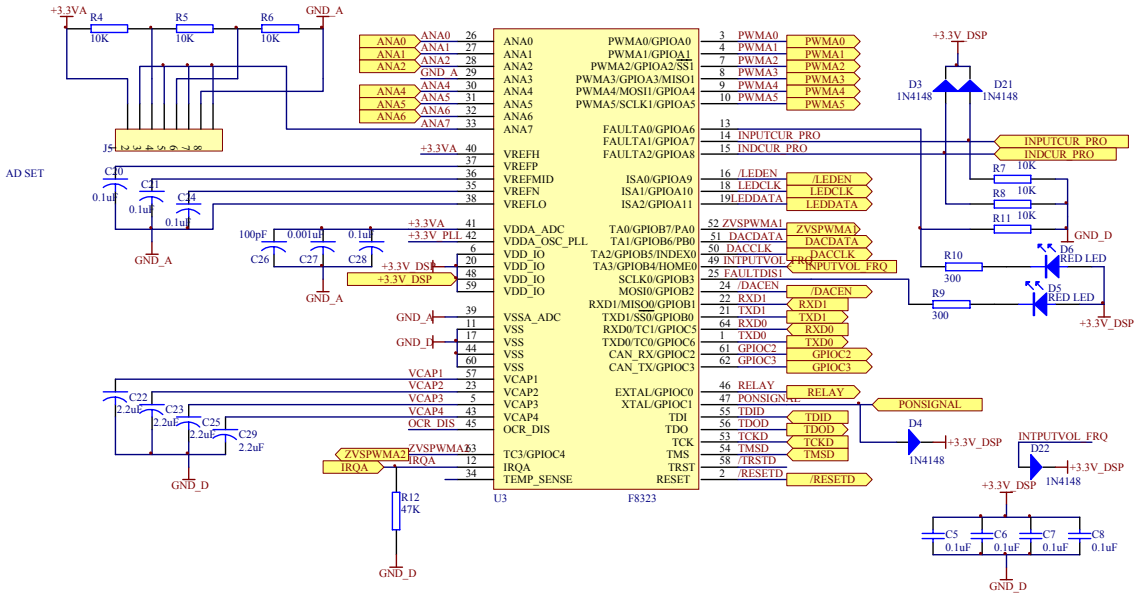


Figure 3-2. CPU Circuit

Table 3-5 shows the resources of General Purpose Inputs/Outputs (GPIOs).

Table 3-5. GPIO Resources

PIN#	Name	Description
GPIOC0	RELAY	Relay on control signal; if high, the relay is closed
GPIOB6	DACDATA	DAC control signals
GPIOB5	DACCLK	
GPIOB2	/DACEN	
GPIOA11	LEDDATA	LED control signals
GPIOA10	LEDCLK	
GPIOA9	/LEDEN	
GPIOB2	FAULTDIS3	Fault display
GPIOB3	FAULTDIS2	
GPIOB4	FAULTDIS1	
GPIOC2	GPIOC2	I^2C reserved ports
GPIOC3	GPIOC3	
GPIOC1	PONSIGNAL	Tests the power-on signal

Figure 3-3 shows the reset circuit. If S1 is pressed, /RESETD and /TRSTD become low, resetting both the device and the JTAG.

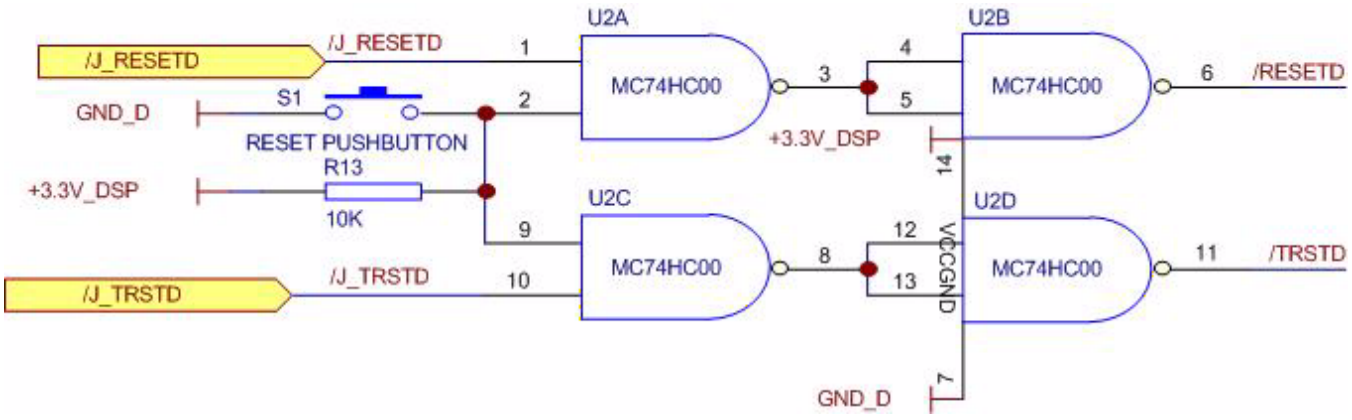


Figure 3-3. Reset Circuit

3.4 ADC Circuit

The ADC circuit filters the analog signals for sampling. There are six analog signals: three for PFC control and three for DC/DC control.

Table 3-6. ADC Resource Configuration

PIN#	Name	Description
ANA0	INPUT_VOL	Input voltage sample
ANA1	INPUT_CUR	Input current sample
ANA2	IND_CUR	DC/DC inductance current sample
ANA3	GND_A	GND
ANA4	DCBUS	DCBus sample
ANA5	OUTPUT_VOL	Output voltage sample
ANA6	OUTPUT_CUR	Output current sample
ANA7	CONFIG	Reserved for software configuration

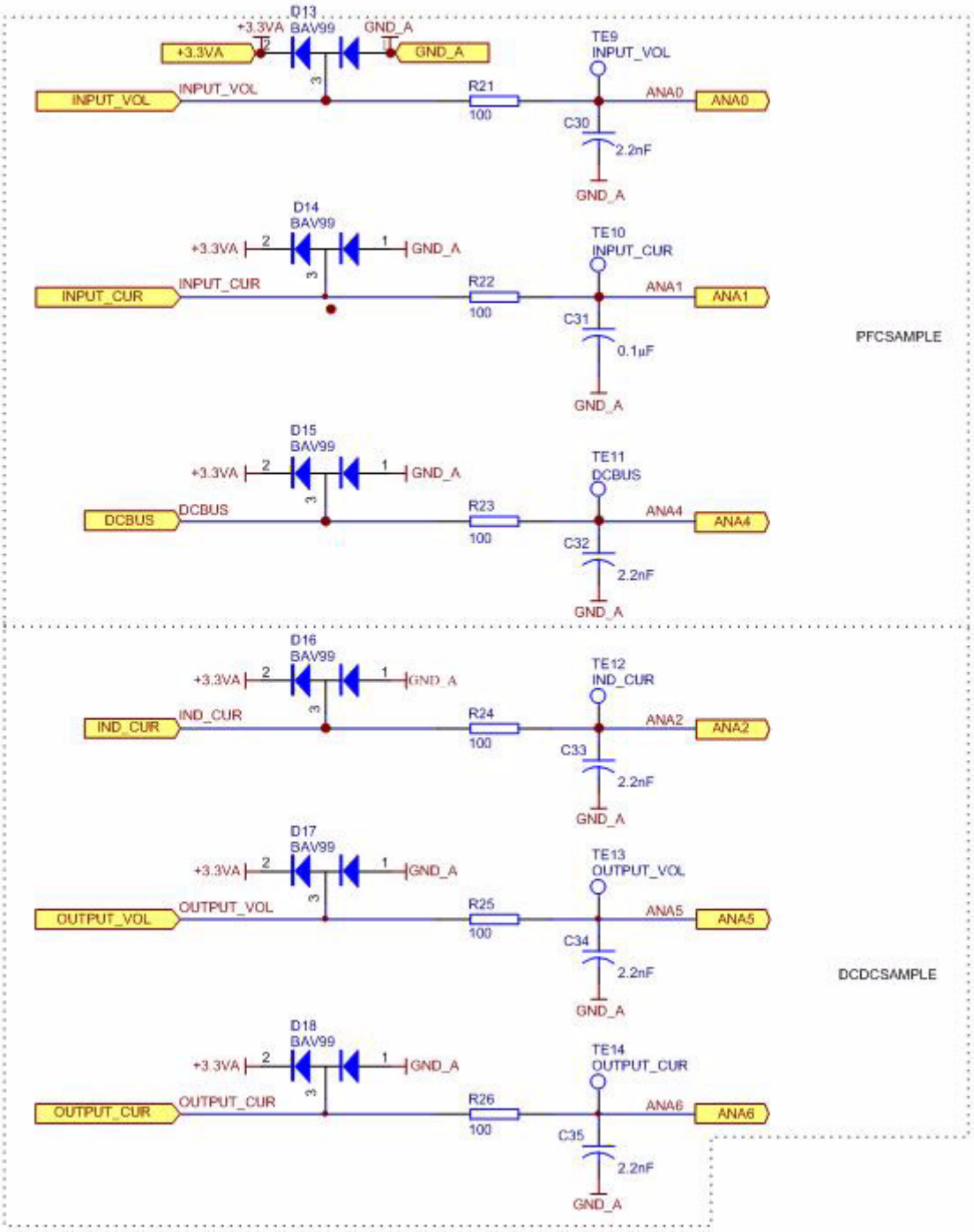


Figure 3-4. ADC Input Circuit

3.5 Power Supply Circuit

The power supply circuit changes +5V DC to +3.3V regulated DC power, used to power the device.

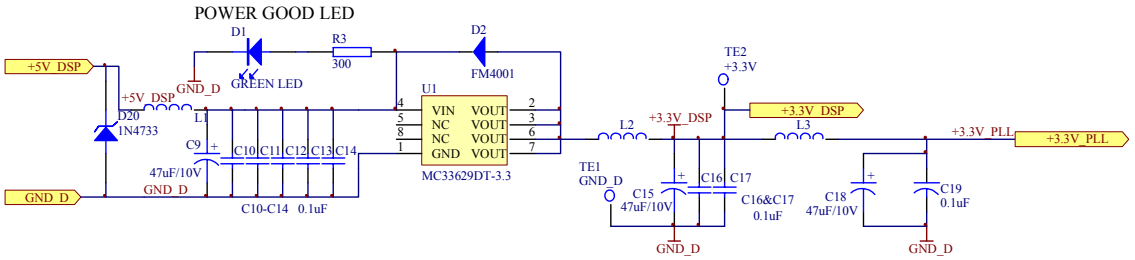


Figure 3-5. Power Supply Circuit

3.6 DAC Circuit

The DAC circuit has no control function and is used only to debug the system.

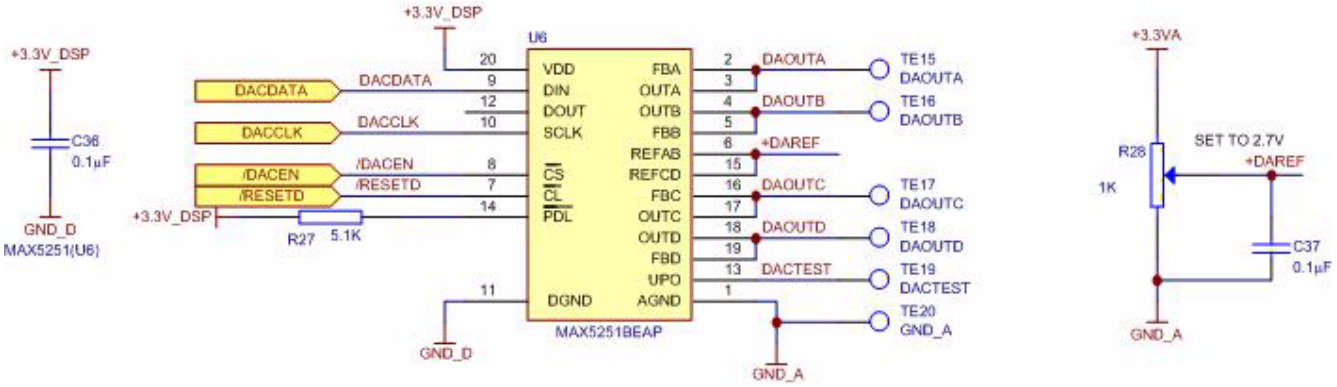


Figure 3-6. DAC Circuit

3.7 LED Display Circuit

This circuit displays the system parameters, such as input voltage, input current, output voltage, output current, and so on.

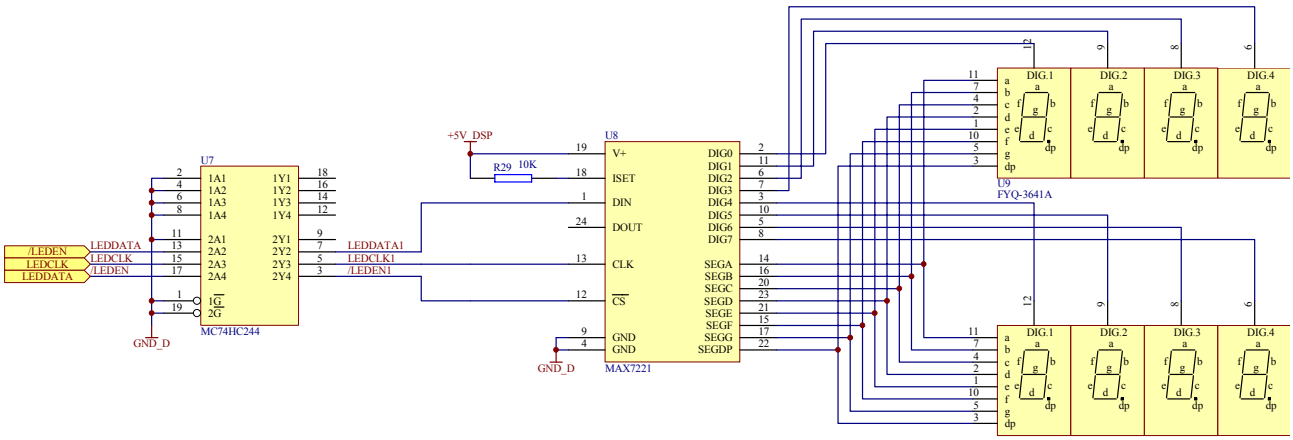


Figure 3-7. LED Display Circuit

3.8 Signals Output Interface

This interface changes the +3.3V level voltage to the +5V level.

Table 3-7. PWM Resources Configuration

Pin #	PFC Part	Descriptions	DC/DC Part	Descriptions
PWM0	PFCPWM1	PFC driver signals	PWM5	Synchronous driver signals
PWM1	PFCPWM2		PWM6	
PWM2			PWM1	Full bridge of DC/DC converter driver signals
PWM3			PWM2	
PWM4			PWM3	
PWM5			PWM4	
TA0	ZVSPWM1	ZVS assistant driver signals		
TC3	ZVSPWM2			

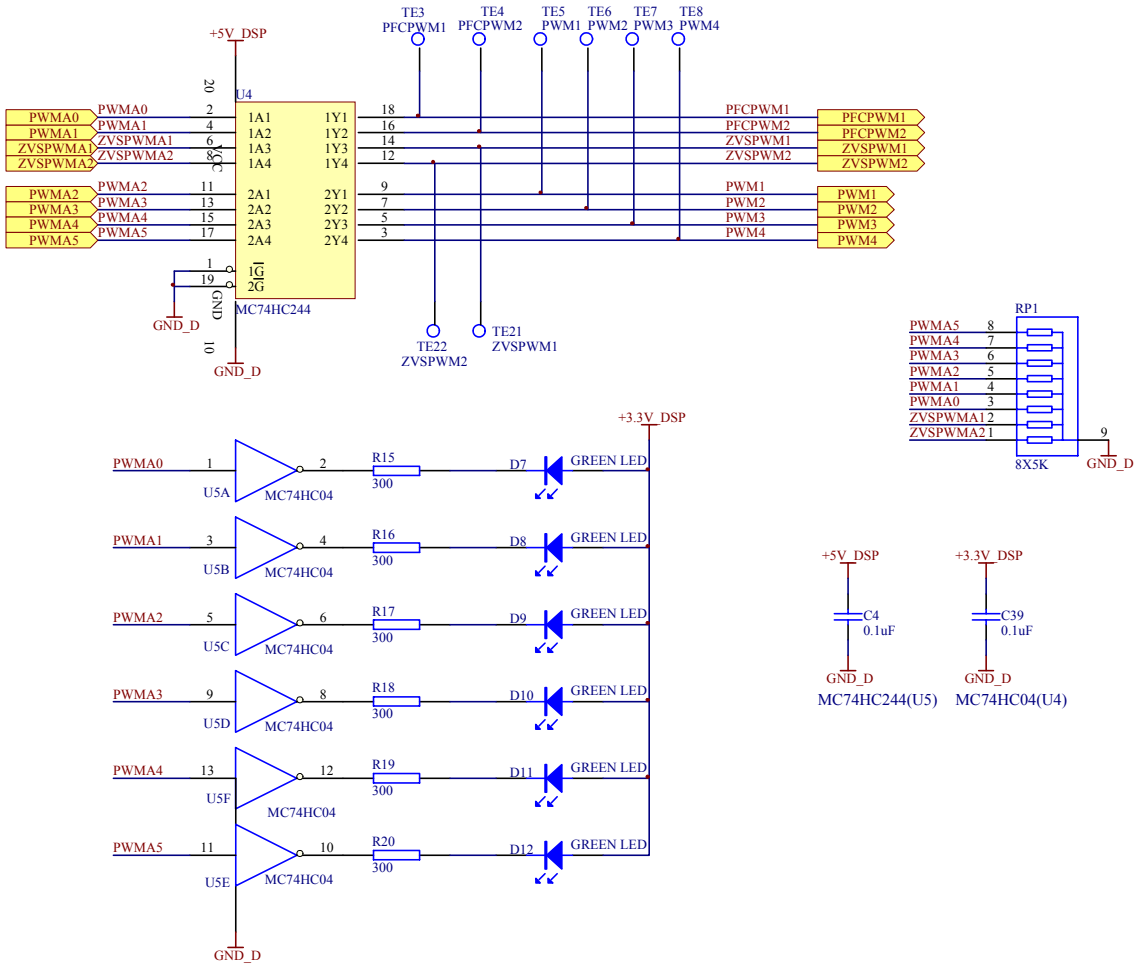


Figure 3-8. Signals Output Interface

Chapter 4
Communication Interface Board Hardware Architecture

4.1 Introduction

The communication interface board decreases the controller's size and creates a universal-purpose communication platform. This board provides mixed communication functions, such as JTAG debug and SCI interface, between the power module and the PC. At the same time it provides isolation between the power electronics and microelectronics which is needed to insure safety.

The communication system consists of two parts: the JTAG circuit and SCI. JTAG is designed for debugging and programming the device. SCI is designed for background communication to software running on the PC or for power management and supervision from an external system.

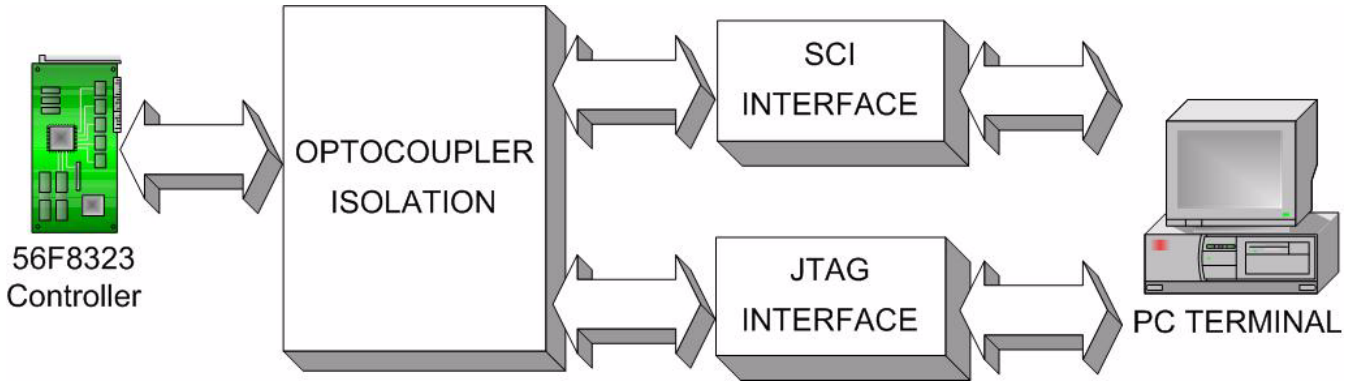


Figure 4-1. Communication Board Frame

Table 4-1. JTAG Interface Pin-Out Description (Connected to the Controller's J2)

Pin #	Name	Description	Pin#	Name	Description
J204-1	TDID1	Test Data Input	J204-2	GND_D	Digital ground
J204-3	TDOD1	Test Data Output	J204-4	GND_D	Digital ground
J204-5	TCKD1	Test Clock Input	J204-6	GND_D	Digital ground
J204-7	NOP		J204-8	NOP	
J204-9	/J_RESETD1	Reset	J204-10	TMSD1	Test Mode Select Input
J204-11	+3.3V_DSP	+3.3V digital power	J204-12	+5V_DSP	+5V digital power
J204-13	PULLUP	+3.3V Pull-up pin	J204-14	/J_TRSTD1	Test Reset

Table 4-2. SCI Interface Pin-Out Description (Connected to the Controller's J3)

Pin #	Name	Description	Pin#	Name	Description
J3-1	+3.3V_DSP	+3.3V digital power	J3-2	+5V_DSP	+5V digital power
J3-3	GND_D	Digital ground	J3-4	GND_D	Digital ground
J3-5	TXD11	SCI0 transmit data output	J3-6	TXD11	SCI0 transmit data output
J3-7	RXD11	SCI0 receive data output	J3-8	RXD11	SCI0 receive data output

4.2 Parallel JTAG Interface

Because the 56F800E core integrates the JTAG/EOnCE function, the device can be debugged and programmed by a simple interface circuit through the parallel port without any special emulator. All communications signals between the device and the PC are isolated by optocouplers-HCPL 2611 for safety.

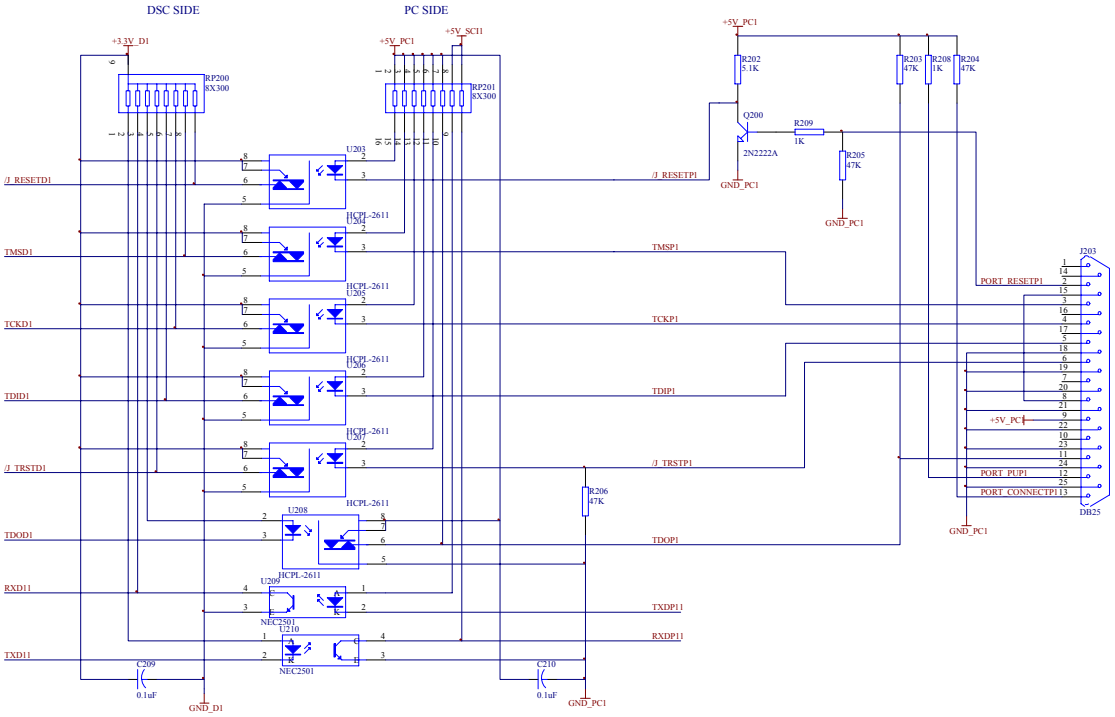


Figure 4-2. Parallel JTAG Interface

4.3 SCI Interface

This circuit is the serial communication interface between the device and the PC. A charge pump voltage converter, TC7660, generates +5V power from the PC, which is the power supply for the MAX202CSE, the RS-232 communication protocol transformer's special IC.

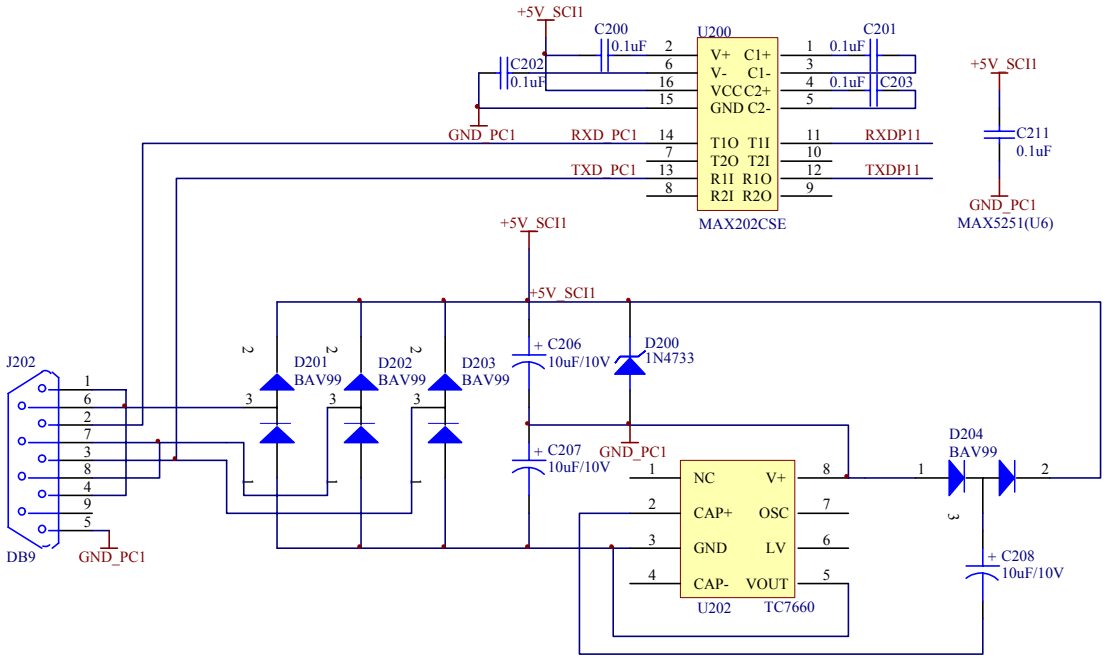


Figure 4-3. SCI Interface Circuit

Chapter 5
Control Strategy Design

5.1 Control of Power Factor Correction System

Based on the 56F8323, a digital PFC rectifier is implemented as shown in **Figure 5-1**. The main circuit contains two switches operated in interleaved mode. The circuit is composed of Q_1/Q_2, D_1/D_2, L_q/L_w, and filter capacitance C and includes EMI filter, input relay and full-wave rectifier.

5.2 Arithmetic of Power Factor Correction

Power Factor (PF) is defined as the ratio between AC input's real power and apparent power. Assuming input voltage is a perfect sine wave, PF can be defined as the product of current distortion and phase shift. Consequently, the PFC circuit's main tasks are:

- **Controls inductor current**, which makes the current sinusoidal and maintains the same phase as the input voltage
- **Controls output voltage**, which insures the output voltage's stability

Two closed loops are needed to control the circuit:

- The **voltage loop** is the outer loop, which samples the output voltage and maintains a stable level
- The **current loop** is the inner loop, which samples inductor current and forces the current to follow the standard sinusoidal reference in order to reduce the input harmonic current

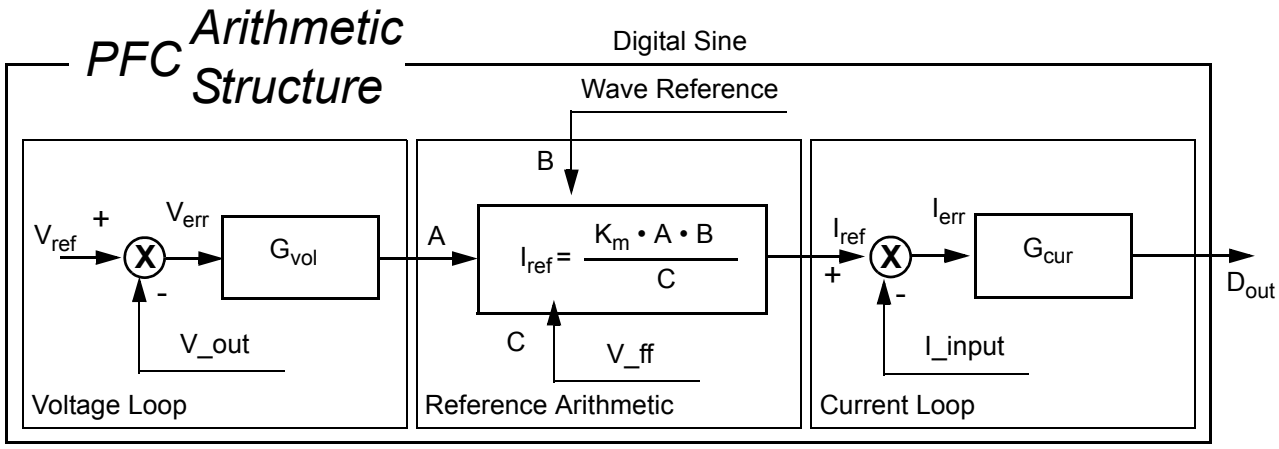


Figure 5-1. Digital PFC Arithmetic Structure Design

According to PFC theory, PFC arithmetic can be divided into three parts:

- **Voltage outer loop** insures the output voltage follows the reference-constant voltage output
- **Reference arithmetic** insures that the current reference follows the sine reference and constant power feed forward
- **Current inner loop** insures the input current follows the given current reference and implements PRC function

5.2.1 Arithmetic of Current Reference

In analog control arithmetic, the current reference wave is referred to as input voltage; at the same time, it introduces the squared input voltage as reciprocal to maintain constant power control.

$$i_L^* = \frac{K_m \cdot v_{vo}}{V_{ff}^2} V_s \left|\sin \varpi_0 t\right|$$

Eqn. 5-1

Where:

K_m is the proportion value

V_{vo} is the output of the voltage regulator

V_s is the instantaneous value of input voltage

V_{ff} is the RMS value of feed forward voltage

In analog arithmetic, the input voltage sample must be introduced as the input current's reference so the ripple voltage is introduced to current control at the same time. The PFC will be greatly affected under conditions of extreme input. In addition, because the input voltage acts as current reference, the denominator of current reference will be the square of input voltage. It will be additional calculation spending, which consequently affects system performance. In a digital control system, sine reference can be given accurately and conveniently by the controller's software, which not only will create a perfect sine wave, so there will be no effect from input voltage, but will also simplify the arithmetic structure.

$$i_L^* = \frac{K_m \cdot V_{vo}}{V_{ff}} I_{shape}$$

Eqn. 5-2

Where:

I_{shape} is the reference sine wave generated by software

K_m is the proportional value

V_{vo} is the output of voltage regulator

V_{ff} is the RMS value of feed forward voltage

This demonstrates that current reference is calculated from input voltage in analog arithmetic, unavoidably introducing ripple voltage to current control. Once the operating condition changes, the PFC effect will be obviously affected, but digital arithmetic can completly avoid this influence. The sine

reference is generated by DSP software and the wave can be perfect even if the input voltage has great distortion, so the system input current can be a very clean sine wave, which results in a perfect PFC effect. In addition, in analog arithmetic, the denominator of current reference must be the square of input voltage to calculate the current reference. The digital equation doesn't require the square of the input voltage, so it is also simpler.

5.2.2 Voltage and Current Loop Design

Because of its simplicity and reliability, PI loop control is widely used in industry control. In this application, the voltage and current loops adopt PI regulator arithmetic.

To simplify the analysis, the following assumptions are made:

- Input current follows reference perfectly, and is proportional to the input voltage
- The power efficiency is 1
- The output power is constant

Figure 5-2. Simple PFC Model

Because input current is proportional to input voltage, and inductor current is assumed to follow reference perfectly:

$$i_{in} = K_i \frac{\sqrt{2}P_{in}}{V_{rms}} \left|\sin \varpi_0 t\right| \qquad \textit{Eqn. 5-3}$$

Where:

K_i is input current sample modulus

P_{in} is average input power

V_{rms} is the virtual value of input voltage

Input power equals output power, so:

$$P_{in} = P_{out} = V_o \cdot I_o \qquad \textit{Eqn. 5-4}$$

Where:

P_{out} is the average output power

V_o is the average output voltage

I_o is the average output current

Substituting **Equation 5-2**, **Equation 5-3** and **Equation 5-4**, and taking the sample modulus of the sine reference as 1 yields:

$$V_o I_o = P_{in} = \frac{i_{in} \cdot V_{rms}}{\sqrt{2} K_i \left| \sin \omega_0 t \right|} = \frac{K_m V_{rms}}{\sqrt{2} K_i K_{ff} V_{ff}} V_{vo} = K \cdot V_{vo}$$

Eqn. 5-5

Including:

$$K = \frac{K_m V_{rms}}{\sqrt{2} K_i K_{ff} V_{ff}}$$

Eqn. 5-6

K is constant value

Assume (V_o, I_o, V_{vo}) is the stable point of voltage

According to small signal analysis, introducing small signal disturbance to **Equation 5-5** yields:

$$(V_0 + \tilde{v}_o)(I_o + \tilde{i}_o) = K(V_{vo} + \tilde{v}_{vo})$$

Eqn. 5-7

If:

V_{vo}, V_o and I_o are stable parts

$\tilde{v}_{vo}$, $\tilde{v}_o$ and $\tilde{i}_o$ are small signal parts
Then:

$$\tilde{i}_o = \frac{K}{V_o} \tilde{v}_{vo} - \frac{I_o}{V_o} \tilde{v}_o$$

Eqn. 5-8

V_o and I_o are stable parts

$\tilde{v}_o$ and $\tilde{i}_o$ are small signal disturbances
Considering the relation of output current:

$$i_o = C \frac{dv_o}{dt} + \frac{P_{out}}{v_o}$$

Eqn. 5-9

Applying small signal analysis to **Equation 5-9** yields:

$$\tilde{i}_o = C \frac{d\tilde{v}_o}{dt} - \frac{P_{out}}{V_o^2} \tilde{v}_o$$

Eqn. 5-10

So:

$$\frac{K}{V_o} \tilde{v}_{vo} - \frac{I_o}{V_o} \tilde{v}_o = C \frac{d\tilde{v}_o}{dt} - \frac{I_o}{V_o} \tilde{v}_o$$

Eqn. 5-11

PFC transfer function can be derived easily from the following:

$$G_v(S) = \frac{\tilde{v}_o}{\tilde{v}_{vo}} = \frac{K}{SCV_o}$$

Eqn. 5-12

Control is discrete digital control, so it's necessary to consider the effect of the sample and hold time and calculation delay when modeling the system. Applying Z transfer to **Equation 5-12** yields the discrete mathematical model of the power transfer function:

$$G_{vh}(z) = Z(G_{vh}(S)) = (1 - z^{-1})Z[\frac{G_v(S)}{S}] = \frac{K \cdot T_S}{CV_o(z-1)}$$

Eqn. 5-13

Where:

T_s is the sample period of the voltage loop

The discrete voltage loop structure is shown in **Figure 5-3**, where:

K_{vs} is the out voltage sample modulus

$G_{VEA}(Z)$ is the discrete control transfer function

$G_{vh}(Z)$ is the discrete power transfer function

After deriving the discrete power transfunction, it's necessary to consider the discrete control transfer function.

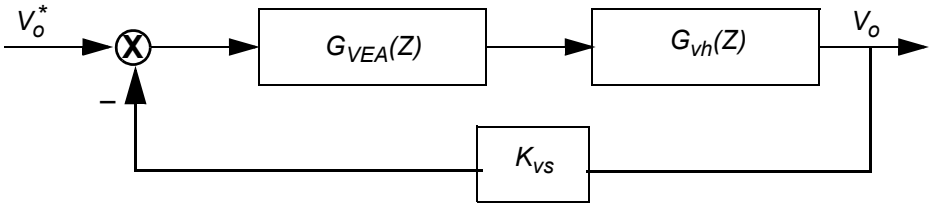


Figure 5-3. Discrete Voltage Loop Structure

The voltage regulator adopts the PI regulator, so:

$$G_{VEA}(z) = K_{pv} + \frac{K_{iv}z}{z-1} = \frac{(K_{pv} + K_{iv})z - K_{pv}}{z-1} = K_p \frac{z-\xi}{z-1}$$

Eqn. 5-14

Where:

K_{pv} is the P parameter

K_{iv} is the I parameter

K_p and ξ are two temporary variables

$$K_p = K_{pv} + K_{iv}, \xi = \frac{K_{pv}}{K_{pv} + K_{iv}}$$

Eqn. 5-15

The voltage open loop transfer function is:

$$G_{vopen}(z) = K_{vs} G_{VEA}(z) G_{vh}(z)$$

Eqn. 5-16

To restrain the effect to the current loop caused by two order harmonics in the output voltage, the voltage loop must have the ability to restrain the harmonics voltage to a range between 100 to 120Hz. If close frequency is 6Hz, and phase abundance is 45, according to the characteristic of the open loop transfer function, it's possible to calculate the P, I parameters of the voltage loop. The current loop is also a PI regulator, with a design course similar to the voltage loop. There is no need to introduce it once again.

The parameters of the voltage and current loops are determined through simulation and experiment. To insure the best system performance in a wide input voltage, different parameters are adopted when the input voltage is between 110V and 220V, which is impossible in analog control.

Table 5-1. PFC Experiment PI Parameters

Input Voltage	Loop	Parameter	Symbol	Value
110V	Voltage loop	Proportion modulus	K_{pv}	5
		Integration modulus	K_{iv}	0.007
	Current loop	Proportion modulus	K_{pi}	0.17
		Integration modulus	K_{ii}	0.044
220V	Voltage loop	Proportion modulus	K_{pv}	5
		Integration modulus	K_{iv}	0.007
	Current loop	Proportion modulus	K_{pi}	0.44
		Integration modulus	K_{ii}	0.09

5.3 Control of DC/DC Converter Subsystem

Figure 5-4 shows the main circuit, composed of four switches (Q_1—Q_4); transformer (T_f); Capacitance (C_r), which prevents saturation of the transformer; secondary synchronous rectifiers (Q_5 and Q_6); filter inductors (L_{f1} and L_{f2}); and output filter capacitance (C_f). Input voltage is 380V DC and switching frequency is 150KHz.

Ignoring the dead time that is inserted by the PWM peripheral, the two switches in one power bridge operate at a 180^o complement to each other. Constant output is achieved by adjusting the value of phase shift. When $\alpha = 0°$, and Q_1/Q_4 or Q_2/Q_3 are on simultaneously, output value is maximum; when $\alpha = 180°$ and Q_1/Q_2 or Q_3/Q_4 are on simultaneously, output voltage is zero. The 56F8323 samples three signals: output voltage (V_o), primary inductor current (i_L), and output current (i_o).

The 56F8323's PWM1—PWM4 output the drive signal, whose dead time and duty have been fixed, and according to α, adjust the value of phase shifted in order to stabilize the output voltage. From the relationship between the synchronous signal and primary drive signal, the synchronous drive signal can be derived easily. The digital DC/DC converter's software also drives the LED circuits to show the output voltage value, protects the output current and communicates with the PC.

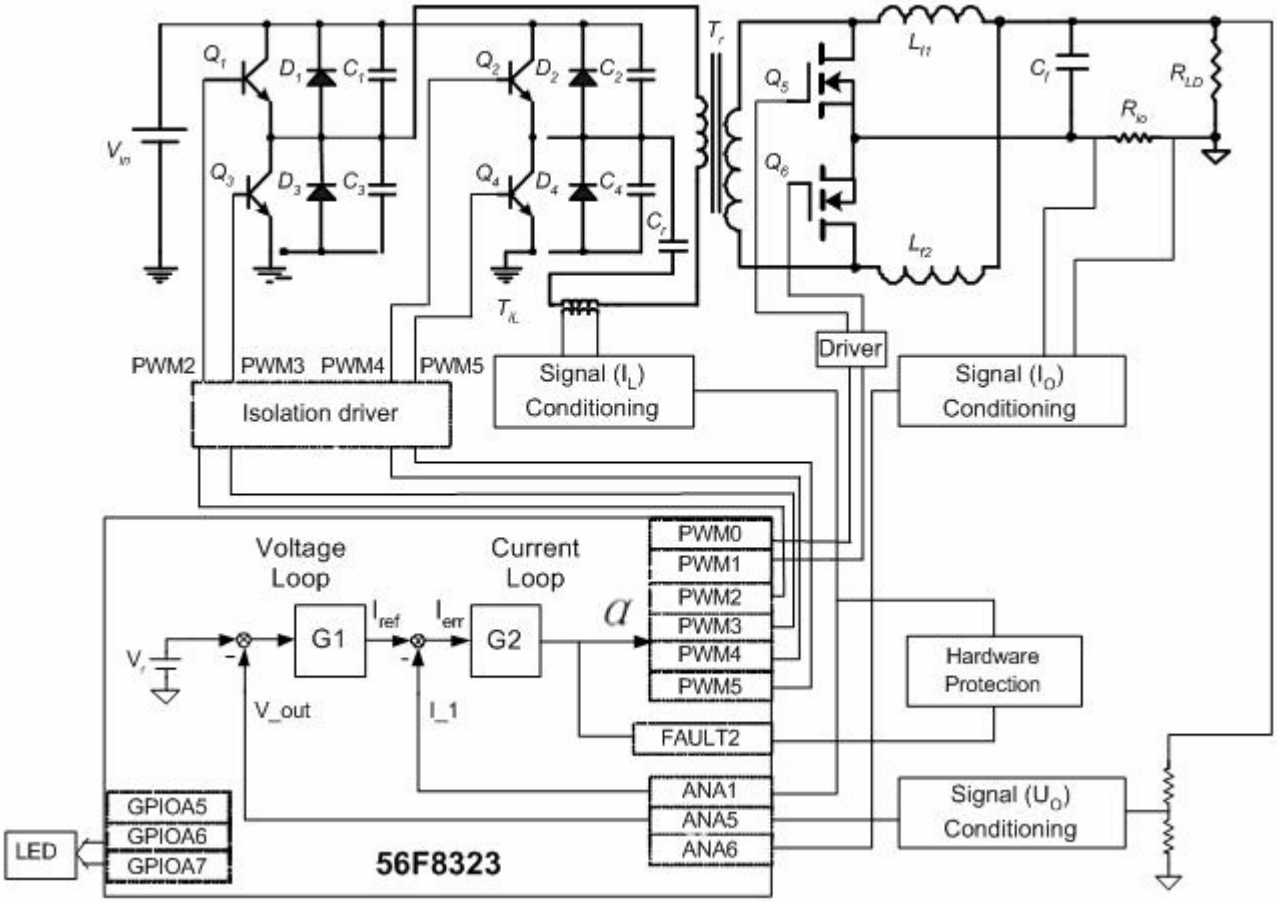


Figure 5-4. PFC Module Frame Based on the 56F8323

5.3.1 DC/DC Converter Arithmetic

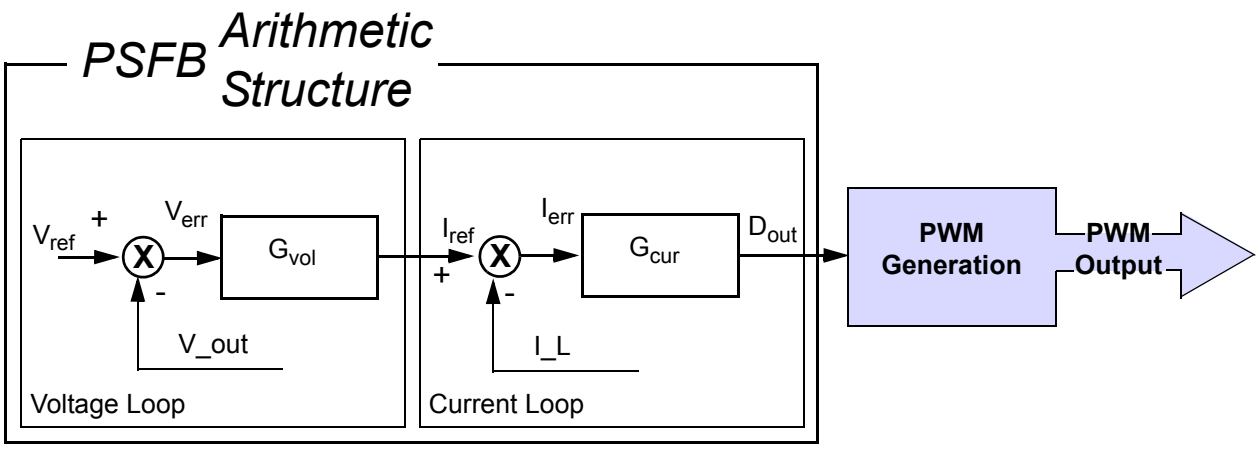


Figure 5-5. Digital Control PSFB Converter

The voltage and current loops are adopted by the system. The error signal is generated by comparing the reference and sample values of output voltage. The voltage loop is composed by a PI regulator whose input is the error signal. The output of voltage acts as the reference of the current loop and the error signal between the primary inductor current, and its reference acts as the input of the current loop's PI regulator. The current loop outputs the results of the PI regulator, which is the control signal of shifted-Phase α.

5.3.2 Voltage and Current Loops Design

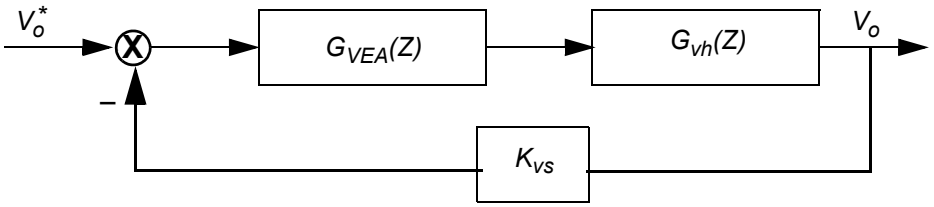


Figure 5-6. Power Factor Correction Arithmetic

PI regulators are also adopted for voltage and current loops of the PSFB DC/DC converter. Device-based control is actually a kind of discrete digital control; control results can be calculated according to the sampled value, so the transfer function of the PI regulator can be shown as follows:

$$\begin{cases} U(n) = K0 \times E(n) + I(n-1) \\ I(n) = I(n-1) + K1 \times E(n) + Kcorr \times Epi \\ Epi = Us - U(n) \end{cases}$$

Us is calculated as follows:

$$Us = \begin{cases} U_{\max} & U(n) \geq U_{\max} \\ U_{\min} & U(n) \leq U_{\min} \\ U(n) & else \end{cases}$$

U(n) is the calculation result corresponding to the nth sample value

E(n) is the variable error at the nth sampling time

I(n)—I(n-1) is the sum of *n* sample values and *n-1* sample values separately

K0 is proportion modulus

KI is integral modulus

Kcorr is the modulus used to prevent saturation

Epi prevents saturation

Kcorr x *Epi* operates only when *U(n)* overflows, so usually *Epi* = 0

Parameters of the voltage and current loops are determined through emulation and experiment. To insure the best system performance in a wide input voltage, different parameters are adopted when the input voltage is between 110V and 220V, which is impossible in analog control.

Table 5-2. PFC Experiment PI Parameters

Loop	Parameter	Symbol	Value
Voltage loop	Proportion modulus	K_{pv}	0.195
	Integration modulus	K_{iv}	0.004
Current loop	Proportion modulus	K_{pi}	0.42
	Integration modulus	K_{ii}	0.001

Chapter 6
Software System Design—PWM Control Strategy

6.1 PFC PWM Control Strategy

PFC control requires two PWM signals, between which there is a 180° phase shift. The 56F8323 device's PWMA0 and PWMA1 are used to generate these two PWM signals.

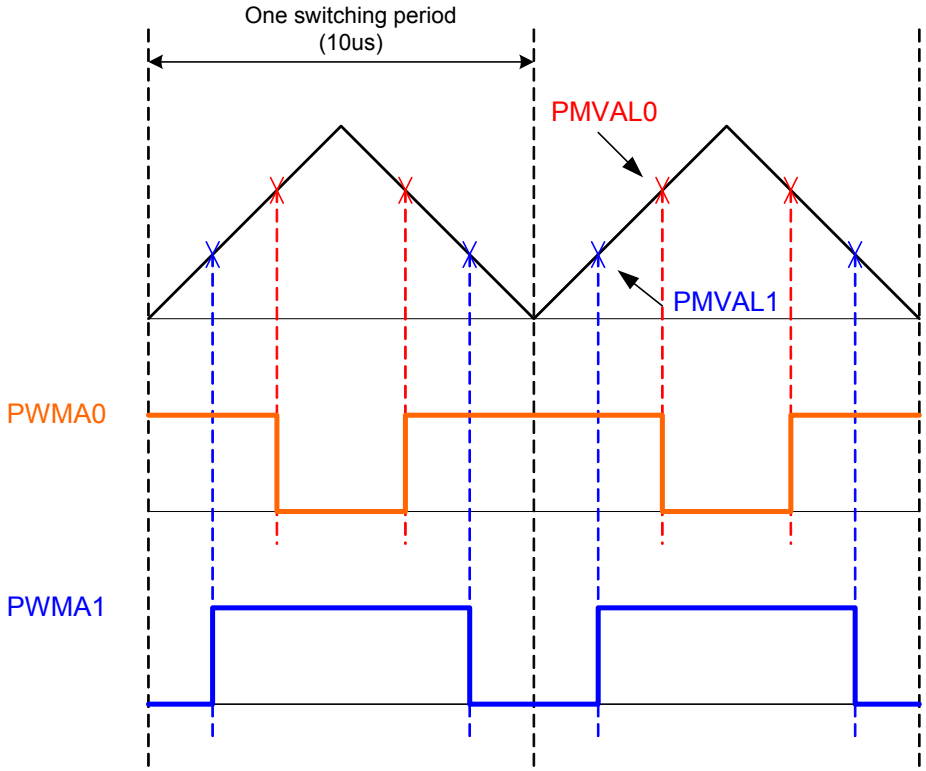


Figure 6-1. PFC PWM Generation

As **Figure 6-1** shows, PMVAL0 is active high and PMVAL1 is active low. Write the result of PFC current control loop to PMVAL0, and PMVAL1 has the following relation with PMVAL0:

$$PMVAL0 + PMVAL1 = PWMCM$$

So:

$$PMVAL1 = PWMCM - PMVAL0$$

The ZVS gate drive precedes the PVC switch's Q gate drive output. The duration of the ZVS output is the time necessary for a controlled turn-off of the boost diode plus the time required for the main MOSFET drain voltage to resonate to zero. The ZVS Q then turns off and the main Q turns on simultaneously.

Figure 6-2 shows the gate drive waveforms of the main and ZVS transistors. The ZVS drive is high until the main transistor switches on. The ZVS transistor keeps active high for a certain time, which is determined by the soft-switching condition of the main MOSFET and DIODE reverse recovery. The ZVS pulse is then terminated and the main gate drive initiated. According to V_g_Q1, the ZVS transistors' gate drive waveform will be generated by the device, shown in Figure 6-2. At t1, the rising edge of ZVS_Q1 can be obtained by the Timer module that operates in variable frequency PWM mode. ZVS_Q1 will remain high until t2.

TMRCMP1 = Const

TMRCMP2 = 2 x PWMCM - PWMVALUE - TMRCMP1 - Delay

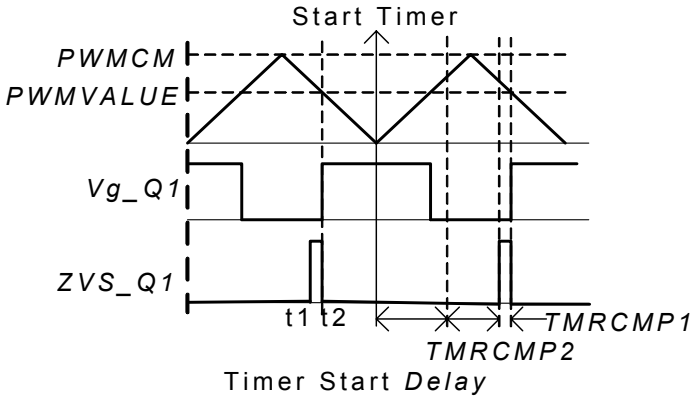


Figure 6-2. Gate Drive Waveforms of the Main and ZVS Transistors

6.1.1 DC/DC PWM Value Register Update

DC/DC requries four PWM signals. PWM signals Q_1 and Q_3 are oppositional; PWM signals Q_2 and Q_4 are oppositional. There is a phase shift between Q_1 and Q_4 and between Q_2 and Q_3.

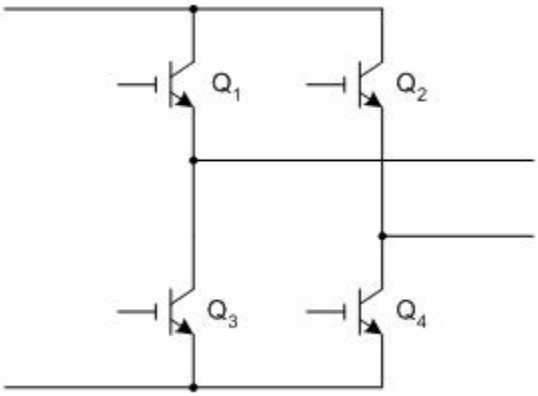


Figure 6-3. DC/DC Full Bridge

The relationship between the device's ports and the control signals is shown in **Table 6-1**.

Table 6-1. Relation Between the 56F8323's Ports and Control Signals

Ports	Control Signals
PWMA2	Q_1
PWMA3	Q_3
PWMA4	Q_4
PWMA5	Q_2

The 56F8323's PWM module has a special feature, asymmetric PWM output mode, which allows the PWM duty cycle the ability to change alternatively at every half-cycle when in complementary mode with center-align operation. The count direction of the PWM counter selects either the odd or even PWM value registers to use in the next PWM cycle. To count up, select the odd PWM value registers to use in the next PWM cycle. To count down, select the even PWM value registers to use in the next PWM cycle. Using this feature, the 56F8323's PWM module can realize phase-shifting operation without any external auxiliary circuit or additional expenditure of software resources.

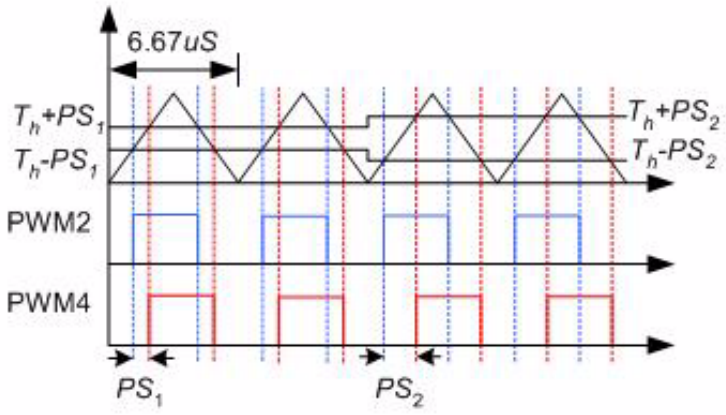


Figure 6-4. DC/DC PWM Generation

Set ICC1 and ICC2 of the PWM Internal Correction Control Register (PMISCCR). PMVAL2 and PMVAL4 will be used when the counter is counting up and PMVAL3 and PMVAL5 will be used when the counter is counting down.

As **Figure 6-4** shows, PMVAL2 and PMVAL 3 are set at initialization and will not be changed during control. The result of the DC/DC current control loop is the *shift_angle*, then:

T_h = *Duty* x *Period*

PMVAL2 = T_h - *Shift_angle*

PMVAL3 = T_h + *Shift_angle*

PMVAL4 = T_h + *Shift_angle*

PMVAL5 = T_h - *Shift_angle*

In this design, the same 56F8323 that drives the DC/DC converter circuitry also drives the synchronous rectifier. According to the analysis of the circuit, there is a direct relationship between the main DC/DC switches and the synchronous rectifiers, so control of the synchronous rectifer can be derived from the control of the DC/DC converter. The relationships are illustrated in **Figure 6-5**.

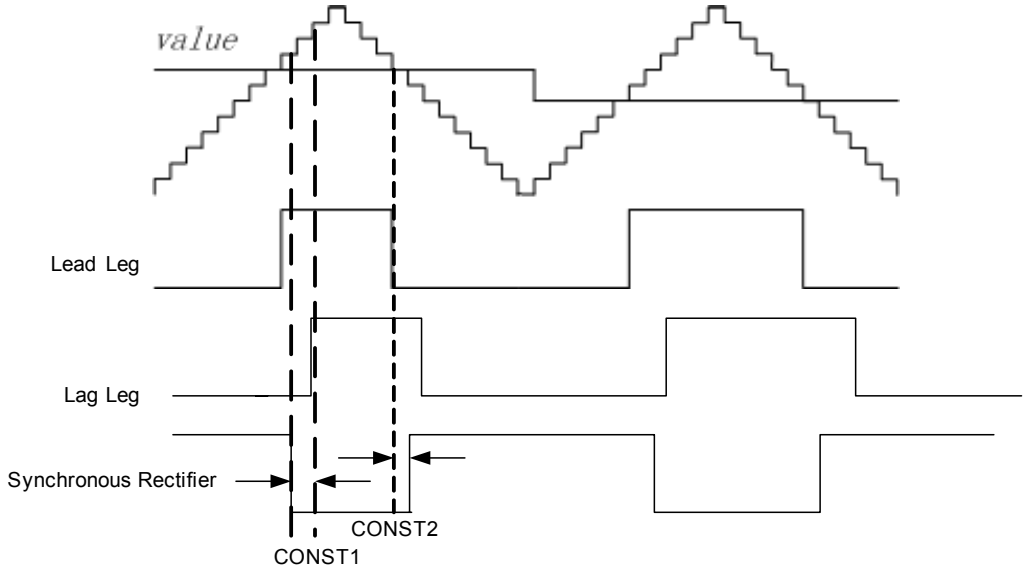


Figure 6-5. Current Doubler and Synchronous Rectification PWM Generation

As shown in **Figure 6-5**, the control of the synchronous rectifier is derived from the DC/DC converter main switches' signals. To avoid short circuiting the transformer when voltage is established, the synchronous rectifier must turn off when the switch in the lag leg turns on. Also, to avoid the current flows from the synchronous rectifier's body diode, it must turn on when the lead leg switches on. But to avoid a short circuit, there must be a delay time between the rectifier's turn on and the lead leg's turn off.

Chapter 7
Software Architecture

7.1 Software Infrastructure—Dual Digital Signal Controllers

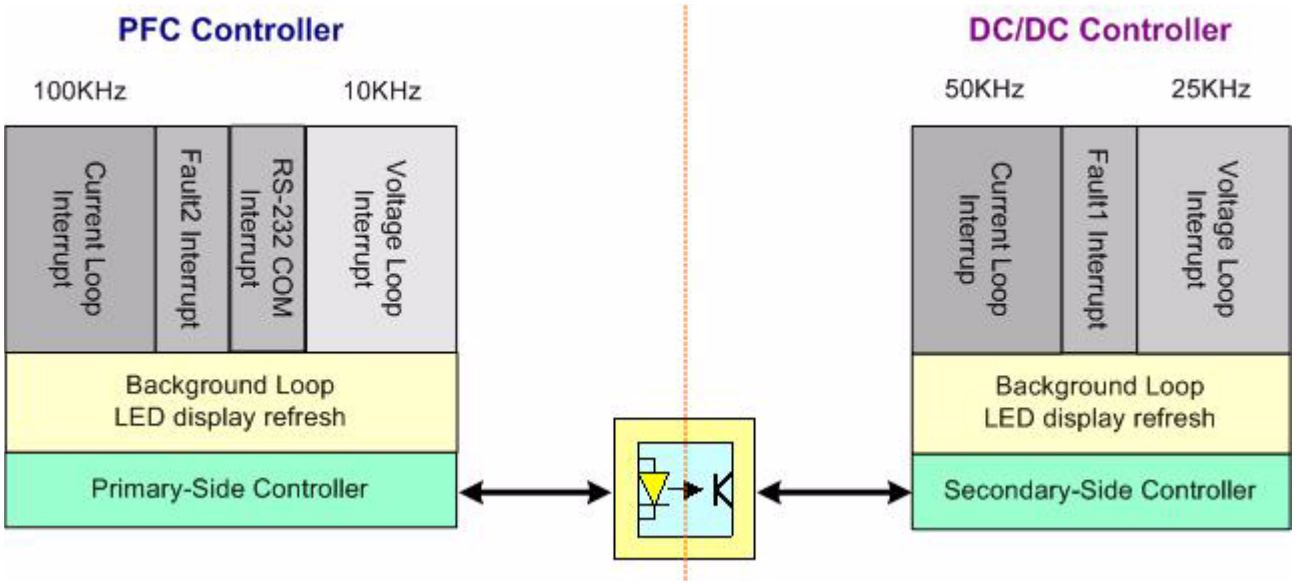


Figure 7-1. System Software Structure

7.2 Details of Interrupt Service Routines

7.2.1 PFC Controller

Current Loop Interrupt—PWM Reload Interrupt (100KHz):

- Configures Timer A0 to gain the delay signal for ZVSPWM
- Calculates current loop
- Calculates the input frequency and confirms the sinusoid table step

Fault2 Interrupt:

- Forces PWM to output logic low
- Sends a fault message to the DC/DC controller

RS-232 Communication Interrupt:

- Receives the communication data from the secondary-side 56F8323
- Sets the Switch-on or Protect directive from the secondary-side 56F8323

Voltage Loop Interrupt—Timer A2 Period Interrupt (10KHz):

- Manages software protection
- Voltage Loop

7.2.2 DC/DC Controller

Current Loop Interrupt—Timer A1 Period Interrupt (50KHz):

- Starts ADC
- Calculates PI current loop
- Calculates each PWM register value and refreshes the new duty PWM output

Voltage Loop Interrupt—Timer A0 Period Interrupt (25KHz):

- Manages software protection
- Calculates PI voltage loop
- Calculates the value of output voltage and output current

Fault2 Interrupt:

- Forces PWM to output logic low
- Sends a fault message to the PFC controller

7.3 Software Interrupt Service Timing

7.3.1 PFC Controller

Table 7-1. Bandwidth Consideration of PFC Controller

56F8323 Frequency		60MHz
Instruction Period		16.67ns
PWM Switching Frequency		100kHz
Sampling Rate		100kHz
Analog-to-Digital		1.7µs
Interrupt Name	Interrupt Period	Interrupt Assignment
Voltage loop	10kHz Timer	Calculates the PI of voltage loop Voltage loop output Calculates the mean of input voltage
Current loop	100kHz Timer	Starts ADC Calculates current loop reference Calculates the PI of the current loop and get sthe new duty Updates the PWM Produces ZVS_PWM
Fault2 Interrupt:	Event trigger	Powers the system off
RS-232 Communication Interrupt	Event trigger	Receives communication data from the secondary-side 56F8323 Sets the Switch-on or Protect directive from the secondary-side 56F8323

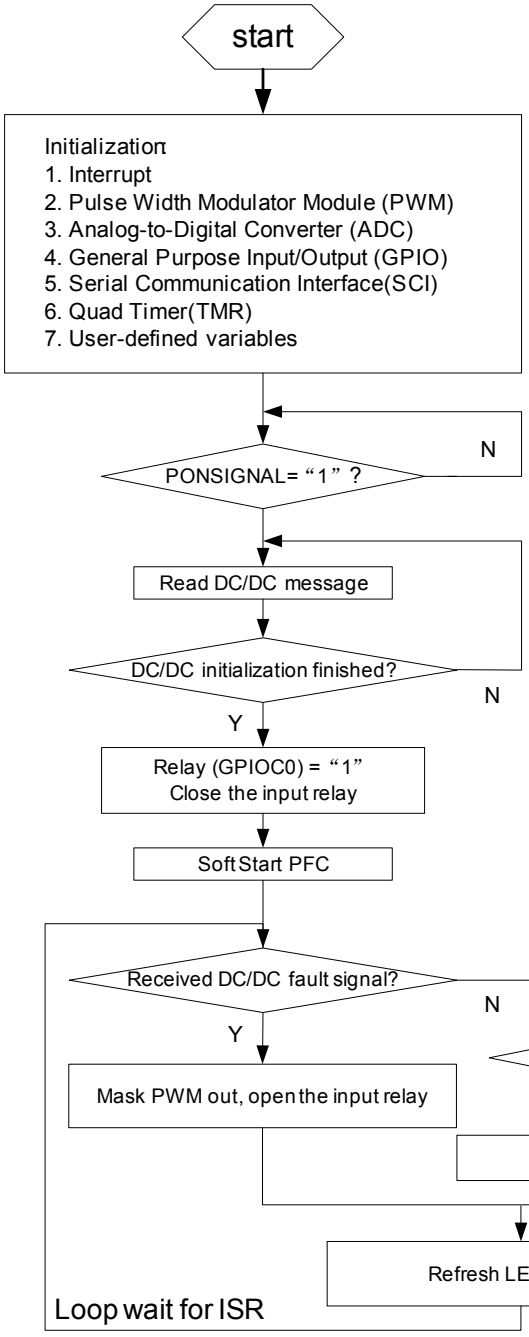
7.3.2 DC/DC Controller

Table 7-2. Bandwidth Consideration of DC/DC Controller

	56F8323 Frequency	60MHz
	Instruction period	16.67ns
	PWM Switching Frequency	150kHz
	Sampling Rate	50kHz
	Analog-to-Digital	1.7µs
Interrupt Name	Interrupt Period	Interrupt Assignment
Voltage loop	25kHz Timer	Software Protection judgement and management Calculates the PI of the voltage loop Calculates the mean of output voltage and output current
Current loop	50kHz Timer	Starts ADC Calculates the PI of the current loop and gets the new duty Updates the PWM output of the main power driver and synchronous driver signal Produces ZVS_PWM
Fault2 Interrupt:	Event trigger	Powers the system off Transmits the communication data to the primary side 56F8323

Chapter 8
Flow Chart of Software System Design

8.1 Software System Design—Flow Chart of PFC Control System



The interrupt includes:
PWM reload interrupt: 100KHZ, which is halved by setting curloop_flag 0 or 1 to get the current loop calculation period, 50KHZ
Timer A2 period interrupt: voltage loop calculation, 10KHZ
PWM initialization considerations:
PWMA0 active high and PWMA1 active low
ADC initialization considerations:
Use the START bit to initiate a conversion
Use channel ANA0, ANA1, ANA4
Once Sequential sampling
SCI0: used for communication between DSC and PC
SCI1: used for communication between two DSCs
GPIO used pins and functions:
GPIOC0: RELAY, output
output logic one to close the input relay
GPIOB6: DADATA, output
GPIOB5: DACLK, output
GPIOB2: DACEN, output
these three pins are used for Digital-to-Analog Conversion
GPIOA7: output, used for fault display
GPIOA11: LEDDATA, output
GPIOA10: LEDCLK, output
GPIOA9: LEDEN, output
these three pins are used to drive LED display
GPIOC2, GPIOC3: reserved for I^2C
GPIOC1: PONSIGNAL, input
logic one: enable the system
logic zero: disable the system

Figure 8-1. PFC Main Program Flow Chart

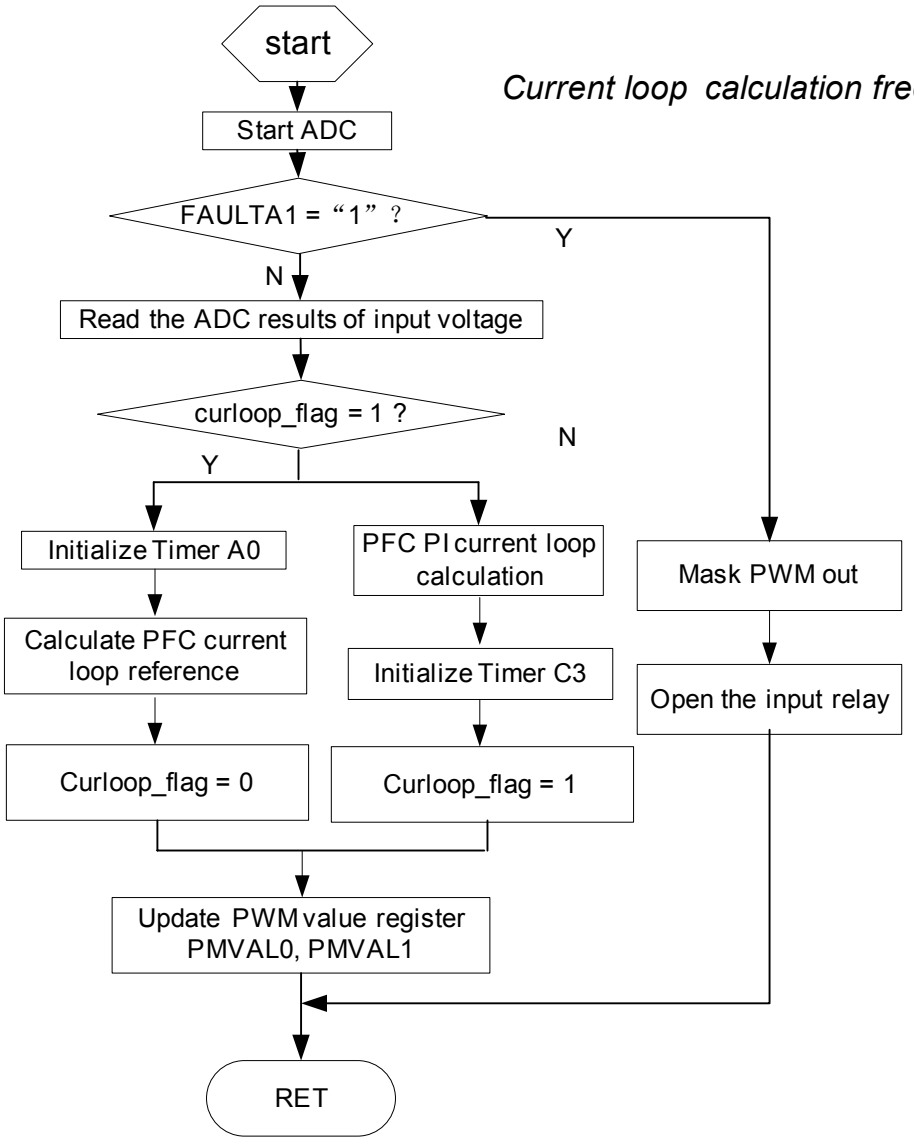


Figure 8-2. PFC Reload Interrupt ISR Flow Chart

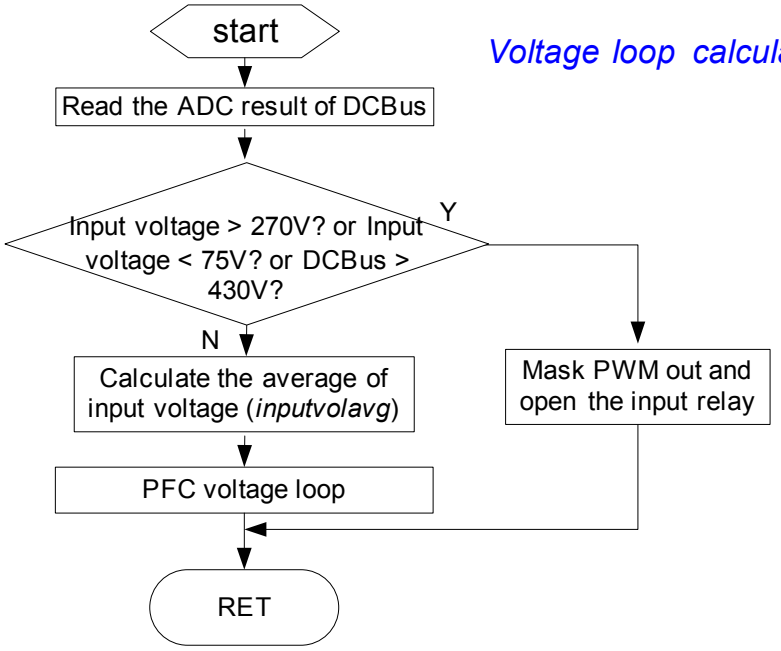
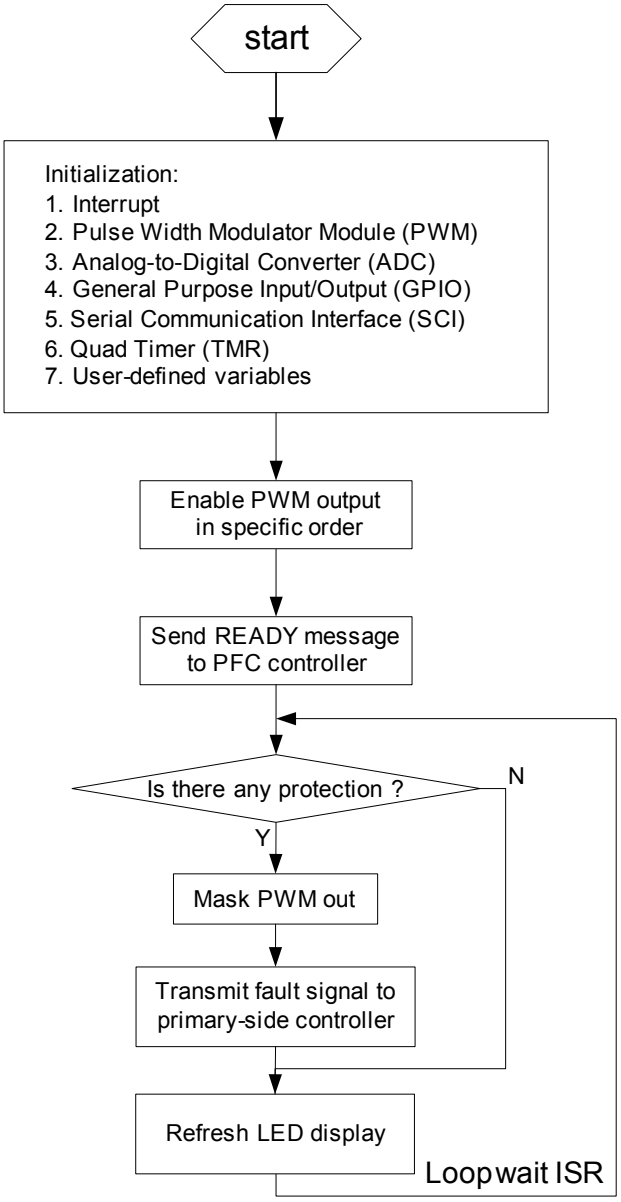


Figure 8-3. PFC Timer A2 Period Interrupt ISR Flow Chart

8.2 Software System Design—Flow Chart of DC/DC Control System



The interrupt includes:
Timer A1 period interrupt: current loop calculation, 50KHz
Timer A0 period interrupt: voltage loop calculation, 25KHz
PWM initialization considerations:
PWMA2, PWMA3, PWMA4, PWMA5 active high
ADC initialization considerations:
Use the START bit to initiate a conversion
Use channel ANA2, ANA5, ANA6
Once Sequential sampling
SCI0: used for communication between DSC and PC
SCI1: used for communication between two DSCs
GPIO used pins and functions:
GPIOA9: DADATA, output
GPIOA10: DACLK, output
GPIOA11: /DACEN, output
these three pins are used for Digital-to-Analog Conversion
GPIOB2,GPIOB3,GPIOB4: output, used for fault display
GPIOB5: LEDDATA, output
GPIOB6: LEDCLK, output
GPIOB7: /LEDEN, output
these three pins are used to drive LED display
GPIOC2, GPIOC3: reserved for I^2C

Figure 8-4. DC/DC Main Program Flow Chart

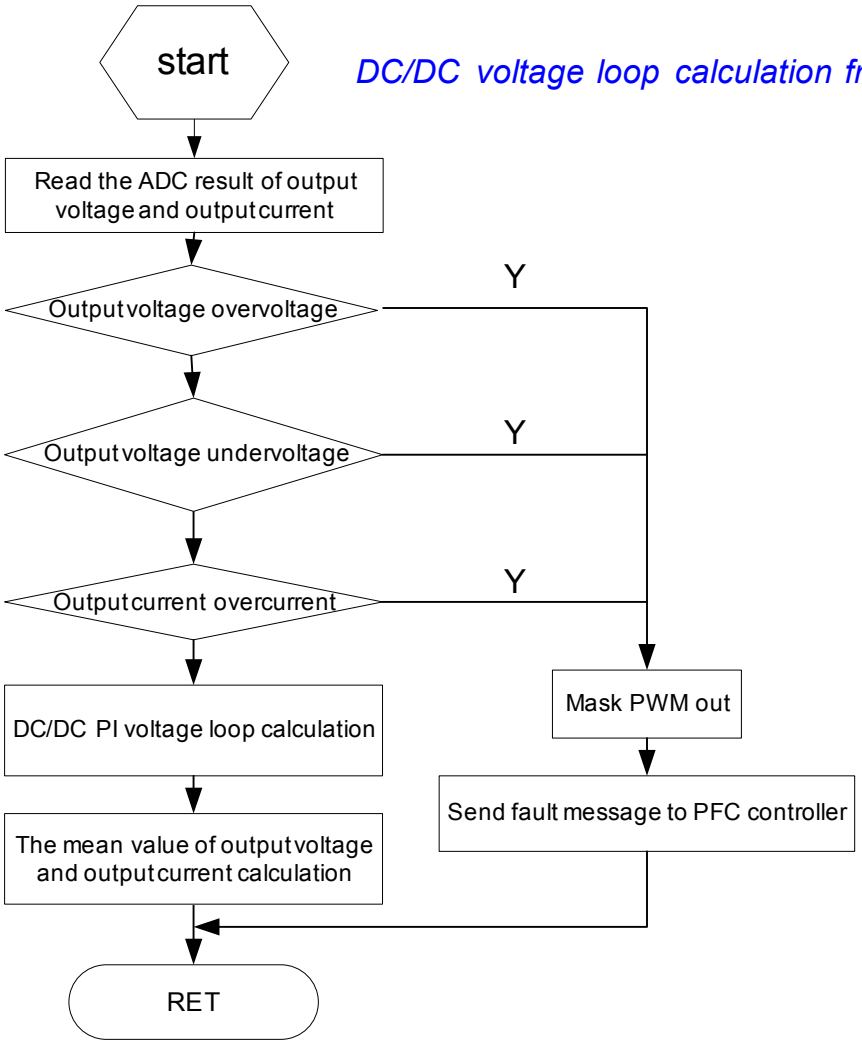


Figure 8-5. DC/DC Timer A0 Period Interrupt ISR Flow Chart

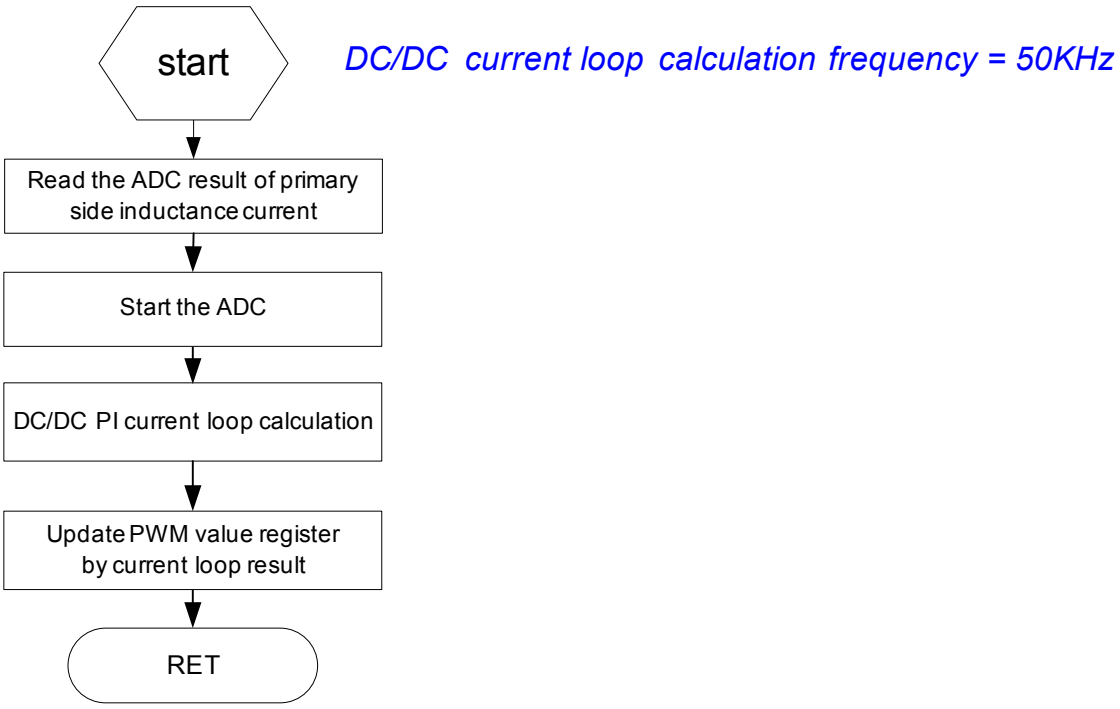
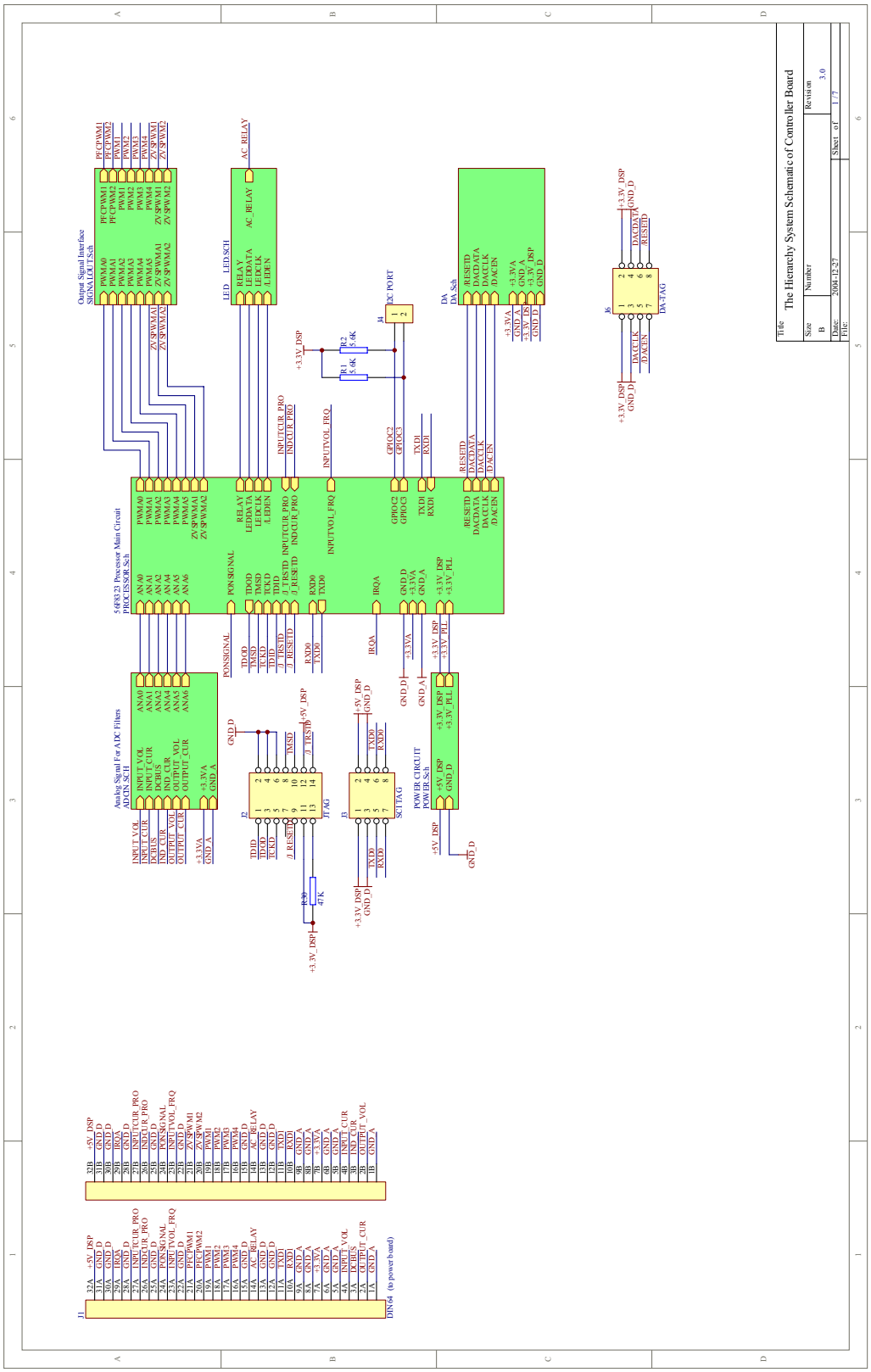
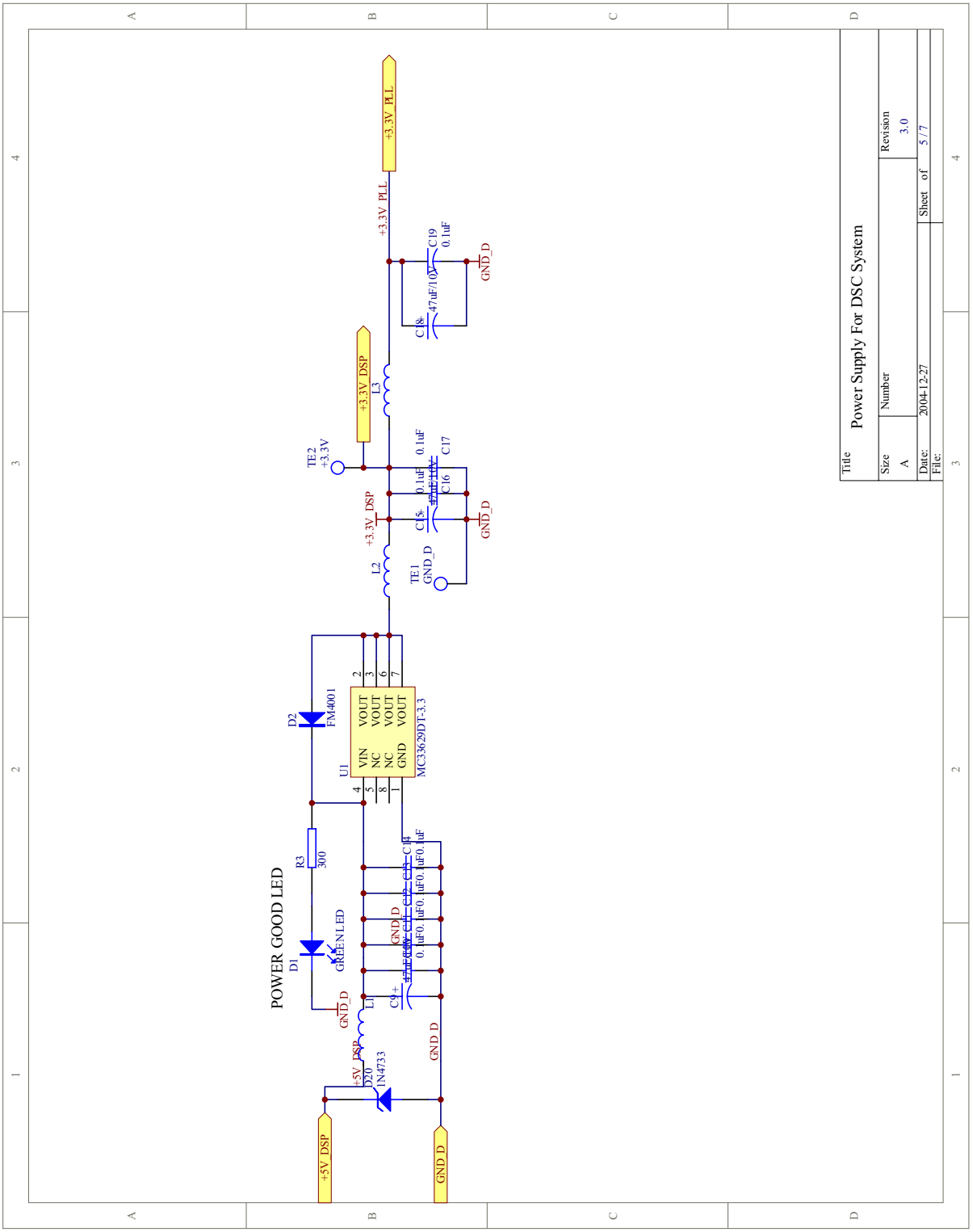


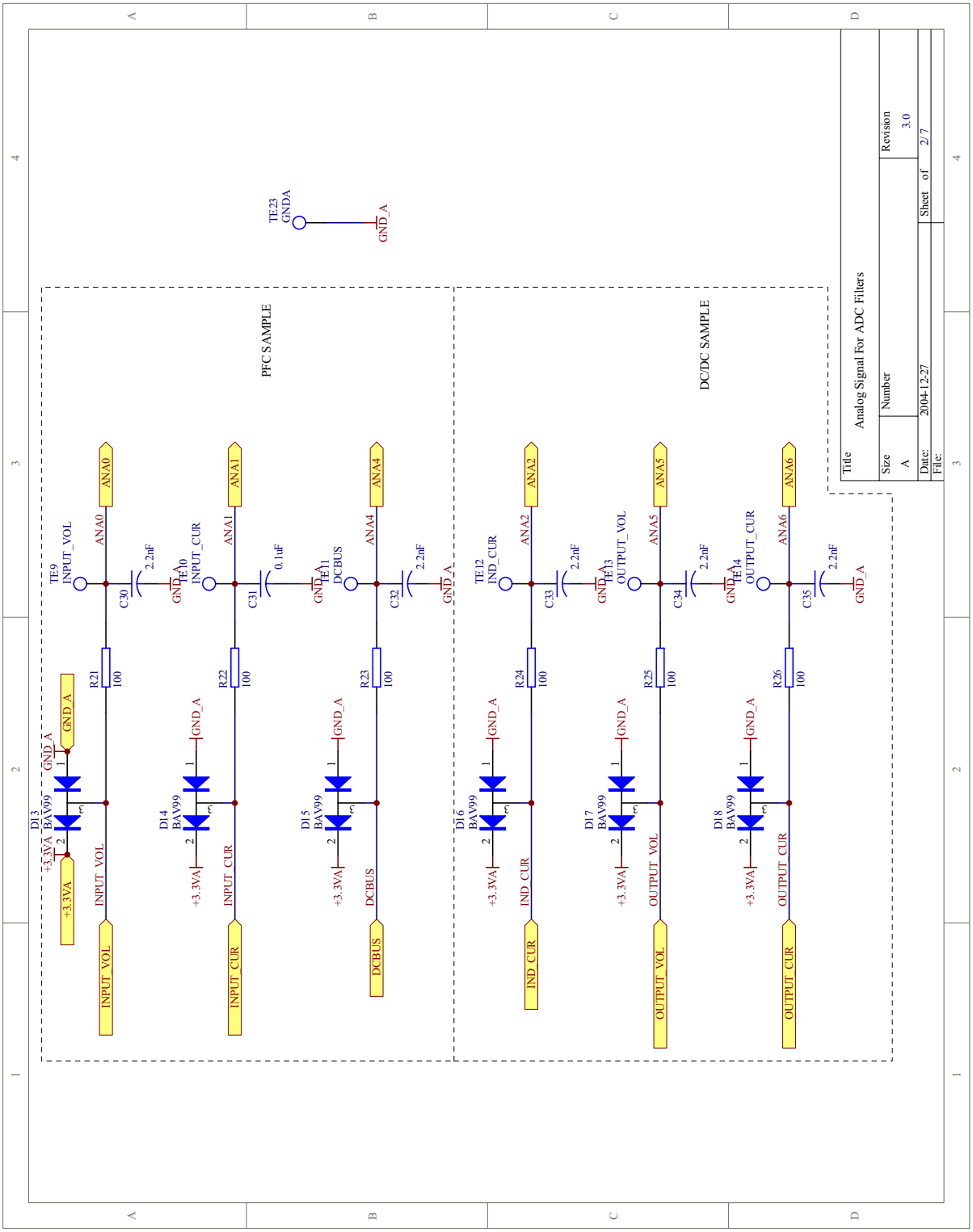
Figure 8-6. DC/DC Timer A1 Period Interrupt ISR Flow Chart

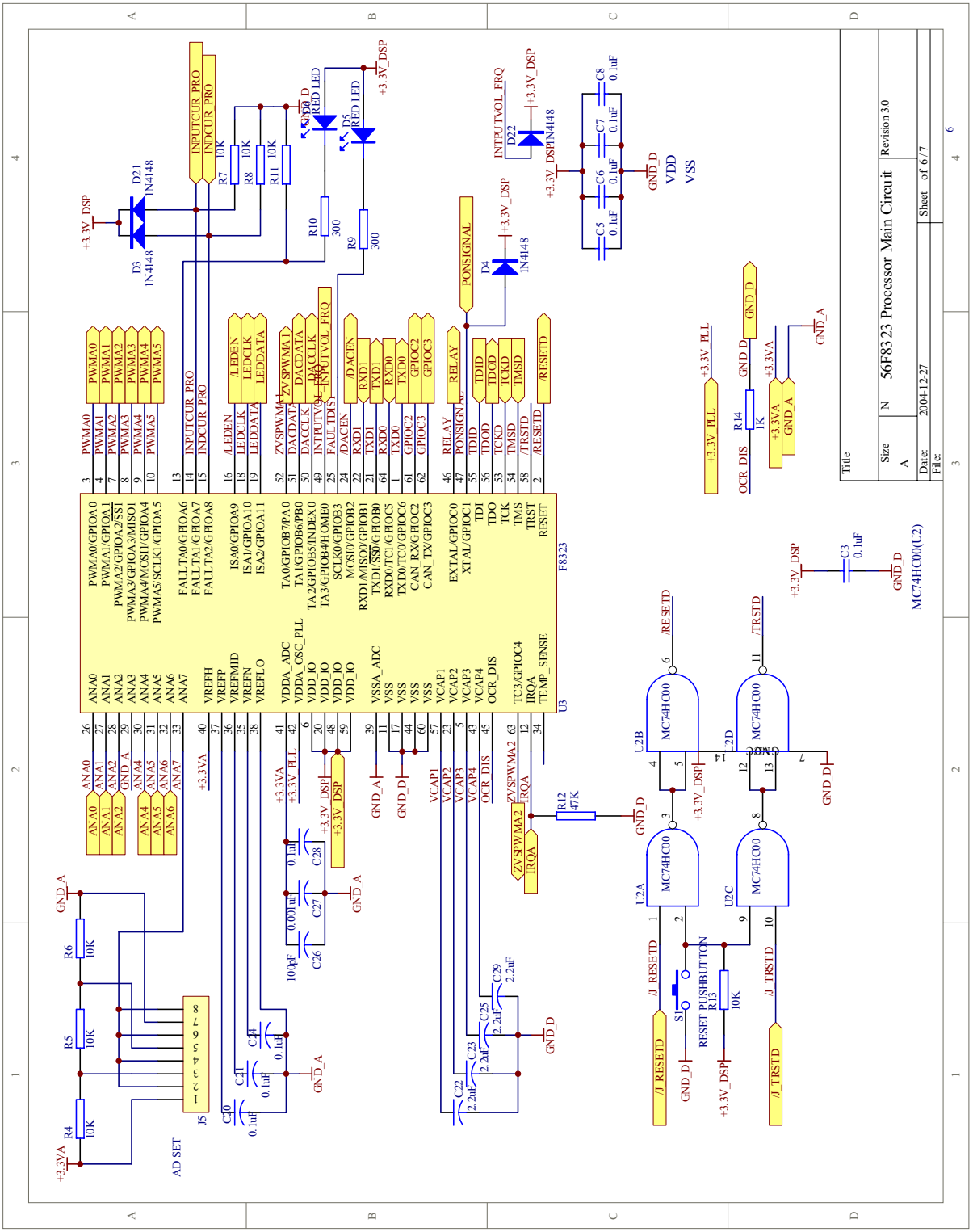
Appendix A
Schematics


The Hierarchy System Schematic of Controller Board
Output Signal Interface
SIGNALOUT.SCH
LED LED.SCH
AC_RELAY
DA DA.Sch
Analog Signal For ADC Filters
ADCIN.SCH
56F83 23 Processor Main Circuit
PROCESSOR.SCH
POWER CIRCUIT
POWER.Sch
JTAG
SCI TAG
DC PORT
DA-TAG
DIN64 (to power board)

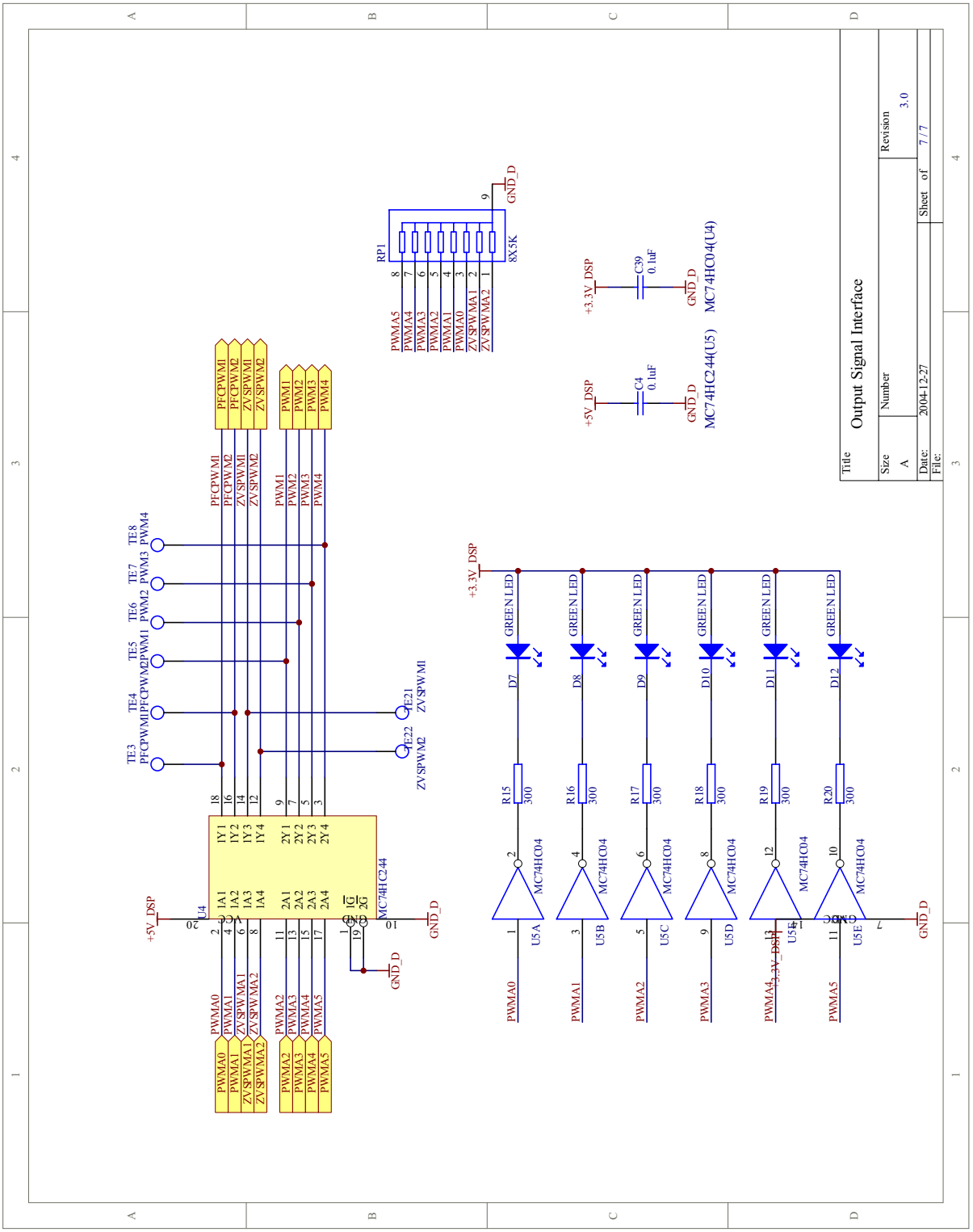


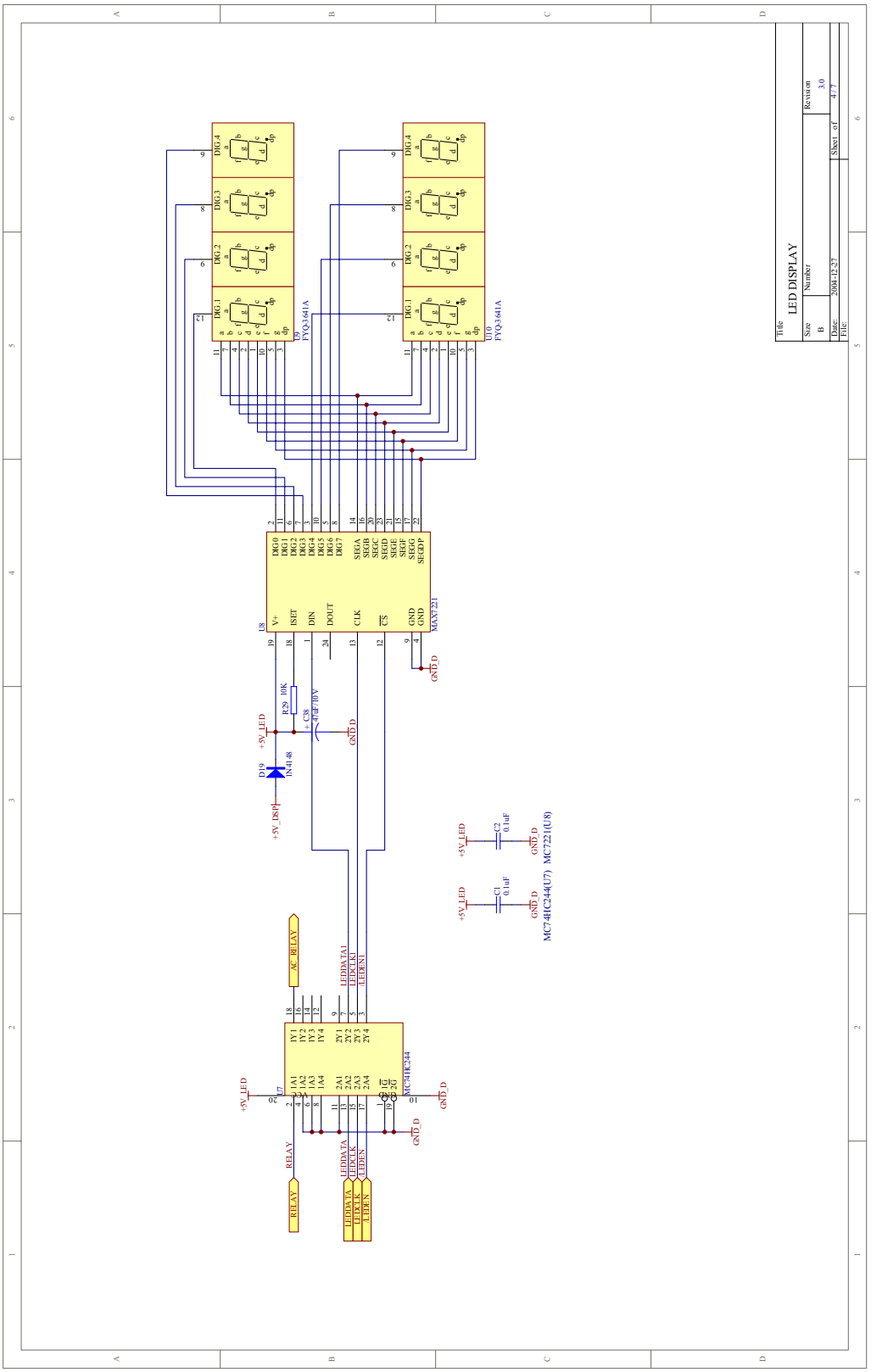
Schematics, Rev. 0


PFC SAMPLE
DC/DC SAMPLE
Analog Signal For ADC Filters
Number
Revision
3.0
Sheet of 2/7
2004-12-27
TE23 GNDA
TE9 INPUT_VOL
TE10 INPUT_CUR
TE11 DCBUS
TE12 IND_CUR
TE13 OUTPUT_VOL
TE14 OUTPUT_CUR
ANA0
ANA1
ANA4
ANA2
ANA5
ANA6
C30 2.2nF
C31 0.1uF
C32 2.2nF
C33 2.2nF
C34 2.2nF
C35 2.2nF
R21 100
R22 100
R23 100
R24 100
R25 100
R26 100
D13 BAV99
D14 BAV99
D15 BAV99
D16 BAV99
D17 BAV99
D18 BAV99
+3.3VA
GND_A
INPUT_VOL
INPUT_CUR
DCBUS
IND_CUR
OUTPUT_VOL
OUTPUT_CUR

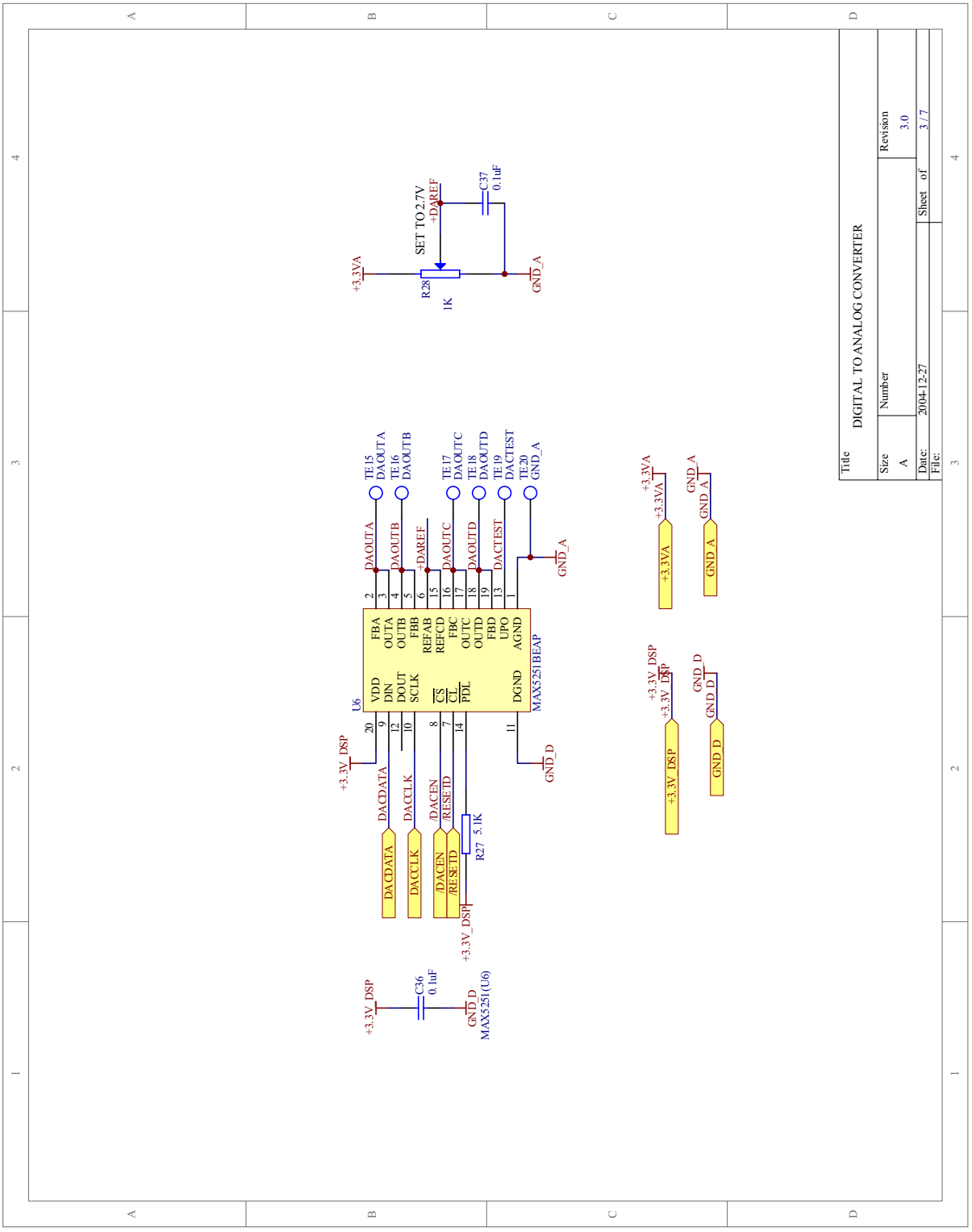


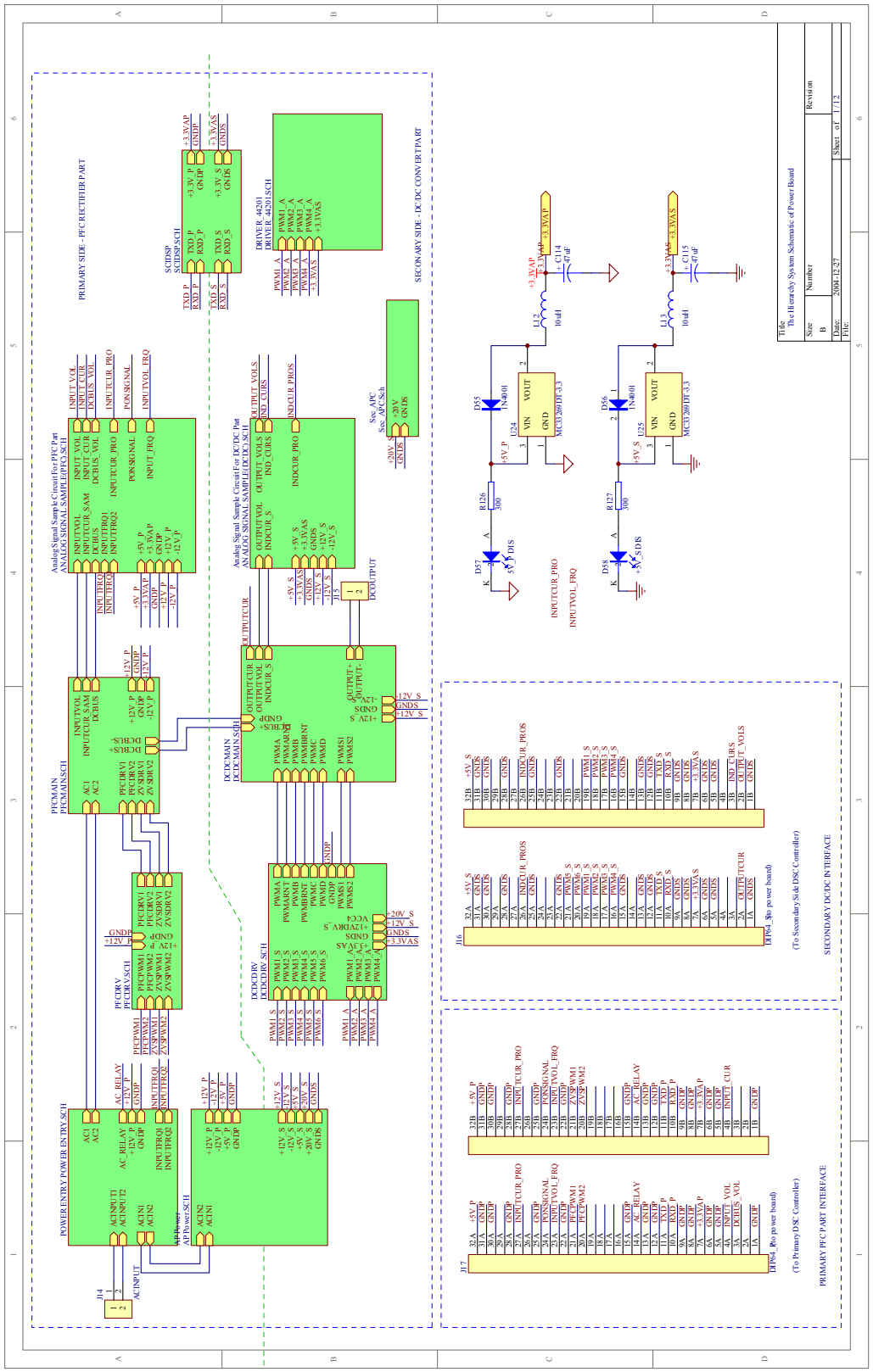
Schematics, Rev. 0


Title
Output Signal Interface
Size
A
Number
Revision
3.0
Date: 2004-12-27
Sheet of 7 / 7
File:
RP1
8X5K
PWMA5
PWMA4
PWMA3
PWMA2
PWMA1
PWMA0
ZVSPWMA1
ZVSPWMA2
GND_D
+3.3V_DSP
C39
0.1uF
MC74HC04(U4)
+5V_DSP
C4
0.1uF
MC74HC244(U5)
PFCPWM1
PFCPWM2
ZVSPWM1
ZVSPWM2
PWM1
PWM2
PWM3
PWM4
TE3
TE4
TE5
TE6
TE7
TE8
TE21
TE22
U4
MC74HC244
GREEN LED
D7
D8
D9
D10
D11
D12
R15
R16
R17
R18
R19
R20
300
MC74HC04
U5A
U5B
U5C
U5D
U5E
U5F

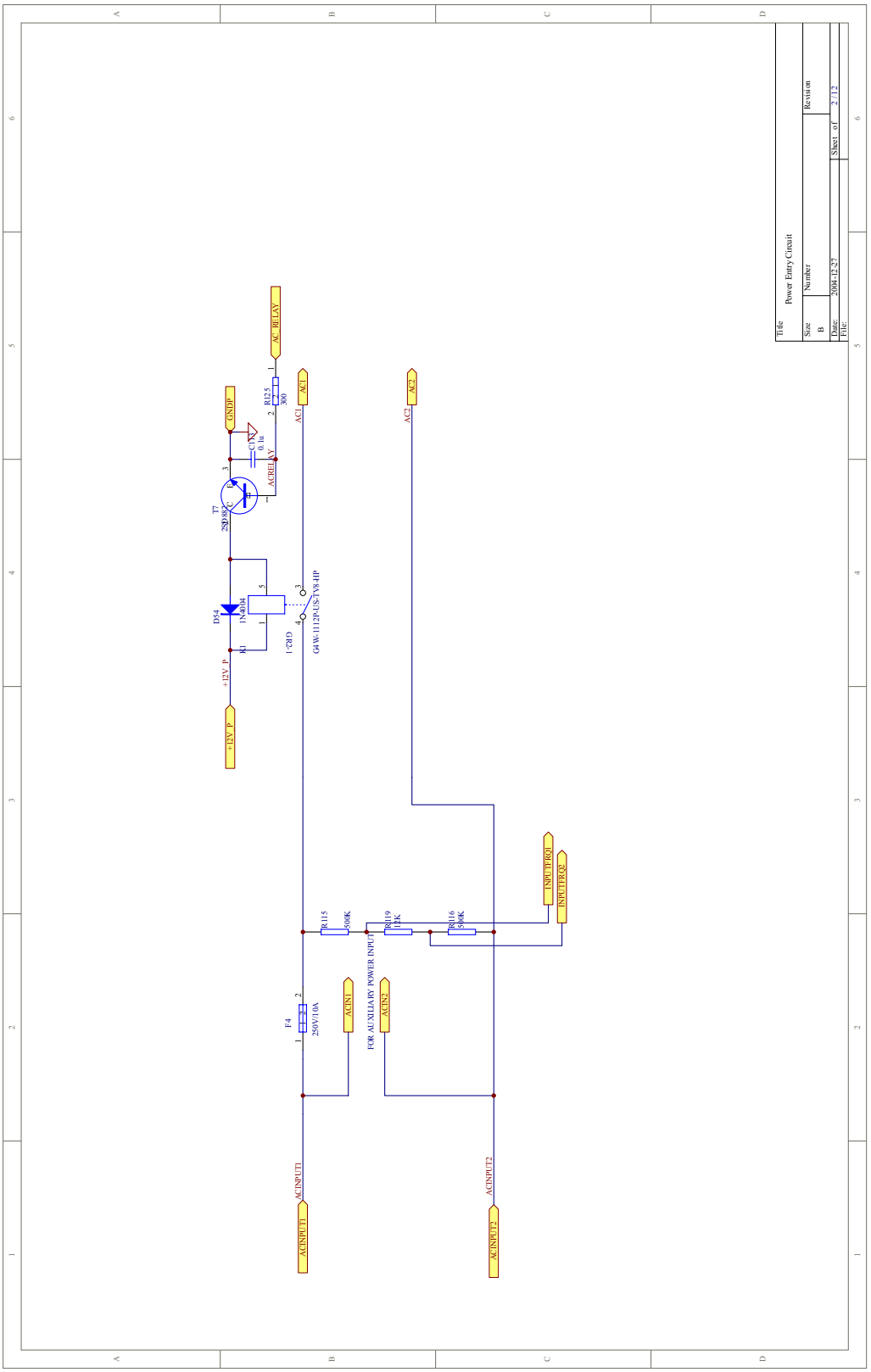


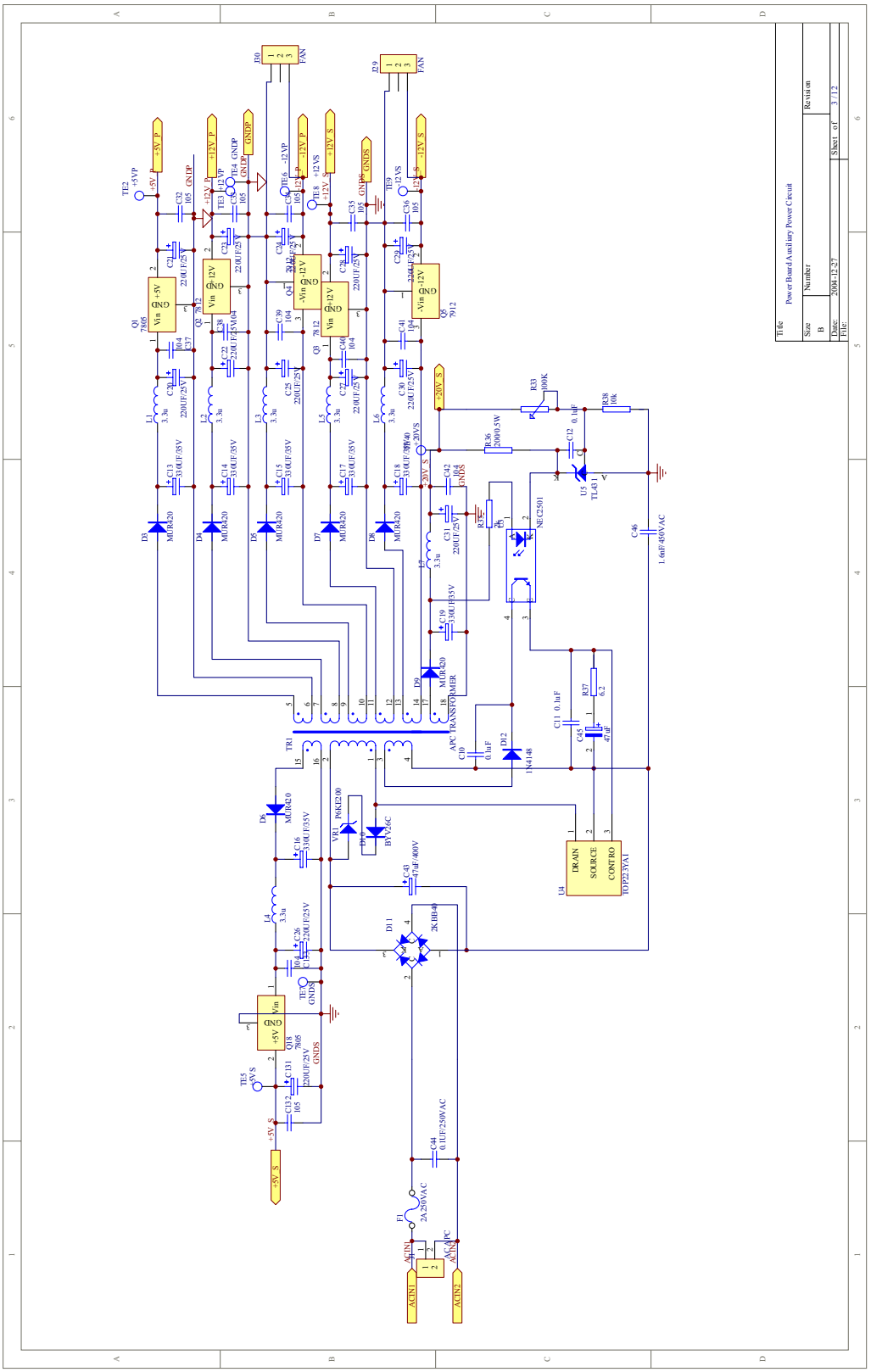
Schematics, Rev. 0


DIGITAL TO ANALOG CONVERTER
Title
Size
A
Number
Revision
3.0
Date: 2004-12-27
Sheet of 3 / 7
File:
SET TO 2.7V
+DAREF
C37
0.1uF
+3.3VA
R28
1K
GND_A
U6
MAX5251BEAP
VDD
DIN
DOUT
SCLK
CS
CL
PDL
DGND
FBA
OUTA
OUTB
FBB
REFAB
REFCD
FBC
OUTC
OUTD
FBD
UPO
AGND
DACOUTA
DACOUTB
DACOUTC
DACOUTD
DACTEST
DACDATA
DACCLK
/DACEN
/RESETD
+3.3V_DSP
GND_D
R27 5.1K
C36
0.1uF
MAX5251(U6)

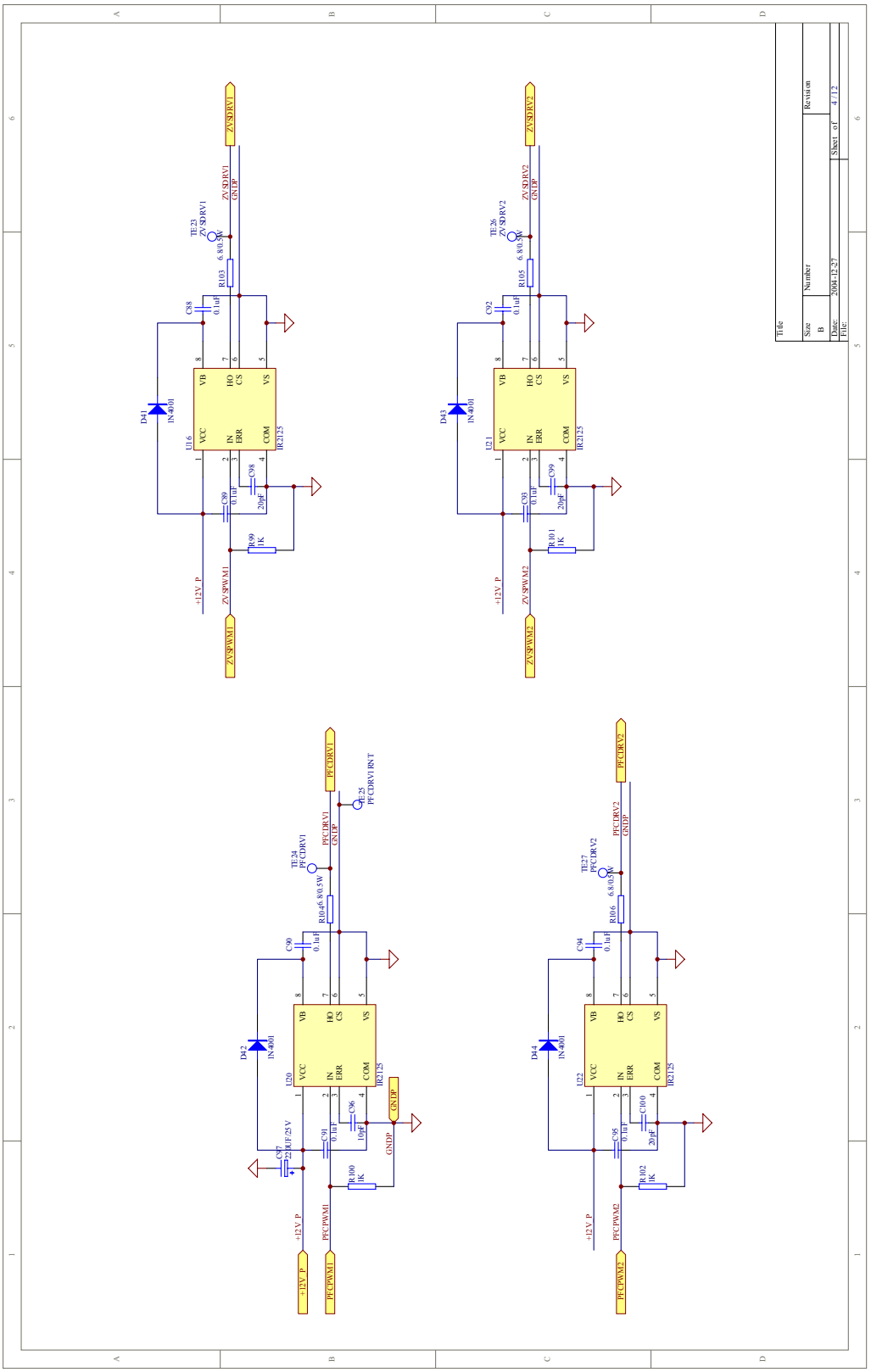


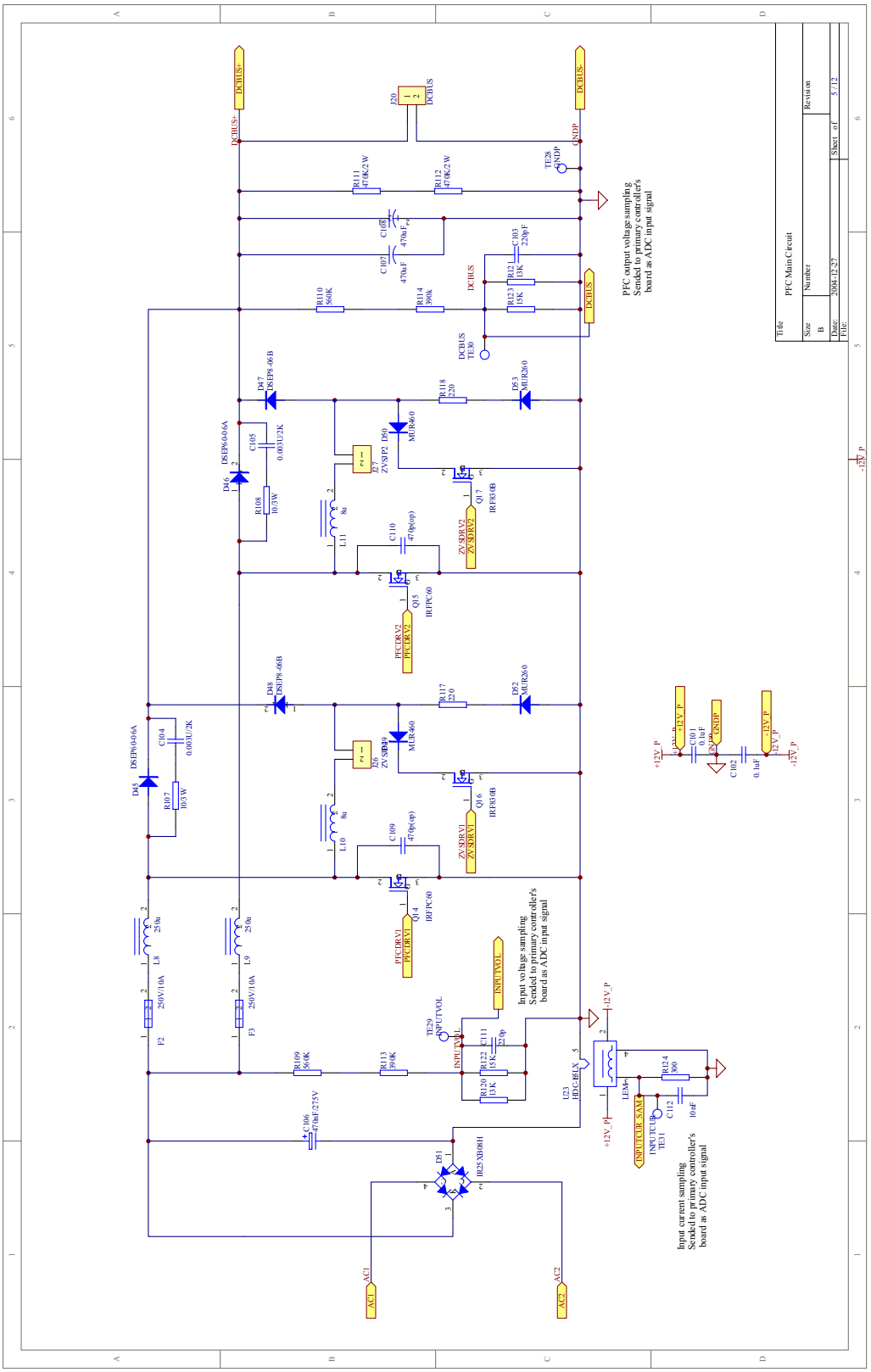
Schematics, Rev. 0


Power Entry Circuit
AC_RELAY
GNDP
+12V_P
ACRELAY
ACINPUT1
ACINPUT2
FOR AUXILIARY POWER INPUT
INPUTFREQ0
INPUTFREQ1

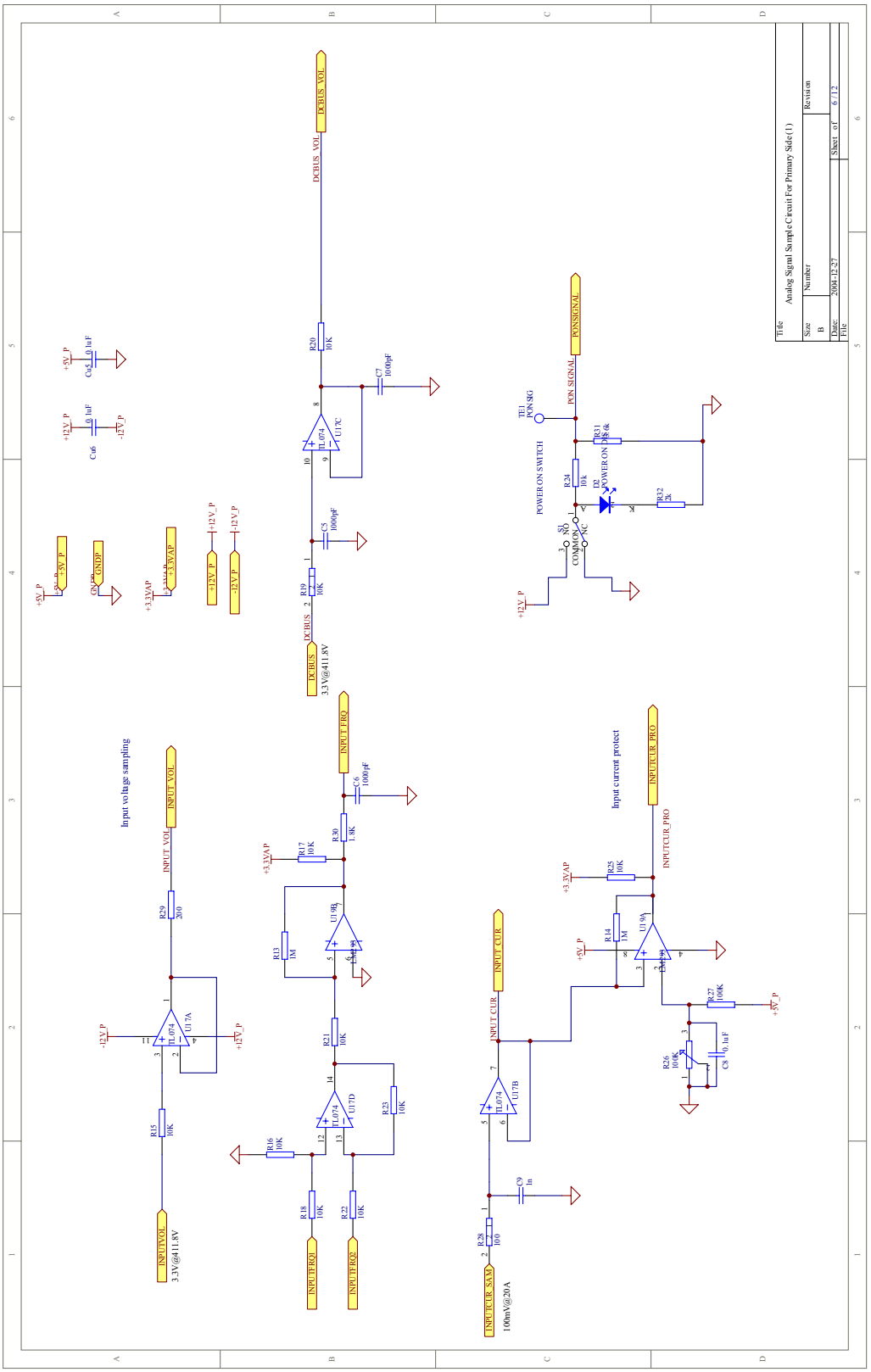


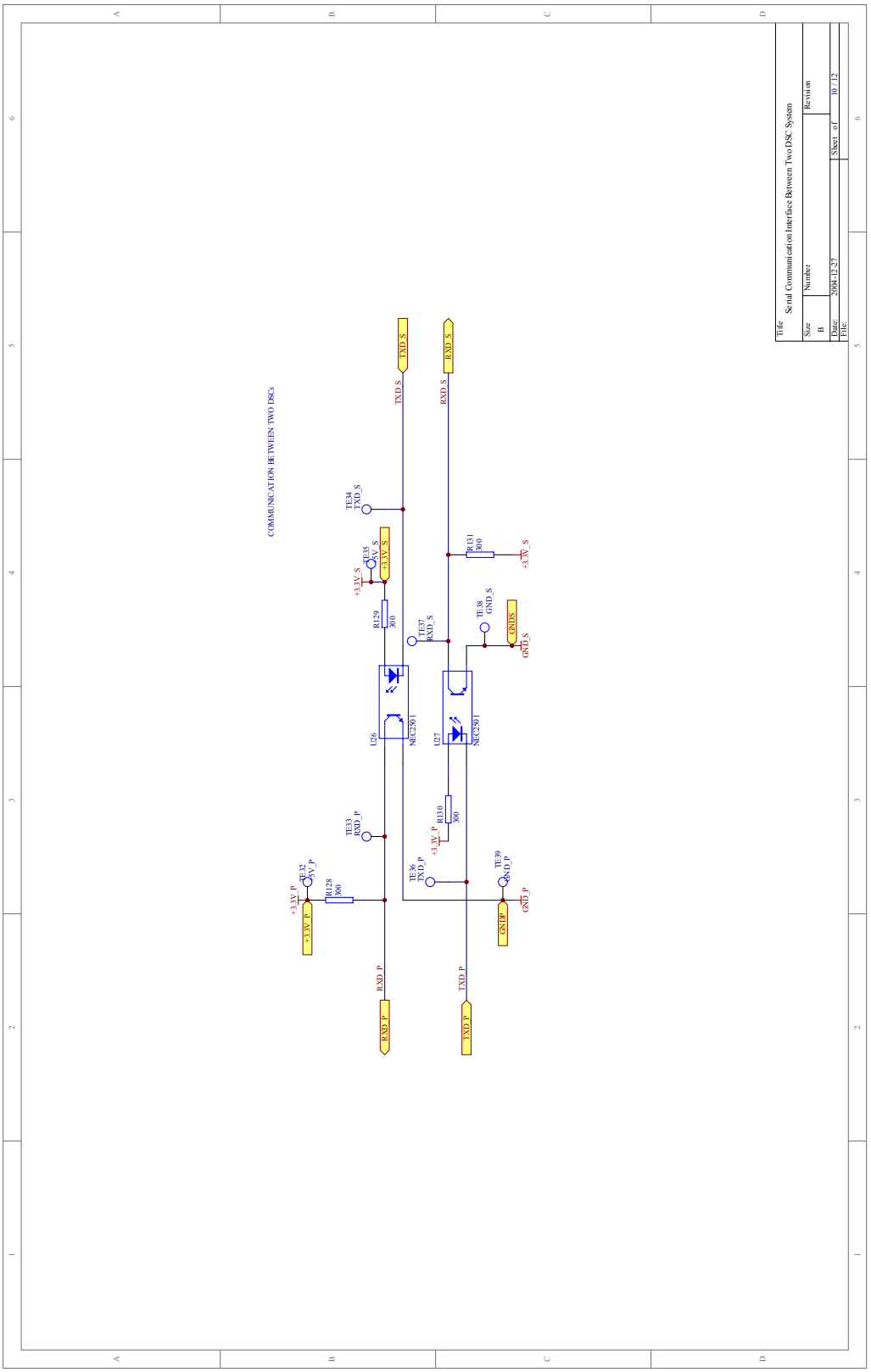
Schematics, Rev. 0


ZVSDRV1
ZVSDRV2
PFCDRV1
PFCDRV2
+12V_P
GNDP
IR2125
IN4001
Title
Number
Revision
Sheet 1 of 1
Date: 2004-12-27
File:
Size
B

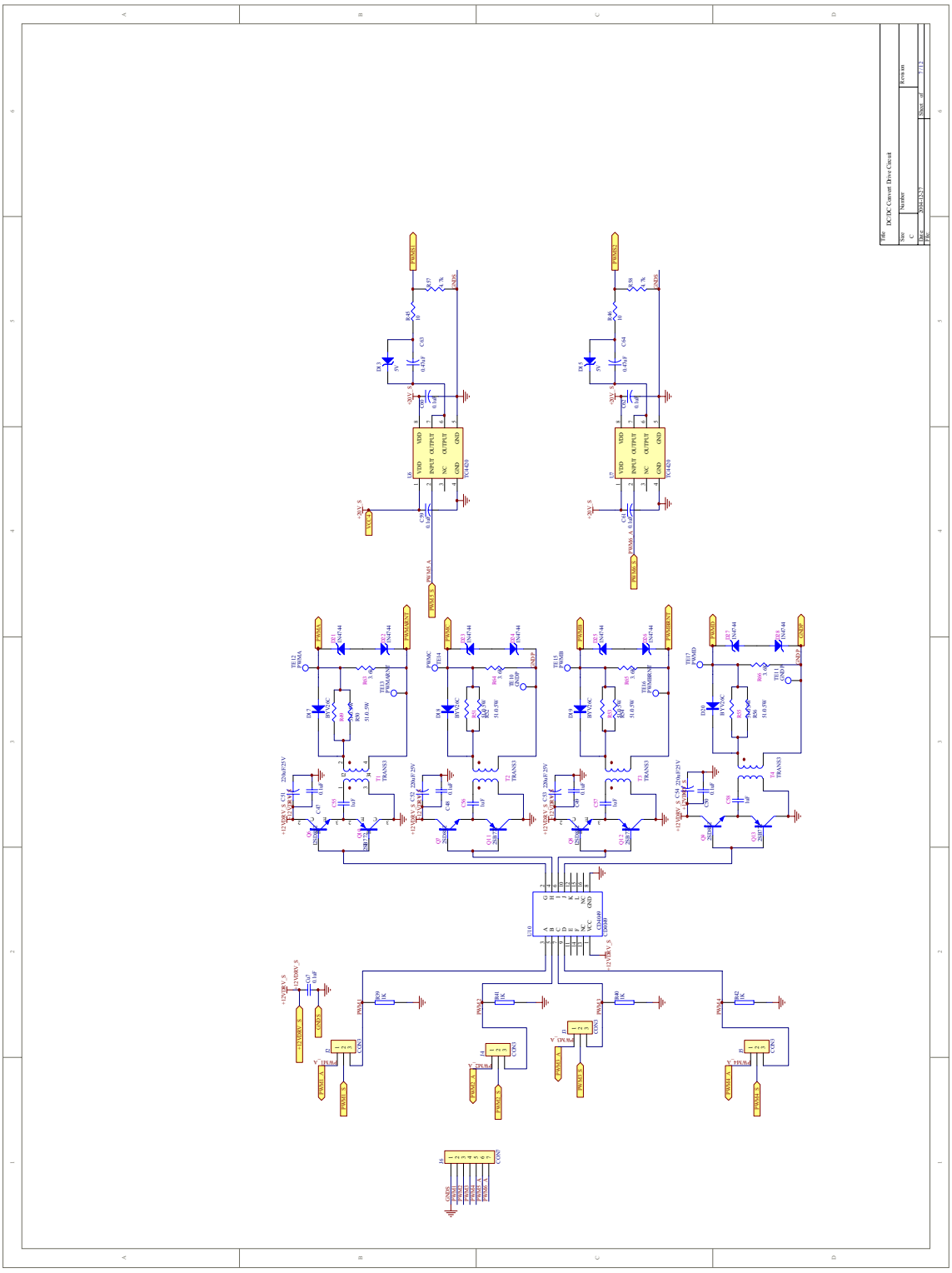


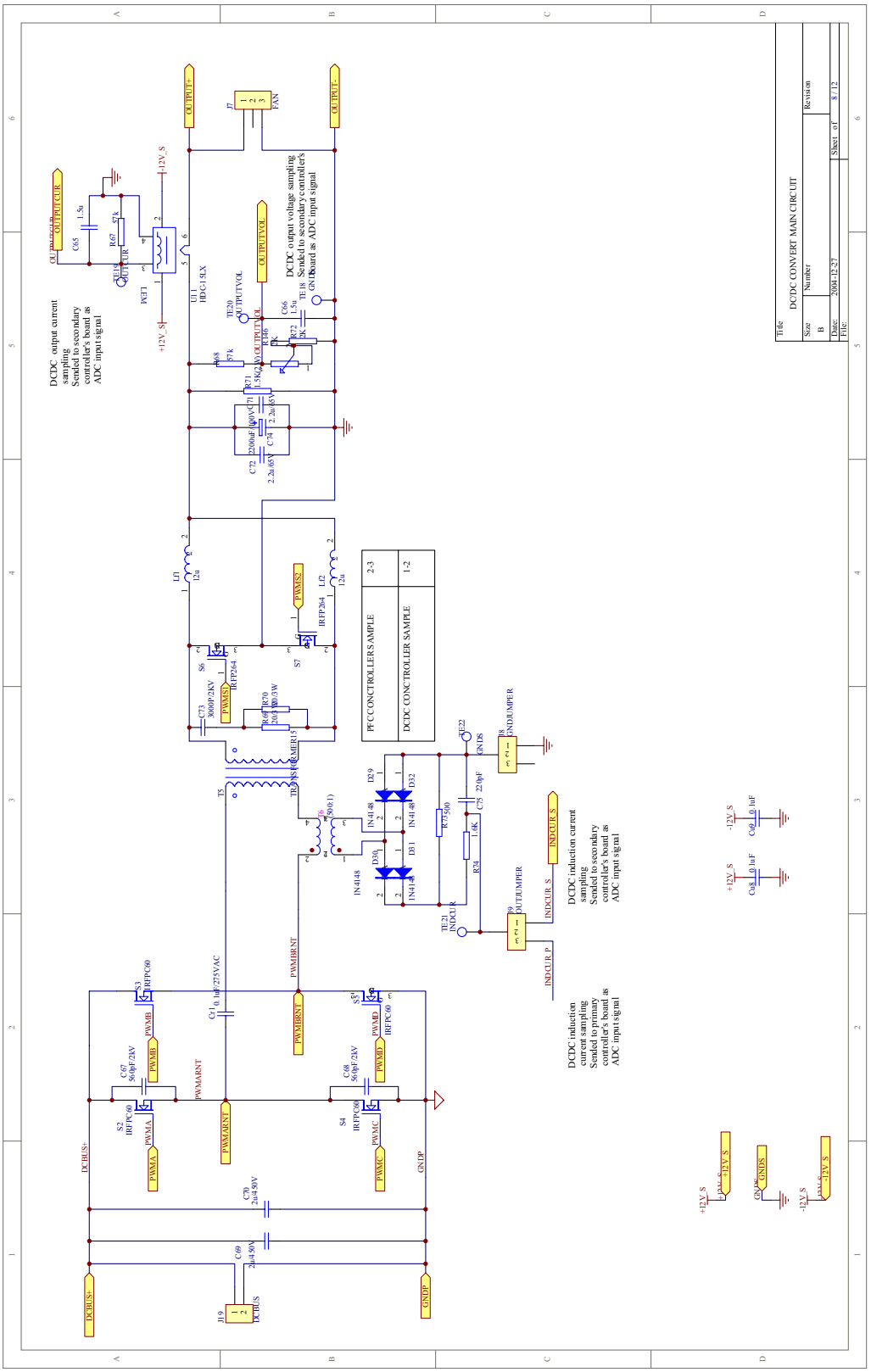
Schematics, Rev. 0


Analog Signal Sample Circuit For Primary Side(1)
DCBUS_VOL
PONSIGNAL
INPUT_FBQ
INPUT_VOL
INPUT_CUR
INPUTCUR_PRO
Input voltage sampling
Input current protect
POWER ON SWITCH
3.3V@411.8V
100mV@20A

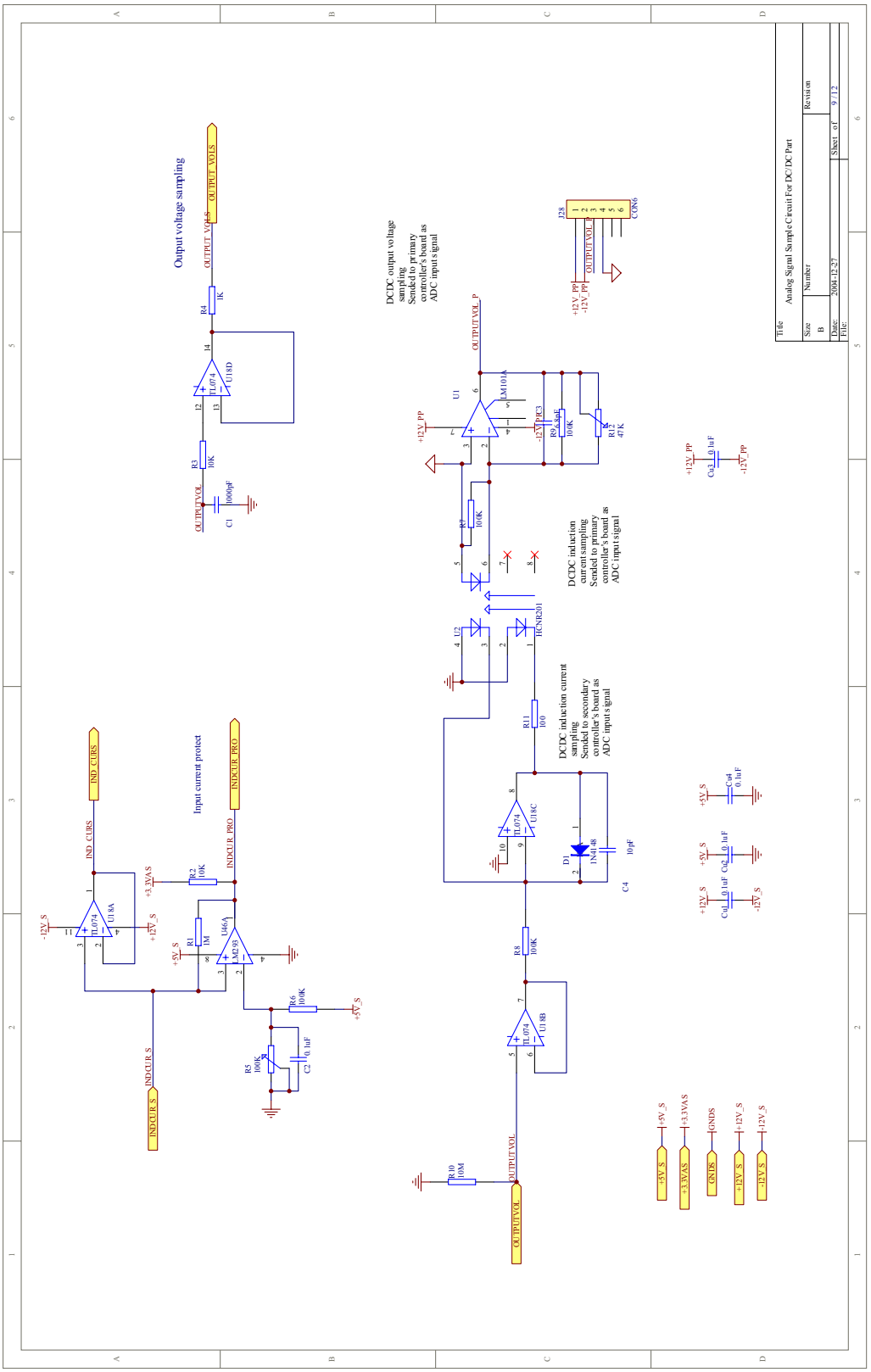


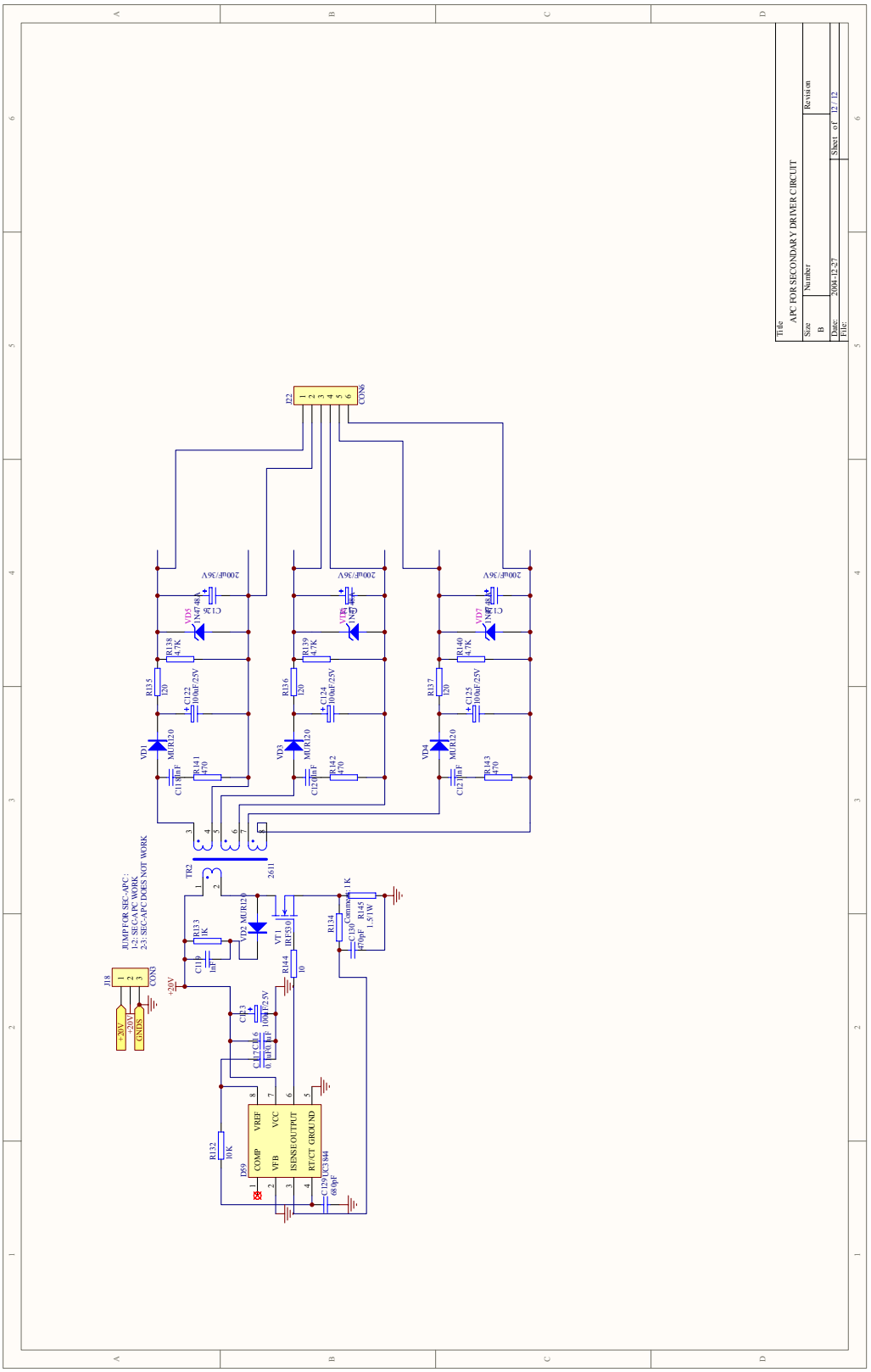
Schematics, Rev. 0



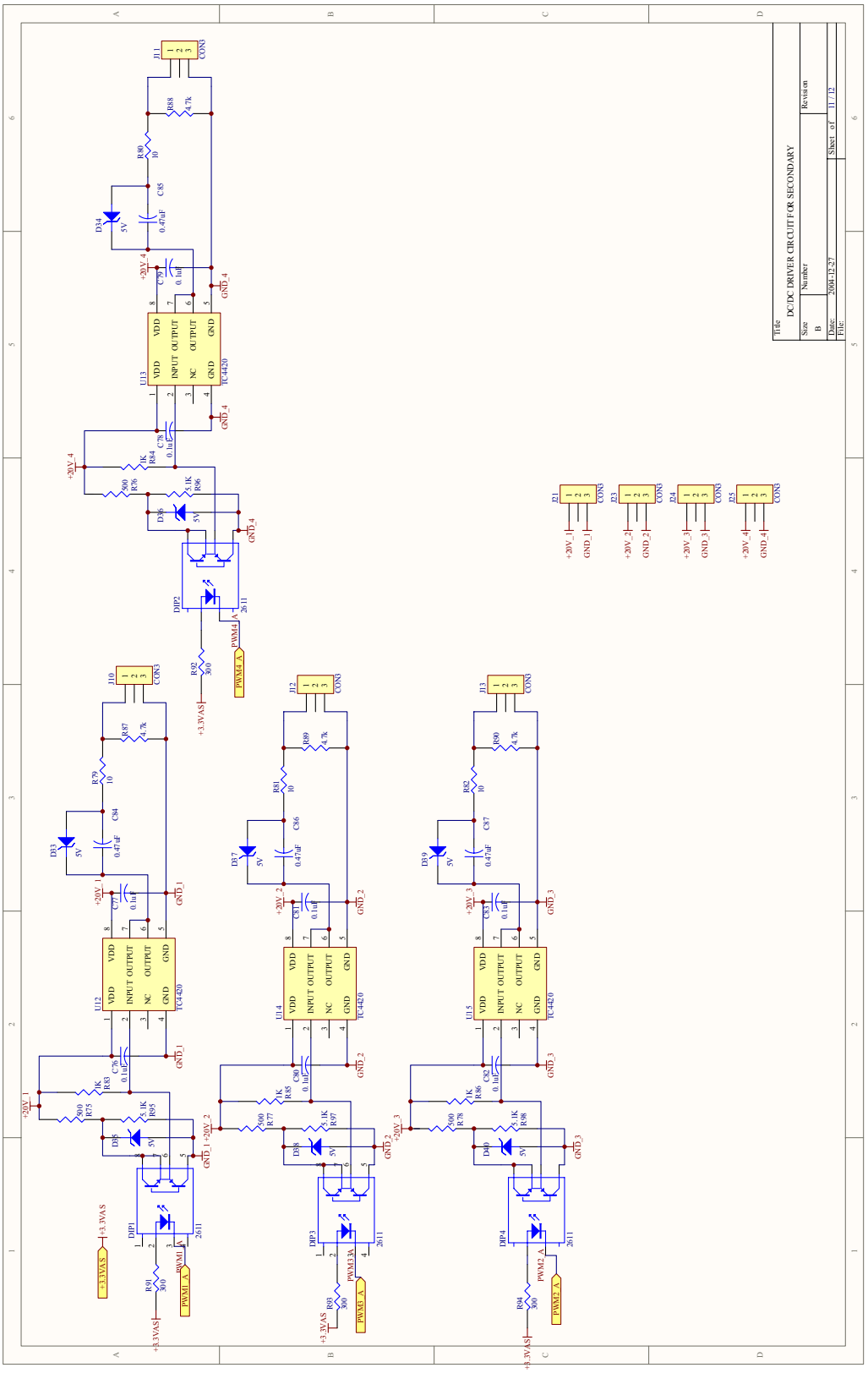


Schematics, Rev. 0


Output voltage sampling
DCDC output voltage sampling Sended to primary controller's board as ADC input's signal
DCDC induction current sampling Sended to primary controller's board as ADC input signal
DCDC induction current sampling Sended to secondary controller's board as ADC input signal
Input current protect
Analog Signal Simple Circuit For DC/DC Part



Schematics, Rev. 0


DC/DC DRIVER CIRCUIT FOR SECONDARY
Size
B
Number
Revision
Date: 2004-12-27
Sheet of 11 / 12
File:
TC4420
CON3
CON2
2611
5V
+20V_1
+20V_2
+20V_3
+20V_4
GND_1
GND_2
GND_3
GND_4
+3.3VAS
PWM1_A
PWM2_A
PWM3_A
PWM4_A

Appendix B
SMPS Bill of Materials

Controller Board					
Designator	**Comment**	**Footprint**	**Description**	**Library Reference**	**Quantity**
C1—C8, C10—C14, C16, C17, C36, C37, C39	0.1μF	1206C	Capacitor	CAP	18
C9, C15, C18, C38	47μF/10V	4025T	Capacitor	CAPACITOR POL	4
C19—C21, C24, C28, C31	0.1μF	1206C	Capacitor	CAPACITOR	6
C22, C23, C25, C29	2.2μF	1206C	Capacitor	CAPACITOR	4
C26	100pF	1206C	Capacitor	CAPACITOR	1
C27	0.001μF	1206C	Capacitor	CAPACITOR	1
C30, C32—C35	2.2nF	1206C	Capacitor	CAPACITOR	5
D1	Green LED	1808LED		LED	1
D2	FM4001	3216d	Diode	FM4001	1
D3, D4, D19, D21, D22	1N4148	3216d	Diode	1N4148	5
D5, D6	Red LED	1808LED		LED	2
D7—D12	Green LED	1808LED		LED	6
D13—D18	BAV99	SOT-23	Double Diode	BAV99	6
D20	1N4733	3216D	Zener Diode	ZENER3	1
J1	DIN64	DIN64RA		DIN64	1
J2	JTAG	IDC14		HEADER 7x2	1
J3	SCI TAG	IDC8		HEADER 4x2	1

Controller Board (Continued)					
Designator	**Comment**	**Footprint**	**Description**	**Library Reference**	**Quantity**
J4	I2C PORT	SIP2	Connector	CON2	1
J5	AD SET	IDC8	Connector	CON8	1
J6	DA-TAG	IDC8		Header 4x2	1
L1—L3	1μh	3225L		INDUCTOR1	3
R1, R2	5.6K	1206R		RES2	2
R3	300	1206R		RES2	1
R4—R8, R11, R13, R29	10K	1206R		RES2	8
R9, R10, R15—R20	300	1206R		RES2	8
R12, R30	47K	1206R		RES2	2
R14	1K	1206R		RES2	1
R21—R26	100	1206R		RES2	6
R27	5.1K	1206R		RES2	1
R28	1K	VR	Potentiometer	POT2	1
RP1	8 x 5K	SIP9		RESPACK8	1
S1	RESET PUSHBUTTON	KG		SW-PB	1
TE1	GND_D	SIP-1		TESTPORT	1
TE2	+3.3V	SIP-1		TESTPORT	1
TE3	PFCPWM1	SIP-1		TESTPORT	1
TE4	PFCPWM2	SIP-1		TESTPORT	1
TE5	PWM1	SIP-1		TESTPORT	1
TE6	PWM2	SIP-1		TESTPORT	1
TE7	PWM3	SIP-1		TESTPORT	1
TE8	PWM4	SIP-1		TESTPORT	1
TE9	IPUT_VOL	SIP-1		TESTPORT	1
TE10	INPUT_CUR	SIP-1		TESTPORT	1

Controller Board (Continued)					
Designator	**Comment**	**Footprint**	**Description**	**Library Reference**	**Quantity**
TE11	DCBUS	SIP-1		TESTPORT	1
TE12	IND_CUR	SIP-1		TESTPORT	1
TE13	OUTPUT_VOL	SIP-1		TESTPORT	1
TE14	OUTPUT_CUR	SIP-1		TESTPORT	1
TE15	DAOUTA	SIP-1		TESTPORT	1
TE16	DAOUTB	SIP-1		TESTPORT	1
TE17	DAOUTC	SIP-1		TESTPORT	1
TE18	DAOUTD	SIP-1		TESTPORT	1
TE19	DACTEST	SIP-1		TESTPORT	1
TE20	GND_A	SIP-1		TESTPORT	1
TE21	ZVSPWM1	SIP-1		TESTPORT	1
TE22	ZVSPWM2	SIP-1		TESTPORT	1
TE23	GNDA	SIP-1		TESTPORT	1
U1	MC33629DT-3.3	SO-8		MC33629DT-3.3	1
U2	MC74HC00	SO-14	Quad 2-IN Pos Nand G	MC74F00	1
U3	56F8323	LQFP64	MC56F8323	56F8323	1
U4	MC74HC244	SO20-300		74LS244	1
U5	MC74HC04	SO-14	Hex Inverters	MC74F04	1
U6	MAX5251BEAP	SSOP20		MAX5251BEAP	1
U7	MC74HC244	SO20-300		74LS244	1
U8	MAX7221	SOL-24		MAX7221	1
U9, U10	FYQ-3641A	LG3641AH		7-SEG	2

Power Board					
Designator	**Comment**	**Footprint**	**Description**	**Library Reference**	**Quantity**
C1, C5—C7	1000pF	RAD0.2	Capacitor	CAP	4
C2, C8, C10—C12, C47—C50, C59—C62, C76—C83 C88—C95, C101, C102, C116, C117, Cu1—Cu9	0.1μF	RAD0.2	Capacitor	CAPACITOR	42
C3	6.8pF	RAD0.2	Capacitor	CAP	1
C4	10pF	RAD0.2	Capacitor	CAP	1
C9	1n	RAD0.2	Capacitor	CAP	1
C13—C19	330μF/35V	CAP RB5/10		ELECTRO	7
C20—C31	220μF/25V	RB3/8		ELECTRO	12
C32—C36, C132	105pF	RAD0.2		CAP	6
C37—C42, C133	104pF	RAD0.2		CAP	7
C43	47μF/400V	RB10/22.4		ELECTRO	1
C44	0.1μF/250VAC	RAD15/18/6	Capacitor	CAP	1
C45	47μF	RB2.5/5		ELECTRO2	1
C46	1.6nF/450VAC	RAD0.4	Capacitor	CAP	1
C51—54	220μF/25V	RB3/8	Capacitor	CAPACITOR POL	4
C55—C58	1μF	RAD0.2	Capacitor	CAP	4
C63, C64, C84—C87	0.47μF	RAD0.2	Capacitor	CAPACITOR	6
C65, C66	1.5μ	RAD0.2	Capacitor	CAP	2
C67, C68	560pF/2kV	RAD0.3	Capacitor	CAP	2
C69, C70	2μ/450V	RAD27/30/14	Capacitor	CAP	2
C71, C72	2.2μ/65V	RAD10/13/6	Capacitor	CAP	2

Power Board (Continued)					
Designator	**Comment**	**Footprint**	**Description**	**Library Reference**	**Quantity**
C73	3000P/2KV	RAD0.3	Capacitor	CAP	1
C74	2200μF/100V	RB10.5/30	Electrolytic Capacitor	ELECTRO1	1
C75, C103	220pF	RAD0.2	Capacitor	CAP	2
C96	10pF	RAD0.2	Capacitor	CAP	1
C97, C131	220μF/25V	RB3/8		ELECTRO	2
C98—C100	20pF	RAC0.2	Capacitor	CAP	3
C104, C105	0.003μ/2K	RAD10/13/6	Capacitor	CAP	2
C106	470nF/275V	RAD22/26/9		ELECTRO	1
C107, C108	470μF	RB10/35	Capacitor	CAPACITOR	2
C109, C110	470p(op)	RAD0.2	Capacitor	CAP	2
C111	220p	RAD0.2	Capacitor	CAP	1
C112	10nF	RAD0.2	Capacitor	CAP	1
C113	0.1μ	RAD0.2	Capacitor	CAP	1
C114, C115	47μF	RB2.5/5	Capacitor	CAPACITOR POL	2
C118—C121	1nF	RAD0.2		CAP	4
C122—C125	100μF/25V	RB3/8		ELECTRO	4
C126—C128	200μF/36V	RB3/8		ELECTRO	3
C129	680pF	RAD0.2		CAP	1
C130	470pF	RAD0.2		CAP	1
Cr1	0.1μF/275VAC	RAD15/18/6	Capacitor	CAP	1
D1, D12, D29—D32	1N4148	DIODE0.4	Diode	DIODE	6
D2	POWER ON DIS	LEDA		LED	1
D3—D9	MUR420	DIODE0.5		DIODE1	7
D10	BYV26C	DIODE0.4		DIODE1	1
D11	2KBB40	2KBB40	Full Wave Diode Bridge	Bridge1	1

Power Board (Continued)					
Designator	**Comment**	**Footprint**	**Description**	**Library Reference**	**Quantity**
D13, D15, D33—D40	5V	DIODE0.4	Zener Diode	ZENER3	10
D17—D20	BYV26C	DIODE0.4		DIODE2	4
D21—D28	1N4744	DIODE0.4	Zener Diode	ZENER3	8
D41—D44	1N4001	DIODE0.4	Diode	DIODE	4
D45, D46	DSEP60-06A	TO247AD		DIODE1	2
D47, D48	DSEP8-06B	TO220AC		DIODE1	2
D49, D50	MUR460	DIODE0.5		DIODE1	2
D51	IR25XB08H	IR25XB	Full Wave Diode Bridge	Bridge1	1
D52, D53	MUR260	D-E		DIODE1	2
D54	1N4004	CASE 267-03		DIODE1	1
D55, D56	1N4001	DIODE0.4	Diode	FM4001	2
D57	5V_P DIS	LEDA		LED	1
D58	+5V_S DIS	LEDA		LED	1
D59	UC3844	DIP8	UC3844		1
DIP1—DIP4	HCPL2611	DIP8		OPTOISO3	4
F1	2A250VAC	FUSE20/5/7		D-FOR3.SCH_5A250V_116	1
F2—F4	250V/10A	FUSE20/5/7	Fuse	FUSE1	3
J1	AC APC	CON5/3.96	Connector	CON2	1
J2—J5, J10—J13, J18, J21, J23—J25	CON3	SIP3	Connector	CON3	13
J6	CON7	SIP7	Connector	CON7	1
J7	FAN	CON3/2.54	Connector	CON3	1
J8	GNDJUMPER	SIP3		CON3R	1
J9	OUTJUMPER	SIP3		CON3R	1
J14	ACINPUT	CON5/3.96	Connector	CON2	1

Power Board (Continued)					
Designator	**Comment**	**Footprint**	**Description**	**Library Reference**	**Quantity**
J15	DCOUTPUT	OUTTAG	Connector	CON2	1
J16	DIP64_S	DIN64RA-CON		DIN64	1
J17	DIP64_P	DIN64RA-CON		DIN64	1
J19, J20	DCBUS	CON5/3.96	Connector	CON2	2
J22	CON6	SIP6	Connector	CON6	1
J26, J27	ZVSJP2	CON2/3.96	Connector	CON2	2
J28	CON6	SIP4	Connector	CON6	1
J29, J30	FAN	CON3/2.54	Connector	CON3	2
K1	G4W-1112P-US-TV8-HP	GR2L-1		RELAY-SPDT(1C)	1
L1—L7	3.3μ	IND 3.3μ		INDUCTOR1	7
L8, L9	250μ	CORE EI33		INDUCTOR IRON	2
L10, L11	8μ	IND-EE25.4		INDUCTOR IRON	2
L12, L13	10μH	AXIAL0.4		INDUCTOR	2
Lf1, Lf2	12μ	IND-EI33		INDUCTOR	2
Q1, Q18	LM7805	TO220V		Component_1	2
Q2, Q3	LM7812	TO220V		7812	2
Q4, Q5	LM7912	TO220V		7912	2
Q6—Q9	2SD882	882	NPN Transistor	NPN	4
Q10—Q13	2SB772	772	PNP Transistor	PNP	4
Q14, Q15	IRFPC60	TO247AC		MOSFET N	2
Q16, Q17	IRF830B	TO220AB		MOSFET N	2
R1	1M	AXIAL0.4		RES2	1
R2, R3, R15—R23, R25, R132	10K	AXIAL0.4		RES2	13

Power Board (Continued)					
Designator	**Comment**	**Footprint**	**Description**	**Library Reference**	**Quantity**
R4, R39—R42, R99—R102, R133, R134	1K	AXIAL0.4		RES2	11
R5, R26, R33	100K	VRESLV		RES-VRAU	3
R6—R9	100K	AXIAL0.4		RES2	4
R10	10M	AXIAL0.4		RES2	1
R11	100 Ohm	AXIAL0.4		RES2	1
R12	47K	VRESLV		RES-VRAU	1
R13, R14	1M	AXIAL0.4		RES2	2
R24, R38	10k	AXIAL0.4		RES2	2
R27	100K	AXIAL0.4		RES2	1
R28	100 Ohm	AXIAL0.4		RES2	1
R29	200 Ohm	AXIAL0.4		RES2	1
R30	1.8K	AXIAL0.4		RES2	1
R31	3.6k	AXIAL0.4		RES2	1
R32	2k	AXIAL0.4		RES2	1
R35	2k	AXIAL0.4		RES2	1
R36	200/0.5W	AXIAL0.5		RES2	1
R37	6.2 Ohm	AXIAL0.4		RES2	1
R45	10 Ohm	AXIAL0.4		RES1	1
R46	10 Ohm	AXIAL0.4		RES1	1
R49—R56	51/0.5W	AXIAL0.5		RES1	8
R57, R58, R87—R90	4.7k	AXIAL0.4		RES1	6
R63	3.6k	AXIAL0.4		RES1	1
R64—R66	3.6K	AXIAL0.4		RES1	3
R67, R68	56k	AXIAL0.4		RES2	2

Power Board (Continued)					
Designator	**Comment**	**Footprint**	**Description**	**Library Reference**	**Quantity**
R69, R70	20/3W	R2WV		RES2	2
R71	1.5K(2W)	R2WV		RES2	1
R72	2K	AXIAL0.4		RES2	1
R73	500 Ohm	AXIAL0.4		RES2	1
R74	1.6K	AXIAL0.4		RES2	1
R75—R78	500 Ohm	AXIAL0.4		RES1	4
R79—R82	10 Ohm	AXIAL0.4		RES1	4
R83—R86	1K	AXIAL0.4		RES1	4
R91—R94	300 Ohm	AXIAL0.4		RES1	4
R95—R98	5.1K	AXIAL0.4		RES1	4
R103—R106	6.8/0.5W	AXIAL0.5		RES2	4
R107, R108	10/3W	R2WV		RES2	2
R109, R110	560K	AXIAL0.4		RES2	2
R111, R112	470K/2W	R2WV		RES2	2
R113	390K	AXIAL0.4		RES2	1
R114	390k	AXIAL0.4		RES2	1
R115, R116	500K	AXIAL0.4		RES2	2
R117, R118	220 Ohm	AXIAL0.4		RES2	2
R119	12K	AXIAL0.4		RES2	1
R120, R121	13K	AXIAL0.4		RES2	2
R122, R123	15K	AXIAL0.4		RES2	2
R124—R131	300 Ohm	AXIAL0.4		RES2	8
R135—R137	120 Ohm	AXIAL0.4		RES2	3
R138—R140	4.7K	AXIAL0.4		RES2	3
R141—R143	470 Ohm	AXIAL0.4		RES2	3
R144	10 Ohm	AXIAL0.4		RES2	1

Power Board (Continued)					
Designator	**Comment**	**Footprint**	**Description**	**Library Reference**	**Quantity**
R145	1.5/1W	R2WV		RES2	1
R146	2K	VRESLV		RES-VRAU	1
S1	POWER ON SWITCH	CON3/2.54		SW SPDT	1
S2—S5	IRFPC60	TO247AC		MOSFET N	4
S6, S7	IRFP264	TO247AC		MOSFET N	2
T1—T4	TRANS3	DRVTRAN		TRANS3	4
T5	TRANSFORMER15	TRAN-EI40		TRANSFORMER15	1
T6	(500:1)	CURTRAN		TRANS3	1
T7	2SD882	882	NPN Transistor	NPN	1
TE1	PONSIG	SIP-1		TESTPORT	1
TE2	+5VP	SIP-1		TESTPORT	1
TE3	+12VP	SIP-1		TESTPORT	1
TE4	GNDP	SIP-1		TESTPORT	1
TE5	+5VS	SIP-1		TESTPORT	1
TE6	-12VP	SIP-1		TESTPORT	1
TE7	GNDS	SIP-1		TESTPORT	1
TE8	+12VS	SIP-1		TESTPORT	1
TE9	-12VS	SIP-1		TESTPORT	1
TE10, TE11, TE28	GNDP	SIP-1		TESTPORT	3
TE12	PWMA	SIP-1		TESTPORT	1
TE13	PWMARNT	SIP-1		TESTPORT	1
TE14	PWMC	SIP-1		TESTPORT	1
TE15	PWMB	SIP-1		TESTPORT	1
TE16	PWMBRNT	SIP-1		TESTPORT	1
TE17	PWMD	SIP-1		TESTPORT	1

Power Board (Continued)					
Designator	**Comment**	**Footprint**	**Description**	**Library Reference**	**Quantity**
TE18, TE22	GNDS	SIP-1		TESTPORT	2
TE19	OUTCUR	SIP-1		TESTPORT	1
TE20	OUTPUTVOL	SIP-1		TESTPORT	1
TE21	INDCUR	SIP-1		TESTPORT	1
TE23	ZVSDRV1	SIP-1		TESTPORT	1
TE24	PFCDRV1	SIP-1		TESTPORT	1
TE25	PFCDRV1RNT	SIP-1		TESTPORT	1
TE26	ZVSDRV2	SIP-1		TESTPORT	1
TE27	PFCDRV2	SIP-1		TESTPORT	1
TE29	INPUTVOL	SIP-1		TESTPORT	1
TE30	DCBUS	SIP-1		TESTPORT	1
TE31	INPUTCUR	SIP-1		TESTPORT	1
TE32	+5V_P	SIP-1		TESTPORT	1
TE33	RXD_P	SIP-1		TESTPORT	1
TE34	TXD_S	SIP-1		TESTPORT	1
TE35	+5V_S	SIP-1		TESTPORT	1
TE36	TXD_P	SIP-1		TESTPORT	1
TE37	RXD_S	SIP-1		TESTPORT	1
TE38	GND_S	SIP-1		TESTPORT	1
TE39	GND_P	SIP-1		TESTPORT	1
TE40	+20VS	SIP-1		TESTPORT	1
TR1	APC TRANSFORMER	TRAN-EI33-2		TRANSFORMER 8	1
TR2	2611	TRAN-EI25		TRANSFORMER 5	1
U1	LM101A	DIP8		741	1
U2	HCNR201	DIP8EXB		HCNR201	1
U3	NEC2501	DIP4		OPTOISO1	1

Power Board (Continued)					
Designator	**Comment**	**Footprint**	**Description**	**Library Reference**	**Quantity**
U4	TOP223YAI	TO-220		D-FOR3.SCH_TOP_202	1
U5	TL431	TL431		TL431	1
U6, U7, U12—U15	TC4420	DIP8	Generic Driver Module	TC4420	6
U10	CD4049	DIP16	CD4049	CD4049	1
U11	HDC-15LX	HLX-15		HE	1
U16	IR2125	DIP8		IR2125	1
U17, U18	TL074	DIP14	Op-Amp Quad	LF444A	2
U19	LM293	DIP8		LM193	1
U20—U22	IR2125	DIP8		IR2125	3
U23	HDC-15LX	HLX-15		HE	1
U24, U25	MC33269DT-3.3	TO220AB		MC33269DT-3.3(TO220)	2
U26, U27	NEC2501	DIP4		NEC2501	2
U46	LM293	DIP8		LM193	1
VD1—VD4	MUR120	DIODE0.4	Diode	DIODE	4
VD5—VD7	IN4748A	DIODE0.4	Zener Diode	ZENER3	3
VR1	P6KE200	DIODE0.4	Zener Diode	ZENER3	1
VT1	IRF530	TO220V		MOSFET-N	1

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