PMSM and BLDC Sensorless Motor Control using the 56F8013 Device

Designer Reference Manual

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16-bit Digital Signal Controllers

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PMSM and BLDC Demonstration using the 56F8013 Device

Designer Reference Manual

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
11/2005	0	Initial release	N/A

TABLE OF CONTENTS

Chapter 6
Hardware Implementation

Chapter 7
Software Design

Chapter 8
JTAG Simulation and SCI Communication

Chapter 9
Operation

LIST OF FIGURES

LIST OF TABLES

About This Document

This manual describes the use of a 56F8013 device in a Permanent Magnet Synchronous Motor (PMSM) and Brushless DC (BLDC) motor demonstration.

Audience

This manual targets design engineers interested in developing a PMSM vector control and BLDC control drive application.

Organization

This User's Manual consists of the following sections:

- **Chapter 1, Introduction,** explains how a PMSM, a BLDC and a 56F8013 device facilitate a vector control drive design.
- **Chapter 2, Benefits and Features of the 56F8013 Controller,** highlights the advantages in using a 56F8013 controller.
- **Chapter 3, Motor Drive System,** details the features and design of a motor drive system.
- **Chapter 4, PMSM Theory,** describes software, control and configuration of an Permanent Magnet Synchronous Motor.
- **Chapter 5, Design Concept of a PMSM Vector Control Drive and BLDC Control Drive,** details the design concept of PMSM and BLDC drives.
- **Chapter 6, Hardware Implementation,** describes how to set up the hardware needed for the PMSM and BLDC demonstration application.
- **Chapter 7, Software Design,** explains the software system design.
- **Chapter 8, JTAG Simulation and SCI Communication,** describes the application's debugging and communications functions.
- **Chapter 9, Operation,** explains how to use the application.
- **Appendix A, Schematics,** contains schematics for the PMSM and BLDC demonstration application.
- **Appendix B, PMSM and BLDC Demonstration Bill of Materials,** lists all parts used in the application.

Conventions

This document uses the following notational conventions:

Typeface, Symbol or Term	Meaning	Examples
`Courier Monospaced Type`	Code examples	`//Process command for line flash`
Italic	Directory names, project names, calls, functions, statements, procedures, routines, arguments, file names, applications, variables, directives, code snippets in text	...and contains these core directories: *applications* contains applications software... ...CodeWarrior project, *3des.mcp* is... ...the *pConfig* argument.... ...defined in the C header file, *aec.h*....
Bold	Reference sources, paths, emphasis	...refer to the **Targeting DSP56F83xx Platform** manual.... ...see: **C:\Program Files\Freescale\help\tutorials**
Blue Text	Linkable on-line	...refer to Chapter 7, License....
Number	Any number is considered a positive value, unless preceded by a minus symbol to signify a negative value	3V -10 DES^{-1}
ALL CAPITAL LETTERS	# defines/ defined constants	# define INCLUDE_STACK_CHECK
Brackets [...]	Function keys	...by pressing function key [F7]
Quotation marks, “...”	Returned messages	...the message, “Test Passed” is displayed.... ...if unsuccessful for any reason, it will return “NULL”...

Definitions, Acronyms, and Abbreviations

The following list defines the acronyms and abbreviations used in this document. As this template develops, this list will be generated from the document. As we develop more group resources, these acronyms will be easily defined from a common acronym dictionary. Please note that while the acronyms are in solid caps, terms in the definition should be initial capped ONLY IF they are trademarked names or proper nouns.

BLDC	Brushless DC Motor
ADC	Analog-to-Digital Conversion
COP	Computer Operating Properly
DCM	Discontinuous Current Mode
EMF	Electro-Magnetic Force
EVM	Evaluation Module
FOC	Field-Oriented Control
GPIO	General Purpose Input/Output
HMI	Human Machine Interface
I^2C or I2C	Inter-Integrated Circuit
IC	Integrated Circuit
IGBT	Insulated-Gate Bipolar Transistor
IM	Induction Motor
IPM	Integrated Power Module
ISR	Interrupt Service Routine
LPF	Low-Pass Filter
PFC	Power Factor Correction
PI	Proportional-Integral
PLL	Phase Locked Loop
PMSM	Permanent Magnet Synchronous Motor
PWM	Pulse Width Modulation or Modulator
RMS	Root Mean Square
SCI	Serial Communication Interface
SMO	Sliding Mode Observer
SPI	Serial Peripheral Interface
SV	Space Vector
SVPWM	Space Vector Pulse Width Modulation
V_{CE}	Collector to Emitter Voltage

Chapter 1
Introduction

1.1 Introduction

This manual describes the design of a 3-phase Permanent Magnet Synchronous Motor (PMSM) sensorless vector control drive and a Brushless DC (BLDC) Motor drive without postiion encoder coupled to the motor shaft. It uses a Freescale 56F8013 with Processor Expert™ (PE) software support.

A PMSM consists of a magnetic rotor and wound stator construction. Its wound stators can rapidly dissipate heat to the motor housing and environment. In contrast, a brush motor traps the heat under a non-conductive air gap, resulting in greater efficiency and power density for the PMSM design and providing high torque-to-inertia ratios. A PMSM motor generates magnetic flux using permanent magnets in the rotors, which are driven by the stators applying a synchronous rotational field. On the other hand, the flux that is applied by the stators (the armature-reaction flux) generates torque most effectively when it is perpendicular to flux generated by the rotors. To maintain near-perpendicularity between stator flux and rotor flux, two control methods with position-speed feedback loop are popularly used for controlling a PMSM: Field-Oriented Control and Brushless DC Control.

A PMSM abandons the excitation winding and the rotor turns at the same speed as the stator field. The PMSM's design eliminates the rotor copper losses, giving very high peak efficiency compared with a traditional induction motor. The power-to-weight ratio of a PMSM is also higher than induction machines. Progress in the field of power electronics and microelectronics enables the application of PMSMs for high-performance drives, where, traditionally, only DC motors were applied. Thanks to sophisticated control methods, a PMSM offers the same control capabilities as high performance four-quadrant DC drives.

A PMSM/BLDC is a excellent alternative in an appliance application. This application will employ sensorless Field-Oriented Control (FOC) to control a PMSM and a sensorless algorithm to control BLDC, using the 56F8013 device, which can accommodate the complicated sensorless FOC algorithm.

The PMSM/BLDC drive system will meet the air conditioning and compressor requirements while it runs. The system demonstrates the features of the 56F8013 in motor control. The flexible Human Machine Interface (HMI) communicates between the control board and a PC and its simplified form, using the push buttons on the processor board, make the system easy to use.

This drive application allows sensorless vector control of the PMSM and BLDC running in a dual closed-loop control without the speed/position sensor coupled to the shaft.

This document describes the Freescale 56F8013 controller's features, basic PMSM and BLDC theory, the system design concept, and hardware implementation and software design, including the PC master software visualization tool.

Chapter 2
Benefits and Features of the 56F8013 Controller

The 56F8000 family of devices offers an excellent complement of peripherals and a broad range of memory and packages.

2.1 Features

Some of the 56F8000 devices' benefits include:

- **High-performance 56800E Core**
  - Superior 16-bit, fixed-point signal processing performance provided by the bus architecture and the controller core
  - Excellent control and protocol processing capability and code density
  - Superior MCU control performance
- **Performance-leading Flash Memory**
  - Unbeatable, field-proven reliability in the harshest environments
  - Features that enable emulation of EEPROM
  - Flexible, full in-circuit Flash programmability
  - Performance-enhancing interfacing and bus structure, enabling the superior signal processing capability from Flash
  - Flash security protection features for IP protection
- **Voltage Regulator and Power Supervisor**
  - The chips come equipped with an on-board voltage regulator and power supervisor. When supplied with a 3.3V voltage, the chip creates all required internal voltages.
  - Includes features such as Power-On Reset (POR) and low-voltage detection, eliminating external components and saving system costs
- **On-chip Relaxation Oscillator**
  - Some 56F8000 devices are equipped with a precision on-chip, factory-trimmed oscillator (0.25% of 8MHz), enabling the elimination of an external crystal and providing system cost savings
- **On-Chip Clock Synthesis (OCCS)**
  - 56F8000 digital signal controllers are capable of using an external clock input
  - The OCCS capability includes a flexible, programmable Phase-Locked Loop (PLL), enabling selection of an exact operating frequency
  - The OCCS also includes unique loss-of-lock detection, allowing the detection of a cut crystal and the proper safety-critical shut down

- **16-bit Timer**
  - 56F8000 devices are equipped with powerful timer modules. Each timer module has four independent 16-bit timers that can be:
    - Cascaded
    - Used for input capture
    - Used to generate output waveforms
    - Used to trigger the ADC
    - Used to generate auxiliary PWM waveforms
    - Used as a Digital-to-Analog Converter (DAC) when utilized in conjunction with an external low-pass filter
    - Optionally synchronized together with a common start signal
    - Operated at rates up to 96Mhz
- **3-Phase PWM Module**
  - The high-performance 15-bit PWMs can be used in edge-aligned and center-aligned modes, as well as in complementary and independent modes, and have programable dead time generation
  - Excellent resolution, with a clock rate of up to 96Mhz
  - These PWM modules have a sophisticated set of programmable fault lines that do not require a system clock for proper operation
  - These and other features make these PWM modules industry leaders in safety, reliability, and performance
  - Enhanced features to support digital power conversion, power factor correction, lighting, and motor control
  - Hardware support for advanced phase-shifting PWM techniques
- **Analog-to-Digital Converter (ADC) Module**
  - Each high-performance 12-bit ADC has two sample and hold circuits, enabling simultaneous or sequential conversion at a rate of up to 1.125s per conversion
  - ADCs can be used in single-ended or differential modes and have a sophisticated set of unique features, including:
  - Superior absolute accuracy
  - High/low and zero-crossing detection
  - Offset
  - ADCs can be triggered through variety of methods, including PWM synchronization
  - ADCs have a sophisticated set of standby and power down modes for improved low-power performance
  - The ADC’s two sample-and-holds circuits can be configured separately to enable two independent sampling rates or start triggers

- **Inter-Integrated Circuit (I^2C) Serial Bus Interface**
  - Compatible with I^2C Bus standard
  - Features include:
    - Multi-master operation
    - Software programmable for one of 256 different serial clock frequencies
    - Arbitration-lost interrupt with automatic mode switching from master to slave
    - Calling-address identification interrupt
- **Serial Communication Interface (SCI)**
  - This module operates as a full-duplex Universal Asynchronous Receiver Transmitter (UART)
  - Fully interrupt driven and programmable, providing a multitude of operating modes and baud rates
- **Serial Peripheral Interface (SPI)**
  - This synchronous serial interface is double buffered
  - Operates in wide variety of modes, rates, and bit lengths, enabling the glueless connection to external peripherals and other processors at rates up to 16Mbps
- **General Purpose Input/Output (GPIO)**
  - All digital and analog signal pins for the on-board peripherals can also be individually assigned to be GPIO and individually assigned a direction
  - In addition to I/O capability, the GPIO can also generate interrupts
  - Each GPIO has programmable pull-ups
  - The GPIO also has a push-pull mode to efficiently implement a keypad interface
- **Computer Operating Properly (COP)**
  - Assists software recovery from runaway code
  - The COP is a free-running down counter which, once enabled, is designed to generate a reset when reaching zero
  - Software must periodically service the COP to clear the counter and prevent a reset
  - The COP enhances end-system reliability and safety
- **JTAG/EOnCE™**
  - This enhanced on-board emulation module enables true full-rate emulation without the need for expensive hardware emulators
  - To perform powerful, non-intrusive, real-time debugging, simply attach to the processor with the industry-standard JTAG interface

Chapter 3
Motor Drive System

3.1 Introduction

The Permanent Magnet Synchronous Motor (PMSM) is an excellent choice for air conditioning and compressor applications. This application employs sensorless Field-Oriented Control (FOC) to control a PMSM using the 56F8013 device. Software running on the 56F8013 device implements the complicated sensorless FOC algorithm.

3.2 Motor Drive System Features

- The motor drive system meets the compressor requirements
- The motor control algorithm employs Field-Oriented Control (FOC). The power stage switches are controlled by means of Space Vector Pulse Width Modulation (SVPWM).
- The feedback hardware elements are limited to the motor stator phase currents and the bus voltage. No position information devices or stator flux measurement are used; sensorless speed methods are employed.
- The Motor is capable of forward and reverse rotation and has a speed range of 500rpm to 6000rpm.
- The motion profiles, rotation direction, and speed are under user control. Tuning control parameters is easy with the user-friendly Human Machine Interface (HMI).
- The motor drive system is designed to produce minimal acoustic noise and have optimum control parameters.
- Some common PMSM advantages of Field-Oriented Control and Brushless DC Control:
  - Ability to control motors over a wide range of speeds
  - Precise speed regulation without additional cost
  - Rapid acceleration and deceleration capability
  - Starting torque and dynamic response equal to or better than conventional DC drives
  - Ability to operate several brushless drives from a common DCBus
  - No mechanical wear or conductive brush dust from brushes

System features include:

- The power stage is a 3-phase IGBT inverter. To reduce costs, isolation is eliminated between the power stage and the control circuit, except the communication ports.
- The power stage has all circuitry required to power 3-phase sinusoidal PMSM motor applications and BLDC sensorless applications
- The system includes a 50W-300W BLDC motor and PMSM motor, both of the appropriate size and at a competitive price
- The controller uses a 56F8013 device and both the control and power stage boards have been designed to be low cost, while meeting the required performance requirements.

- The PMSM motor control algorithm employs sensorless, indirect FOC; the power stage switches are controlled by Space Vector Pulse Width Modulation (SVPWM)
- BLDC motor control employs dual-loop feedback control with an inner current feedback loop and an outer speed feedback loop. The rotor position and speed are determined by back-EMF.
- The feedback hardware elements are limited to the DCBus currents, the DCBus voltage, phase back-EMF and phase voltage. Motor control has a speed range of 300rpm to 4500rpm.
- Software includes a speed start-up profile
- The motor control board's LEDs indicate status
- The system implements an HMI using a Windows PC and an electrically isolated serial RS-232 communication to the 56F8013 device. A simplified HMI capability is implemented via the push button on a 56F8013 Demonstration Board, enabling simple operation without the need for a Windows PC. Basic information displayed on the HMI includes speed, current, voltage, and direction of rotation.
- The system uses a standard Freescale 56F8013 Demonstration Board as the processor, JTAG interface, button and LED interface requirements. The power stage board has an interface to the 56F8013 Demonstration Board's standard connector.

Power Features:

- 50/60Hz input frequency range
- 110VAC or 220VAC operating voltage range
- Maximum output power is 500W

Motor control demonstrates superior efficiency at both low speeds and high speeds.

3.3 Introduction to System Design

This section describes the design of the system.

3.3.1 Hardware Overview

This application is directed toward applications requiring high performance and low-cost sensorless motor control such as designs for air conditioners and refrigerator compressors, so the 3-phase PMSM is driven under the air conditioning and refrigerator compressor machine requirements. To contain costs, resistors replace the phase current sensors and an optocoupler is not used.

PC master software communicates through the RS-232 to a PC and facilitates viewing the mid-variables and modifying the control-variables during debug.

The system comprises an 56F8013 Demonstration Board and a PMSM board. The PMSM board includes 3-phase power stage, power factor correction, a communication module linking a PC with the 56F8013 Demonstration Board, simplified Human Machine Interface (HMI), a protection module and effective electrical isolation.

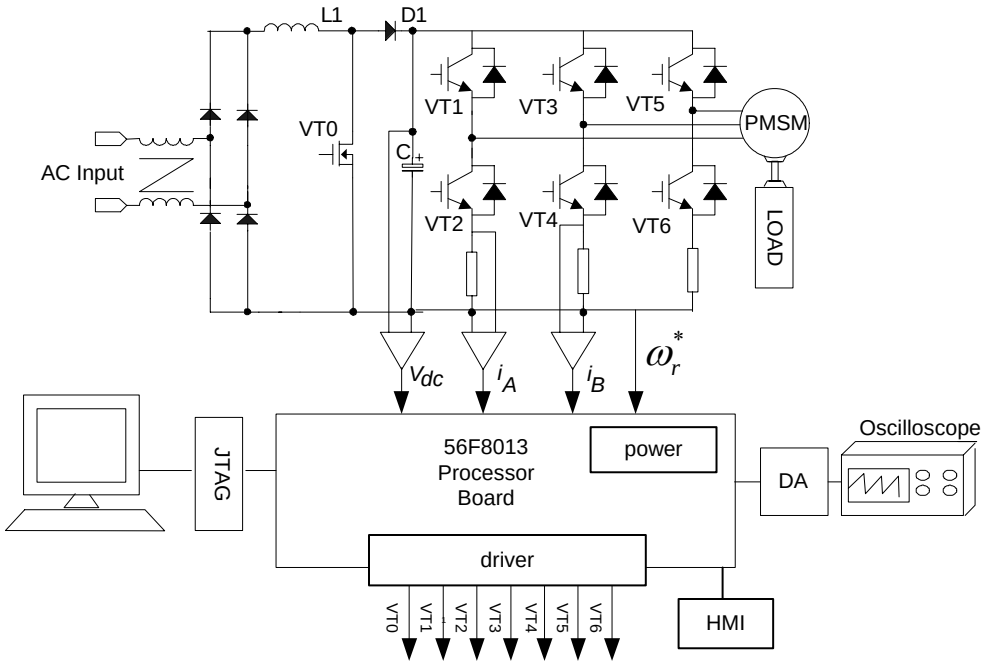


Figure 3-1. System Block Diagram

3.3.1.1 Integrated Power Module (IPM)

An IRAMS10UP60A, which is a 600V, 10-Ampere IPM, powers the PMSM. Its built-in control circuits provide optimum gate drive and protection for the IGBT. Three bridges are integrated in its body. **Figure 3-2** shows the Circuit Diagram.

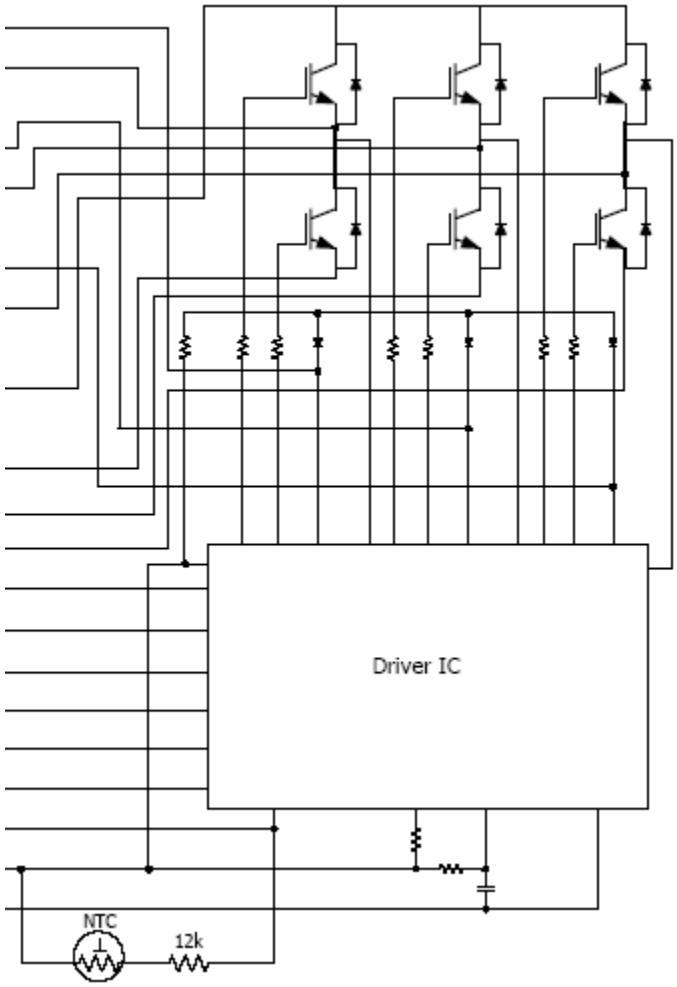


Figure 3-2. IRAMS10UP60A Circuit Diagram

3.3.1.2 56F8013

The PMSM's performance and accurate control demands require sophisticated and computationally complex software, delivered by a powerful DSC like the 56F8013.

The controller board includes:

- Control system circuit
- CPU circuit
- ADC circuit
- Power supply circuit
- SCI interface
- Parallel JTAG interface
- LED display circuit
- Signals output interface

3.3.1.3 Optocoupler Omitted

To contain application costs, an optocoupler is not used as the interface between the 56F8013 and IPM. A reliable protection circuit is applied to improve system safety.

3.3.1.4 Power Stage for PMSM and BLDC

The power stage can control PMSM, BLDC, and ACIM motors by changing jumpers and resister values.

3.3.1.5 Signal Sample and Process Board

To control hardware costs, a simple difference amplifier circuit replaces a Hall effect transducer to detect current and voltage signals.

3.3.1.6 56F8013 Demonstration Board

Freescale's 56F8013 Demonstration Board connects to the main board and highlights the capabilities of the Demonstration Board.

3.3.2 Software Overview

This system is designed to drive a 3-phase PMSM using stator flux orientation and incorporates:

- The control technique, which involves:
  - Sampling phase currents and DCBus voltages
  - Sliding Mode Observer (SMO) sensorless algorithm
  - Rotor position and speed estimation used for FOC calculation
  - Speed closed-loop allows the motor a good transient response
  - Current closed-loop allows the motor superior torque
  - PI regulation for the speed and current dual closed-loop control
  - SVPWM generates the desired voltage by the inverter
- Minimum speed of 500rpm
- Maximum speed of 6000rpm
- Power factor correction eliminates negative effects on the input electric by the use of switches
- Fault protection against:
  - Bus overvoltage
  - Bus undervoltage
  - Bus overcurrent
  - IPM overheating

PC master software is used for debugging and for remote control of the PMSM system.

3.4 Specification and Performance

Input voltage:	85 ~265VAC
Input frequency:	45 ~65Hz
Rating bus voltage:	350V
Rating output power:	200W
Switch frequency of PFC switch:	100KHz
Switch frequency of inverter:	10KHz
Power factor:	>95%
Efficiency:	>90%

Chapter 4
PMSM Theory

4.1 Permanent Magnet Synchronous Motor (PMSM)

A PMSM provides rotation at a fixed speed in synchronization with the frequency of the power source, regardless of the fluctuation of the load or line voltage. The motor runs at a fixed speed synchronous with mains frequency, at any torque up to the motor's operating limit. PMSMs are therefore ideal for high-accuracy fixed-speed drives.

A 3-phase PMSM is a permanently excited motor. Boasting a very high power density, a very high efficiency and high response, the motor is suitable for most sophisticated applications in mechanical engineering. It also has a high overload capability. A PMSM is largely maintenance free, which ensures the most efficient operation.

Precise speed regulation makes a PMSM an ideal choice for certain industrial processes. PMSM has speed/torque characteristics ideally suited for direct drive of large-horsepower, low-rpm loads. Synchronous motors operate at an improved power factor, thereby improving the overall system power factor and eliminating or reducing utility power factor penalties. An improved power factor also reduces the system's voltage drop and the voltage drop at the motor terminals.

4.2 PMSM Model

Stator voltage differential equations:

$$u_A = R_s i_A + p\psi_A$$
$$u_B = R_s i_B + p\psi_B$$
$$u_C = R_s i_C + p\psi_C$$

Stator and rotor flux linkages:

$$\psi_A = L_{AA} i_A + M_{AB} i_B + M_{AC} i_C + \psi_{fA}$$
$$\psi_B = M_{BA} i_A + L_{BB} i_B + M_{BC} i_C + \psi_{fB}$$
$$\psi_C = M_{CA} i_A + M_{CB} i_B + L_{CC} i_C + \psi_{fC}$$
$$\psi_{fA} = \psi_f \cos\theta$$
$$\psi_{fB} = \psi_f \cos(\theta - 2\pi/3)$$
$$\psi_{fC} = \psi_f \cos(\theta + 2\pi/3)$$

Where:

U_A, U_B, U_C	Stator voltage vector
i_A, i_B, i_C	Stator current vector
Ψ_A, Ψ_B, Ψ_C	Stator flux vector
Ψ_{fA}, Ψ_{fB}, Ψ_{fC}	Rotor flux vector
L_{AA}, L_{BB}, L_{CC}	Stator equivalent inductance
L_{AB}, L_{BC}, L_{CA}, L_{BA}, L_{CB}, L_{AC}	Mutual equivalent inductance

4.3 Digital Control of a Permanent Magnetic Synchronous Motor

In an adjustable speed application, PMSM and BLDC are powered by inverters. The inverter converts DC power to AC power at the required frequency and amplitude.

Figure 4-1 shows the system configuration of the hardware.

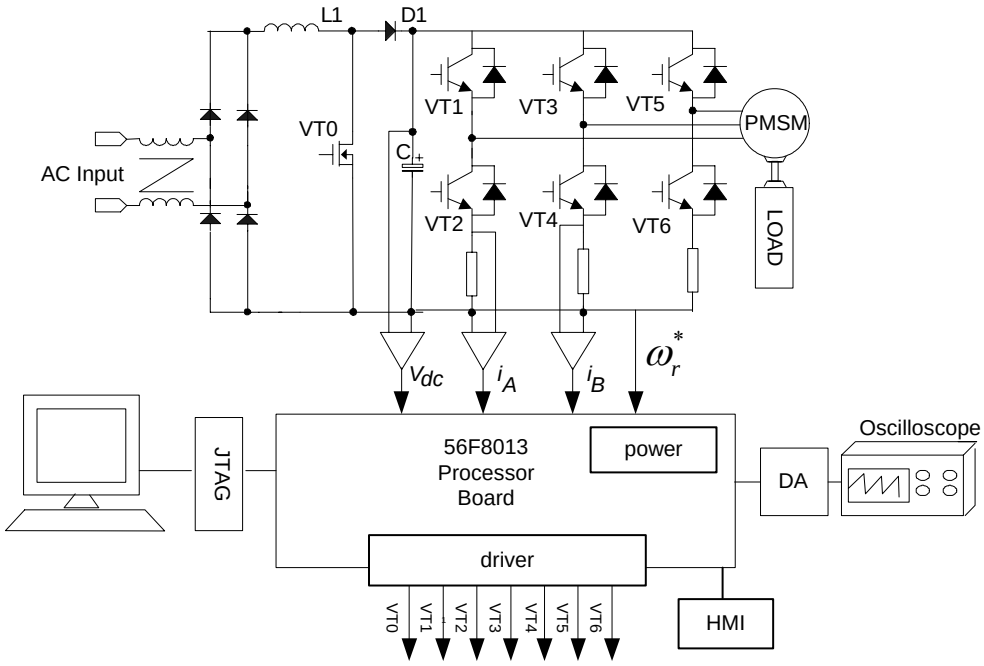


Figure 4-1. System Configuration

The inverter consists of three half-bridge units in which the upper and lower switches are controlled complimentarily, meaning when the upper switch is turned on, the lower switch must be turned off, and vice versa. As the power device's turn-off time is longer than its turn-on time, some dead time must be inserted between the time one transistor of the half-bridge is turned off and its complementary device is turned on. The output voltage is created by a Pulse Width Modulation (PWM) technique, where an isosceles triangle carrier wave is compared with a fundamental-frequency sine-modulating wave. The

natural points of intersection determine the switching points of the power devices of a half-bridge inverter. This technique is shown in **Figure 4-2**. The 3-phase voltage waves are shifted 120° to one another and thus a 3-phase motor can be supplied.

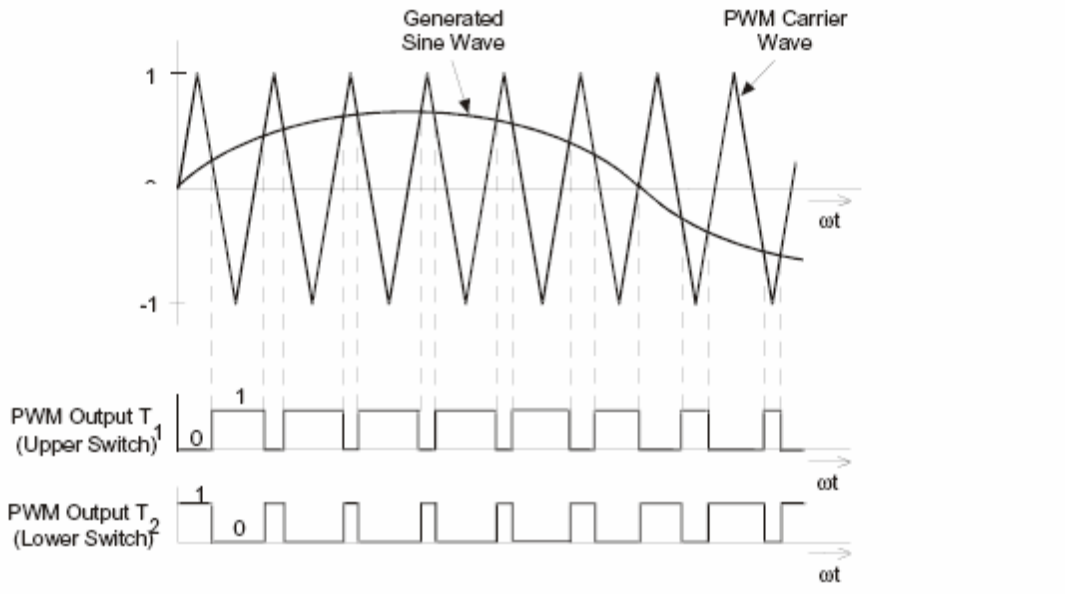


Figure 4-2. Pulse Width Modulation

The most popular power devices for motor control applications are Power MOSFETs and IGBTs. A Power MOSFET is a voltage-controlled transistor. It is designed for high-frequency operation and has a low-voltage drop, so it has low power losses. An Insulated-Gate Bipolar Transistor (IGBT) is controlled by a MOSFET on its base. The IGBT requires low drive current, has fast switching time, and is suitable for high switching frequencies.

Incorporated in this application, an Integrated Power Module (IPM) is widely used in today's household appliances. A built-in temperature monitor and overtemperature/overcurrent protection, along with the short circuit-rated IGBTs and integrated undervoltage lockout function, make the IPM more convenient for an engineer to develop his systems.

Chapter 5
Design Concept of a PMSM Vector Control Drive and BLDC Control Drive

5.1 PMSM Vector Control

Field-oriented control is commonly called vector control. This control method will maintain near-perpendicular stator flux and rotor flux by keeping the sum of stator fluxes constant. When the control axis is coincident with the stator flux, the stator flux in the load angle can be calculated from the stator current and the motor constants. When attempts are made to control this calculated stator flux at the same magnitude as the permanent magnet flux, the error in the flux can be calculated from the stator flux and the load angle. This makes it possible to construct a control system by feeding back the flux phase current calculation to the stator voltages for the various axes of the Permanent Magnet Synchronous Motor (PMSM), with the control axis coincident with the stator flux, producing a control voltage command. This voltage command is applied to the PMSM at the described frequency. Although the vector control method can achieve high performance and efficiency, it is based on the accuracy of the motor constants' values. The variation of motor internal resistance and inductance by temperature can decrease the system's performance and efficiency. To compensate for parameter variations, complex parameter observation and control algorithms are needed to correct those errors. On other hand, the field-oriented control method is often applied to PMSM motors with a sinusoidal back-EMF waveform shape to achieve high torque performance and efficiency. **Figure 5-1** shows a sensorless PMSM vector control system.

The field-oriented controller is based on a current-controlled voltage source inverter structure. The current control loops are arranged in the 2-phase synchronously rotating reference frame d-q aligned with rotor flux, while the rotor position and speed detection operates in the 2-phase stationary reference frame $\alpha\beta$.

During normal operations, the output of the speed regulator represents the q axis reference current, *iq*, while the d axis reference current, *id*, is set to zero in order to maximize the torque-to-current ratio of the PMSM. The outputs of the current regulators represent the reference voltages in the rotating reference frame. A d-q to $\alpha\beta$ transformation then yields the reference voltage values in the stator reference frame, which are the inputs of a Space Vector Pulse Width Modulator (SVPWM).

Current feedback is obtained by measuring the 3-phase currents and the successive transformations to the stator and rotor components, respectively. The stator current components are used inside the observer, while the rotor current components are needed for current regulation. Standard PI controllers, with limitation, are used for all regulators.

The combined Sliding Mode Observer (SMO) and low-pass filter provide the rotor position used for the field orientation and the rotor speed feedback used for the speed control loop.

Based on the analysis, the control scheme can be obtained as shown in **Figure 5-1**.

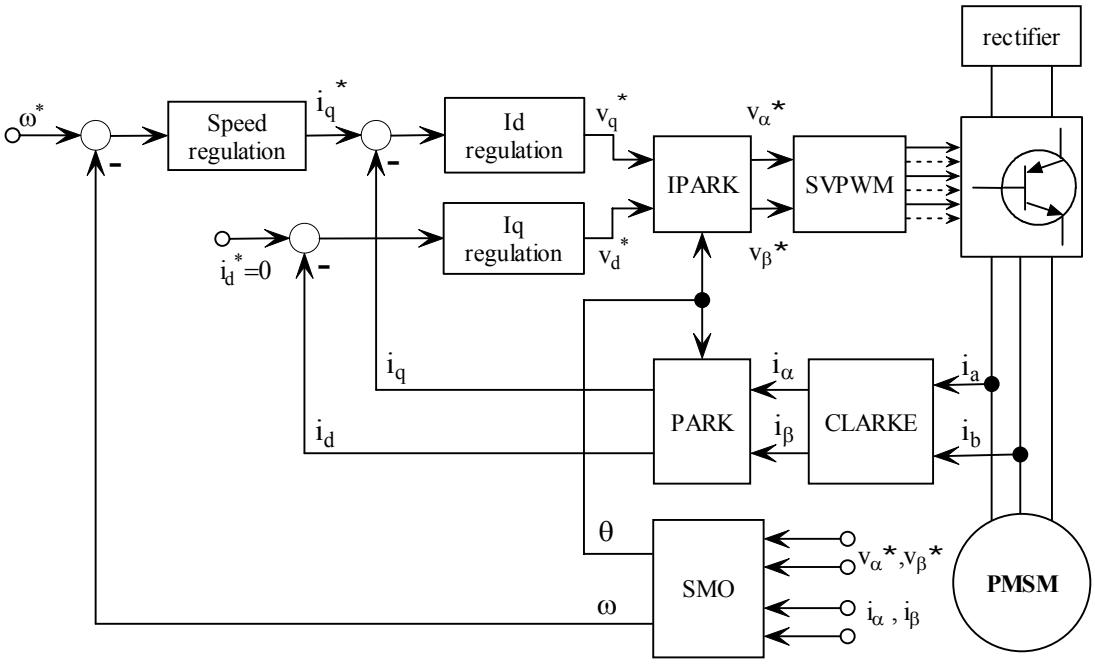


Figure 5-1. PMSM System Block Diagram

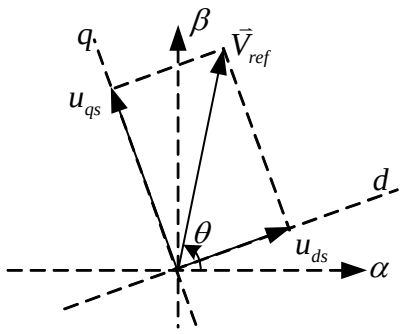


Figure 5-2. Stator Reference Voltage, V_{ref}

Brushless DC (BLDC) systems combine the positive attributes of AC and DC systems. In contrast to a brush DC motor, motors conventionally used for a BLDC system are a type of permanent magnet AC synchronous motors with a trapezoidal back-EMF waveform shape and electronic commutation replaces the mechanical brushes in the DC motor. Although this control method will generate torque glitches during phase commutation, it satisfies most applications in which rotor speed is the control target.

PMSM motors with a sinusoidal back-EMF waveform shape can also be used in a BLDC system. But the phasor angle between stator flux and rotor flux are maintained between 60° electrical and 120° electrical. Torque ripples will occur during operation, but average torque will remain constant, meeting the requirements of most low-end applications.

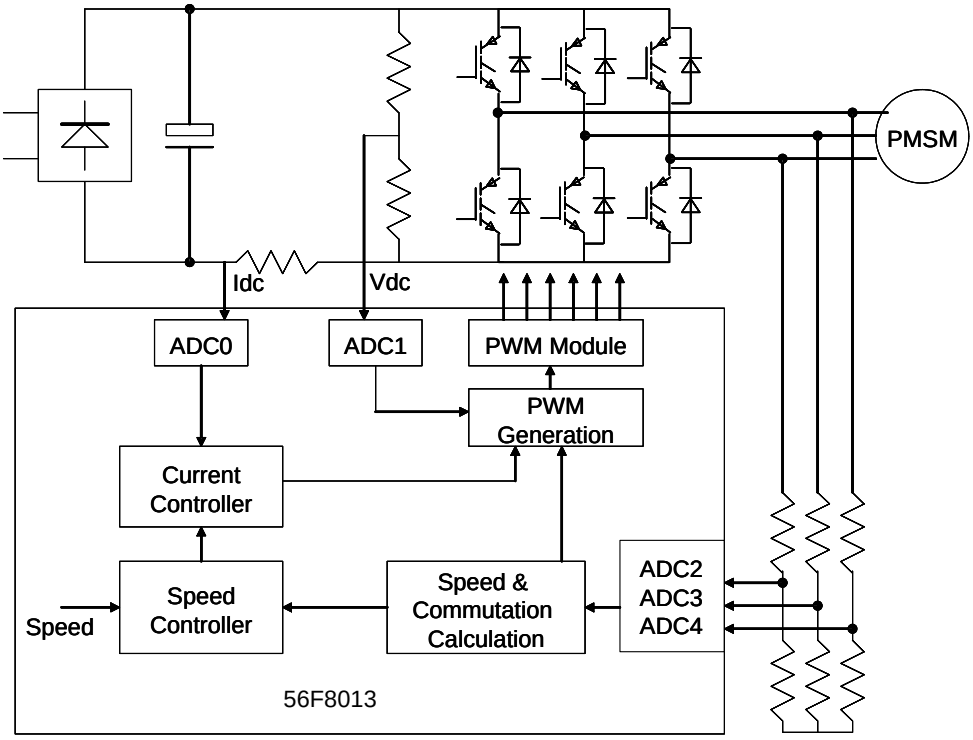


Figure 5-3. BLDC Sensorless Control System

The information from back-EMF zero crossing can be used to determine the rotor position for proper commutation and to determine which power transistors to turn on to obtain maximum motor torque. The cheapest and the most reliable method to sample back-EMF zero crossing information is to feed the resistor network samples' back-EMF signal into ADC inputs or GPIOs.

In sensored control structure, phases are commutated once every 60° electrical rotation of the rotor. This implies that only six commutation signals are sufficient to drive a BLDC motor. Furthermore, efficient control implies a synchronization between the phase Bemf and the phase supply so that the Bemf crosses zero once during the non-fed 60° sector.

As only two currents flow in the stator windings at any one time, two phase currents are opposite and the third phase is equal to zero. Knowing that the sum of the three stator currents is equal to zero (star-wound stator), the anticipated instantaneous Bemf waveforms can be calculated. The sum of the three stator terminal voltages is equal to three times the neutral point voltage (*Vn*). Each of the Bemfs crosses zero twice per mechanical revolution, and as the Bemfs are numerically easy to compute, thanks to the signal processing capability of the 56F8013, it is possible to get the six required items of information regarding the commutation.

5.2 Procedure for Sliding Mode Observer (SMO)

To perform SMO, follow these steps:

1. Measure phase currents to get the voltage command
2. Transform them into a 2-phase system using Clarke transformation
3. Sliding mode current observer

   The sliding mode current observer consists of a model-based current observer and a bang-bang control generator driven by the error between estimated motor currents and actual motor currents.

   The goal of bang-bang control is to drive the current estimation error to zero. It is achieved by proper selection of *k* and correct formation of estimated back-EMF.
4. Estimated Back-EMF

   Estimated back-EMF is obtained by filtering the bang-bang control with a first order low-pass filter.
5. Calculating Rotor Flux Position

   The estimated back-EMF can be calculated to estimate rotor position and rotor speed.
6. Correcting Rotor Flux Position

   The low-pass filter used to obtain back-EMF introduces a phase delay. This delay is directly linked to the phase response of the low-pass filter and is often characterized by the filter's cut-off frequency. The lower the cut-off frequency, the bigger the phase delay for a fixed frequency.

5.3 Forward and Inverse Clarke Transformation (a,b,c to α,β and backwards)

The forward Clarke transformation converts a 3-phase system (a, b, c) to a 2-phase coordinate system (α, β). **Figure 5-4** shows graphical construction of the space vector and projection of the space vector to the quadrature-phase components, α, β. Assuming that the a axis and the α axis are in the same direction, the quadrature-phase stator currents $i_{s\alpha}$ and $i_{s\beta}$ are related to the actual 3-phase stator currents as follows:

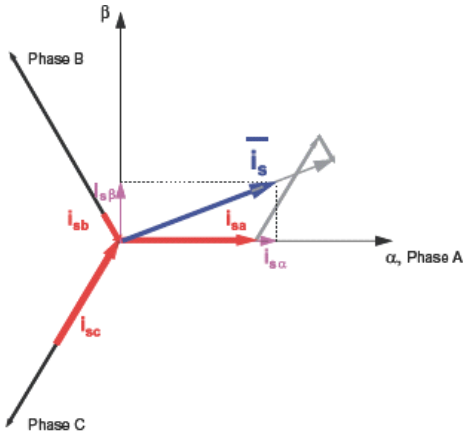


Figure 5-4. Clarke Transformation

$$i_{s\alpha} = i_{sa} \qquad \textit{Eqn. 5-1}$$

$$i_{s\beta} = \frac{1}{\sqrt{3}} i_{sa} + \frac{2}{\sqrt{3}} i_{sb} \qquad \textit{Eqn. 5-2}$$

The inverse Clarke transformation transforms from a 2-phase (α, β) to a 3-phase (i_{sa}, i_{sb}, i_{sc}) system.

$$i_{sa} = i_{s\alpha} \qquad \textit{Eqn. 5-3}$$

$$i_{sb} = -\frac{1}{2} i_{s\alpha} + \frac{\sqrt{3}}{2} i_{s\beta} \qquad \textit{Eqn. 5-4}$$

$$i_{sc} = -\frac{1}{2} i_{s\alpha} - \frac{\sqrt{3}}{2} i_{s\beta} \qquad \textit{Eqn. 5-5}$$

5.4 Forward and Inverse Park Transformation (α, β to d-q and backwards)

In stator-vector oriented control, the quanties in the stator reference frame should be transformed into the synchronous rotation with the stator flux vector reference frame. The relationship of the two reference frames is shown in **Figure 5-5**. The d axis is aligned with the stator flux vector, where $\theta_{\bar{\Psi}\ s}$ is the position of the stator flux.

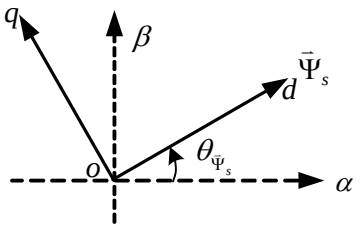


Figure 5-5. Park Transformation

The quantity in the stationary frame is transformed into synchronous frame by:

$$i_{sd} = i_{s\alpha}\cos\theta_{\bar{\Psi}_s} + i_{s\beta}\sin\theta_{\bar{\Psi}_s} \qquad \textit{Eqn. 5-6}$$

$$i_{sq} = -i_{s\alpha}\sin\theta_{\bar{\Psi}_s} + i_{s\beta}\cos\theta_{\bar{\Psi}_s} \qquad \textit{Eqn. 5-7}$$

And the inverse relation is:

$$i_{s\alpha} = i_{sd}\cos\theta_{\bar{\Psi}_s} - i_{sq}\sin\theta_{\bar{\Psi}_s} \qquad \textit{Eqn. 5-8}$$

$$i_{s\beta} = i_{sd}\sin\theta_{\bar{\Psi}_s} + i_{sq}\cos\theta_{\bar{\Psi}_s} \qquad \textit{Eqn. 5-9}$$

5.5 Rotor Speed Estimation

Rotor speed can be calculated by the following formula in both PMSM and BLDC:

$$\omega = \frac{\Delta\theta}{\Delta t} \qquad \textit{Eqn. 5-10}$$

The theta (θ) can be obtained from the SMO; time can be calculated from the counter of the PWM interrupt.

5.6 Speed Regulator

The speed regulator uses the standard PI controller with integral anti-windup correction.

The discrete-time equations used for the PI controller with anti-windup correction can be summarized as follows:

$$e_n = spd^* - spd \quad \textbf{Eqn. 5-11}$$

$$i_n = X_{(n-1)} + k_p \cdot e_n \quad \textbf{Eqn. 5-12}$$

$$if \quad i_n > i_{\max} \quad i_{ref} = i_{\max} \quad \textbf{Eqn. 5-13}$$

$$elseif \quad i_n < i_{\min} \quad i_{ref} = i_{\min} \quad \textbf{Eqn. 5-14}$$

$$else \quad i_{ref} = i_n \quad \textbf{Eqn. 5-15}$$

$$i_n = i_{(n-1)} + k_i \cdot e_n + k_c \cdot \left(i_{ref} - i_n\right) \quad \textbf{Eqn. 5-16}$$

$$where \quad k_c = k_i / k_p \quad \textbf{Eqn. 5-17}$$

5.7 PFC Design

The main circuit adopted in the paper is a single-switch PFC circuit, shown in **Figure 5-6**. The circuit is composed of Q, D, L, and filter capacitance C2, C3, and includes EMI filter, input relay and full wave rectifier.

In the 56F8013-based PFC module system, the controller samples the voltage signal output and voltage *DC_bus*, and processes these samples in the digital control loop. Because system is based on current Discontinuous Current Mode (DCM) mode, there is only a voltage loop. Outer voltage loop G insures the output voltage is constant.

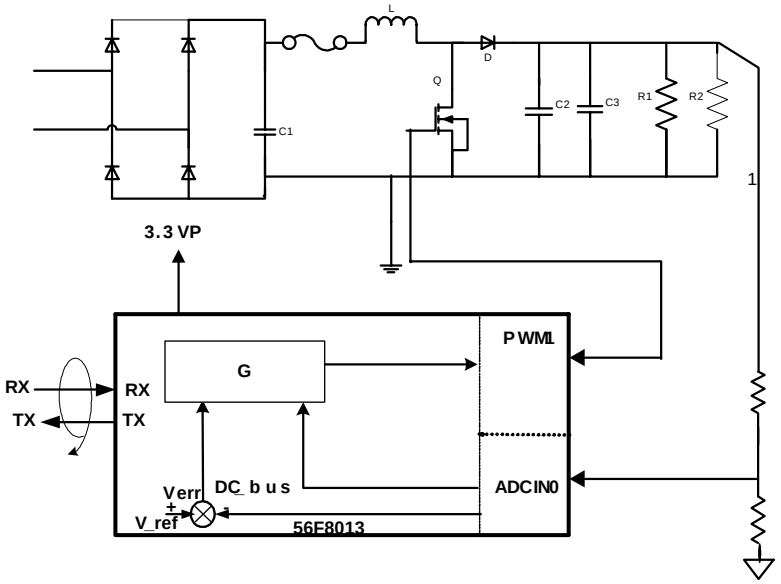


Figure 5-6. PFC Configuration Diagram

5.7.1 Inductor Selection

A. Maximum peak line current:

$$I_{pk(\max)} = \frac{\sqrt{2} \times P_O}{\eta V_{in(\min)}} = \frac{\sqrt{2} \times 500}{0.9 \times 85} = 9.24A$$

Eqn. 5-18

B. Ripple current:

$$\Delta I_L = 20\% I_{pk} = 0.2 \times 9.24 = 3.7A$$

Eqn. 5-19

C. Determine the duty factor at I_{pk}, where $V_{in(peak)}$ is the peak of the rectified line voltage.

$$D = \frac{V_o - V_{in(peak)}}{V_o} = \frac{380 - \sqrt{2} \times 85}{380} = 0.68$$

Eqn. 5-20

D. Calculate the inductance; f_S is the switching frequency.

$$L = \frac{V_{in} \times D}{fs \times \Delta I} = \frac{\sqrt{2} \times 85 \times 0.68}{100000 \times 3.7} = 221\,\mu H$$

Eqn. 5-21

Round up to 250μH.

5.7.2 Output Capacitor

Output filter inductor can be calculated by the following equation:

$$C = \frac{2 \times P_O \times \Delta t}{V_{O(\max)}^2 - V_{O(\min)}^2}$$

Eqn. 5-22

P_o = 500W
$V_{o(min)}$ = 380 × (1-10%) = 342V
$V_{o(max)}$ = 380×(1+10%) = 418V
⊿t= 50ms

According to **Equation 5-21**, C = 866*μH*.
Select the output capacitor to be C = 940*μH*.
Two 470*μH*/450*V* electrolytic capacitors connected in parallel are chosen.

5.7.3 Main Switch

The voltage limit of the main switch is:

$$V_{CEM(S)} > 1.5V_{cem(S)} = 1.5V_{in(max)} = 1.5 \text{ X } 380 = 570V$$

Eqn. 5-23

The circuit limit of the main switch is calculated by RMS value:

$$I_{CEM(S)} > 1.5I_{L(max)} = 1.5 \times \frac{\sqrt{2} \cdot P_O}{\eta \cdot V_{in(\min)}} = 1.5 \times \frac{\sqrt{2} \cdot 500}{0.9 \times 85} = 13.86A$$

Eqn. 5-24

Select main switch Q_{400}—Q_{401} to be the MOSFET IRFPC60LC. Parameters are described as follows:

V_{DSS} = 600*V*
I_D = 16*A*
$R_{DS}(on)tye$ = 0.4Ω
TO-247AC Package

5.7.4 Output Diode

The voltage limit of the output diode is:

$$V_{CEM(S)} > 1.5V_{cem(S)} = 1.5V_{in(max)} = 1.5 \text{ X } 380 = 570V$$

Eqn. 5-25

The circuit limit of the output diode is calculated by RMS value:

$$I_{CEM(S)} > 1.5I_{L(max)} = 1.5 \times \frac{\sqrt{2} \cdot P_O}{\eta \cdot V_{in(\min)}} = 1.5 \times \frac{\sqrt{2} \cdot 500}{0.9 \times 85} = 13.86A$$

Eqn. 5-26

Select output diode D_{400}—D_{402} to be FRED DSEP60-06A. Parameters are described as follows:
V_{RRM} = 600V
I_{FAVM} = 60A
t_{rr} = 35nS
TO-247AD Package

5.7.5 Inductor Design

In **Section 5.7.1**, it was found that L=250μH.
Select B_m=0.3T.
Select magnetic core to be EI33, with an effective area of 118mm^2.

The number of inductor windings can be calculated as follows:

$$N = \frac{LI_{L(\max)}}{A_e B_m} \text{ =38.2}$$

Eqn. 5-27

Select N = 38.The gap is:

$$\delta = \frac{\mu_o N^2 A_e}{L} = \frac{1.25\times10^{-6}\times38^2\times118\times10^{-6}}{250\times10^{-6}} = 0.85mm$$

Eqn. 5-28

When work frequency of inductance is 100kHz, the penetrate depth of copper lead is:

$$\Lambda = \sqrt{\frac{2}{2\pi f_s \mu\gamma}} = \sqrt{\frac{1}{3.14\times100\times10^3\times1.25\times10^{-6}\times58\times10^6}} = 0.209mm$$

Eqn. 5-29

Where:
γ is the electric conductive ratio of lead
μ is magnetical conductive ratio of lead

A copper lead with a smaller diameter than 0.42mm can be selected. In this case, select high intensity lead with a diameter of 0.33mm and an effective area of 0.0855mm^2.

By selecting circuit density to be J = 3.5A/mm^2, the area of leads is $S = \frac{3.84}{3.5} = 1.1mm^2$.
Thirteen leads with a diameter of 0.33mm must be used.

$$Kc = \frac{38\times13\times0.0855}{132} = 0.32 \text{ <<0.35}$$

Eqn. 5-30

Chapter 6
Hardware Implementation

The motor control system is designed to drive the 3-phase PMSM motor in a dual closed-loop (speed closed-loop and current closed-loop). The system is pictured in **Figure 6-1** and consists of the following blocks:

- 56F8013
- High-voltage power stage circuitry with sensor circuitry
- Power supply and PFC circuitry
- 3-phase PMSM motor without speed transducer

6.1 56F8013

The demonstration system is illustrated in **Figure 6-1** and the hierarchy diagram is depicted in **Figure 6-2**. it clearly shows that the 56F8013 is the core of the system, highlighted atop the mother board. **Figure 6-3** shows the motor control system configuration.

Figure 6-1. Demonstration System

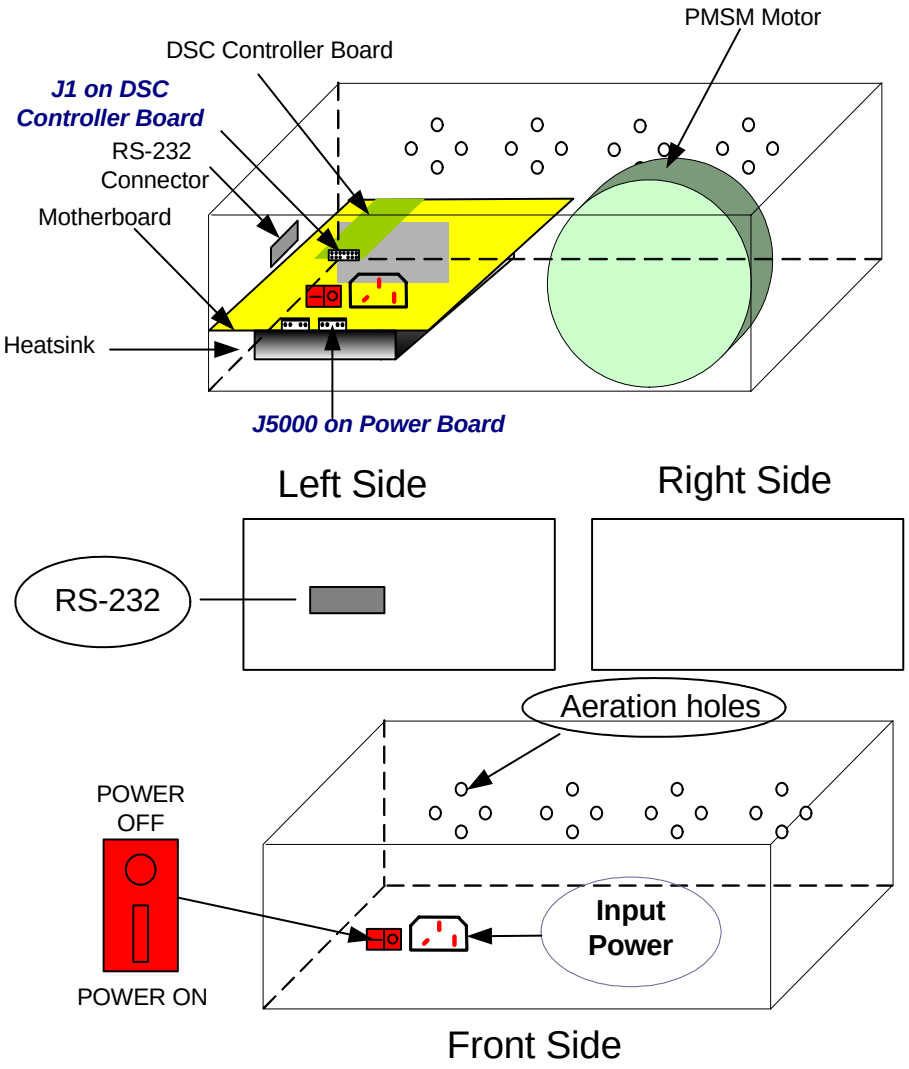


Figure 6-2. Hierarchy Diagram

The 56F8013 is the drive's brain. All algorithms are carried out in this single smart chip, which reads the input commands, processes the routine, and generates the PWM to govern the power switches driving the motor and the PFC to make the input current sinusoidal.

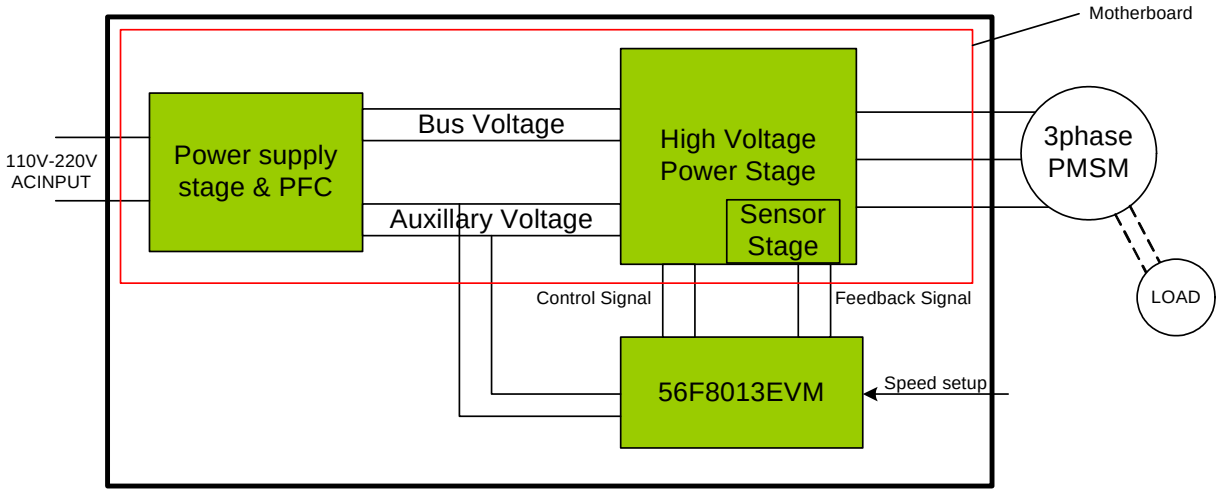


Figure 6-3. Motor Control System Configuration

6.2 High-Voltage Power Stage

The HV Medium Power Board is designed to meet the power needed by a household washing machine and lower-power industrial applications. An Integrated Power Module (IPM) is used to simplify the design and board layout and to lower the cost. IPMs are available from various suppliers and it is simple to use one from a supplier of choice. The IRAMS10UP60A is an IPM which targets the household appliance market. Its features include:

- Integrated gate drivers and bootstrap diodes
- Temperature monitor
- Temperature and overcurrent shutdown
- Fully isolated package
- Low V_{CE} (on) non-punch-through IGBT technology
- Undervoltage lockout for all channels
- Matched propagation delay for all channels
- Low-side IGBT emitter pins for current conrol
- Schmitt-triggered input logic
- Cross-conduction prevention logic
- Lower di/dt gate driver for better noise immunity

Its maxium IGBT block voltage is 600V; phase current is 10A at 25°C and 5A at 100°C, making it suitable for this appliance.

6.3 Sensor Stage

The control algorithm requires DCBus voltage and phase current sensing for a PMSM, and DCBus current and phase voltage sensing for a BLDC, so these sensors are built on the power stage board. Schematics of the sensors' circuits can be found in **Appendix A**.

6.3.1 DCBus Voltage Sensor

The DCBus voltage must be checked because overvoltage protection and PFC are required. A simple voltage sensor is created by a diffential amplifier circuit. The voltage signal is transferred through a resistor and then amplified to the reference level. The amplifier output is connected to the 56F8013's ADC.

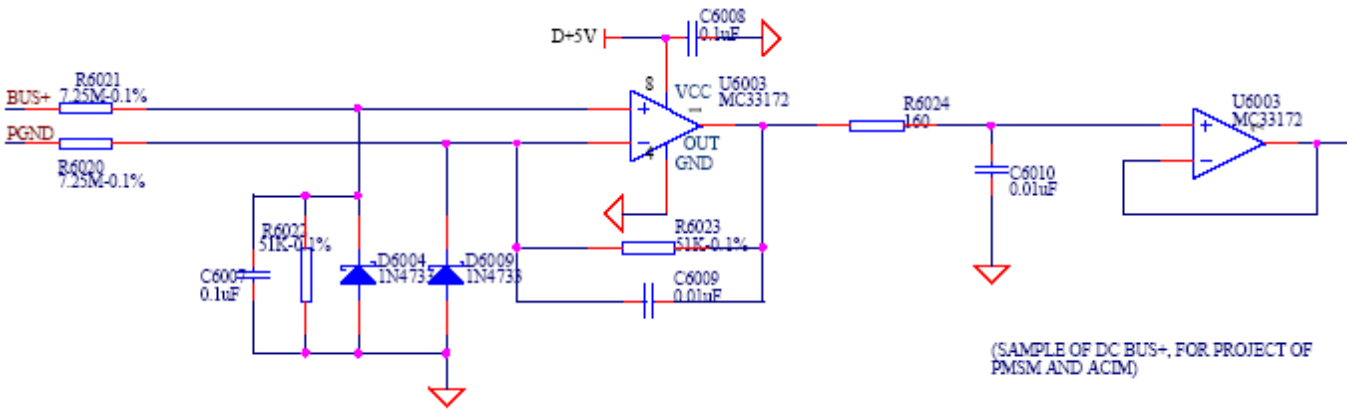


Figure 6-4. DCBus Sampling Circuit

6.3.2 DCBus Current Sensor

The bus current is sensed through the detection of the voltage drop across the resistor cascade into the negative bus link. A differential amplifier is then used to draw the voltage out and transform it to a level the 56F8013's AD channel can accommodate. The sample circuit is depicted in **Figure 6-5**.

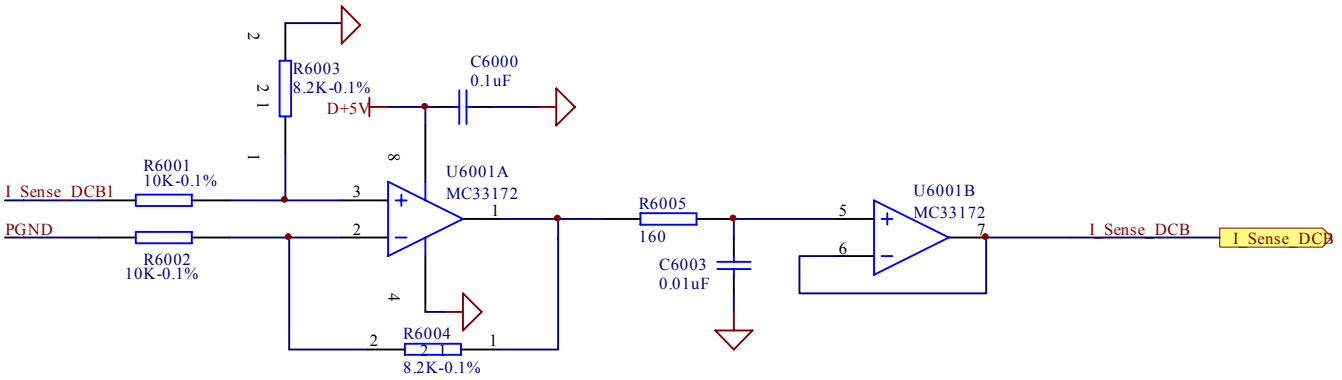
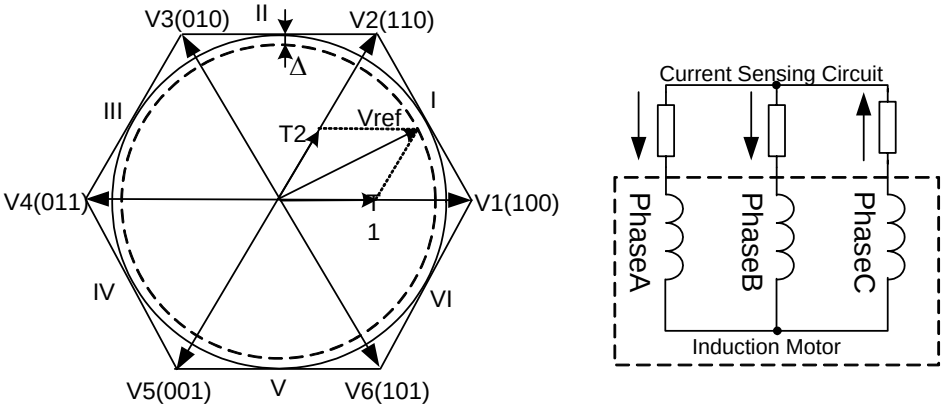


Figure 6-5. Bus Link Current Sample Circuit

6.3.3 Phase Current Sensor

The stator flux and electromagnetic torque can be derived from two phase currents and voltages. The use of a Hall current transducer will sharply increase the cost, and two channel differential amplifiers are used as the Analog-to-Digital Converter (ADC) to sample phase currents as shown in **Figure 6-6** (a). The SVPWM is employed to control the six IGBTs. The state in which all bottom switches are turned on and upper switches are turned off is defined as state 0, and the corresponding equivalent topology is depicted in **Figure 6-6** (b). The sample is triggered at state 0, shown in **Figure 6-6** (c). In this way, two phase currents can be derived through the differential amplifier channels. The spot worth consideration is that a certain margin Δ should be maintained between the circle track formed by the reference voltage vector $\hat{V}_{ref}$ and the inscribed circle of the hexagon shaped by the six base vectors as described in **Figure 6-6** (a), especially at the high speed range.



(a) SVPWM **(b) Equivalent Topology**

Figure 6-6. Methods to Detect Phase Currents

6.3.4 Phase Voltage Sensor

Phase voltage sensing is same as DCBus voltage sensing; see **Section 6.3.1**.

6.3.5 Power Supply Stage

The power supply stage provides a high-voltage DCBus +5V power supply for the drive and auxillary power and +15V for the 56F8013, IPM, high-voltage drivers and amplifiers. A topswitch generates auxiliary power supply of +15V for both the ICs and the IPM. PFC is employed to make the input current trace the input voltage and to reduce the EMI.

6.4 Protection Circuit

To improve the system safety level, overcurrent and overvoltage in the bus link detection and protection are introduced into the system, illustrated in **Figure 6-7**. The signal generated by the circuit “IPMLOCK” will be connected to the IPM’s drive IC (74HC244) and to the 56F8013’s fault pin. When a fault is generated, the IPMLOCK signal draws to high level. On the one hand, the IPMLOCK will disable the 74HC244 and the PWM signals won’t pass through; on the other hand, the IPMLOCK signal will drive the 56F8013’s fault0 pin, and the 56F8013 will block the PWM signal instantly.

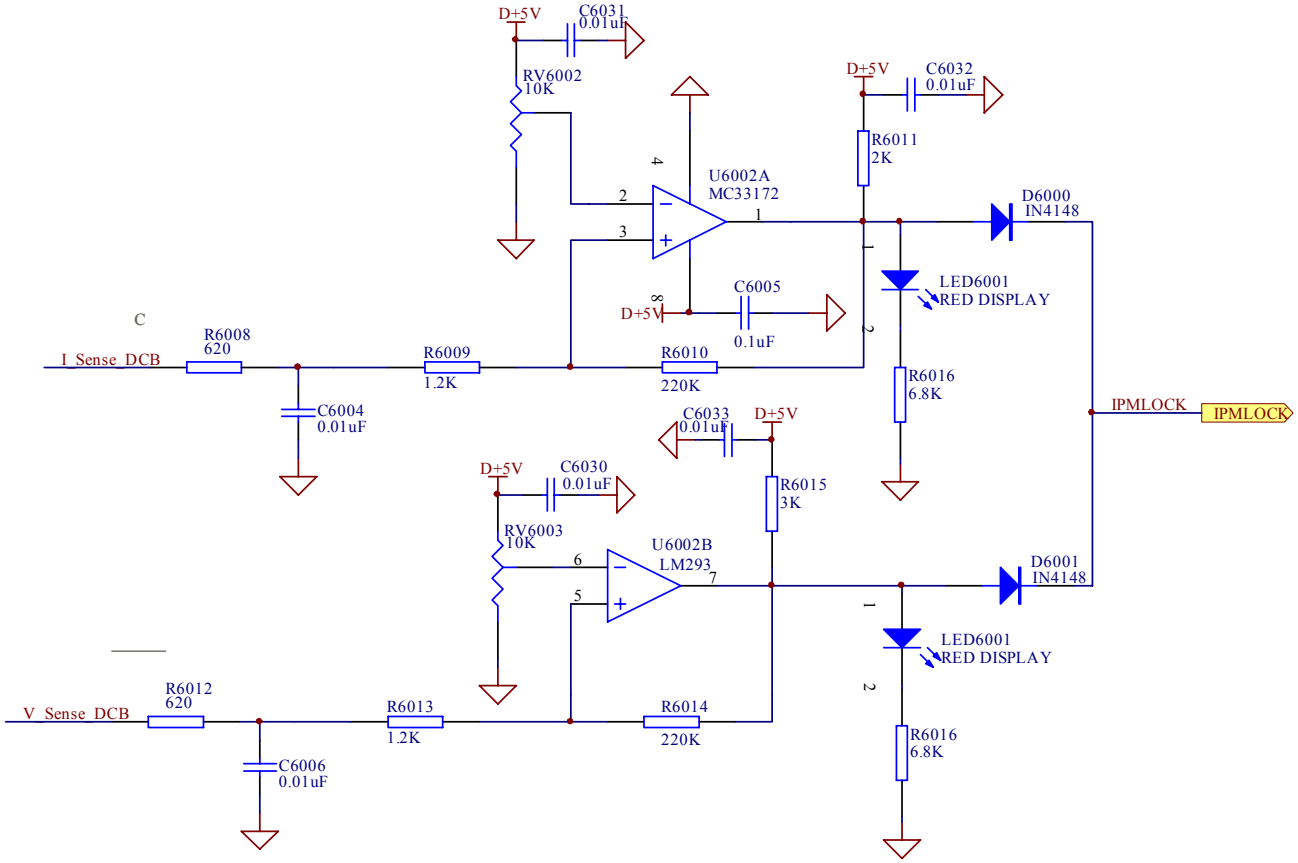


Figure 6-7. Protection Circuit

6.5 PFC Hardware Design

The topology of the main circuit is a boost circuit. One signal, output bus voltage *DC_bus,* is sampled and sent to the 56F8013.

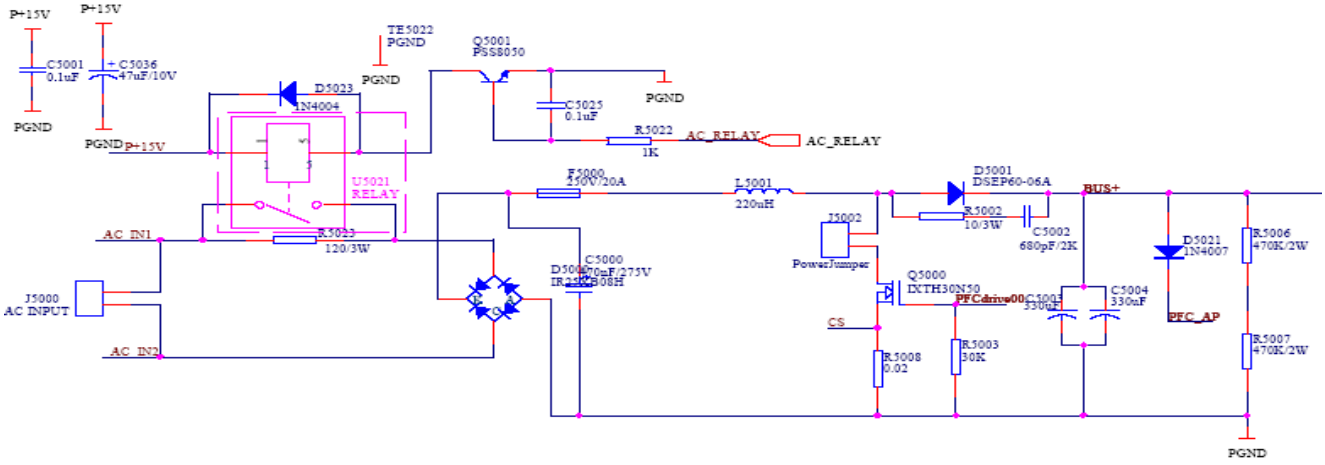


Figure 6-8. Main PFC Circuit

6.5.1 Drive Circuit Hardware Design

IC IR2125, a simple and reliable gate drive circuit based on a current-limiting single channel driver, is used; it is shown in **Figure 6-9**.

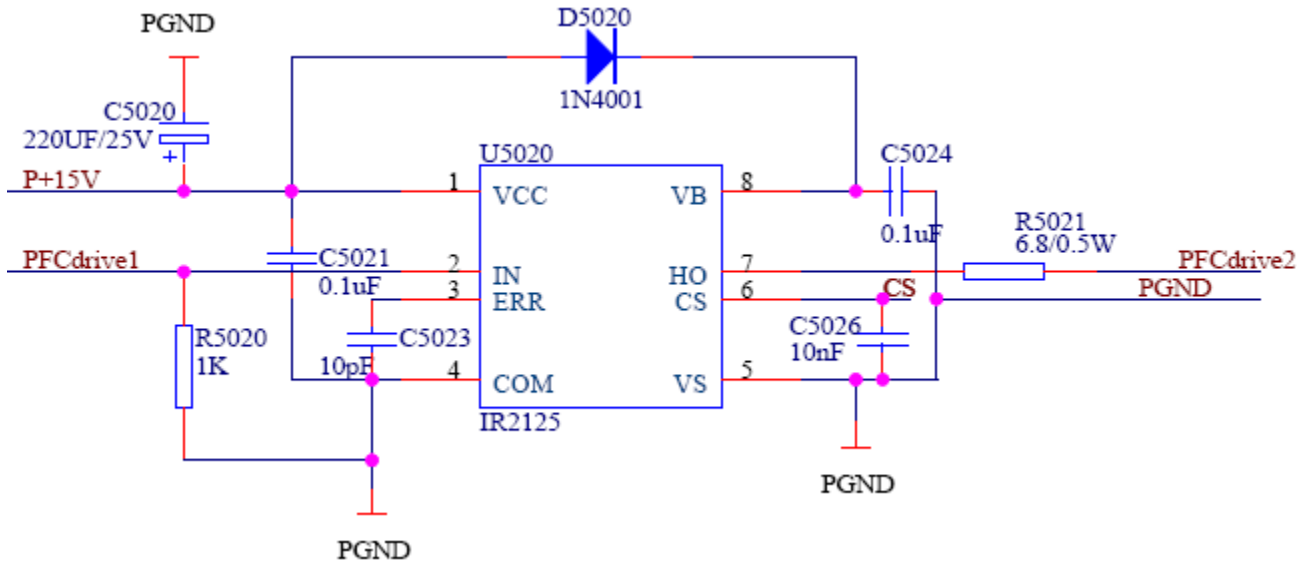


Figure 6-9. PFC Drive Circuit

6.5.2 Sample Circuit Hardware Design

The output bus voltage, V_{bus}, sample circuit is shown in **Figure 6-10**. A simple voltage divider is used for the bus voltage sample.

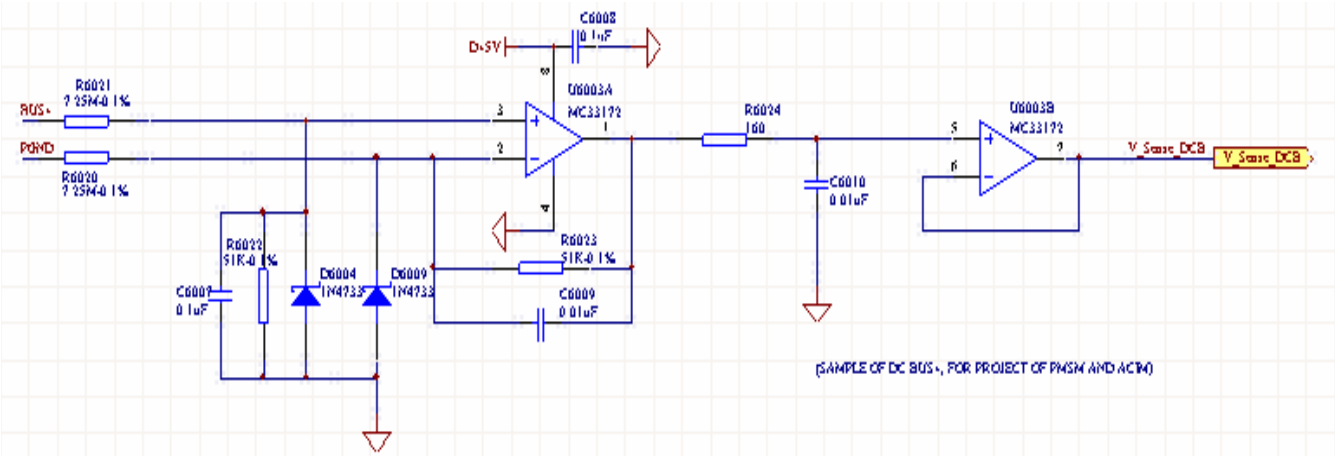


Figure 6-10. PFC Sampling Circuit

6.6 Detailed Motherboard Configurations for ACIM

The motherboard shown in **Figure 6-2** comprises a high-voltage power stage, a sensor stage, a protection circuit and PFC. It is a general board which can be used for PMSM, BLDC and ACIM after simple configuration with resistances and jumpers.

Configurations for PMSM are shown in **Figure 6-11**; BLDC configurations are illustrated in **Figure 6-12**. Shorten circuits for the jumpers circled in red and blue.

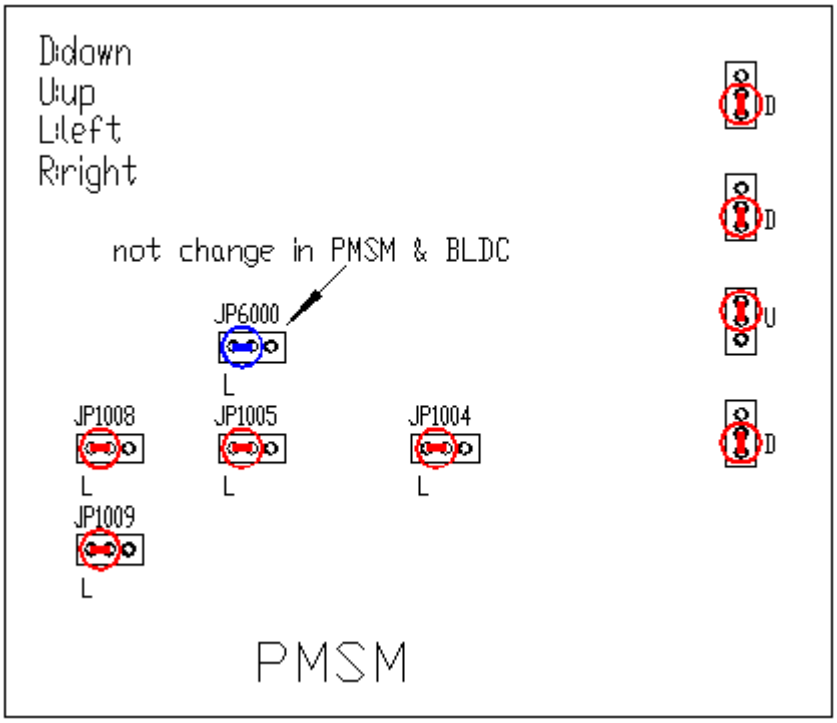


Figure 6-11. PMSM Jumper Configuration

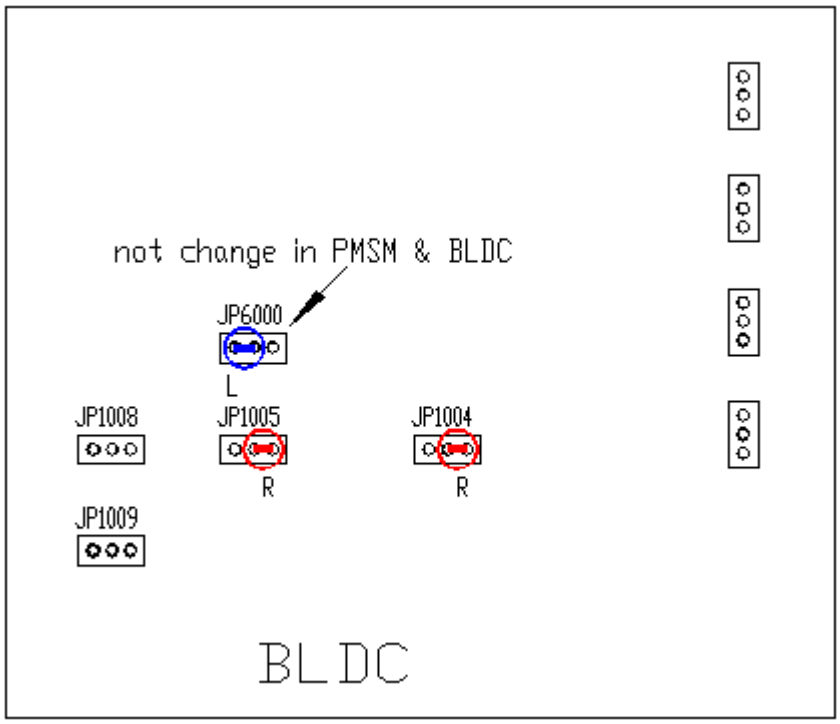


Figure 6-12. BLDC Jumper Configuration

Table 6-1 details the configurations of the 56F8013 resources used in the system and the corresponding variables used in the software.

Table 6-1. Configuration of the 56F8013's Resources

Target Variables	56F8013 Resources	Software Resources	
DCBus Voltage: V_sense_DCB	ANB1 (PC5)	sample3	AD_VDC
U phase Current Sample: I_sense_U	ANA1 (PC1)	sample0	AD_iA
V phase Current Sample: I_sense_V	ANA0 (PC0)	sample1	AD_iB
DCBus Current Sample: I_Sense_DCB	ANB0 (PC4)	sample4	AD_iDC
Relay: AC_RELAY	PB5		
OPEN: OPEN	PB2		
DACCLK	PB0		
DACDATA	PB3		
DACEN	PB1		
TXD	PB7		
RXD	PB6		
FAULT0	PA6		

Chapter 7
Software Design

This section describes the design of the drive's software blocks. The software will be described in terms of:

- Block Diagram
- Control Algorithm

7.1 Block Diagram

The drive's requirements dictate that the software gathers and processes values from the user interface, then generates 3-phase PWM signals for the inverter. The control algorithm contains the processes described in the following sections.

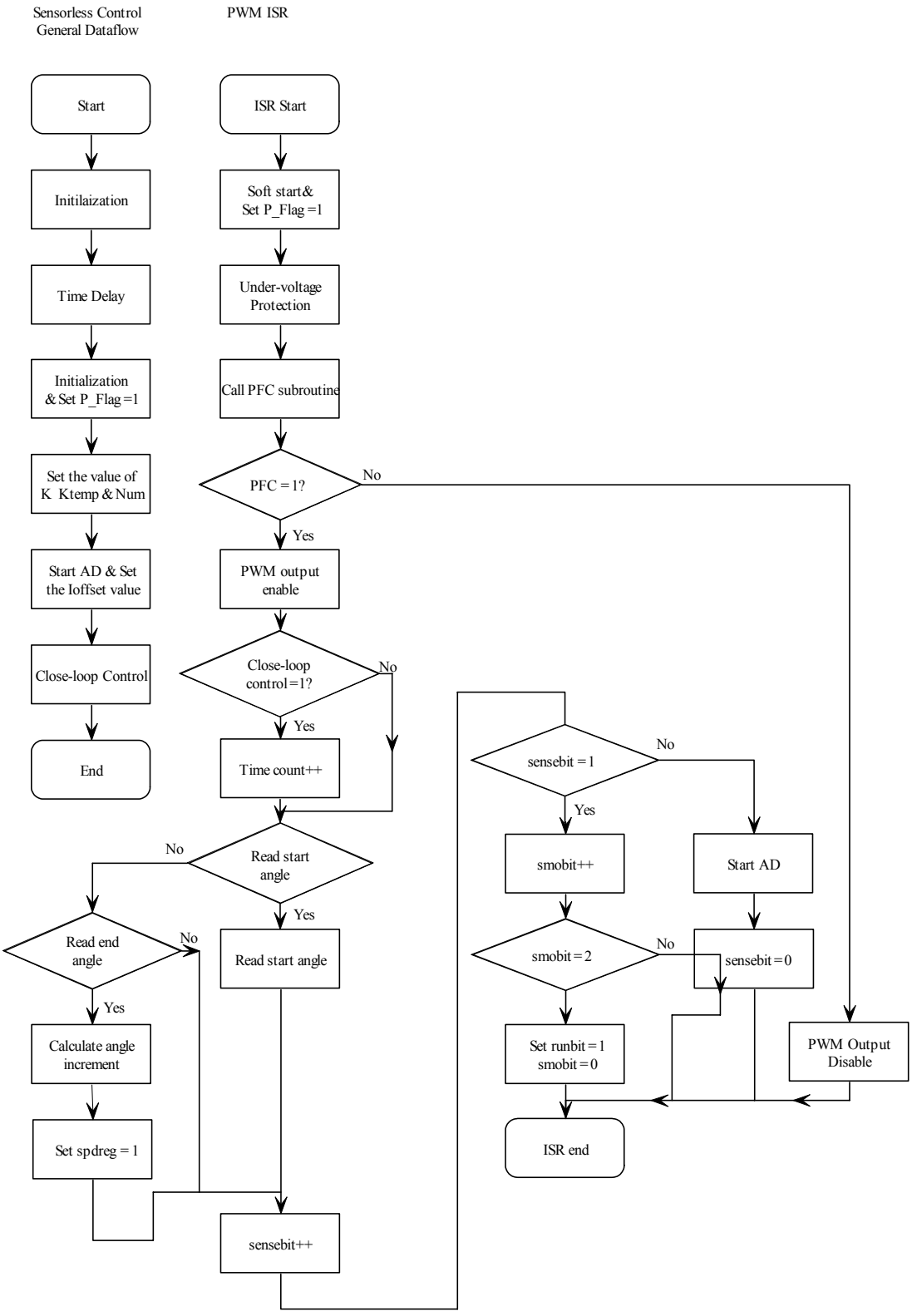


Figure 7-1. PMSM Block Diagram (Part 1 of 3)

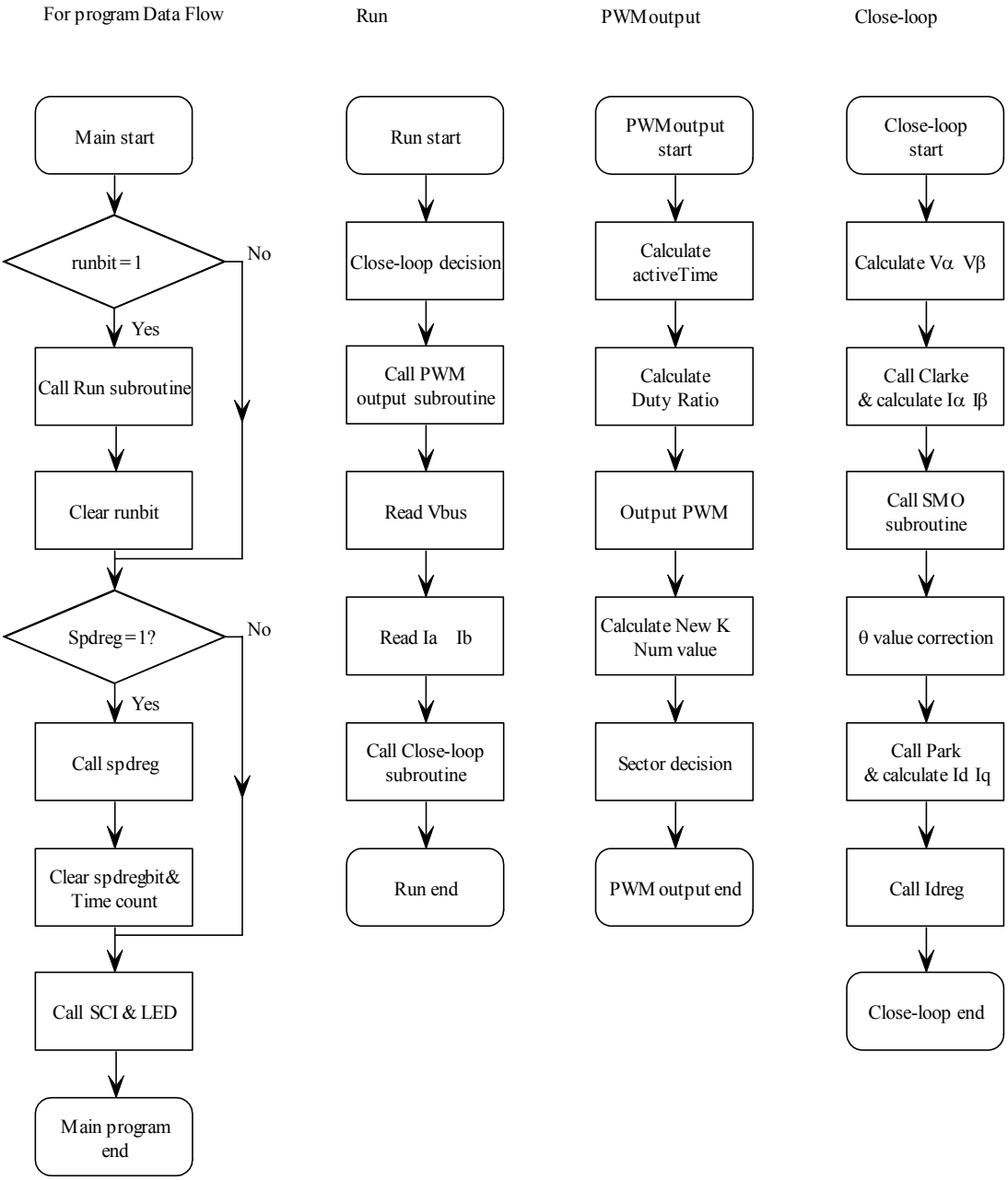


Figure 7-2. PMSM Block Diagram (Part 2 of 3)

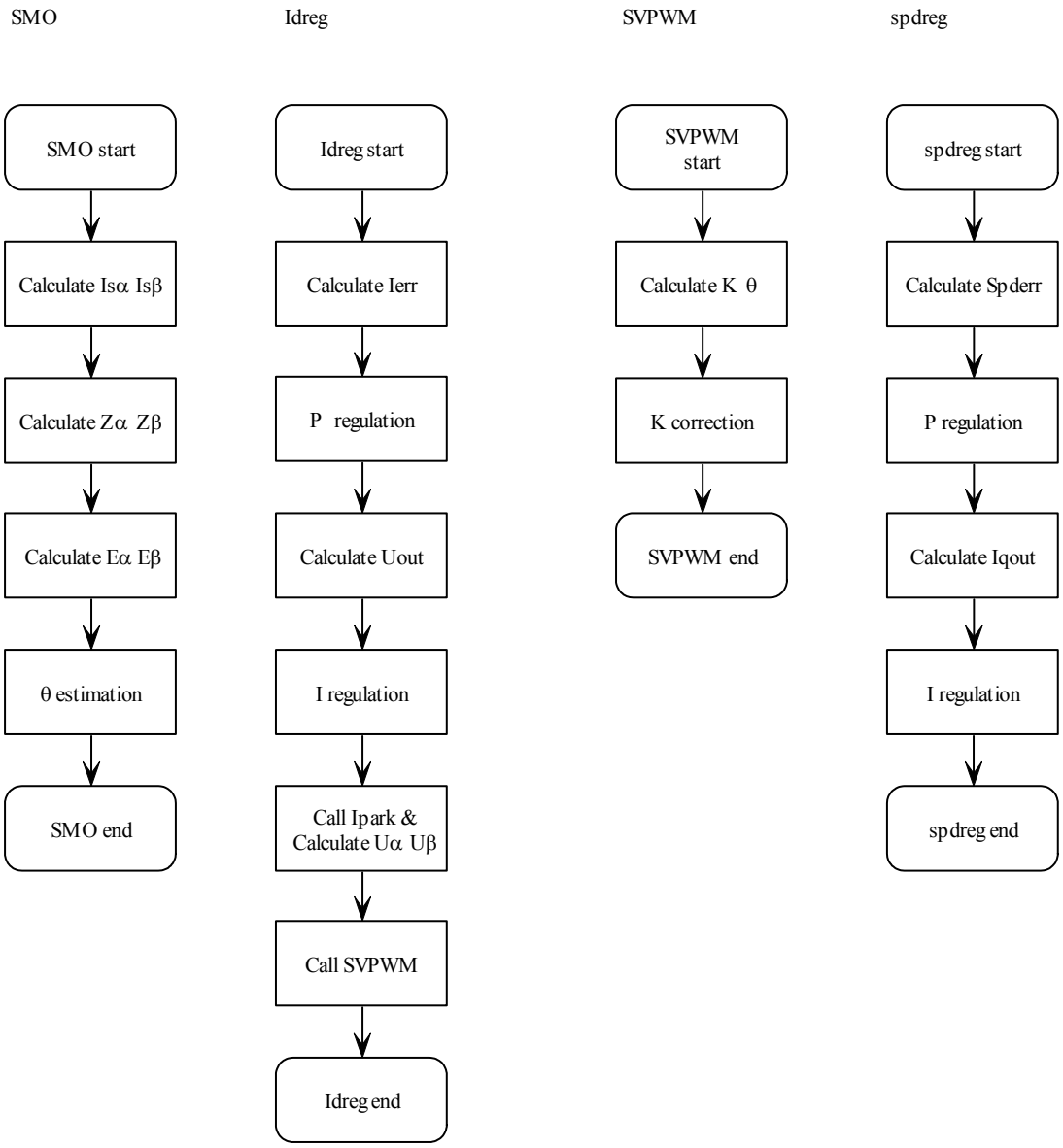


Figure 7-3. PMSM Block Diagram (Part 3 of 3)

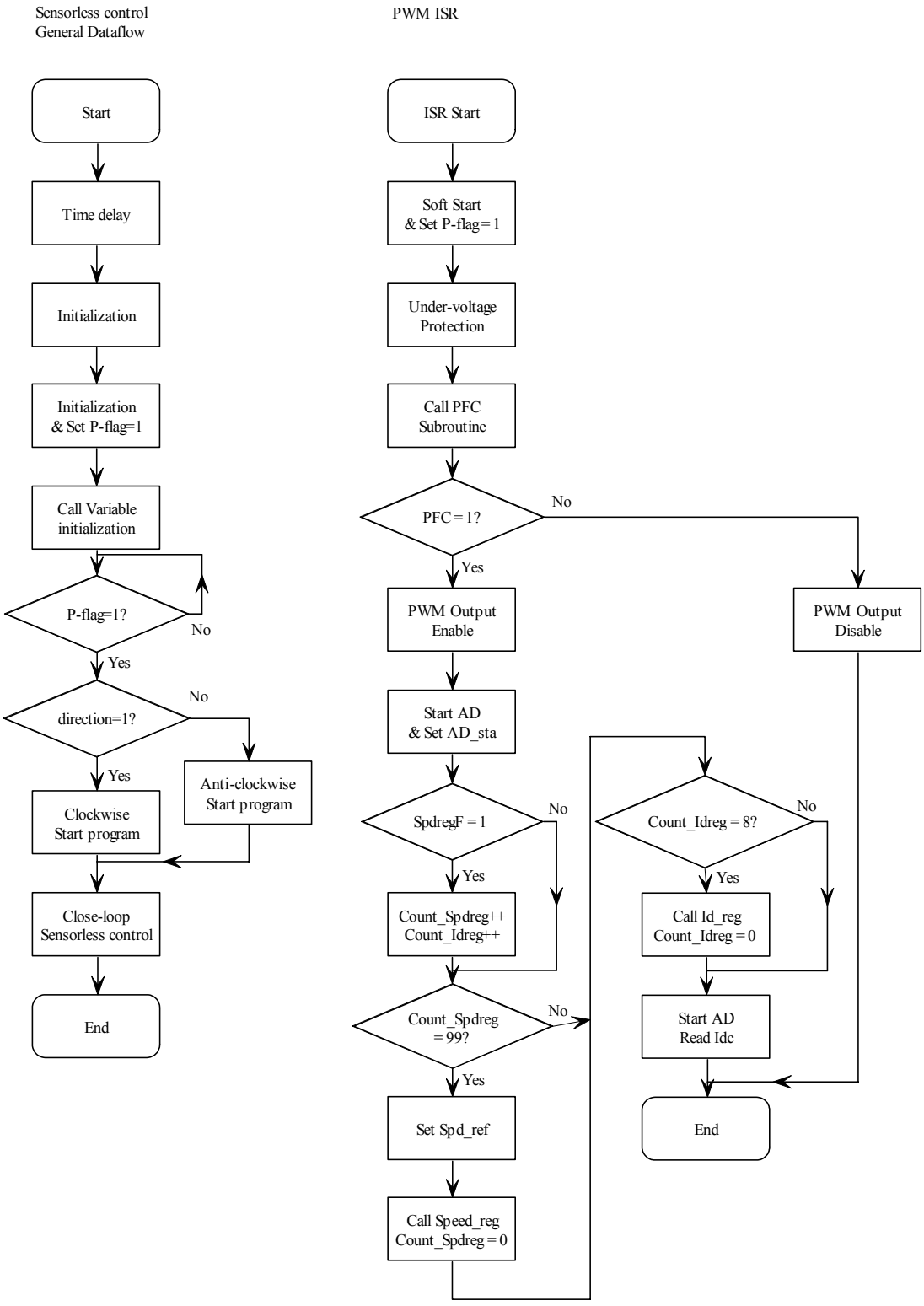


Figure 7-4. BLDC Block Diagram (Part 1 of 3)

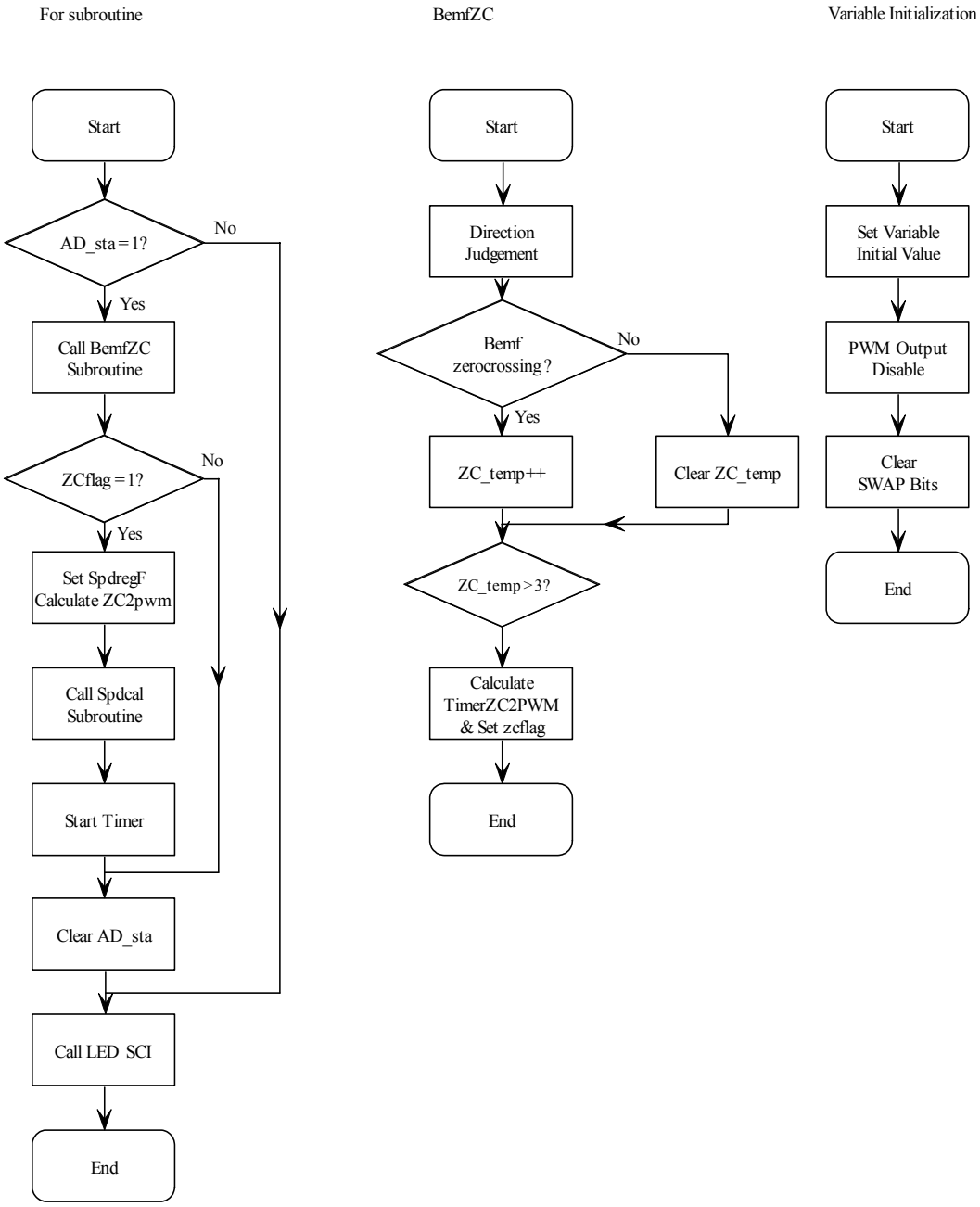


Figure 7-5. BLDC Block Diagram (Part 2 of 3)

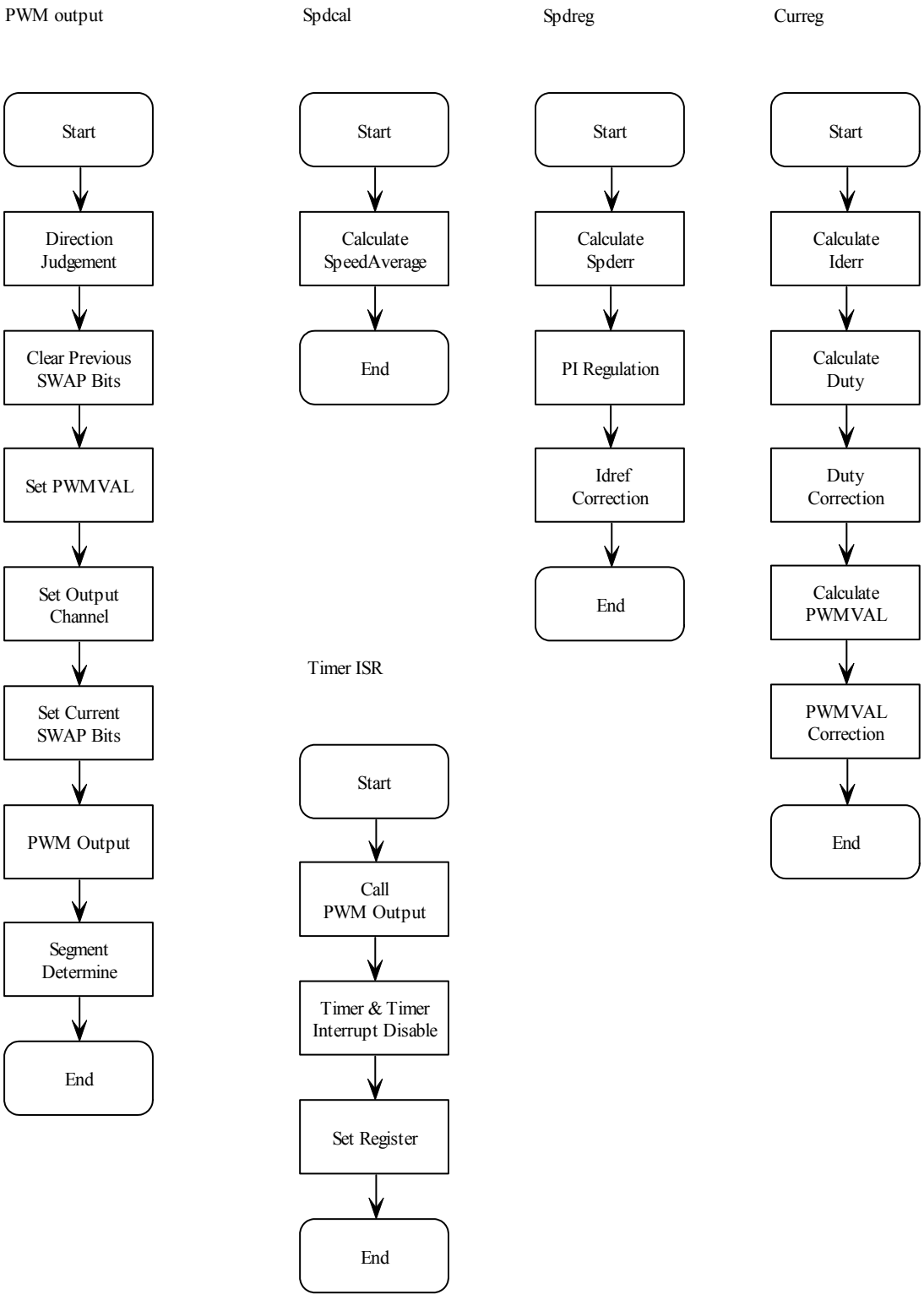


Figure 7-6. BLDC Block Diagram (Part 3 of 3)

7.2 Rotor Speed Estimation

A speed sensorless induction motor drive is a trend in today's low cost variable speed applications. Due to the cost and maintenance required by a speed transducer, speed sensorless technology is drawing more attention. For convenience, this application assumes a simple method to estimate rotor speed, described in Section 5.5.

7.3 Space Vector Pulse Width Modulation (SVPWM)

Space Vector Modulation (SVM) can directly transform the stator voltage vectors from an α, β-coordinate system to Pulse Width Modulation (PWM) signals (duty cycle values).

The standard technique for output voltage generation uses an inverse Clarke transformation to obtain 3-phase values. Using the phase voltage values, the duty cycles needed to control the power stage switches are then calculated. Although this technique gives good results, space vector modulation is more straightforward and realized more easily by a digital signal controller.

7.4 Fault Control

From the consideration of the cost control, optocoupler is not used in this system. The fault control process and its hardware should be designed to provide a solid protection against damage. In this application, due to the high complex of the pins, the fault1 to fault3 input pins are coupled with the PWM output pads. Only fault0 is valid for the detection of the rising edge generated by the fault signals. The overcurrent, overvoltage and overheat protections are merged together with the OR relation; that is, if any of them occur, the pin Fault0 will catch the edge and the fault process will dominate all resources and disable the PWM output pads. The routine will trap into the Interrupt Service Routine (ISR) once the fault occurs.

7.5 PFC Software Design

Power Factor (PF) is defined as the ratio between real power and apparent power of AC input. Assuming input voltage is a perfect sine wave, PF can be defined as the product of current distortion and phase shift. Consequently, the PFC circuit's main tasks are:

- Controlling inductor current, making the current sinusoidal and the same phase as input voltage
- Controlling output voltage, insuring the output voltage is stable

  The PFC main current needs two closed loops to control the circuit:

  — The voltage loop is the outer loop, which samples the output voltage and controls it to a stable level

  — The current loop is the inner loop, which samples inductor current and forces the current to follow the standard sinusoidal reference in order to reduce the input harmonic current

The system in this application is based on current Discontinuous Current Mode (DCM), in which there is only a voltage loop. DCM can make the current both sinusoidal and the same phase as input voltage.

PI loop control is widely used in industry control because of its simplicity and reliability. In this application, the voltage loop adopts PI regulator arithmetic.

These assumptions simplify analysis:

- Input current follows reference perfectly, which is proportional to the input voltage
- There is no additional power depletion in the circuit; power efficiency is 1
- Output power is constant

Figure 7-7. Simple PFC Mode

The function for output voltage:

$$\begin{cases} Uv(n) = K0v \times Ev(n) + Iv(n-1) \\ Iv(n) = Iv(n-1) + K1v \times Ev(n) + Kcorrv \times Epiv \\ Epiv = Usv - Uv(n) \end{cases}$$

$$Usv = \begin{cases} Uv_{\max} & when Uv(n) \geq Uv_{\max} \\ Uv_{\min} & when Uv(n) \leq Uv_{\min} \\ Uv(n) & else \end{cases}$$

Uv(n)	=	the result of PI unit
Ev(n)	=	input error
Iv(n)	=	integral unit
K0v	=	proportional constant
K1v	=	integral constant
Kcorrv	=	resistant saturation constant
Usv	=	result of voltage loop after limit
Uv_{max}	=	maximum of voltage loop
Uv_{min}	=	minimum of voltage loop

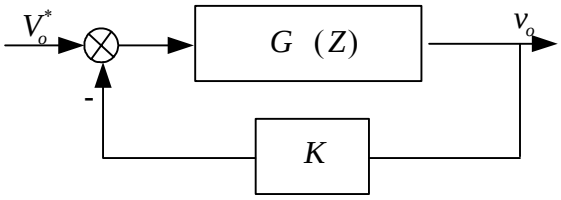


Figure 7-8. Discrete Voltage Loop Structure

Chapter 8
JTAG Simulation and SCI Communication

There are abundant software and hardware resources for JTAG simulation and communication in the 56F8013 device. With these resources, a 56F8013-based motor system can accomplish mixed communication functions, such as JTAG debug and SCI interface, between the power module and PC. Isolation is necessary between power electronics and microelectronics in the power system for safety.

The communication system consists of two parts:

- JTAG circuit, designed for debugging and programming the 56F8013
- SCI circuit, designed for background communication from the PC; power management and supervision can be realized conveniently

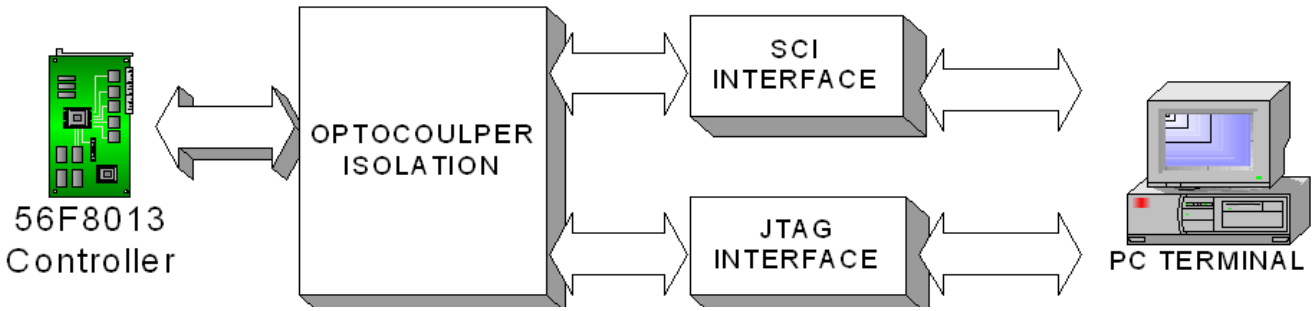


Figure 8-1. Communication Board's Frame Figure

8.1 JTAG Simulation Function

Because the 56800E core integrates the JTAG/EOnCE function, the 56F8013 can be debugged and programmed through the parallel port by a simple interface circuit without any special emulator. The debug function is provided by JTAG interface.

The power main circuit must be removed to ensure safety. During debugging, the connection for main power circuit should be cut off by disconnecting the J5000 connector on power board; see **Figure 8-2**.

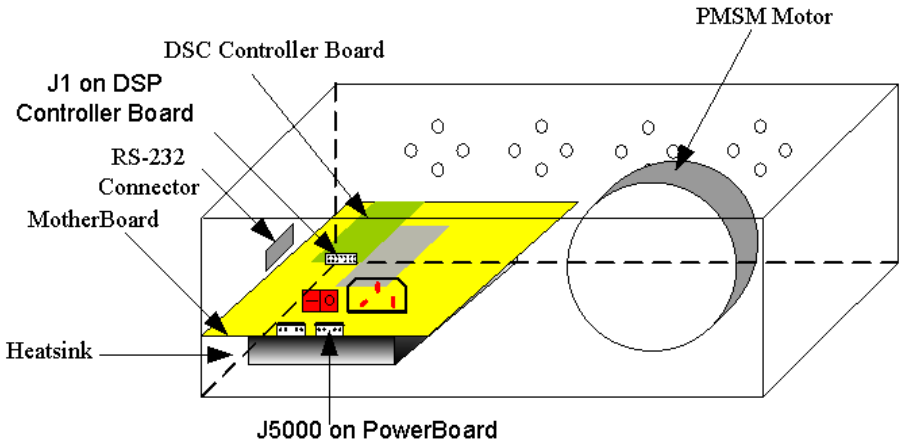


Figure 8-2. System Diagram

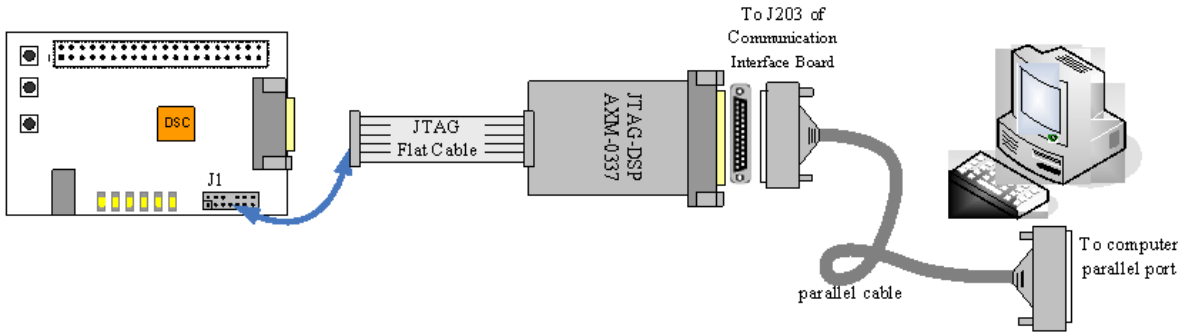


Figure 8-3. Connections for JTAG Simulation

As shown in **Figure 8-3**, the JTAG flat cable is connected to the 56F8013's J1. A parallel cable links the JTAG to PC's parallel port.

CAUTION
Disconnect J5000 in the Power Board before debugging or refreshing the control program. Otherwise, damage to or invalidation of the demo, or even electrical shock, can occur. Debugging or refreshing the control program should only be done by experienced personnel.

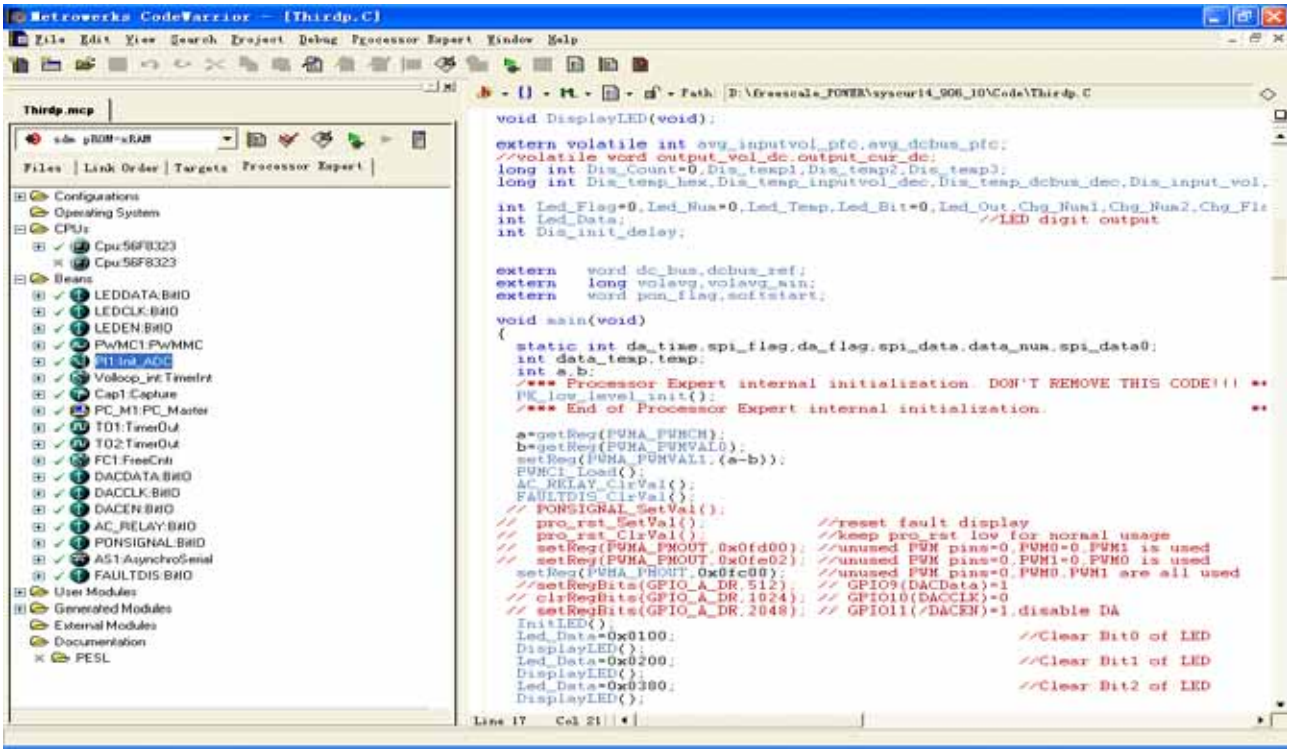


Figure 8-4. CodeWarrior Development Tool Interface

CodeWarrior IDE is necessary to debug software and refresh the program; version 7.0 or later is recommended. **Figure 8-4** shows the software interface. Details about installation and use can be found in the CodeWarrior documentation.

8.2 SCI Communication Function

Connections for SCI communication are shown in **Figure 8-5**. A serial cable links the RS-232 connector on the demonstration board to the PC's serial port.

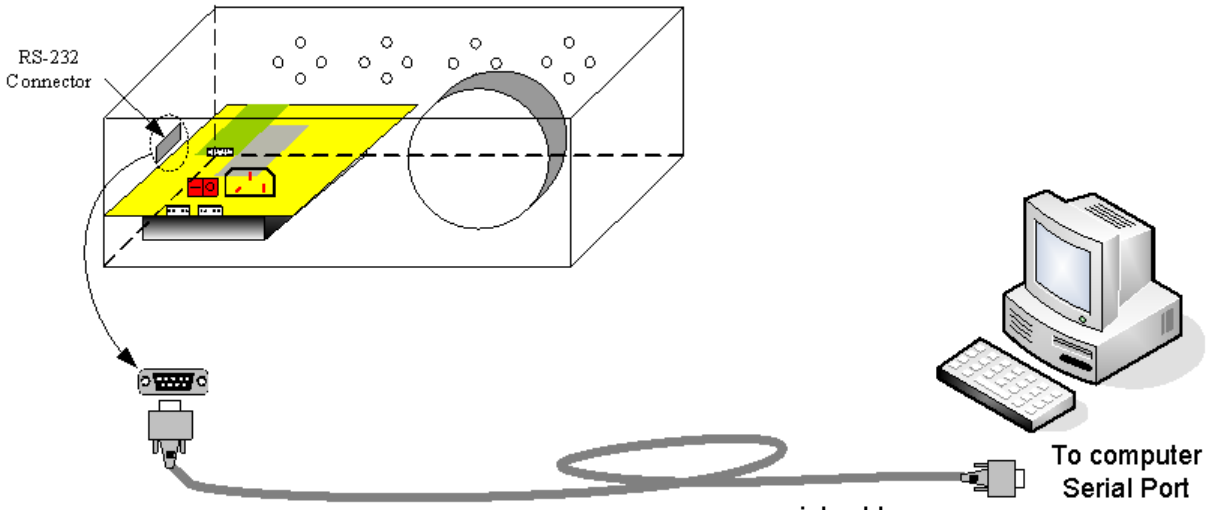


Figure 8-5. SCI Communication Connections

The PC master software tool can be used for development and control of the application. Details about installation and use of PC master software can be found in the CodeWarrior tool.

Chapter 9
Operation

This section offers brief instructions on operating the PMSM application.

9.1 Switch-on

Follow these steps to start the PMSM application:

1. Make sure the power switch is on the POWEROFF state, then put the plug in a wall socket
2. Switch the appliance on by pressing down the POWERON button.

   The 56F8013 starts the main power, and the PMSM begins to work

9.2 During Operation

1. LEDs on controllers can display system information
   - LED 1 displays the operating mode
   - LED 2 displays the rotation speed
2. SCI communication provides background supervision for the power module
   - SCI baud rate configuration: 4800 BPS
3. Debug function is provided by the JTAG interface

   See Caution, **Section 8.1** and **Section 9.4**.
4. To ensure the demo plate coupled on the shaft of the motor will not fly out, be sure the upper cover of the box is closed

9.3 Switch-off

To turn the application off, follow these steps:

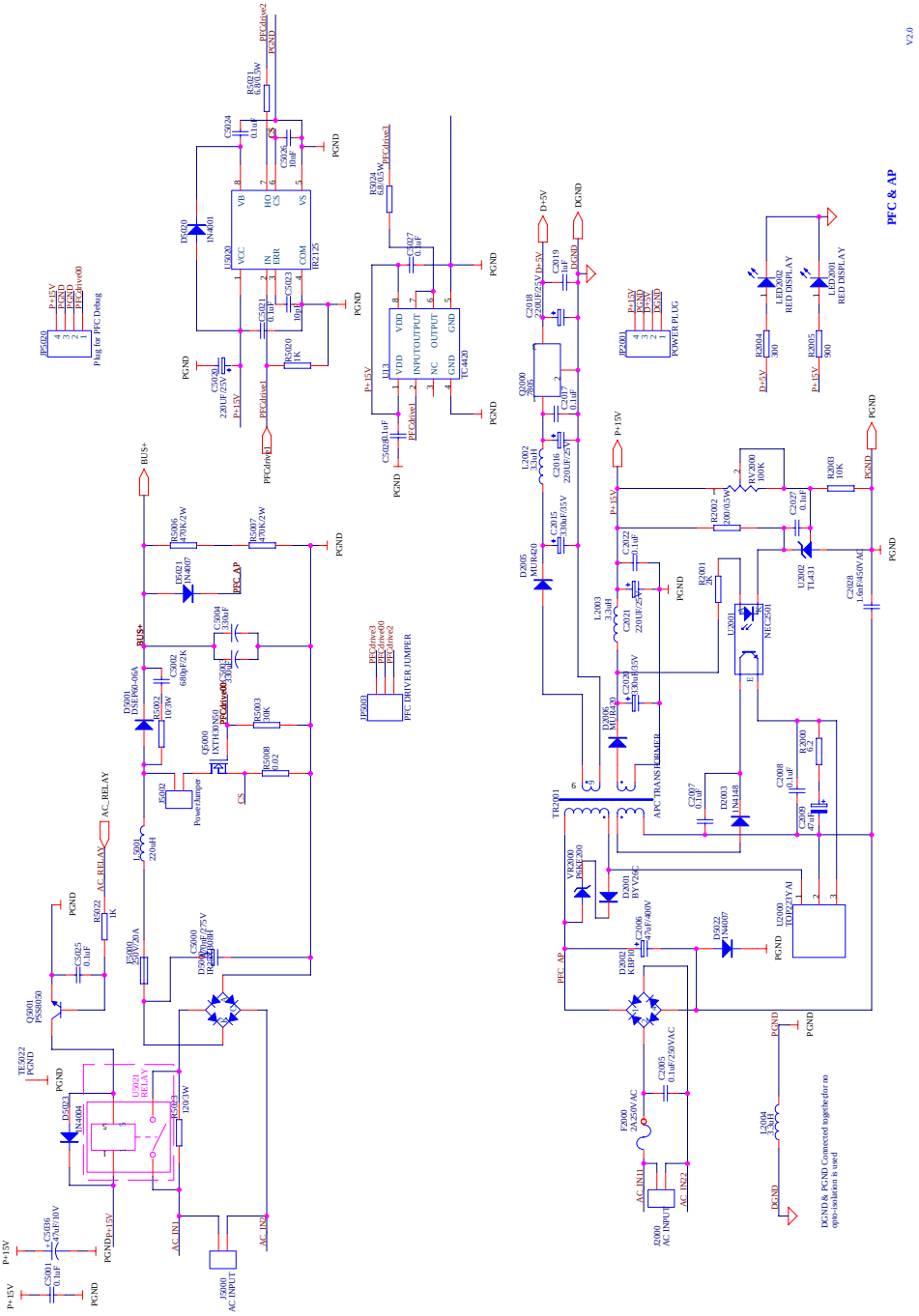
1. Switch off the POWERON Button
   - The 56F8013 cuts off the main power and the bus voltage is decreased
2. Unplug the power line.
   - The controller is powered off, and system is switched off

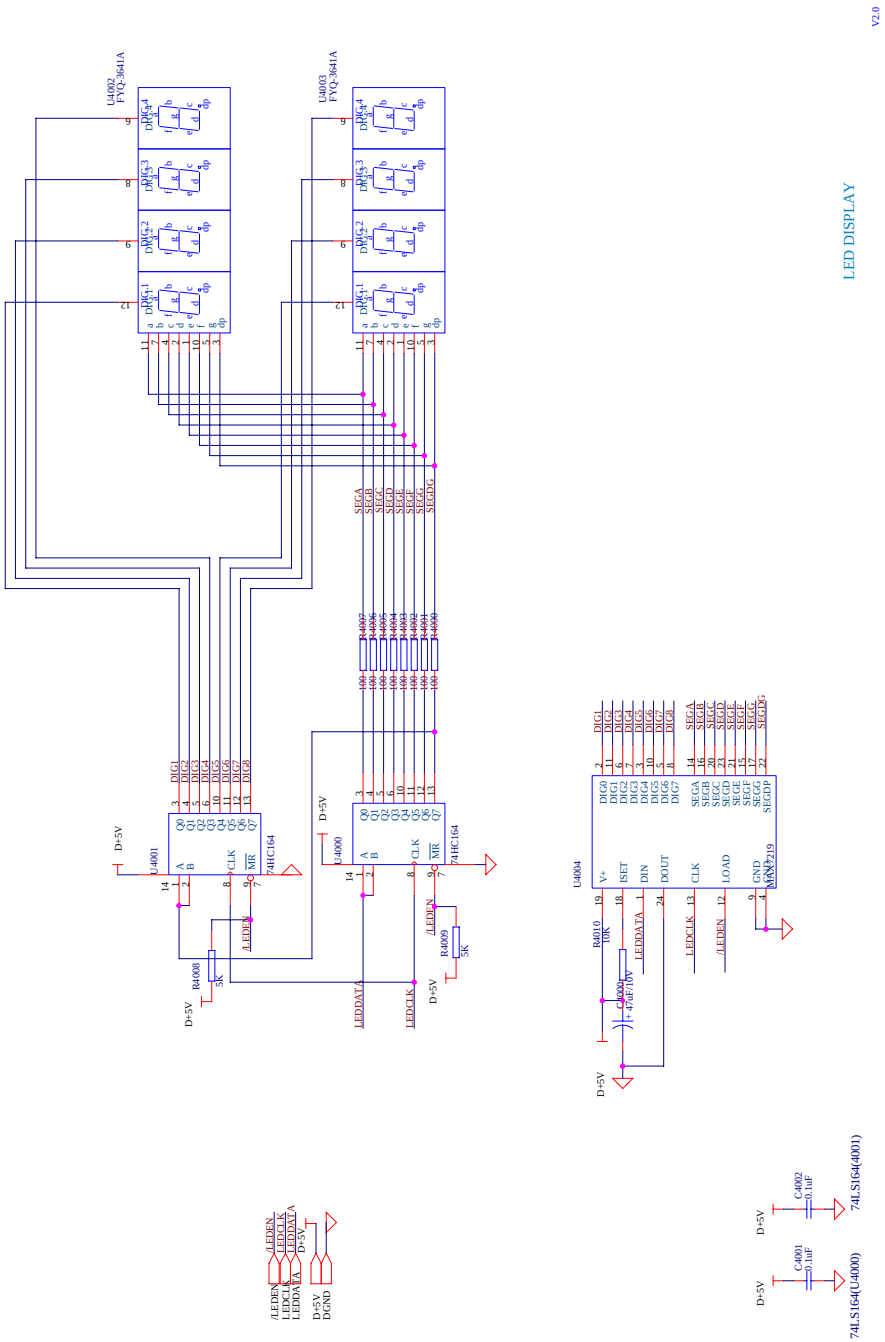
9.4 Cautions

To ensure safety, take care when:

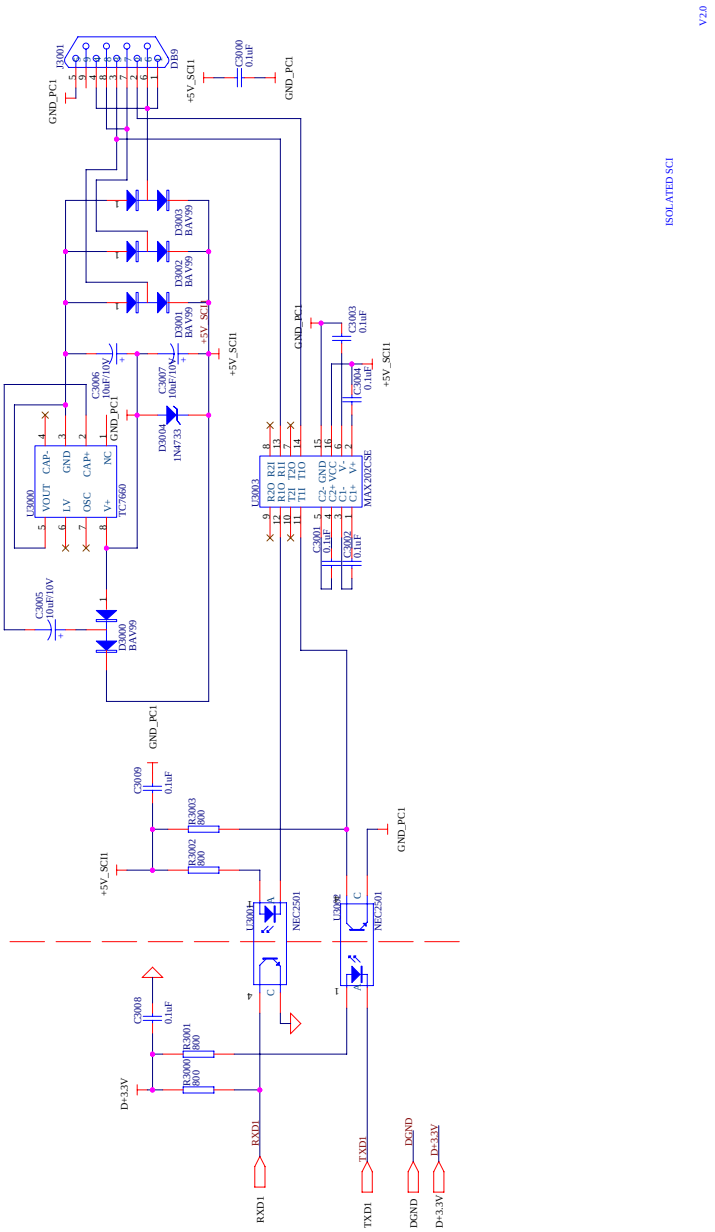
1. Pressing the POWERON Button down after the power line is plugged in during the switch-on process
2. Pressing the POWERON Button up before the power line is unplugged during the switch-off process
3. Debugging
   Before beginning the debug process, cut off power to the main power circuit by disconnecting the J5000 connector on the Power Board

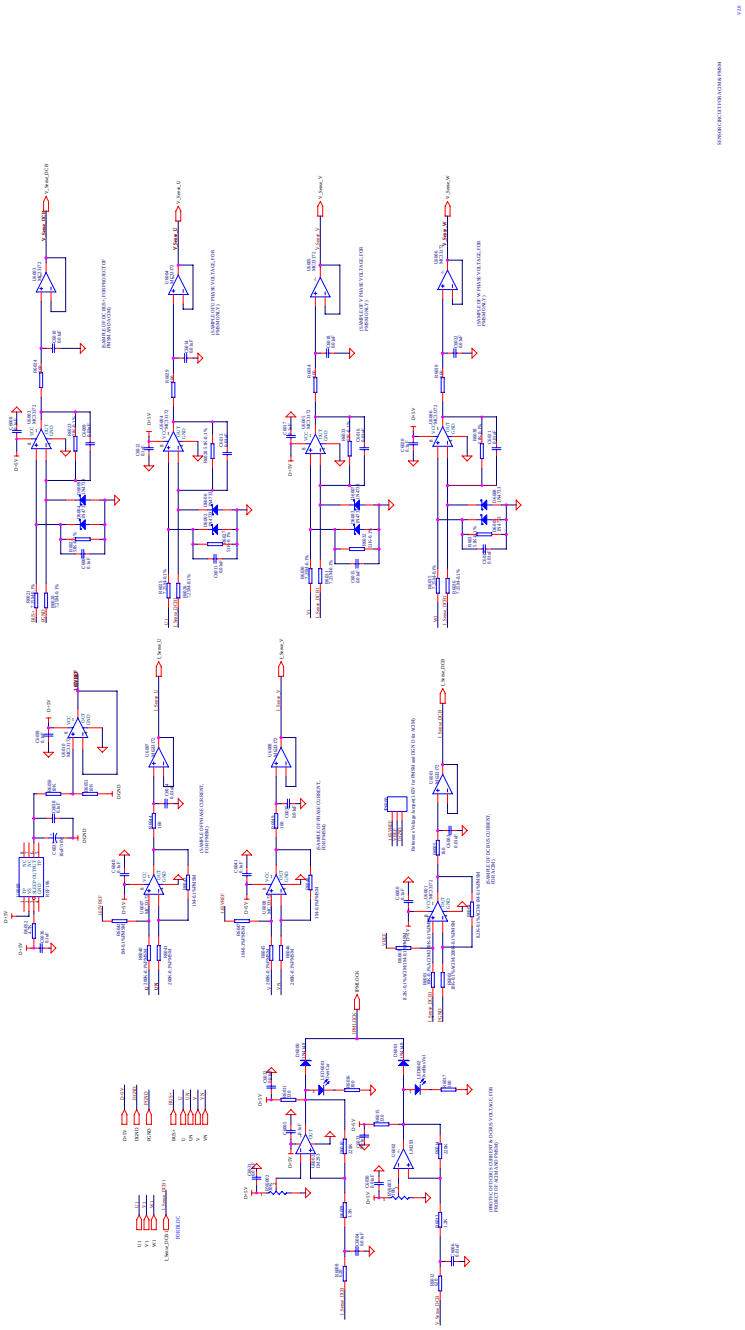
Appendix A
Schematics


PFC & AP
V2.0
BUS+
PGND
DGND
P+15V
D+5V
AC_RELAY
PFC_AP
PFCdrive1
PFCdrive2
PFCdrive3
PFCdrive4
Plug for PFC Debug
POWER PLUG
PFC DRIVER JUMPER
DCND & PGND Connected together for no opto-isolation is used



Schematics, Rev. 0


ISOLATED SCI
V2.0
J3001
DB9
GND_PC1
+5V_SCI1
C3000
0.1uF
D3003
BAV99
D3002
BAV99
D3001
BAV99
C3006
10uF/10V
C3007
10uF/10V
D3004
1N4733
U3000
TC7660
VOUT
CAP-
GND
CAP+
LV
NC
OSC
V+
C3005
10uF/10V
D3000
BAV99
U3003
MAX202CSE
R2O
R2I
R1O
R1I
T2I
T2O
T1I
T1O
C2-
GND
C2+
VCC
C1-
V-
C1+
V+
C3001
0.1uF
C3002
0.1uF
C3003
0.1uF
C3004
0.1uF
C3009
0.1uF
R3003
800
R3002
800
U3001
NEC2501
U3002
NEC2501
C3008
0.1uF
R3001
800
R3000
800
D+3.3V
RXD1
TXD1
DGND



Schematics, Rev. 0

Appendix B
PMSM and BLDC Demonstration Bill of Materials

Designator	Description	Footprint	Quantity
C1000, C6003, C6004,C6006, C6009, C6010, C6011, C6013, C6014, C6015, C6016, C6018, C6019, C6021, C6022, C6030, C6031, C6032, C6033, C6034, C6035	0.01 µF	RAD-0.1	21
C1001, C1009, C1037, C1038, C1039, C1040, C2007, C2008, C2017, C2022, C2027, C3000, C3001, C3002, C3003, C3004, C3008, C3009, C4001, C4002, C5001, C5021, C5024, C5025, C5027, C5028, C6000, C6005, C6007, C6008, C6012, C6017, C6020, C6036, C6038, C6039, C6040, C6041	0.1 µF	RAD-0.1	38
C1002, C1003	2.2 µF / 25 V	RB2.5/5	2
C1006, C1036	0.1 µF / 630V CBB	RAD15/18/6	2
C1008	0.1 mF / 25V	RB2.5/6	1
C1030, C1031, C1032, C1033, C1034, C1035	1 nF	RAD-0.1	6
C2005	0.1 uF / 250VAC	RAD15/18/6	1
C2006	47 µF / 400V	RB10/22.4	1
C2009	47 µF	RB2.5/5	1
C2015, C2020	330 µF / 35V	RB5/10	2
C2016, C2018, C2021, C5020	220 µF / 25V	RB3/8	4
C2019	1 µF	RAD-0.2	1
C2028	1.6 nF / 450VAC	RAD-0.4	1
C3005, C3006, C3007	10 µF / 10V	RB2.5/5	3
C4000, C5036	47 µF / 10V	RB2.5/5	2
C5000	470 nF / 275V	RAD22/26/9	1
C5002	650 pF / 2K	RAD-0.2	1
C5003, C5004	330 µF	RB10/30	2
C5023	10 pF	RAD-0.1	1
C5026	10 nF	RAD-0.1	1

Designator	Description	Footprint	Quantity
C6037	10 µF / 16V	RB2.5/5	1
D1000, D1001	IN4148	DIODE-0.4	2
D2001	BYV26C	DIODE-0.4	1
D2002	KBP10	KBP19	1
D2003	IN4148	DIODE-0.4	1
D2005, D2006	MUR420	DIODE-0.5	2
D3000, D3001, D3002, D3003	BAV99	SOT-23	4
D3004	IN4733	DIODE-0.4	1
D5000	IR25XB08H	IR25XB	1
D5001	DSEP60-06A	TO247AD	1
D5020	IN4001	IN4007	1
D5021, D5022	IN4007	IN4007	2
D5023	IN4004	IN4004	1
D6000, D6001	IN4148	DIODE-0.4	2
D6002, D6003, D6004, D6005, D6006, D6006, D6008, D6009	IN4733	DIODE-0.4	8
F2000	Fuse 2A 250 VAC	FUSE20/5/7	1
F5000	Fuse 250V / 20A	FUSE20/5/7	1
J2000, J5000	AC INPUT Connectors	CON5/3.96	2
J3001	DB9 Connector	DB9/M	1
J5002	Power Jumper	CON2/3.96	1
JP1000	Jumper HEAD	CON5/3.96	1
JP1001	Jumper UVW_OUTPUT	UVW	1
JP1002	Jumper LEM (For Debug Purpose)	HDR1X3	1
JP1004, JP1005	ADC Channel Jumper	HDR1X3	2
JP1006	Jumper Rotor Speed	HDR1X3	1
JP1007	Jumper SCI	IDC10	1
JP1008	ADC Channel Jumper	HDR1X3	1

Designator	Description	Footprint	Quantity
JP1009	ADC Channel Jumper	HDR1X3	1
JP1010	DSC Demo Board Connector	HDR2X20	1
JP1011, JP1012, JP1013, JP1014	Jumper for Push Button	HDR1X2	4
JP1015	Jumper PhaseU_up	HDR1X3	1
JP1016	Jumper PhaseU_down	HDR1X3	1
JP1017	Jumper PhaseV_up	HDR1X3	1
JP1018	Jumper PhaseV_down	HDR1X3	1
JP2001	Jumper PowerPlug	HDR1X4-5	1
JP4000	LED and DA	IDC10	1
JP5003	PFC Driver Jumper	HDR1X3	1
JP5020	Jumper Plug for PFC Debug	HDR1X4	1
JP6000	Reference Voltage Jumper (1.65 for PMSM and DGND for ACIM)	HDR1X3	1
L2002, L2003	3.3 µH	IND3.3u	2
L2004	3.3 µH	IND	1
L5001	220 µH	IND_PFC	1
LED1001	LED OverTemp	LEDA	1
LED2001, LED2002	RED LED DISPLAY	LEDA	2
LED6001	LED OverCur	LEDA	1
LED6002	LED OverBusVol	LEDA	1
Q1000, Q5001	PSS8050	TO-92A	2
Q5000	IXTH30N50	TO247AC	1
R1000, R1001	1.2K Ohm	AXIAL-0.4	2
R1002	130K Ohm	AXIAL-0.4	1
R1004	6.8K Ohm	AXIAL-0.4	1
R1008	6.8K Ohm	AXIAL-0.4	1

Designator	Description	Footprint	Quantity
R1009	10.2K	AXIAL-0.4	1
R1010	300 Ohm	AXIAL-0.4	1
R1011	4.7K Ohm	AXIAL-0.4	1
R1012	470V 1K Ohm	VVR	1
R1013	5.1K Ohm	AXIAL-0.4	1
R1014, R1015, R1016	2 Ohm (PMSM)	SHANT-0.5	3
R1017, R1018, R1019	0.5 Ohm (ACIM)	SHANT-0.5	3
R2000	6.2 Ohm	AXIAL-0.4	1
R2001	2K Ohm	AXIAL-0.4	1
R2002	200 Ohm / 0.5W	AXIAL-0.5	1
R2003	10K Ohm	AXILA-0.4	1
R2004	300 Ohm	AXIAL-0.4	1
R2005	900 Ohm	AXIAL-0.4	1
R3000, R3001, R3002, R3003	800 Ohm	AXIAL-0.4	4
R4000, R4001, R4002, R4003, R4004, R4005, R4006, R4007	100 Ohm	AXIAL-0.4	8
R4008, R4009	5K Ohm	AXIAL-0.4	2
R4010, R6050, R6051	10K Ohm	AXIAL-0.4	3
R5002	10 Ohm / 3W	R2WV	1
R5003	30K Ohm	AXIAL-0.4	1
R5006, R5007	470K Ohm / 2W	R2WV	2
R5008	0.02 Ohm	SHANT-0.2	1
R5020, R5022	1K Ohm	AXIAL-0.4	2
R5021, R5024	6.8 Ohm / 0.5W	AXIAL-0.5	2
R5023	120 Ohm / 3W	RXWV	1
R6001, R6002	10K Ohm - 0.1% (ACIM) / 200K Ohm - 0.1% (PMSM)	AXIAL-0.4	2
R6003, R6004	8.2K Ohm -0.1% (ACIM) / 1M Ohm -0.1% (PMSM)	AXIAL-0.4	2

Designator	Description	Footprint	Quantity
R6005, R6024, R6029, R6034, R6039, R6044, R6049	160 Ohm	AXIAL-0.4	7
R6008	620 Ohm	AXIAL-0.4	1
R6009, R6013	1.2K Ohm	AXIAL-0.4	2
R6010, R6014	220K Ohm	AXIAL-0.4	2
R6011, R6015	330 Ohm	AXIAL-04	2
R6012	620 Ohm	AXIAL-04	1
R6016, R6017	300 Ohm	AXIAL-04	2
R6020, R6021, R6025, R6026, R6030, R6031, R6035, R6036	7.25M Ohm - 0.1%	AXIAL-04	8
R6022, R6023, R6027, R6028, R6032, R6033, R6037, R6038	51K Ohm - 0.1%	AXIAL-04	8
R6040, R6041, R6045, R6046	200K Ohm - 0.1% (PMSM)	AXIAL-04	4
R6042, R6043, R6047, R6048	1M Ohm - 0.1% (PMSM)	AXIAL-04	4
R6052	4.7K Ohm	AXIAL-04	1
RP1000	Resistor Pack 8 X 5K Ohm	SIP9	1
RV1000, RV6002, RV6003	10K Ohm	VRESLV	3
RV2000	100K Ohm	VRESLV	1
S1000	Button Function1	BUTTON	1
S1001, S1002	Button Function2	BUTTON	2
S1003	Button Function3	BUTTON	1
TE10	Test point PWM0	SIP-1	1
TE11	Test point PWM1	SIP-1	1
TE12	Test point PWM2	SIP-1	1
TE13	Test point PWM3	SIP-1	1
TE14	Test point PWM4	SIP-1	1
TE15	Test point PWM5	SIP-1	1
TE5022	PGND	SIP-1	1
TR2001	APC Transformer	TRAN-E133-2	1

Designator	Description	Footprint	Quantity
U13	TC4420	DIP8	2
U1000	MC74HC244	DIP20	1
U1001, U6002	LM293	DIP8	2
U1002	IRAMS10UP60A	IRAMS10UP60A-2	1
U2000	TOP223YAI	TO-220	1
U2001, U3001, U3002	NEC2501	DIP4	3
U2002	TL431	TL431	1
U3000	TC7660	SO-8	1
U3003	MAX202CSE	DIP16	1
U4000, U4001	74HC164	DIP14	2
U4002, U4003	FYQ-3641A	LG3641AH	2
U4004	MAX7219	DIP24	1
U5020	IR2125	DIP8	1
U5021	RELAY		1
U6001, U6003, U6004, U6005, U6006, U6007, U6008, U6010	MC33172	DIP8	8
U6009	REF196	DIP-8	1
VR2000	P6KE200	DIODE-0.4	1

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