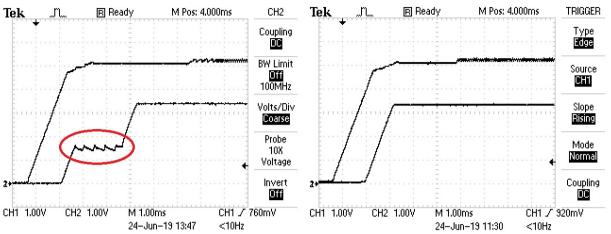


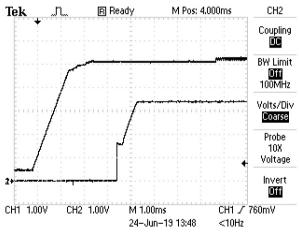
Using contact<u>less</u> interface only with internal RF transmitter power TVDD_OUT.

The 3.3V PVDD_OUT has a 2ms unstable plateau during power up while the PN7462 RESET input is low (active)

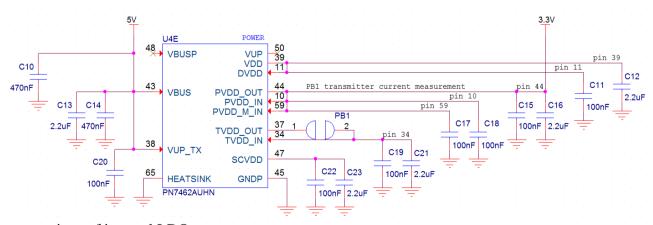


1: VBUS 5V, 2: PVDD_OUT 3.3V

OK if RST_N is pulled-up to PVDD_OUT



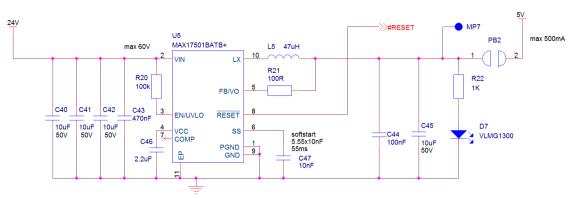
1: VBUS 5V, 2: RST_N input



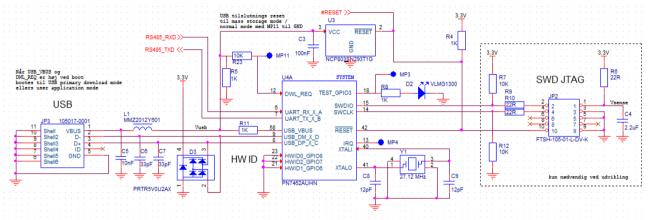
connections of internal LDOs.

Total capacity on PVDD_OUT 2.2+2.2+0.1+0.1uF. More or less does'nt change anything.

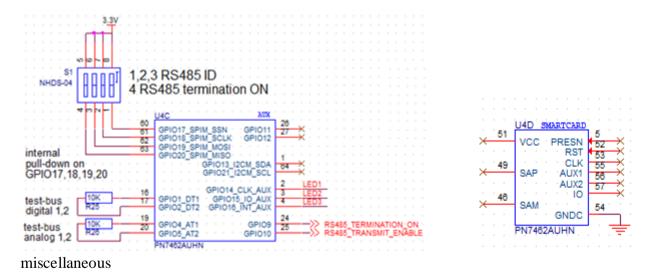




standard 5V swithmode powersupply



USB/SWD interface



What is preventing the PVDD_OUT startup when RST_N is active?

Why is the RST_N input pin not listed in the PN7462 family datasheet rev. 4.3, 24 January 2019, chap 8.16.1 table 25 ?