AH1103

LIN transceiver TJA1021 / TJA1022 / TJA1024 / TJA1027 / TJA1029

Rev. 3.0 — 13 January 2015 **Application Hints**

Document information

Info	Content
Title	LIN transceiver TJA1021 / TJA1022 / TJA1024 / TJA1027 / TJA1029
Author(s)	Rainer Evers
Department	Systems & Applications (AIC)
Keywords	TJA1021; TJA1022; TJA1024; TJA1027; TJA1029; Local Interconnect Network (LIN); LIN 2.0; LIN 2.1; LIN 2.2; LIN 2.2A; SAE J2602; ISO 17987; ISO 9141; K-Line; LIN transceiver; Physical Layer; Single channel; Dual channel; Quad channel

Revision history

Rev	Date	Description
3.0	20150113	TJA1024 application hints added and TJA1021 changeover hints added
2.0	20121114	TJA1029 application hints added
1.1	20121029	Section 3 added
1.0	20120308	Initial version

Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

This report describes the technical implementation of the LIN transceiver TJA1021 [3], TJA1022 [5], TJA1024 [24], TJA1027 [4] and TJA1029 [22] as Physical Medium Attachment within LIN. Its focus is to provide application hints / recommendations for the design of LIN electronic control units (ECUs) using the LIN transceiver TJA1021, TJA1022, TJA1024, TJA1027 and TJA1029 from NXP Semiconductors.

1.1 LIN basics

The Local Interconnect Network (LIN) is a low speed (max. 20 kBd) Class-A, serial bus protocol. A LIN sub-bus is primarily intended for modules like seat, door, roof, switch panel, steering wheel, etc. Its task is to connect switches, actuators and sensors into a sub-bus that links to the main bus e.g. a CAN bus.

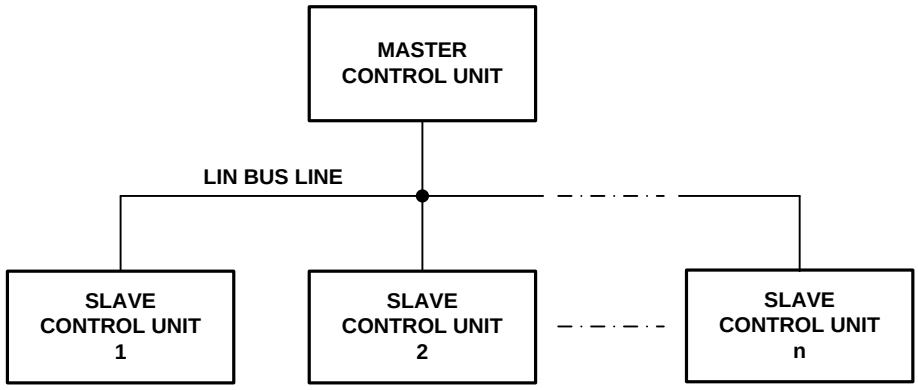


Fig 1. Single-master / multiple-slave concept

The LIN protocol [6] is based on the UART/SCI serial data link format using 8N1-coded byte fields. A LIN network consists of one master node and one or more slave nodes; the medium access is controlled by the master node. Such a single-master/multiple-slave concept is shown in Fig 1.

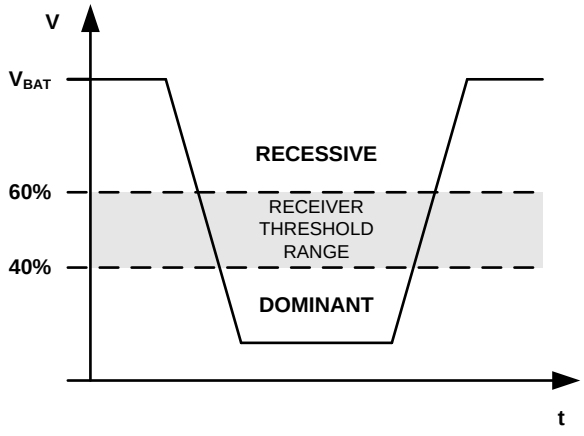


Fig 2. Voltage levels on the LIN bus line

The LIN physical layer has been derived from the ISO 9141 [11] standard but has some enhancements to meet the particular operation requirements in automotive environments such as EMC, ESD, etc. The LIN bus is a single-wire, wired AND bus with a 12V-battery related recessive level. Beside the LIN [6] and SAE J2602-1 [10] specifications the LIN physical layer is specified in the ISO 17987 standard [26]. The voltage levels on the LIN bus line are shown in Fig 2.

Fig 3 illustrates a block diagram of a typical LIN ECU.

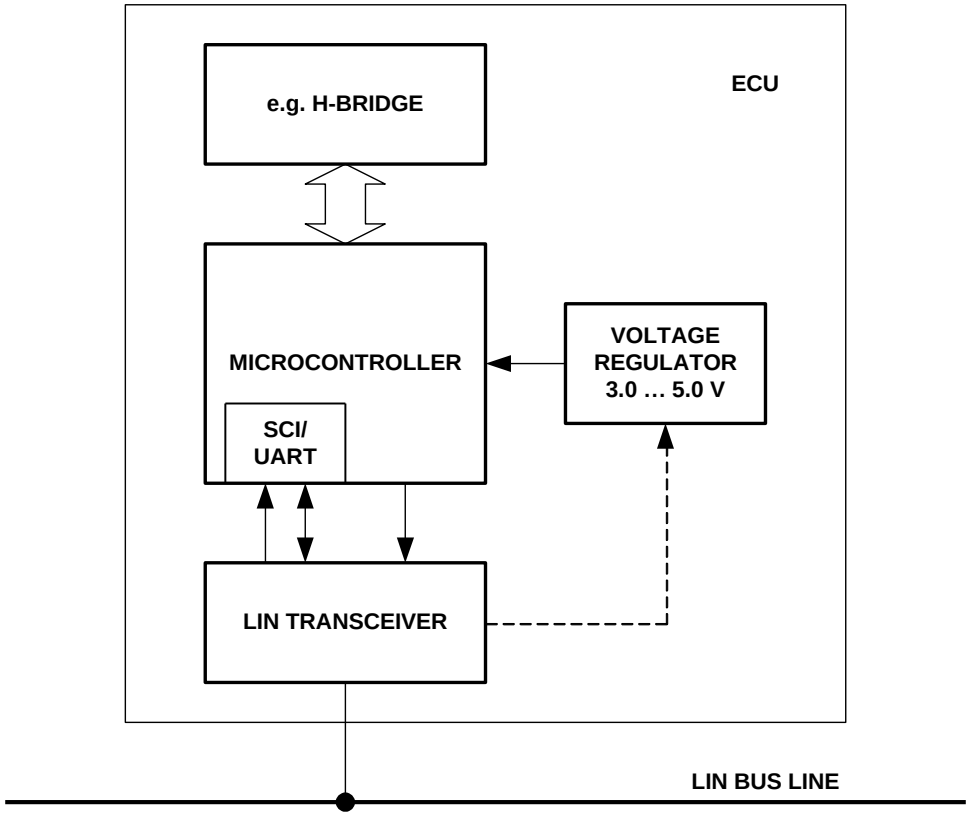


Fig 3. Block diagram of a typical LIN ECU

1.2 Standalone LIN transceiver overview

Table 1 lists a feature overview of the LIN transceiver TJA1020 [1], TJA1021 [3], TJA1022 [5], TJA1024 [24], TJA1027 [4] and TJA1029 [22].

Table 1. Feature overview

Feature	TJA1020	TJA1021	TJA1027	TJA1029	TJA1022	TJA1024
General						
LIN transceiver channels	1	1	1	1	2	4
ISO 17987 compliant		✓	✓	✓	✓	✓
LIN 2.x compliant (LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A)		✓	✓	✓	✓	✓
LIN 1.3 compatible	✓	✓	✓	✓	✓	✓
SAE J2602 compliant	✓	✓	✓	✓	✓	✓

Feature	TJA1020	TJA1021	TJA1027	TJA1029	TJA1022	TJA1024
K-Line compatible	✓	✓	✓	✓	✓	✓
Baud rate up to 20 kBd	✓	✓	✓	✓	✓	✓
Sleep mode with very low power consumption (max 10 µA)	✓	✓	✓	✓	✓	(max 20 µA)
• LIN bus remote wake-up	✓	✓	✓	✓	✓	✓
• Local wake-up	✓	✓				
• Wake-up source recognition	✓	✓				
Input levels compatible with 3.0 V, 3.3 V and 5.0V	✓	✓	✓	✓	✓	✓
Integrated termination resistor for LIN slave applications	✓	✓	✓	✓	✓	✓
Passive behavior in unpowered state	✓	✓	✓	✓	✓	✓
Operational during cranking pulse: full operation	>5.0 V [1]	> 5.5 V	> 5.0 V	> 5.0 V	> 5.0 V	> 5.0 V
Undervoltage detection		✓	✓	✓	✓	✓
Very low ElectroMagnetic Emission (EME)	✓	✓	✓	✓	✓	✓
Low slope mode / variant	✓	✓				
Protection						
Very high ElectroMagnetic Immunity (EMI)	✓	✓	✓	✓	✓	✓
Very high ESD robustness according to IEC 61000-4-2 for pins LIN, V_{BAT} and WAKE_N (if pin is available)	(±6 kV) [2]	±6 kV	±8 kV	±8 kV	±8 kV	±8 kV
Bus terminal and battery pin protected against transients in the automotive environment (ISO 7637)	✓	✓	✓	✓	✓	✓
Very high load dump robustness according to IEC 16750-2 for pins LIN, V_{BAT} and WAKE_N (if pin is available)	40 V	40 V	42 V	42 V	42 V	42 V
Bus terminal short-circuit proof to battery and ground	✓	✓	✓	✓	✓	✓
Thermally protected	✓	✓	✓	✓	✓	✓
Initial transmit data (TXD) dominant check	✓	✓	✓	✓	✓	✓
Transmit data (TXD) dominant time-out function	✓	✓		✓	✓	✓
Packages						
SO8 (SOT96-1)	✓	✓	✓	✓		
HVSON8 (SOT782-1); leadless package (3.0 mm x 3.0 mm) with improved Automated Optical Inspection (AOI) capability		✓	✓	✓		
SO14 (SOT108-1)					✓	
HVSON14 (SOT1086-2); leadless package (3.0 mm x 4.5 mm) with improved Automated Optical Inspection (AOI) capability					✓	
HVQFN24 (SOT815-1); leadless package (3.5 mm x 5.5 mm) with improved Automated Optical Inspection (AOI) capability						✓

[1] In the supply voltage operation range between 5.0 V and 7.3 V are parameter deviations possible.

[2] With additional external LIN-bus ESD protection diode PESD1LIN.

1.2.1 TJA1020

The TJA1020 [1] is the first LIN transceiver released from NXP Semiconductors. Application hints for the TJA1020 are covered in the Application Note AN00093 [2].

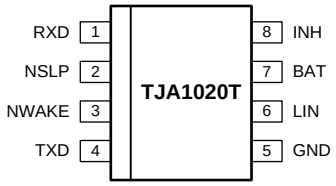
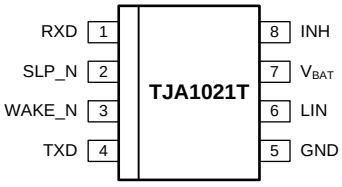


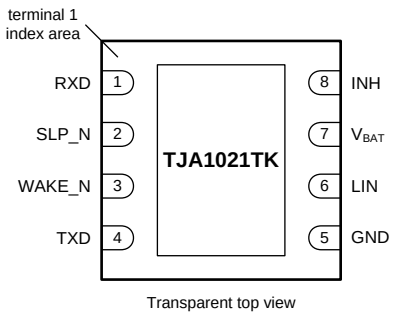
Fig 4. TJA1020 pinning diagram

1.2.2 TJA1021

The TJA1021 [3] was the first LIN 2.1 compliant LIN transceiver worldwide. The pinning (see Fig 5) is compatible to the TJA1020 and the feature set (see Table 1) is similar to the TJA1020. Details on the transceiver differences are described in section 2.



(1) SO8



(2) HVSON8

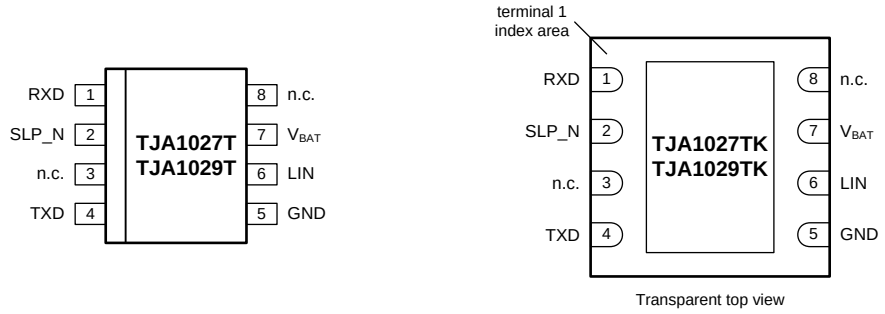
Fig 5. TJA1021 pinning diagram

1.2.3 TJA1027 and TJA1029

The LIN transceivers TJA1027 [4] and TJA1029 [22] are system efficient transceivers for LIN applications, where neither switch event detection via WAKE pin nor voltage regulator control via INH pin is required. With these transceivers the functional overhead and the hardware and software complexity is reduced to a minimum. Beside the SO8 package both transceivers are also provided in a very small leadless HVSON8 package, which supports automated optical inspection (see Fig 6).

Only difference between TJA1027 and TJA1029 is the TXD dominant time-out function, which is not provided by the TJA1027.

The differences to the TJA1021 are described in section 2.

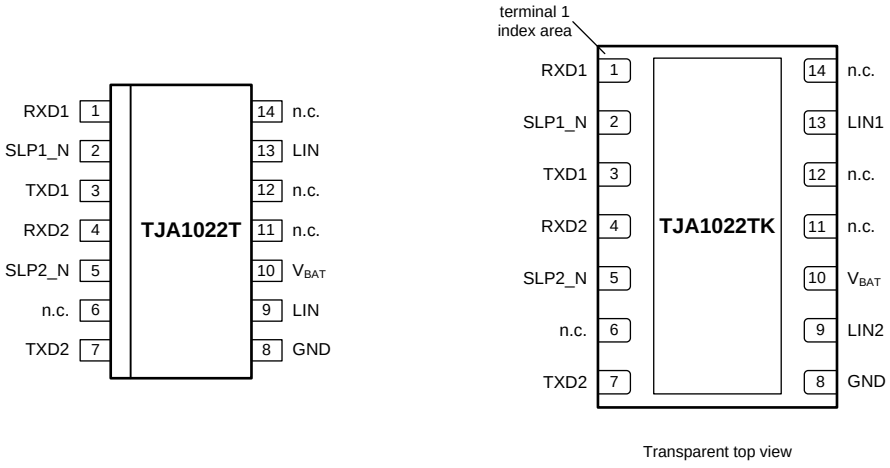


(1) SO8 (2) HVSON8

Fig 6. TJA1027 and TJA1029 pinning diagram

1.2.4 TJA1022

The TJA1022 is a so-called dual LIN transceiver, i.e. this transceiver has two LIN transceiver channels. In order to support LIN channel scalability on the board the lower part of the TJA1022 pinning (see Fig 7) is compatible to single channel LIN transceivers such as TJA1020, TJA1021, TJA1027 and TJA1029. The state diagram per LIN channel is equal to TJA1027, TJA1024 and TJA1029, which enables LIN software driver reuse.



(1) SO14 (2) HVSON14

Fig 7. TJA1022 pinning diagram

1.2.5 TJA1024

The TJA1024 is a LIN device with four LIN transceiver channels. It provides independent mode control for each channel respectively. The state diagram per LIN channel is equal to TJA1027, TJA1022 and TJA1029, which enables LIN software driver reuse. The TJA1024 is available in a DHVQFN24 package (3.5 mm × 5.5 mm). This package is a leadless package, which supports automated optical inspection. In Fig 8 the TJA1024 pinning is illustrated.

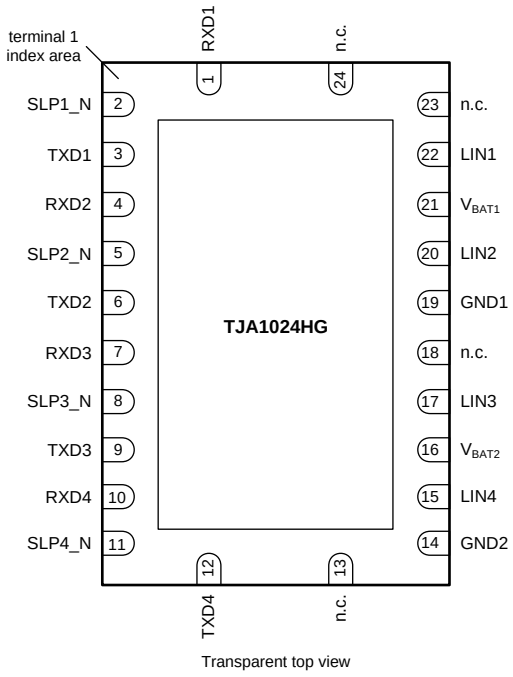


Fig 8. TJA1024 pinning diagram

2. Transceiver differences

An overview of the functional differences between TJA1021, TJA1022, TJA1024 TJA1027 and TJA1029 is listed in Table 2.

Table 2. Overview of functional differences

Feature	TJA1021	TJA1022	TJA1024	TJA1027	TJA1029	Description
LIN channels	1	2	4	1	1	
EMC	approved at automotive manufacturers	further improved EMC performance	further improved EMC performance	further improved EMC performance	further improved EMC performance	
ESD	± 6kV [17] (150pF/330Ω)	± 12kV [19] (150pF/330Ω)	± 11kV [25] (150pF/330Ω)	± 12kV [18] (150pF/330Ω)	± 12kV [23] (150pF/330Ω)	Table 9
Low slope variant (/10)	yes	no	no	no	no	Section 4.3.2
Mode after power-on	Power-on mode	Sleep mode	Sleep mode	Sleep mode	Sleep mode	
Operation during cranking pulse (for e.g. Start-Stop, RKE, …)	LIN operation down to 5.5 V (fully specified in data sheet)	LIN operation down to 5.0 V (fully specified in data sheet)	LIN operation down to 5.0 V (fully specified in data sheet)	LIN operation down to 5.0 V (fully specified in data sheet)	LIN operation down to 5.0 V (fully specified in data sheet)	
LIN speed	1 … 20 kBd	2.4 … 20 kBd	2.4 … 20 kBd	0 … 20 kBd	2.4 … 20 kBd	
TXD dominant time-out	yes	yes	yes	no	yes	
INH (High-side switch for VReg, master termination, battery monitoring, etc)	yes	no	no	no	no	Section 4.1.7
WAKE_N (local wake-up input)	yes	no	no	no	no	Section 4.1.6

3. Upgrading hints

3.1 TJA1020 upgrading guidance

Motivations for an upgrade of existing TJA1020 applications towards the newer products TJA1021 or TJA1027 or TJA1029 are

- Compliance to LIN 2.x
- Enhanced ESD performance
- System cost optimization, if not all features of the TJA1020 are used
- Board space reduction

Depending on the application the TJA1021, the TJA1027 or the TJA1029 is the optimum choice to upgrade a TJA1020 ECU. If in the application pin NWAKE and/or pin INH of the TJA1020 are used, the TJA1021 should be applied as replacement. Else if a TXD dominant time-out function is required the TJA1029 is recommended to replace the TJA1020. Otherwise the TJA1027 could be the optimum choice to upgrade a TJA1020 ECU. In Fig 9 this is illustrated.

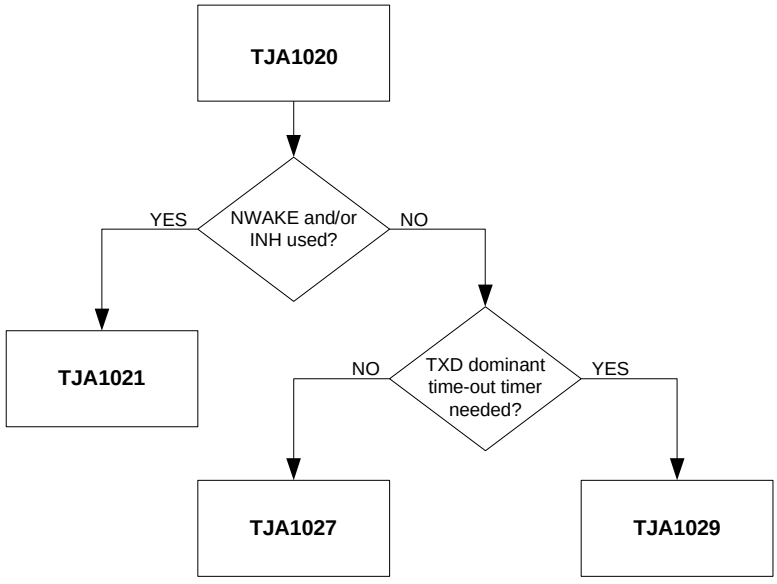


Fig 9. TJA1020 upgrading guidance

3.2 TJA1020 – TJA1021

Table 3 lists the differences between the TJA1021 and TJA1020. In the following chapters the details are described

Table 3. Overview of functional improvements compared to the TJA1020

No.	Functional improvement TJA1021	Description in …
1	LIN 2.x / SAE J2602 / ISO 17987 Physical Layer	Section 3.2.1
2	ESD robustness	Section 3.2.2
3	Normal Slope mode only (no Low Slope mode provided)	Section 3.2.3
4	1st state after BAT power-on enables INH switch	Section 3.2.4
5	TxD dominant time-out has been made longer	Section 3.2.5
6	Start-up time entering Normal mode	Section 3.2.6
7	Transmitter and Receiver Operation Range	Section 3.2.7

3.2.1 LIN 2.x / SAE J2602 / ISO 17987 physical layer

The physical layer of the TJA1021 [3] is compliant to LIN 2.0 [8], LIN 2.1 [7], LIN 2.2A [6] SAE J2602-1 [10] and ISO 17987-4 [26]. Hence, compared to the TJA1020 [1] the TJA1021 provides improved transmission reliability.

TJA1021 drop-in compatibility impact to TJA1020 applications:

- No impact to software.
- No impact to hardware (Note: The LIN driver is specified for the supply range from 5.5 V to 18 V).

3.2.2 ESD robustness

The robustness of the TJA1021 against ESD has been increased compared to the TJA1020. The TJA1021 withstands ESD voltages up to ±8 kV according to JESD22-A114-B (100 pF / 1.5 kΩ) and up to ±6 kV according to IEC 61000-4-2 [21] (150 pF / 330 Ω). Hence, it can be considered to omit external ESD protection devices.

TJA1021 drop-in compatibility impact to TJA1020 applications:

- No impact to software.
- No impact to hardware.

3.2.3 Normal Slope mode only

The TJA1021 provides one transmission mode only. Thus the Low Slope mode control function from the TJA1020 is not implemented into the TJA1021. Instead a low slope variant of TJA1021 for 10.4 kBd is provided (see also Section 4.3.2). This has the advantage that the mode pin SLP_N might be connected to the microcontroller supply directly, if no dedicated low power mode control is required. For the TJA1020 it is recommended to connect the SLP_N to a microcontroller port pin in order to enter a defined transmission mode (Normal Slope or Low Slope).

Regardless whether a TJA1020 software driver was used to enter the Normal Slope mode or Low Slope mode, such a software driver, when applied to the TJA1021, would enter the Normal mode of the TJA1021.

TJA1021 drop-in compatibility impact to TJA1020 applications:

- No impact to software.
- No impact to hardware.

3.2.4 Power-on behavior

After power-on (supply voltage on V_{BAT} is switched on) the TJA1021 enables the INH switch. This 1st state is called the Power-on mode [3]. The 1st state after power-on of the TJA1020 is the Sleep mode [1], where the INH switch is disabled. Thus, for TJA1020 applications using the INH to control the microcontroller supply the application stays in low power mode when being powered the first time on BAT while TJA1021 applications start to power up.

With this change of the power-on behavior it is possible to distinguish between a power-on event on V_{BAT} and a local or remote wake-up event. In the Power-on mode the RXD output remains floating, while in the Standby mode the RXD output goes LOW signaling a wake-up event. During Power-on mode the TJA1021 will not detect and signal local and remote wake-up events.

TJA1021 drop-in compatibility impact to TJA1020 applications:

- Software impact: From the system point of view it has to be checked whether the different power-on behavior of the TJA1021 has an impact or not. After power-on the TJA1021 switches via INH an external voltage regulator on whereas the TJA1020 keeps it off.
- Hardware impact: If the INH output is used to control the microcontroller supply, then no hardware change is required. Otherwise the INH output state of the TJA1021 should be read by the microcontroller. See Section 4.1.7.3 for further details. Basically it should be considered to use the TJA1027 instead, if INH is not used to control the supply.

3.2.5 TxD dominant time-out

The TxD dominant time-out of the TJA1021 has been lengthened (see parameter $t_{to(dom)TXD}$ [3]). It supports LIN master transmission down to 1 kBd and K-Line master transmission. Thus the supported bit rate range has extended.

TJA1021 drop-in compatibility impact to TJA1020 applications:

- No impact to software.
- No impact to hardware.

3.2.6 Start-up time of the Normal mode

After the Normal mode of the TJA1021 is entered the transmitter block and the receiver block require a short initialization time $t_{init(norm)}$ [3] before they are enabled. This initialization time prevents spikes on LIN and RXD during the mode transition to Normal. This means once the Normal mode is entered (SLP_N = HIGH for $t > t_{gotonorm}$ [3]) the transmitter and the receiver remain disabled until the initialization time $t_{init(norm)}$ [3] has passed.

TJA1021 drop-in compatibility impact to TJA1020 applications:

- Software impact: The LIN transmitter of the TJA1020 needs also a short initialization time (max 11.5 µs). Nevertheless, the time period from putting SLP_N to HIGH until the start of transmission (and reception) has to be checked. As a rule of thumb this time period should be longer than 30 µs (maximum of $t_{gotonorm} + t_{init(norm)}$). Otherwise the 1st dominant pulse (one or more bits) is not transmitted.
- No impact to hardware.

3.2.7 Transmitter and receiver operating supply range

For the TJA1021 the operating supply range of the LIN transmitter and the LIN receiver is fully specified from 5.5 V to 18 V. The operating supply range of the TJA1020 is between 7.3 V and 27 V.

TJA1021 drop-in compatibility impact to TJA1020 applications:

- No impact to software.
- No impact to hardware.
- System impact: LIN transmission during Jump Start ($V_{BAT(jump)}$ = 27 V) might be disturbed, but in return LIN transmission during energizing of the starter motor ($V_{ECU(pulse\_4)}$ = 6 V) is supported.

3.2.8 Checklist for ECU upgrade from TJA1020 to TJA1021

For ECUs where currently the TJA1020 is applied the checklist in Table 4 provides all issues, which should be considered for an upgrade with the TJA1021.

Table 4. Checklist for ECU upgrade from TJA1020 to TJA1021

Subject	Item	Check
System	Operating supply range for LIN transmitter and receiver of TJA1021 differs from TJA1020. Check whether LIN communication during jump start is required.	
Hardware	The power-on behavior of the TJA1021 differs from the TJA1020 (see Section 3.2.4). It has to be checked whether the INH output is used to control the microcontroller supply.	
Software	The power-on behavior of the TJA1021 differs from the TJA1020 (see Section 3.2.4). It has to be checked whether the different power-on behavior has an impact to application and system environment.	
	After transition to Normal mode the TJA1021 needs additional start-up time (see Section 3.2.6). The time period from putting SLP_N to HIGH until start of transmission (and reception) should be longer than 30 µs	

3.3 TJA1020 – TJA1027 and TJA1029

Table 5 lists the differences of the TJA1020 to the TJA1027 and the TJA1029. In the following chapters the details are described.

Table 5. Overview of functional improvements and differences compared to the TJA1020

No.	Functional improvement TJA1027 / TJA1029	Description in …
1	No local wake-up input pin (NWAKE)	Section 3.3.1
2	No microcontroller supply control output pin (INH)	Section 3.3.2
3	LIN 2.x / SAE J2602 / ISO 17987 Physical Layer	Section 3.3.3
4	ESD robustness	Section 3.3.4
5	Normal Slope mode only (no Low Slope mode provided)	Section 3.3.5
6	No TxD dominant time-out (TJA1027 only)	Section 3.3.6
7	Start-up time entering Normal mode	Section 3.3.7
8	Transmitter and Receiver Operation Range	Section 3.3.8

3.3.1 No local wake-up input pin (NWAKE)

The TJA1020 has a local wake-up input (NWAKE) at pin 3. This function is not available at the TJA1027 and TJA1029. Pin 3 of the TJA1027 and TJA1029 is a real 'not connected' pin, i.e. without bond wire and lead frame connection to the transceiver die.

TJA1027 and TJA1029 drop-in compatibility impact to TJA1020 applications:

- No impact to software.
- Hardware impact: If no local wake-up input is needed, then no hardware change is necessary. Otherwise the TJA1021 should be used.

3.3.2 No microcontroller supply control output pin (INH)

The TJA1020 has a microcontroller supply control output (INH) at pin 8. This function is not available for the TJA1027 and TJA1029. Pin 8 of the TJA1027 and TJA1029 is a real 'not connected' pin, i.e. without bond wire and lead frame connection to the transceiver die.

TJA1027 and TJA1029 drop-in compatibility impact to TJA1020 applications:

- No impact to software.
- Hardware impact: If no microcontroller supply control output is needed, then no hardware change is necessary. Otherwise the TJA1021 should be used.

3.3.3 LIN 2.x / SAE J2602 / ISO 17987 physical layer

The physical layer of the TJA1027 [4] and TJA1029 [22] is compliant to LIN 2.0 [8], LIN 2.1 [7], LIN 2.2A [6], SAE J2602-1 [10] and ISO 17987-4 [26]. Hence, compared to the TJA1020 [1] the TJA1027 and the TJA1029 provides improved transmission reliability.

TJA1027 and TJA1029 drop-in compatibility impact to TJA1020 applications:

- No impact to software.
- No impact to hardware (Note: The LIN driver is specified for the supply range from 5.0 V to 18 V).

3.3.4 ESD robustness

The robustness of the TJA1027 and TJA1029 against ESD has been increased compared to the TJA1020. The TJA1027 and TJA1029 withstands ESD voltages up to ±8 kV according to JESD22-A114-B (100 pF / 1.5 kΩ) and up to ±12 kV [18] [23] according to IEC 61000-4-2 [21] (150 pF / 330 Ω). Hence, it can be considered to omit external ESD protection devices.

TJA1027 and TJA1029 drop-in compatibility impact to TJA1020 applications:

- No impact to software.
- No impact to hardware.

3.3.5 Normal Slope mode only

TJA1027 and TJA1029 provide one transmission mode only. Thus the Low Slope mode control function from the TJA1020 is not implemented into TJA1027 and TJA1029. This has the advantage that the mode pin SLP_N might be connected to the microcontroller supply directly, if no dedicated low power mode control is required. For the TJA1020 it is recommended to connect the SLP_N to a microcontroller port pin in order to enter a defined transmission mode (Normal Slope or Low Slope).

Regardless whether a TJA1020 software driver was used to enter the Normal Slope mode or Low Slope mode, such a software driver, when applied to TJA1027 or TJA1029, would enter the Normal mode of the TJA1027 respectively TJA1029.

TJA1027 and TJA1029 drop-in compatibility impact to TJA1020 applications:

- No impact to software.
- No impact to hardware.

3.3.6 No TxD dominant time-out (TJA1027 only)

The TJA1027 has no TxD dominant time-out function (disables LIN transmitter if TXD dominant time exceeds time-out), but it has an initial TXD dominant check function. The TXD input level is checked after a transition to Normal mode. If TXD is LOW, the transmit path will remain disabled and will only be enabled when TXD goes HIGH. This check prevents the bus line from being driven to a permanent dominant state (blocking all network communications) if pin TXD is forced permanently LOW by a hardware and/or software application failure.

TJA1027 drop-in compatibility impact to TJA1020 applications:

- No impact to software.
- No impact to hardware.

3.3.7 Start-up time of the Normal mode

After the Normal mode of TJA1027 or TJA1029 is entered the transmitter block and the receiver block require a short initialization time $t_{init(norm)}$ [4][22] before they are enabled. This initialization time prevents spikes on LIN and RXD during the mode transition to Normal. This means once the Normal mode is entered (SLP_N = HIGH for $t > t_{gotonorm}$ [4]) the transmitter and receiver path remains disabled until the initialization time $t_{init(norm)}$ [4] has passed.

TJA1027 and TJA1029 drop-in compatibility impact to TJA1020 applications:

- Software impact: The LIN transmitter of the TJA1020 needs also a short initialization time (max 11.5 µs). Nevertheless, the time period from putting SLP_N to HIGH until the start of transmission (and reception) has to be checked. As a rule of thumb this time period should be longer than 30 µs (maximum of $t_{gotonorm} + t_{init(norm)}$). Otherwise the 1st dominant pulse (one or more bits) is not transmitted.
- No impact to hardware.

3.3.8 Transmitter and receiver operating supply range

For TJA1027 and TJA1029 the operating supply range of the LIN transmitter and the LIN receiver is fully specified from 5.0 V to 18 V. For higher supply voltages with up to 27 V (e.g. during an automotive jump start), the total LIN network pull-up resistance should be higher than 680 Ω and the total LIN network capacitance should be less than 6.8 nF to ensure reliable LIN data transfer. The operating supply range of the TJA1020 is between 7.3 V and 27 V.

TJA1027 and TJA1029 drop-in compatibility impact to TJA1020 applications:

- No impact to software.
- No hardware impact.
- System impact: LIN transmission during Jump Start ($V_{BAT(jump)}$ = 27 V) might be disturbed at big networks, but in return LIN transmission during energizing of the starter motor ($V_{ECU(pulse\_4)}$ = 5.5 V) is supported.

3.3.9 Checklist for ECU upgrade from TJA1020 to TJA1027 and TJA1029

For ECUs where currently the TJA1020 is applied the checklist in Table 6 provides all issues, which should be considered for an upgrade with TJA1027 and TJA1029.

Table 6. Checklist for ECU upgrade from TJA1020 to TJA1027 and TJA1029

Subject	Item	Check
System	Operating supply range for LIN transmitter and receiver of TJA1027 differs from TJA1020. Check whether LIN communication during jump start is required. If yes, check whether the total LIN network pull-up is ≥680 Ω and the total LIN network capacitance ≤6.8 nF.	
Hardware	It has to be checked whether INH output and WAKE input function are needed.	
Software	After transition to Normal mode the TJA1027 needs additional start-up time (see Section 3.3.7). The time period from putting SLP_N to HIGH until start of transmission (and reception) should be longer than 30 µs	

3.4 TJA1021 changeover guidance

In case that not all features of the TJA1021 are used, a changeover from existing applications with TJA1021 (or LIN transceiver from competition) towards the newer products TJA1027 or TJA1029 can help to optimize the system costs. If in the application neither pin NWAKE nor pin INH of the TJA1021 are used, the TJA1029 should be applied as replacement. Furthermore, if a TXD dominant time-out function is not required, the TJA1027 is a good choice.

In addition for applications with multiple LIN channels (typically LIN master applications) the system costs and the board space can be further optimized with the dual LIN transceiver TJA1022 or the quad LIN transceiver TJA1024.

In Fig 10 the TJA1021 changeover options are illustrated.

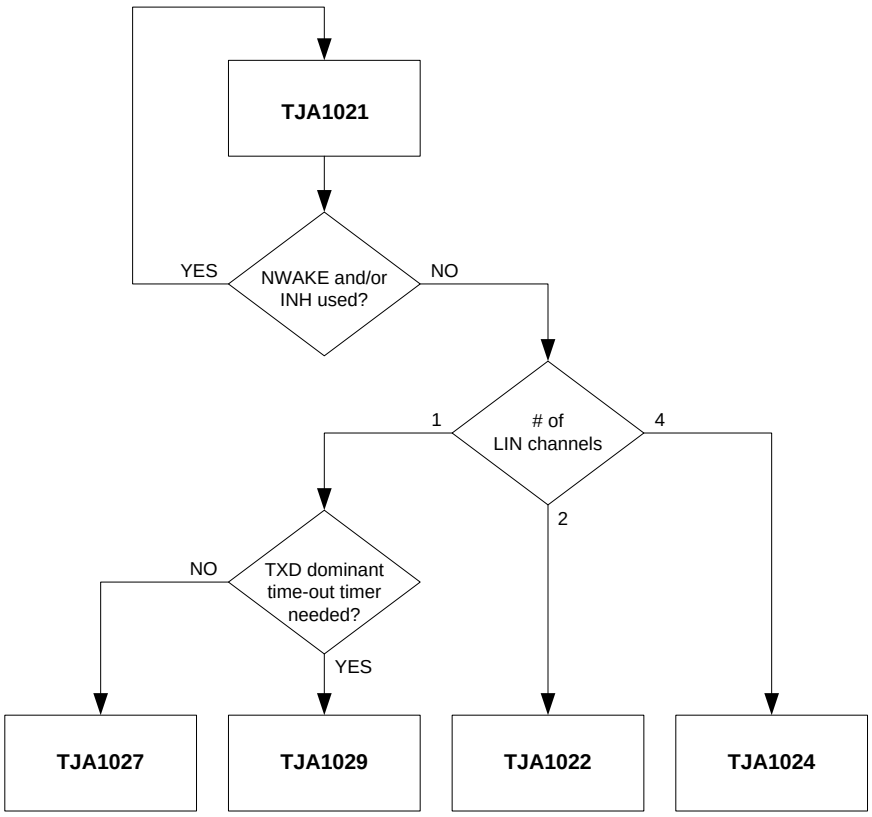


Fig 10. TJA1021 changeover guidance

3.5 TJA1021 – TJA1027 and TJA1029

Table 7 lists the differences of the TJA1021 to the TJA1027 and the TJA1029. In the following chapters the details are described.

Table 7. Overview of functional improvements and differences compared to the TJA1021

No.	Functional improvement TJA1027 / TJA1029	Description in …
1	No local wake-up input pin (WAKE_N)	Section 3.5.1
2	No microcontroller supply control output pin (INH)	Section 3.5.2
3	ESD robustness	Section 3.5.3
4	Initial state after BAT power-on is Sleep mode	Section 3.5.4
5	No TxD dominant time-out (TJA1027 only)	Section 3.5.5

3.5.1 No local wake-up input pin (WAKE_N)

The TJA1021 has a local wake-up input (WAKE_N) at pin 3. This function is not available at the TJA1027 and TJA1029. Pin 3 of the TJA1027 and TJA1029 is a real ‘not connected’ pin, i.e. without bond wire and lead frame connection to the transceiver die.

TJA1027 and TJA1029 drop-in compatibility impact to TJA1021 applications:

- No impact to software.
- Hardware impact: If no local wake-up input is needed, then no hardware change is necessary. Otherwise keep using the TJA1021.

3.5.2 No microcontroller supply control output pin (INH)

The TJA1021 has a microcontroller supply control output (INH) at pin 8. This function is not available at the TJA1027 and TJA1029. Pin 8 of the TJA1027 and TJA1029 is a real 'not connected' pin, i.e. without bond wire and lead frame connection to the transceiver die.

TJA1027 and TJA1029 drop-in compatibility impact to TJA1021 applications:

- No impact to software.
- Hardware impact: If no microcontroller supply control output is needed, then no hardware change is necessary. Otherwise keep using the TJA1021.

3.5.3 ESD robustness

The robustness of the TJA1027 and TJA1029 against ESD has been further improved compared to the TJA1021. The TJA1027 and TJA1029 withstands ESD voltages up to ±8 kV according to JESD22-A114-B (100 pF / 1.5 kΩ) and up to ±12 kV [18] [23] according to IEC 61000-4-2 [21] (150 pF / 330 Ω).

TJA1027 and TJA1029 drop-in compatibility impact to TJA1021 applications:

- No impact to software.
- No impact to hardware.

3.5.4 Power-on behavior

The 1st state after power-on (supply voltage on V_{BAT} is switched on) of the TJA1021 is the Power-on mode [3], where the INH switch is enabled. Depending on the application software the next TJA1021 mode will be set to either Normal mode or Sleep mode. In the TJA1021 Power-on mode the RXD output remains floating, while in the Standby mode the RXD output goes LOW signaling a wake-up event. During Power-on mode the TJA1021 will not detect and signal local and remote wake-up events.

TJA1027 and TJA1029 have neither a Power-on mode nor an INH switch output. After power-on TJA1027 and TJA1029 switch to Sleep mode [4][22].

TJA1027 and TJA1029 drop-in compatibility impact to TJA1021 applications:

- Software impact: From the system point of view it has to be checked whether the different power-on behavior of TJA1027 and TJA1029 has an impact or not. After power-on the application software might read the state of the TJA1021 INH switch output. As TJA1027 and TJA1029 has no INH such read trial of the application software could cause incorrect application behavior.
- No impact to hardware.

3.5.5 No TxD dominant time-out (TJA1027 only)

The TJA1027 has no TxD dominant time-out function (disables LIN transmitter if TXD dominant time exceeds time-out), but it has an initial TXD dominant check function. The TXD input level is checked after a transition to Normal mode. If TXD is LOW, the transmit path will remain disabled and will only be enabled when TXD goes HIGH. This check prevents the bus line from being driven to a permanent dominant state (blocking all

network communications) if pin TXD is forced permanently LOW by a hardware and/or software application failure.

TJA1027 drop-in compatibility impact to TJA1021 applications:

- No impact to software.
- No impact to hardware.

3.5.6 Checklist for ECU upgrade from TJA1021 to TJA1027 and TJA1029

For ECUs where currently the TJA1021 is applied the checklist in Table 8 provides all issues, which should be considered for an upgrade with TJA1027 and TJA1029.

Table 8. Checklist for ECU upgrade from TJA1021 to TJA1027 and TJA1029

Subject	Item	Check
Hardware	It has to be checked whether INH output and WAKE input function are needed.	
Software	The power-on behavior of TJA1027 and TJA1029 differs from the TJA1021 (see Section 3.5.4). It has to be checked whether the different power-on behavior has an impact to application and system environment.	

4. Application information

4.1 Detailed pin description

4.1.1 V_{BAT}

Fig 11 shows the recommended circuitry for the supply pin V_{BAT}. The reverse polarity protection diode is required, because the TJA102x have no internal reverse polarity protection circuits. Moreover, some buffer capacitors should be applied to the V_{BAT} pin to suppress spikes, noise and supply voltage drops, such as cranking pulse 4 [15].

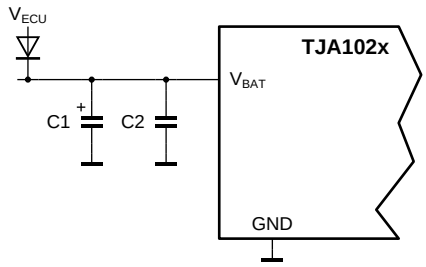


Fig 11. Typical V_{BAT} circuitry

The buffer capacitor C1 in Fig 11 depends on the maximum supply current of the LIN ECU, the minimum cranking pulse voltage and the maximum cranking pulse time. The buffer capacitor C2 should be placed close to the V_{BAT} pin. A typical value for C2 is 68nF.

4.1.2 LIN / LIN1 / LIN2 / LIN3 / LIN4

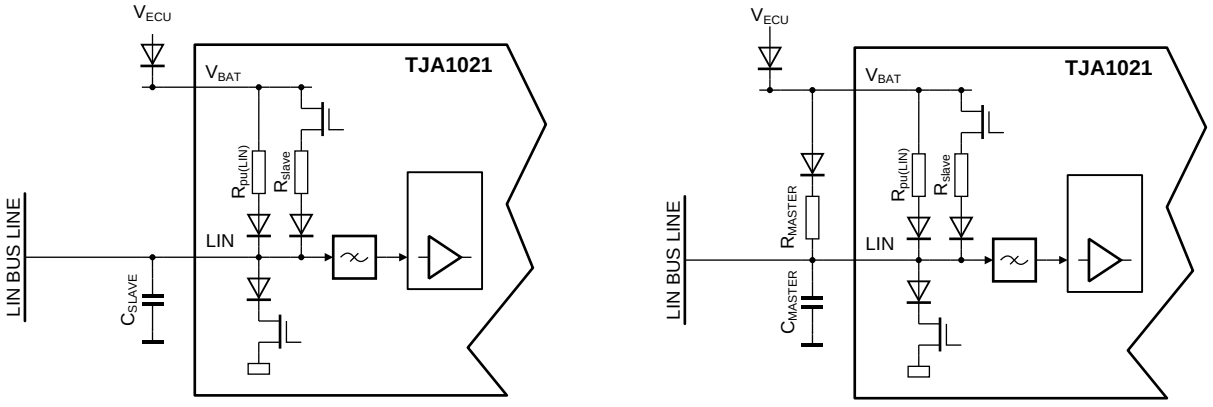
The pin LIN is used to transmit and receive data on the LIN bus line. A low side switch with controlled wave shaping is used for bit transmission while an integrated receive comparator (receiver) converts the LIN bus voltage back to a binary signal. The threshold of the receiver is battery related and has a hysteresis.

4.1.2.1 TJA1021

The LIN pin of the TJA1021 has a high-resistance pull-up of $R_{pu(LIN)}$ [3] and a slave termination resistor of R_{slave} [3] in parallel to pin V_{BAT}. The slave termination resistor and the high-resistance pull-up as well as the low side switch are implemented with a reverse current diode. Thus for a LIN slave application no external components are required. Nevertheless, improvement of EME and EMI can be achieved by applying a capacitive load C_{SLAVE} [6] at the LIN bus line as shown in Fig 12a.

The high-resistance pull-up of $R_{pu(LIN)}$ is used as an additional weak pull-up, because the slave termination resistor R_{slave} is switched off in sleep mode. Thus a transition into the sleep mode minimizes the current consumption in case of LIN short-circuit to ground

For a LIN master application a reverse current diode in series with the LIN master resistor R_{MASTER} [6] is connected between LIN and V_{BAT}. In addition typically a capacitance load C_{MASTER} [6] between LIN and ground is added. Fig 12b shows a typical LIN master termination for the TJA1021.



a. Typical LIN slave termination

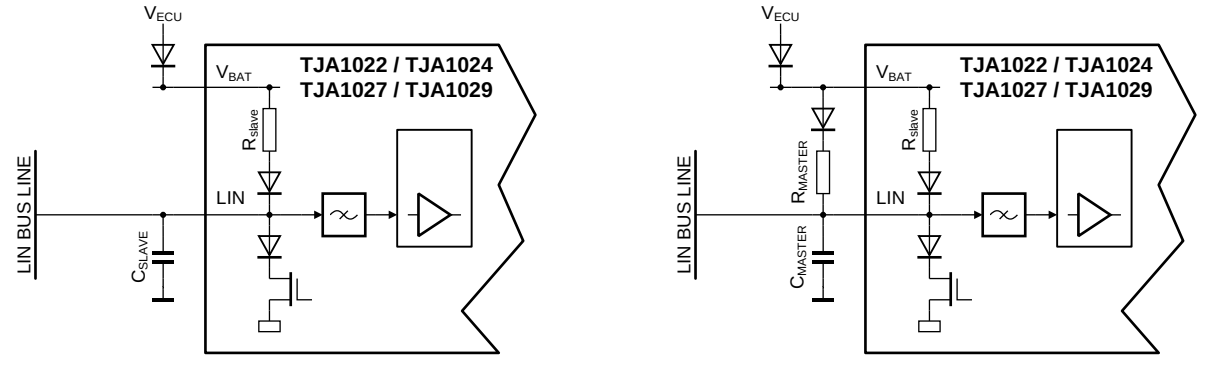
b. Typical LIN master termination

Fig 12. Typical LIN termination with TJA1021

4.1.2.2 TJA1022, TJA1024, TJA1027 and TJA1029

The LIN pins of the TJA1022 and TJA1024 and the LIN pin of TJA1027 and TJA1029 are equal. A LIN slave pull-up R_{slave} connected to V_{BAT} in series with a reverse current protection diode is integrated. The low side driver of the LIN transmitter is also implemented in series with a reverse current protection diode.

In Fig 13a a typical LIN termination for a LIN slave application with the TJA1022, TJA1024, TJA1027 and TJA1029 is shown. Only a LIN slave capacitance load C_{SLAVE} [6] is typically added to improve EME and EMI.



a. Typical LIN slave termination

b. Typical LIN master termination

Fig 13. Typical LIN termination with TJA1022, TJA1024, TJA1027 and TJA1029

For a LIN master termination with TJA1022, TJA1024, TJA1027 and TJA1029 a LIN master pull-up R_{MASTER} [6] in series with a reverse current protection diode is required. The master pull-up and the diode are connected between V_{BAT} and LIN. Typically a LIN master capacitance load C_{MASTER} [6] between LIN and ground is added.

4.1.3 SLP_N / SLP1_N / SLP2_N / SLP3_N / SLP4_N

The sleep control pin SLP_N provides an internal pull-down resistor $R_{PD(SLP\_N)}$ to support a defined input level in case of open circuit failures. A LOW-level results in Sleep mode

and reduces the power dissipation to a minimum. The range of the input threshold is chosen to support 5 V as well as 3.0 V/3.3 V supplied devices. A typical SLP_N pin application is shown in Fig 14.

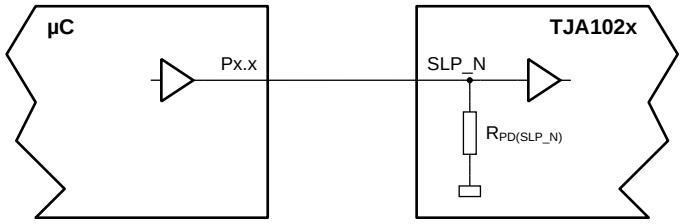


Fig 14. Typical SLP_N pin application

The minimum drive capability of the microcontroller port pin for the SLP_N pin should be 100 µA.

If the low power modes of the transceiver shall be used, it is recommended to connect SLP_N to a microcontroller port pin. Otherwise if the low power modes are not applied, SLP_N can be connected directly to a VCC supply source.

4.1.4 TXD / TXD1 / TXD2 / TXD3 / TXD4

The TXD pin of the TJA1021 is a bi-directional pin whereas the TXD pin of TJA1022, TJA1027 and TJA1029 is an input pin only. The input threshold of the TXD pin supports 3.0 V, 3.3 V and 5.0 V supplied devices.

All TXD pins provide an internal pull-down resistor $R_{PD(TXD)}$ [3][4][5][22] to support a defined input level in case of open circuit failures.

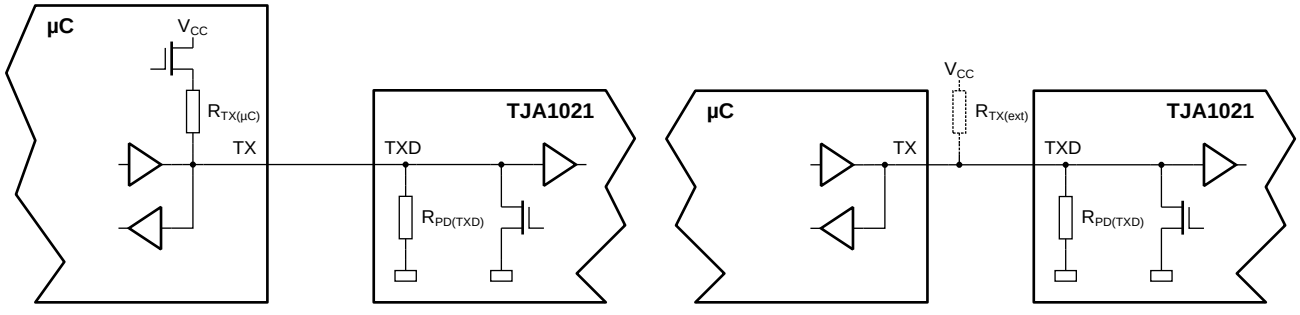
Note: After the transceiver is switched to Normal mode the LOW-level on TXD results not in a dominant LIN output. In order to enable the LIN transmit path the TXD input must be one-time HIGH. This initial TXD dominant check prevents the bus line from being driven to a permanent dominant state (blocking all network communications) if pin TXD is forced permanently LOW by a hardware and/or software application failure.

4.1.4.1 TJA1021

The TXD pin of the TJA1021 is a bi-directional pin. In Normal mode it is used as transmit data input whereas in Standby mode the wake-up source is signaled. Here an active low output of the TXD pin indicates a local wake-up event on the WAKE_N pin. If a local wake-up source at the WAKE_N pin is used, a pull-up behavior at pin TXD is required. This pull-up can be achieved in two ways:

1. The microcontroller port pin provides an integrated pull-up $R_{TX(uC)}$ (see Fig 15a).
2. An external pull-up resistor $R_{TX(ext)}$ towards the local V_{CC} is connected (see Fig 15b).

In case no local wake-up source is present (WAKE_N is unused), no external pull-up resistor is required. Then TXD will never be pulled to a strong LOW-level by the TJA1021.



c. for µC with internal programmable pull-up

d. for µC without internal pull-up

Fig 15. Typical TXD pin application of TJA1021

If the local wake-up feature (WAKE_N) of the TJA1021 is used, the required pull-up strength of the external pull-up R_{TX} is defined by

1. the drive capability of the integrated wake-up source transistor pulling TXD to low in case of a local wake-up event and
2. the integrated TXD pull-down resistor $R_{PD(TXD)}$ of the TJA1021.

The required pull-up current of the microcontroller port pin as well as the external resistor R_{TX} should be in the range from 100 µA to 1.5 mA.

Remark: For LIN the signal symmetry of the falling and rising transition on TXD has an impact on the overall system tolerances. Hence, it is recommended to keep the RC-load time constant on the TXD input as short as possible. A recommended value for the external pull-up resistor R_{TX} is 4.7 kΩ.

4.1.4.2 TJA1022, TJA1024, TJA1027 and TJA1029

The TXD pins of TJA1022 and TJA1024 as well as the TXD pin of TJA1027 and TJA1029 are equal. Fig 16 illustrates the typical TXD pin application.

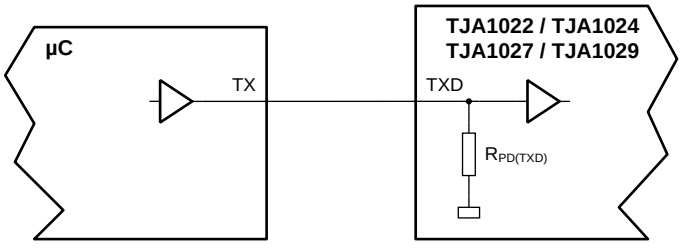


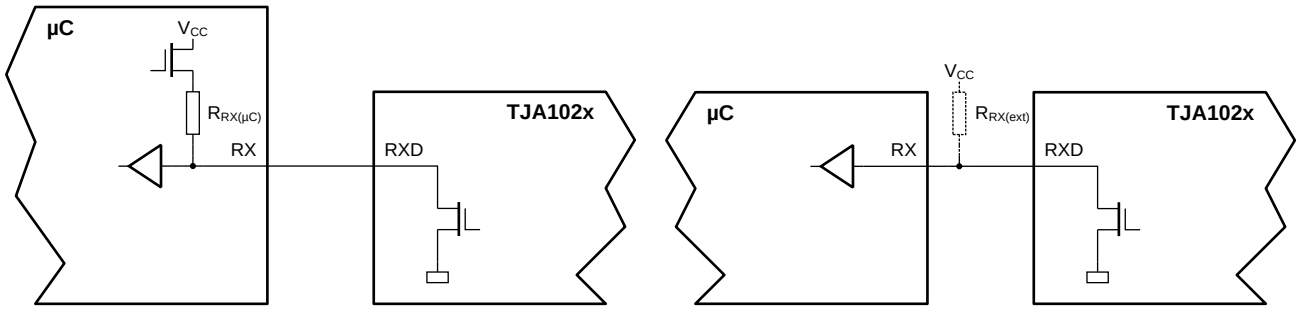
Fig 16. Typical TXD pin application of TJA1022, TJA1024, TJA1027 and TJA1029

The required pull-up current of the microcontroller port pin should be stronger than 200µA.

4.1.5 RXD / RXD1 / RXD2 / RXD3 / RXD4

The receive data output RXD provides an open drain output. The output HIGH-level can be adapted with a pull-up resistor to the microcontroller supply voltage. Thus 3.0 V/3.3 V microcontroller derivatives without 5 V tolerant ports can be used. In case the microcontroller port pin does not provide an integrated pull-up, an external pull-up

resistor connected to the microcontroller supply voltage V_{CC} is required. In Fig 17 typical RXD applications are shown



a. for µC with internal programmable pull-up

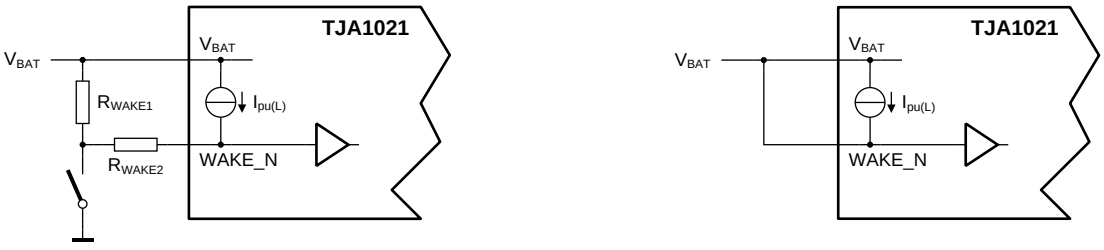
b. for µC without internal pull-up

Fig 17. Typical RXD pin application

Remark: For LIN the signal symmetry of the falling and rising transition on RXD has an impact on the overall system tolerances. Hence, it is recommended to keep the RC-load time constant on the RXD output as short as possible. A recommended value for the external pull-up resistor R_{RX} is 2.4 kΩ.

4.1.6 WAKE_N (TJA1021 only)

The local wake-up input WAKE_N is used to detect local wake-up events using a falling edge. This falling edge has to be followed by a continuous LOW-level of at least $t_{wake(dom)WAKE\_N}$ [3] in order to successfully pass the integrated EMI filter. The WAKE_N pin provides an internal weak pull-up current source $I_{pu(L)}$ [3] towards battery, which results in a HIGH-level in case of open circuit failures. It is recommended to connect an external pull-up resistor R_{WAKE1} to provide sufficient current for an external wake-up switch or transistor. In case the wake-up source (switch or transistor) at WAKE_N has a different ground path than the TJA1021, it is recommended to add a series resistor R_{WAKE2} between the WAKE_N pin and the wake-up source. If the ECU has lost its ground while the wake-up source is still connected to ground, the series resistor R_{WAKE2} protects the ECU against a reverse current supply through the internal protection diodes of WAKE_N. Fig 18a shows a typical WAKE_N pin application for local wake-up via external switch.



a. for local wake-up via external switch

b. for application without local wake-up

Fig 18. Typical WAKE_N pin application of TJA1021

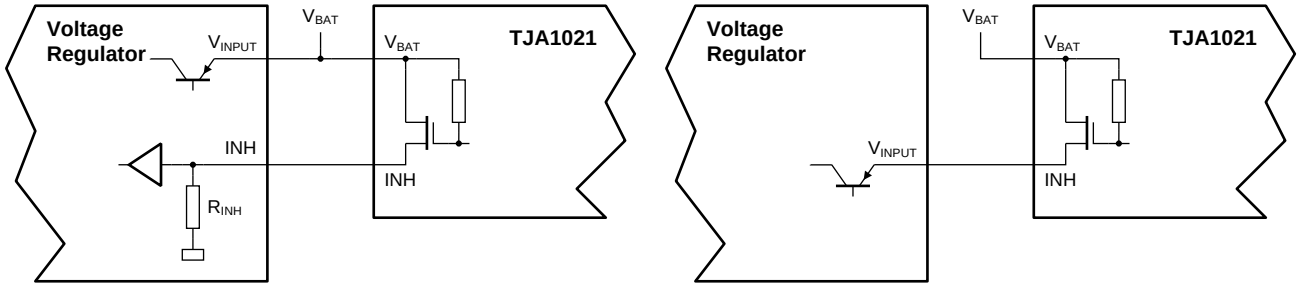
The pull-up resistor R_{WAKE1} depends only on the required current of the wake-up source (switch or transistor), whereas the series resistor R_{WAKE2} is mainly defined by the applications ground shift between the ECU and the external wake-up source.

A typical value for the series resistor R_{WAKE2} is 3 kΩ.

4.1.7 INH (TJA1021 only)

4.1.7.1 INH controlled voltage regulator

The output pin INH is a battery related open drain output to control an external voltage regulator. Therefore an external pull-down resistor R_{INH} connected to ground is necessary. This pull-down is typically integrated within the voltage regulator itself. A typical INH pin application is shown in Fig 19a.



a. for voltage regulators with inhibit input

b. for voltage regulators without inhibit input

Fig 19. Typical INH pin application of TJA1021

4.1.7.2 Direct Voltage Regulator Supply

The TJA1021 is able to supply a voltage regulator via the INH pin directly. Fig 19b shows the typical INH pin application of such a slave application.

Remark: Independent from the following calculation the current through the INH pin I_{INH} should not exceed 50 mA.

The maximum supply current through the INH pin $I_{INH,max}$ for the voltage regulator and the maximum voltage drop V_{DROP} can be calculated by the equations below:

Max. voltage regulator supply current through INH:

$$I_{INH,\max} = \sqrt{\frac{P_{\max} - P_{Q,\max} - P_{TX,\max}}{R_{sw(VBAT-INH),\max}}} \quad \text{with} \quad I_{O(INH),\max} \leq 50mA \quad \text{and}$$

$$P_{\max} = \frac{T_{vj,\max} - T_{amb,\max}}{R_{th(j-a)}}$$

Max. voltage drop at INH:

$$V_{DROP} = R_{sw(VBAT-INH),\max} \times I_{O(INH),\max}$$

with

$P_{Q,max}$	maximum quiescence power dissipation (Normal mode, bus recessive, $V_{INH} = V_{BAT}$), see Fig 20
$P_{TX,max}$	maximum transmitter power dissipation (Normal mode, transmission duty cycle = 50%, $V_{INH} = V_{BAT}$), see Fig 20
$R_{sw(VBAT-INH),max}$	maximum switch-on resistance between BAT and INH [3]

and

$T_{vj,max}$	maximum virtual junction temperature (K) [3]
$T_{amb,max}$	maximum ambient temperature (K)
$R_{th(j-a)}$	thermal resistance (K/W) [3]

The power dissipation depends on the supply voltage V_{BAT} and the bit rate. Fig 20 shows the quiescence power dissipation P_Q and the transmitter power dissipation P_{TX} of the TJA1021 as the function of the supply voltage V_{BAT}. A worst case duty cycle of 50% and a worst case LIN bus load (R_L=500 Ω, C_L=10 nF) are used for the transmitter power dissipation P_{TX} in Fig 20.

The thermal resistance $R_{th(j-a)}$ [3] is the ability of an IC package to conduct heat to its environment and is typically specified for free air conditions. Within real applications the use of large copper planes attached to pin GND can reduce the thermal resistance and therefore increase the maximum INH current $I_{INH,max}$.

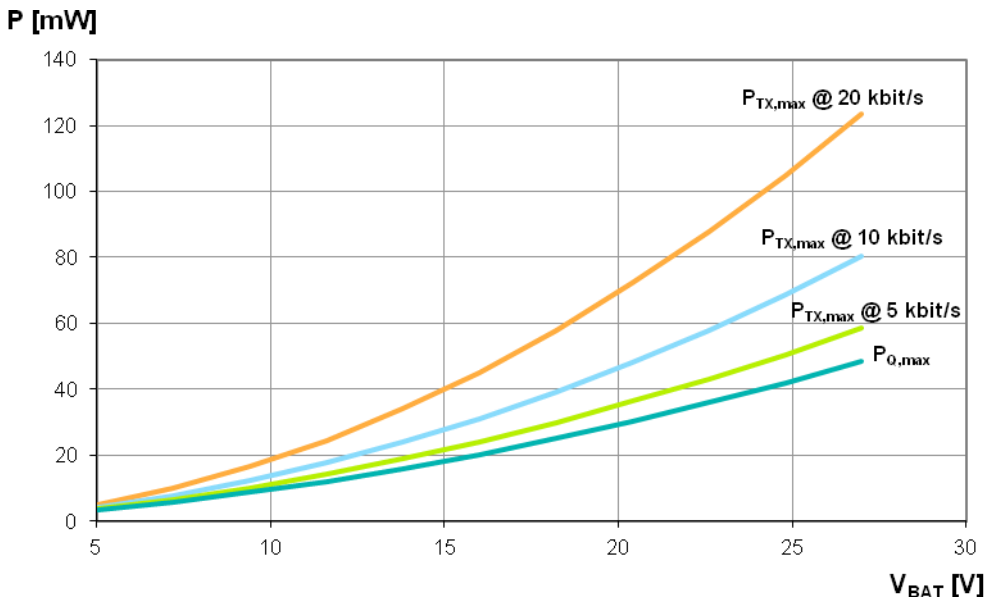


Fig 20. TJA1021 power dissipation in Normal mode

4.1.7.3 No voltage regulator control

In some applications (e.g. with permanently supplied microcontroller) the voltage regulator control via pin INH is not needed. In order to read the Power-on mode of the TJA1021 it is recommended to connect the INH with a microcontroller input port or to SLP_N pin.

Without reading the INH pin the software can miss a battery under-voltage event during Sleep mode. After a battery under-voltage event the TJA1021 switches to Power-on mode. In Power-on mode the RXD output stays floating, the INH output becomes HIGH and LIN bus traffic is ignored, because the battery power-on event is already regarded as wake-up event. As a result after a battery under-voltage event LIN bus wake-up events are detected from the software, if the INH output state is ignored. A HIGH-level on INH output and a LOW-level on SLP_N output signals a battery under-voltage event, which has forced the TJA1021 into Power-on mode.

Microcontroller reads INH output state

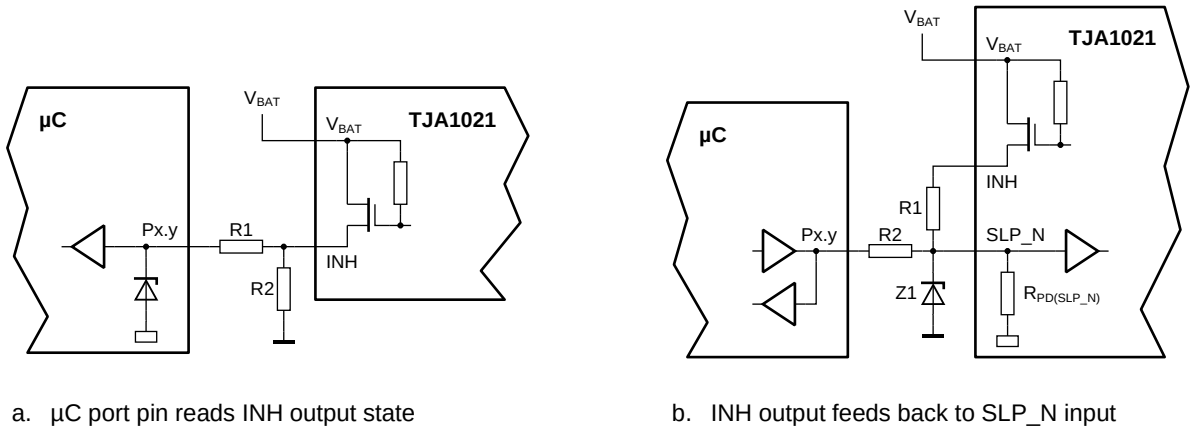
Fig 21a illustrates a typical connection between microcontroller port pin and INH output of the TJA1021. In this example the series resistor R1 limits the pull-up current from the INH output into the microcontroller port pin. The pull-down resistor R2 provides a defined LOW-level when the INH output is floating.

The series resistor R1 can be calculated with following equation:

$$R1 \geq \frac{V_{BAT,\max} - V_{CC(\mu C)}}{I_{Pxy(IN),\max}}$$

with

$I_{Pxy(IN),max}$	maximum µC port pin input current through internal ESD diode
$V_{BAT,max}$	maximum battery voltage
$V_{CC(µC)}$	µC supply voltage



a. µC port pin reads INH output state

b. INH output feeds back to SLP_N input

Fig 21. Typical INH pin application of the TJA1021 if pin is not used for voltage regulator control

INH output feeds back to SLP_N input

In Fig 21b the INH output of the TJA1021 is connected to pin SLP_N. As precondition for this circuitry the microcontroller port pin must provide a high-impedance state. During Sleep mode of TJA1021 the microcontroller port pin is put to high-impedance state. When the TJA1021 has switched to Power-on mode, then the INH output drives the SLP_N input to HIGH-level and forces the TJA1021 to the Normal mode. Thus the microcontroller software can read on SLP_N pin the Power-on event and on RXD the LIN bus messages.

The resistor R1 limits the pull-up current from the INH output. The resistor R2 limits cross currents between microcontroller port pin and Zener diode. The Zener diode Z1 limits the voltage on the microcontroller port pin and SLP_N pin of TJA1021 and shall have a maximum Zener voltage, which is smaller than the maximum limiting values of the pins.

Depending on the microcontroller port pin clamping voltage the Zener diode Z1 and the resistor R2 might be obsolete. In order to omit the Z1 and R2 the maximum microcontroller port pin clamping voltage must be smaller than the maximum limiting value for SLP_N pin. Further the microcontroller pin must be capable to sink the pull-up of R1.

The series resistor R1 can be calculated with following equation:

$$R1 \geq \frac{V_{BAT,\max} - V_{CC(\mu C)}}{I_{Pxy(IN),\max}}$$

with

$I_{Pxy(IN),max}$	maximum µC port pin input current through internal ESD diode
$V_{BAT,max}$	maximum battery voltage
$V_{CC(µC)}$	µC supply voltage

4.1.7.4 Pull-up current switch

The INH pin can be used to switch off a pull-up current in Sleep mode. Current consumption of application functions, not required in Sleep mode, can be saved. For instance if the function for a switch array is not needed in Sleep mode, the INH pin can be used as switch for the pull-up current as illustrated in Fig 22.

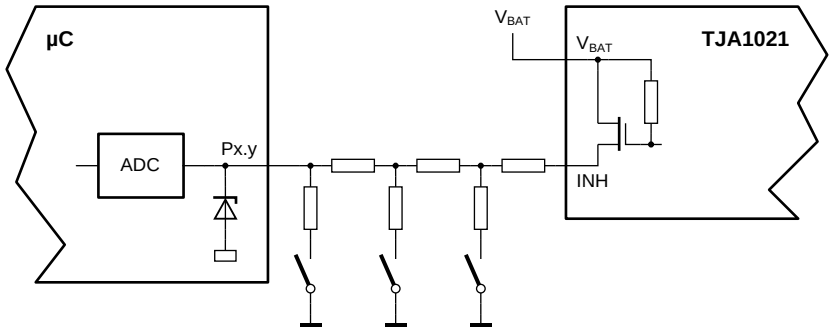


Fig 22. INH pin as pull-up current switch for switch array

The current for a battery monitor function can also be controlled with the INH pin. During Sleep mode the battery monitoring function is often not needed. As shown in Fig 23 the supply current for the voltage divider of the battery monitor can be controlled with the INH pin.

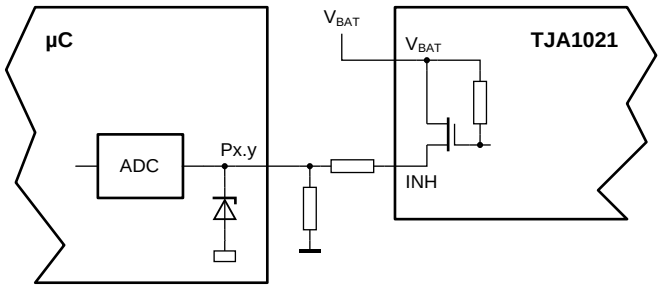


Fig 23. INH pin for battery monitoring function

The calculation of the maximum supply current through the INH pin $I_{INH,max}$ and the maximum voltage drop V_{DROP} of the INH pin is described in Section 4.1.7.2.

4.1.7.5 LIN master switch

Master termination towards INH

For fail-safe reasons the TJA1021 supports an advanced master application solution using the INH pin to drive the master termination resistor R_{MASTER} [6]. As shown in Fig 24 the master termination resistor in series with a reverse current diode is connected to the INH pin instead of the BAT pin. The advantage of this application solution is the ability to switch off the master termination by a transition into the Sleep mode, thus solving the above mentioned short-circuit condition of LIN and ground.

Whenever the application microcontroller detects a permanent dominant level on the LIN bus line caused by a ground short-circuit, the microcontroller is able to minimize the power dissipation by selecting the Sleep mode. Hence, a transition into the Sleep mode switches off the external voltage regulator, the master termination R_{MASTER} [6] as well as the internal slave termination R_{slave} [3]. Only the internal high-resistance pull-up $R_{pu(LIN)}$ [3] and the internal current consumption of the TJA1021 determine the remaining current consumption of a LIN node in such a failure case.

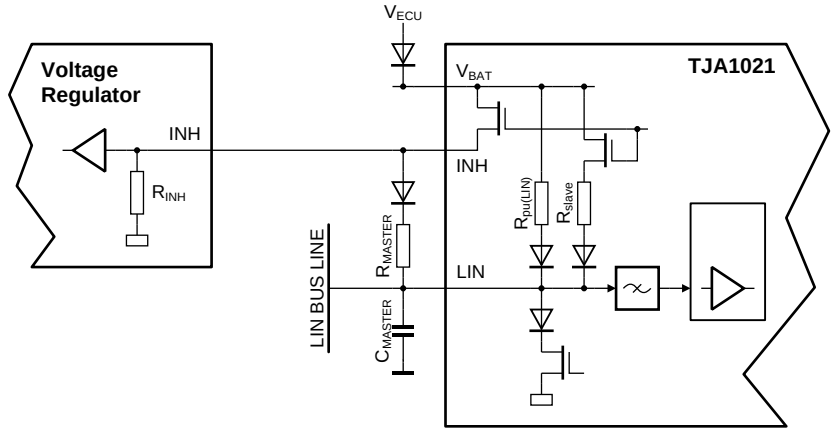


Fig 24. Advanced master termination via the INH pin

Master termination split between INH and V_{BAT}

Since the advanced master termination above provides a fail-safe system behavior but high LIN bus impedance in Sleep mode, a combination of the termination concepts above and Section 4.1.2.1 can be an option, if a higher short-circuit current at the LIN bus can be tolerated (see Fig 25).

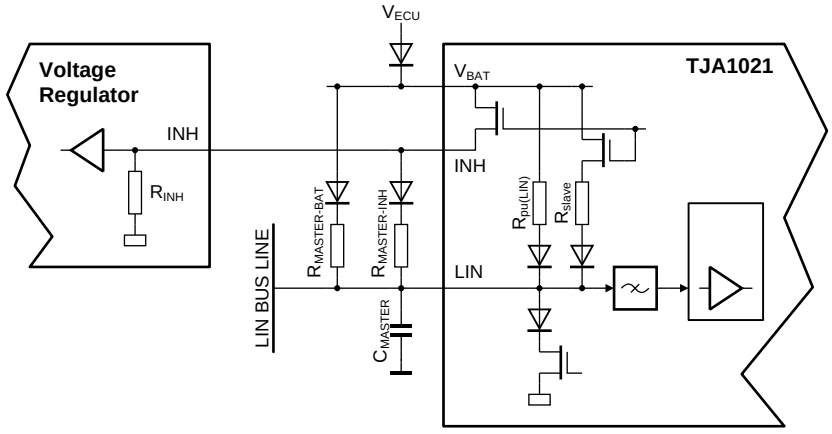


Fig 25. Trimmed master termination

The resistors $R_{MASTER-BAT}$ and $R_{MASTER-INH}$ in parallel determine the master termination while the TJA1021 is in the modes: Power-on, Standby and Normal. In Sleep mode the master termination is determined by $R_{MASTER-BAT}$. Therefore the maximum LIN bus short-circuit current $I_{SC,max}$ can be trimmed by $R_{MASTER-BAT}$:

$$R_{MASTER-BAT} = \frac{V_{BAT,max}}{I_{SC,max}}$$

$$R_{MASTER-INH} = \frac{R_{MASTER-BAT} \times R_{MASTER}}{R_{MASTER-BAT} - R_{MASTER}} \quad \text{with} \quad R_{MASTER} = 1k\Omega$$

4.2 Compatibility to 3V and 5V microcontroller devices

The TJA102x are designed to support the increasing demand for lower supply voltages than 5 V within automotive applications. They provide reduced input thresholds at the input pins TXD and SLP_N and open drains at the output pins RXD and TXD (TJA1021 only). So the LIN transceivers are compatible to 3.0 V and 3.3 V supplied microcontroller as well as to 5 V supplied devices. Between TJA102x and host microcontroller no 5 V tolerant behavior for the interface pins is required. Furthermore no extra VCC supply for the transceiver itself is needed.

To achieve a suitable HIGH-level at RXD and TXD (TJA1021 only) an external pull-up resistor might be required in case such a pull-up resistor is not part of the microcontroller port pins.

Further details about the TJA102x interface to microcontroller devices are described in Section 4.1.3, 4.1.4 and 4.1.5.

4.3 EMC aspects

4.3.1 EME – network design hints

The LIN physical layer is a single-wire, wired AND bus with a battery related recessive level. Here, no compensation effect of the electromagnetic field is present as known from dual-wire concepts making use of differential signals (e.g. High-Speed CAN). Thus a smooth output wave shaping becomes more important. The ElectroMagnetic Emission EME depends mainly on the falling and rising slope of the LIN bus waveform. The smoother these slopes are the more EME reduction can be achieved.

The LIN slope of the TJA102x can be adjusted by modifying the capacitive load (C_{MASTER} [6] or C_{SLAVE} [6]) on the LIN bus. The slope decreases with increasing capacitive load. Therefore increasing the total network capacitance ($C_{BUS} = C_{MASTER} + n * C_{SLAVE} + C_{LINE}$ [6]) can further reduce the EME. On the other hand for high bit rates close to 20 kBd the LIN bus slope times have also impacts to system tolerances such as bitrate deviation and ground shift. Thus the time constant τ of the overall system shall not exceed its specified maximum τ_{max} [6].

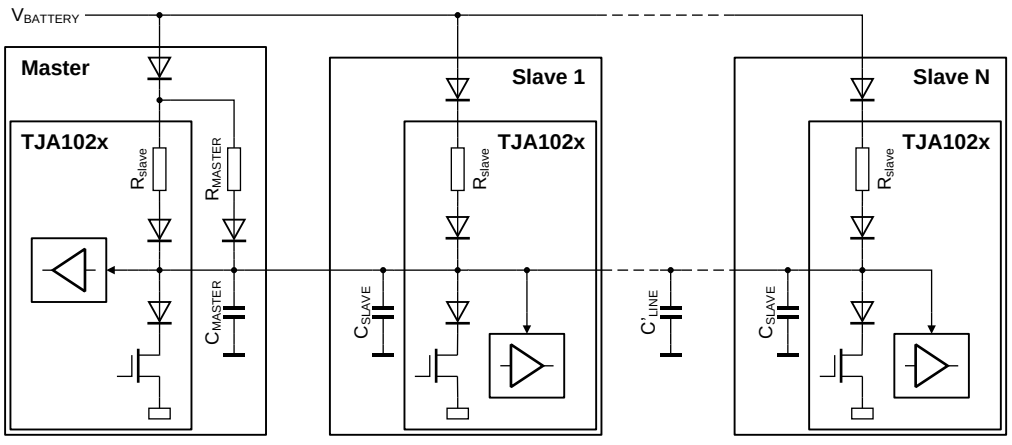


Fig 26. LIN network load

In a LIN network the master resistor R_{MASTER} [6] and the slave resistors R_{SLAVE} [6] are accurately defined by the LIN specification [6]. There no variation is allowed. Also the specified slave capacitance C_{SLAVE} provides almost no room for network optimizations. Only the master capacitor C_{MASTER} can be used to tune the LIN bus signal in either way.

For EME as well as for EMI a big network capacitance is of advantage. Hence, the maximum master capacitance $C_{MASTER,max}$ is of interest. $C_{MASTER,max}$ can be calculated with following equations:

$$C_{MASTER,\max} = \frac{\tau_{\max}}{R_{BUS,\max}} - N \cdot C_{SLAVE} - LEN_{BUS} \cdot C'_{LINE}$$ with

$$R_{BUS,\max} = R_{MASTER,\max} \parallel \frac{R_{slave,\max}}{N+1}$$

with

τ_{max}	maximum time constant of overall LIN network [6]
$R_{MASTER,max}$	maximum LIN master termination resistor [6]
$R_{slave,max}$	maximum LIN slave termination resistor [3][4][5]
C_{SLAVE}	LIN slave capacitance [6]
C'_{LINE}	LIN bus line capacitance [6]
LEN_{BUS}	overall bus line length [6]
N	number of slaves nodes

Example: Assuming a 6-node LIN network with a capacitance of 220 pF per slave and an overall network length of 8 m with a line capacitance of 80 pF/m. It results in a maximum master capacitance of

$$R_{BUS,\max} = R_{MASTER,\max} \parallel \frac{R_{slave,\max}}{N+1} = 965\Omega$$

$$C_{MASTER,\max} = \frac{\tau_{\max}}{R_{BUS,\max}} - N \cdot C_{SLAVE} - LEN_{BUS} \cdot C'_{LINE} = 3.44nF$$

In this example a master capacitor of C_{MASTER} = 3.3 nF is recommended.

4.3.2 EME – low slope variant (TJA1021 only)

The TJA1021 is provided in two variants: normal slope (TJA1021T(K)/20 [3]) and low slope (TJA1021T(K)/10 [3]). The curve shaping of the LIN bus signal of normal slope variant is optimized for the maximum specified LIN transmission speed of 20 kBd. For low speed LIN applications (e.g. 10.4 kBd) the curve shaping of the normal slope variant has unnecessary steep slopes. Therefore the low slope variant of the TJA1021 results in a further reduction of EME.

4.3.3 EMI – capacitive load

A capacitor on the LIN bus pin reduces the impact of RF-interferences. Thus it is recommended to provide a capacitor (e.g. $C_{MASTER/SLAVE}$ = 220 pF) from LIN to ground at each node.

4.4 LIN ESD protection

The on-chip ESD protection of pin LIN of the TJA102x is designed to withstand high ESD. In Table 9 an overview of the TJA102x ESD robustness on pin LIN is listed.

Table 9. TJA102x ESD robustness on pin LIN

LIN transceiver	ESD model	Value	Unit
TJA1021	Human Body Model JESD22-A114-B (100 pF / 1.5 kΩ)	±8	kV
	IEC 61000-4-2 (150 pF / 300 Ω)	(±6) [17]	kV
TJA1022	Human Body Model JESD22-A114-B (100 pF / 1.5 kΩ)	±8	kV
	IEC 61000-4-2 (150 pF / 300 Ω)	±8 (±12) [19]	kV
TJA1024	Human Body Model JESD22-A114-B (100 pF / 1.5 kΩ)	±8	kV
	IEC 61000-4-2 (150 pF / 300 Ω)	±8 (±11) [25]	kV
TJA1027	Human Body Model JESD22-A114-B (100 pF / 1.5 kΩ)	±8	kV
	IEC 61000-4-2 (150 pF / 300 Ω)	±8 (±12) [18]	kV
TJA1029	Human Body Model JESD22-A114-B (100 pF / 1.5 kΩ)	±8	kV
	IEC 61000-4-2 (150 pF / 300 Ω)	±8 (±12) [23]	kV

External ESD protection on the LIN bus connection is recommended if the LIN transceiver is subjected to higher ESD-pulses than listed in Table 9. Fig 27 shows a set-up for such external ESD protection.

The clamping voltage V_{CLAMP} of the ESD protection diodes should be chosen above the maximum battery voltage condition (e.g. jump start) in order not to be damaged, in case the LIN bus line is shorted to the battery line. Furthermore, the positive clamping voltage $V_{CLAMP-POS}$ should be below the maximum LIN bus voltage $V_{LIN,max}$ [3][4][5][22][24] and the negative clamping voltage $V_{CLAMP-NEG}$ should be above the minimal LIN bus voltage $V_{LIN,min}$ [3][4][5][22][24].

According to the LIN Specification [6], the LIN slave node capacitance shall be less than $C_{SLAVE,max}$ = 250 pF to ground. Together with the inherent capacitance of an ESD-protection device (e.g. suppressor diode PESD1LIN [20]) this requirement (< 250 pF) must be fulfilled.

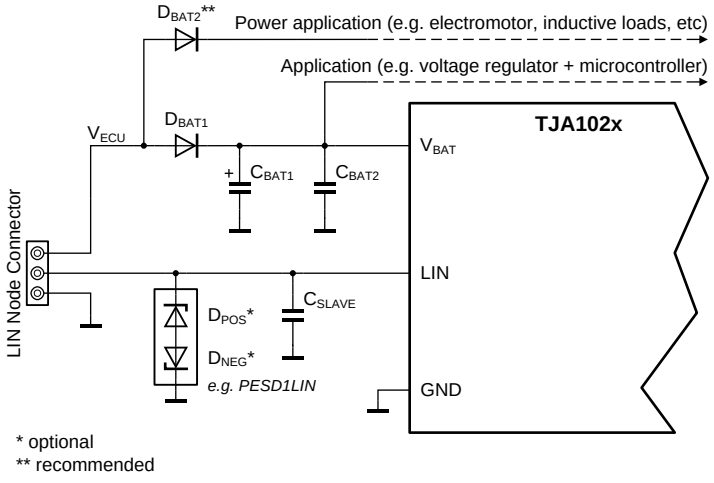


Fig 27. External ESD protection set-up

The suppressor diodes D_{POS} and D_{NEG} and the LIN node capacitor C_{LIN} should be placed as close as possible to the connectors.

5. Physical layer conformance

5.1 LIN 2.x conformance

The TJA102x LIN transceivers are fully compliant to LIN 2.0 [8], LIN 2.1 [7], LIN 2.2 and LIN 2.2A [6]. The LIN conformance was tested by an external test house.

Since the LIN physical layer is independent on higher OSI model layers (e.g. the LIN protocol), nodes containing a TJA102x LIN transceiver can be combined, without restriction, with LIN physical layer nodes that comply with other LIN revisions (i.e. LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3, LIN 2.0, LIN 2.1, LIN 2.2 and LIN 2.2A).

5.2 LIN 1.3 compatibility

LIN 2.x transceivers are per definition compatible to LIN 1.3 [9] and older revisions, because the LIN 2.0 specification [8] has been modified in order to provide higher transmission reliability compared to older LIN physical layer specification versions (e.g. LIN 1.3). In the TJA102x data sheets LIN 1.3 parameters are not specified, because they are redundant and replaced with LIN 2.x parameters.

5.3 SAE J2602 conformance

The TJA102x LIN transceivers are fully compliant to SAE J2602 [10]. The LIN conformance was tested from an external test house.

5.4 ISO 9141 (K-Line) compatibility

The Standard ISO 9141-2 “Road Vehicles – Diagnostic Systems – Part 2” [11] specifies the interchange of digital (diagnostic) information between on-board ECUs of road vehicles and a scan/test tool. The appropriate bus is the so-called “K-Line Bus”.

Although the LIN physical layer [6] has been derived from the ISO 9141 [11] standard there are some differences such as shown in Table 10.

Table 10. Comparison ISO 9141 with LIN and TJA102x

Description	ISO 9141 [11]	LIN [6]	TJA102x
Operating Voltage Range V_B	8 V to 16 V	7 V to 18 V	✓
Receiver High State	> 70% V_B	> 60% V_B	✓
Receiver Low State	< 30% V_B	< 40% V_B	✓
Temperature Range	0 °C to 50 °C	-40 °C to 125 °C	✓
Capacitance			
Diagnose Tester / LIN Master	< 2 nF	-	✓
ECU / LIN Slave	< 500 pF	< 250 pF	✓

Description	ISO 9141 [11]	LIN [6]	TJA102x
Wiring	< 2 nF	< 6 nF	✓
Total	< 9.6 nF	< 10nF	✓
Resistance			
Diagnose Tester / LIN Master	510 Ω	0.9 kΩ to 1.1 kΩ	✓
ECU / LIN Slave	> 100 kΩ	20 kΩ to 60 kΩ	The LIN Slave pull-up is integrated in the TJA102x. For reliable operation the overall pull-up of the network shall be above 450 Ω.
Timings			
Transmission Rate	10.4 kBd	1 kBd to 20 kBd	✓
Slew Rate / Slope Time	< 10 % T_{BIT} = 9.6 µs	duty cycle specification	The timing of the TJA102x is according to the duty cycle specification of LIN, which is designed for communication speed of up to 20 kBd and results in better EMC compared to ISO 9141.

Although the LIN physical layer is not fully compliant to the ISO 9141 standard, the TJA102x LIN transceiver will work in K-Line networks. Only the number of K-Line nodes could be limited, if LIN transceivers are applied. In a K-Line bus the overall network load is mainly caused by the Diagnose Tester (the master in a K-Line bus [11]), which is terminated with a pull-up of R_{TESTER} = 510 Ω. But each LIN transceiver with integrated LIN slave resistor R_{SLAVE}, like the TJA102x, will cause a decrease of the K-Line network resistance. The K-Line network resistance reduction can be calculated with following equation:

Minimum K-Line network load:

$$R_{K(BUS-BAT)\,\min} = \frac{R_{TESTER,\,\min} \times \frac{R_{SLAVE,\,\min}}{N}}{R_{TESTER,\,\min} + \frac{R_{SLAVE,\,\min}}{N}}$$

with

$R_{TESTER,min}$	minimum Diagnose Tester pull-up resistor
$R_{SLAVE,min}$	minimum LIN slave pull-up resistor
N	number of transceivers with integrated LIN slave resistor

Thus the maximum number of LIN transceivers in a K-Line bus is limited by the strength of the weakest bus driver. The TJA102x are specified for the minimum network resistance of $R_{L(LIN-BAT)}$= 500 Ω [3][4][5][22]. Nevertheless the bus driver of the TJA102x can drive a lower network resistance. The minimum bus resistance is $R_{K(BUS-BAT),min}$ = 450 Ω, which is derived from the minimum current limitation I_{BUS_LIM} [3][4][5][22] of the bus driver.

Summary:

Though there are some deviations between the LIN and the ISO 9141 specification, the TJA102x are able to support the K-Line bus from functional point of view. From a formal specification point of view, no LIN transceiver supports by 100% the original ISO 9141-2 specification [11].

6. References

[1] Data Sheet TJA1020, LIN Transceiver, Philips Semiconductors, Jan. 2004

[2] Application Note, AN00093, TJA1020 LIN transceiver, Philips Semiconductors, Sep. 2005

[3] Data Sheet TJA1021, LIN 2.1/SAE J2602 transceiver, NXP Semiconductors, Mar. 2011

[4] Data Sheet TJA1027, LIN 2.2A/SAE J2602 transceiver, NXP Semiconductors, Apr. 2013

[5] Data Sheet TJA1022, Dual LIN 2.2A/SAE J2602 transceiver, NXP Semiconductors, Apr. 2013

[6] LIN Specification Package, LIN Protocol Specification – Rev. 2.2A, LIN Consortium, Dec. 2010

[7] LIN Specification Package, LIN Protocol Specification – Rev. 2.1, LIN Consortium, Nov. 2006

[8] LIN Specification Package, LIN Protocol Specification – Rev. 2.0, LIN Consortium, Sep. 2003

[9] LIN Specification Package, LIN Protocol Specification – Rev. 1.3, LIN Consortium, Dec. 2002

[10] SAE International J2602-1, LIN Network for Vehicle Applications, Nov. 2012

[11] International Standard ISO 9141, Road Vehicles – Diagnostic Systems – Requirement for Interchange of Digital Information, International Standardization Organization, 1989

[12] Technical Report TR0363, The LIN Physical Layer, NXP Semiconductors, Jul. 2008

[13] LIN Conformance Test Specification Package for LIN 2.1, LIN Consortium, Oct. 2008

[14] SAE International J2602-2, LIN Network for Vehicle Applications Conformance Test, Revision Nov. 2012

[15] International Standard ISO 7637-2, Road Vehicles – Electrical disturbances from conduction and coupling – Electrical transient conduction along supply lines only, Mar. 2011

[16] International Standard ISO 16750-2, Road Vehicles – Environmental conditions and testing for electrical and electronic equipment – Electrical loads, Mar. 2010

[17] TJA1021 – LIN EMC Test Report (Nr. 08-02-08a), IBEE Zwickau, Mar. 2008

[18] TJA1027 – LIN EMC Test Report (Nr. 03-04-11), IBEE Zwickau, Oct. 2011

[19] TJA1022 – LIN EMC Test Report (Nr. 11-01-12), IBEE Zwickau, Jan. 2012

[20] Data Sheet PESD1LIN, LIN-bus ESD protection diode, NXP Semiconductors, May 2011

[21] International Standard IEC 61000-4-2, Electromagnetic Compatibility – Testing and Measurement Techniques – Electrostatic Discharge Immunity Test, International Electrotechnical Commission, 2001

[22] Data Sheet TJA1029, LIN 2.2A/SAE J2602 transceiver with TXD dominant timeout, NXP Semiconductors, Apr. 2013

[23] TJA1029 – LIN EMC Test Report (Nr. 11-08-12), IBEE Zwickau, Sep. 2012

[24] Data Sheet TJA1024, Quad LIN 2.2A/SAE J2602 transceiver, NXP Semiconductors, Jan. 2015

[25] TJA1024HG – LIN EMC Test Report (Nr. 03-12-14), IBEE Zwickau, Dec. 2014

[26] International Standard ISO 17987-4, Road Vehicles – Local Interconnect Network (LIN) – Electrical Physical Layer (EPL) specification 12V/24V, 201x

Notes

7. Legal information

7.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

7.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

8. List of figures

9. List of tables

10. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 January 2015
Document identifier: DOC-178856, DOC-197731, DOC-236234