xPC56XXMB User Manual

xPC56XXMBUM

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1 OVERVIEW

The xPC56XXMB Motherboard is an evaluation system supporting Freescale's MPC56xx microprocessors. The complete system consists of an xPC56XXMB Motherboard and an xPC56xxADPT Mini-Module (not included) which plugs into the motherboard. Different Mini-Modules are available for evaluating the different devices in the MPC56xx family of microprocessors. The evaluation system (Motherboard & Mini-Module) allows full access to the CPU, all of the CPU's I/O signals, and the motherboard peripherals (such as CAN, SCI, LIN).

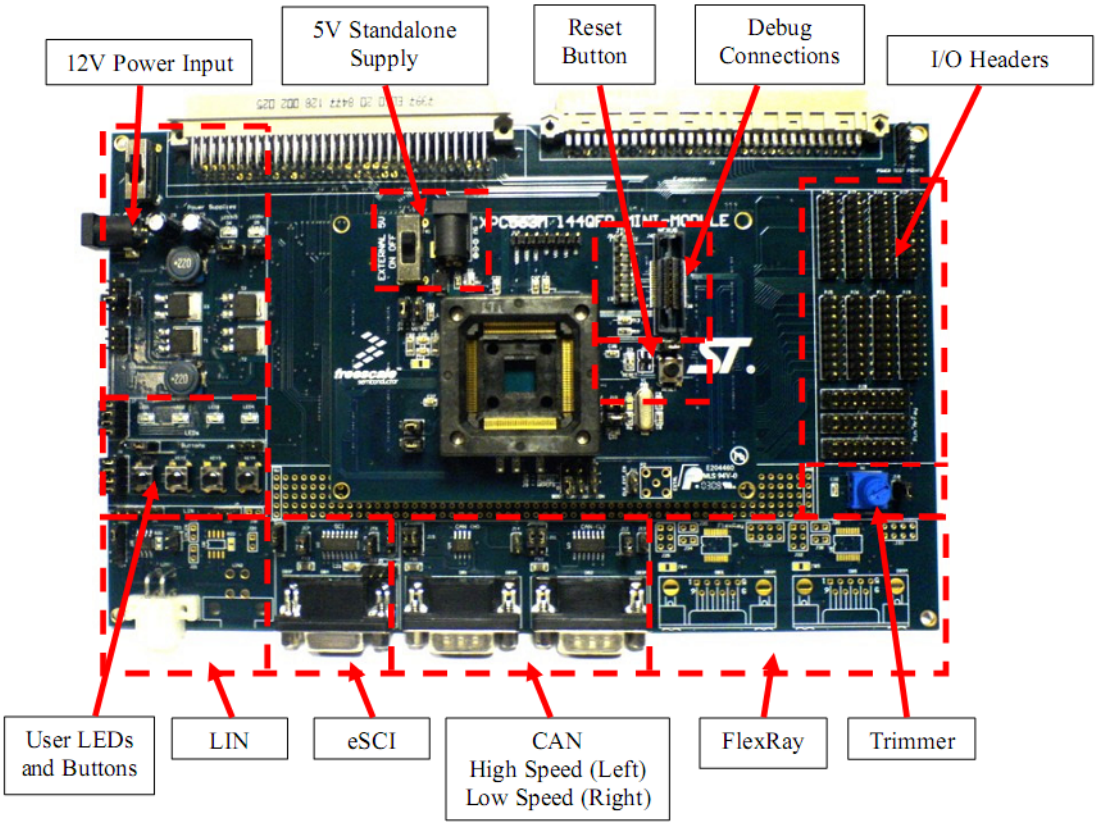

Figure 1-1: Overview of the xPC56XXMB with Mini-Module (not included)

1.1 Package Contents

An xPC56XXMB Evaluation Kit includes the following items:

- One xPC56XXMB Motherboard
- One xPC56XX Resources CD-ROM
- Freescale Warranty Card

1.2 Supported Devices

To work with a specific device in the MPC56xx family of microprocessors, the correct Mini-Module (not included) must be used to plug into the xPC56XXMB motherboard. Below is a list of all available Mini-Modules and their supported devices:

xPC560BADPT100S Mini-Module: Supports MPC560xB (100 LQFP package)

xPC560BADPT144S Mini-Module: Supports MPC560xB (144 LQFP package)

xPC560BADPT176S Mini-Module: Supports MPC560xB (176 LQFP package)

xPC560BADPT208S Mini-Module: Supports MPC560xB (208 BGA package)

xPC560PADPT64S Mini-Module: Supports MPC560xP (64 LQFP package)

xPC560PADPT100S Mini-Module: Supports MPC560xP (100 LQFP package)

xPC560PADPT144S Mini-Module: Supports MPC560xP (144 LQFP package)

xPC560SADPT144S Mini-Module: Supports MPC560xS (144 LQFP package)

xPC560SADPT176S Mini-Module: Supports MPC560xS (176 LQFP package)

xPC560SADPT208S Mini-Module: Supports MPC560xS (208 BGA package)

xPC563MADPT144S Mini-Module: Supports MPC563xM (144 LQFP package)

xPC563MADPT176S Mini-Module: Supports MPC563xM (176 LQFP package)

xPC563MADPT208S Mini-Module: Supports MPC563xM (208 BGA package)

xPC564AADPT176S Mini-Module: Supports MPC564xA (176 LQFP package)

xPC564AADPT208S Mini-Module: Supports MPC564xA (208 BGA package)

xPC564AADPT324S Mini-Module: Supports MPC564xA (324 BGA package)

xPC564LADPT144S Mini-Module: Supports MPC564xL (144 LQFP package)

xPC564LADPT257S Mini-Module: Supports MPC564xL (257 BGA package)

1.3 Recommended Materials

- Freescale device reference manual and datasheet
- xPC56XXMB schematic
- Mini-Module hardware manual and schematics

1.4 Handling Precautions

Please take care to handle the package contents in a manner such as to prevent electrostatic discharge.

2 HARDWARE FEATURES

2.1 xPC56XXMB Board Features

- ON/OFF Power Switch w/ LED indicators
- A 12VDC power supply input barrel connector
- Onboard ST Microelectronics L9758 regulator provides three different power voltages simultaneously: 5V, 3.3V, and 1.2V
- Onboard peripherals can be configured to operate at 5V or 3.3V logic levels
- Two CAN channels with jumper enables
  - One CAN channel with High-Speed transceiver and DB9 male connector
  - One CAN channel with Low-Speed Fault Tolerant and High-Speed transceiver (selectable with jumpers) and DB9 male connector
- Two LIN channels with jumper enables
  - One channel with transceiver and pin header connector populated
  - One channel with footprints only
- One SCI channel with jumper enables
  - Transceiver with DB9 female connector
- Two FlexRay channels with jumper enables
  - One channel with transceiver and DB9 male connector
  - One channel with footprint only
- Four user push buttons with jumper enables and polarity selection
- Four user LED’s with jumper enables
- One potentiometer for analog voltage input
- Pin array for accessing all I/O signals
- Expansion connectors for accessing all I/O signals
- Development zone with 0.1” spacing and SOIC footprint prototyping

- Specifications:
  - Board Size 5.5” x 9.0”
  - 12VDC Center Positive power supply with 2.1/5.5mm barrel connector

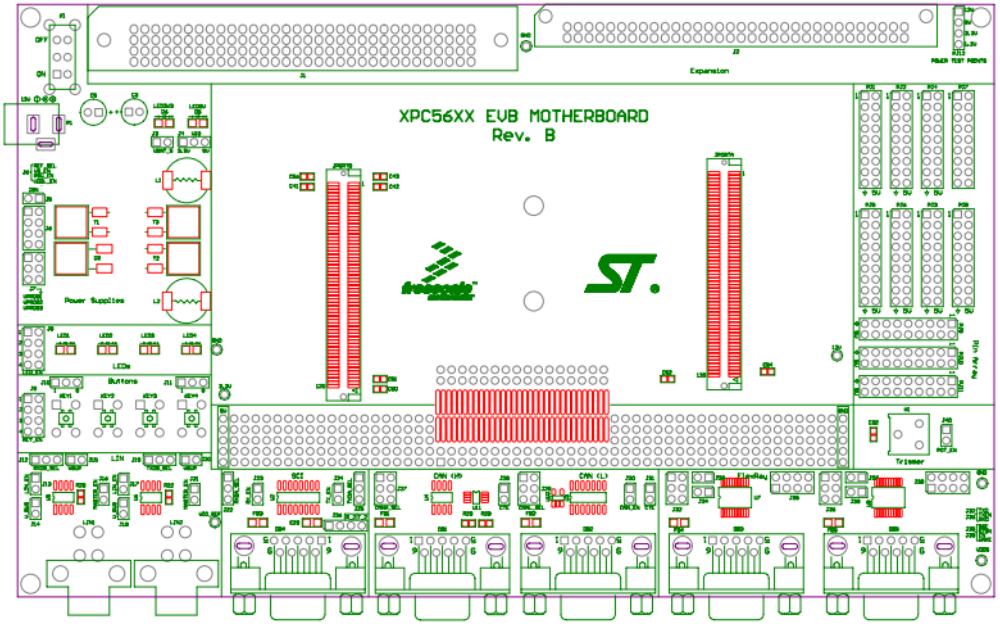

Figure 2-2: xPC56XXMB Top Component Placement

2.2 Pin Numbering for Jumpers

Jumpers for the xPC56XXMB motherboard have a rounded corner to indicate the position of pin 1. See examples below for the numbering convention used in this manual for jumper settings.

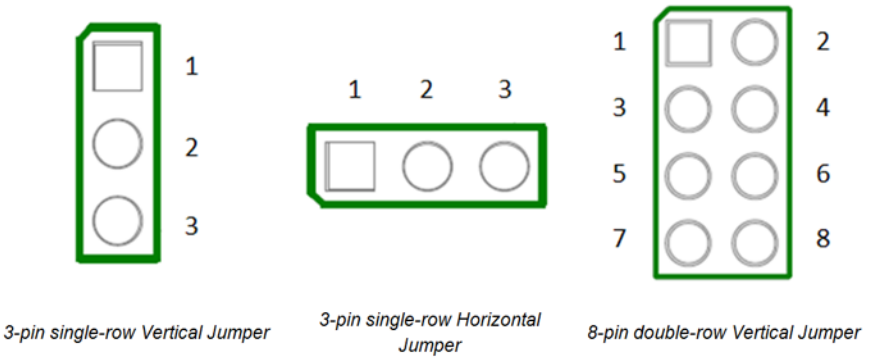

Figure 2-3: Pin Numbering

3 xPC56XXMB HARDWARE & JUMPER SETTINGS

Please note that this section of the manual is written for revision B and C of the xPC56XXMB motherboard. Revision B motherboards are indicated by the “Rev. B” silkscreen text in the center of the motherboard, and Revision C motherboards are indicated by the “Rev. C” silkscreen text in the center of the motherboard.

Revision A motherboards have different jumper numbers. These differences can be found in the table below:

Revision A	Revision B	Revision C	Jumper Description
J3	J6, pins 1+2	-	VSA Tracking Regulator Configuration
-	-	J3	Slew Rate Select
J4	J7	J7	VPROG Regulators Control
J5 (pins 1+2)	J5	-	IGN Control
-	-	J5	Power Reset Pullup Voltage Select
J5 (pins 3+4, 5+6, 7+8)	J6, pins 3+4, 5+6, 7+8	-	Regulators Enable & Standby
-	-	J6	Power Reset Output Enable
J36	J4	J4	VIO Peripherals Logic Level
J37	J3	-	VBat low voltage detection
-	-	J41	Power Reset Pullup Enable
J7	J8	J8	LEDs Enable
J8	J9	J9	Buttons Enable
J9	J10	J10	Buttons Driving Configuration

J40	J11	J11	Buttons Idle Configuration
J22	J13	J13	LIN1 enable
J24	J14	J14	LIN1 VBUS configuration
J6	J15	J15	LIN1 VSUP configuration
J23	J16	J16	LIN1 master selection
J28	J22	J22	LIN1/SCI RxD selection
J27	J25	J25	LIN1/SCI TxD selection
J19	J17	J17	LIN2 enable
J21	J18	J18	LIN2 VBUS configuration
J31	J20	J20	LIN2 VSUP configuration
J20	J21	J21	LIN2 master selection
J30	J12	J12	LIN2/SCI RxD selection
J29	J19	J19	LIN2/SCI TxD selection
J17	J23	J23	SCI RxD Enable
J16	J24	J24	SCI TxD Enable
J27	J25	J25	LIN1/SCI TxD selection
J28	J22	J22	LIN1/SCI RxD selection
J14	J28	J28	CAN (H) Transmit Enable
J15	J27	J27	CAN (H) TxD/RxD Enable
J13	J31	J31	CAN (L) CTE

J12	J30	J30	CAN (L) Enable
J11	J29	J29	CAN (L) TxD/RxD Enable
J25	J32	J32	FlexRay Bus Driver 1 Enable
J26	J35	J35	FlexRay Bus Driver 1 Configuration
J34	J34	J34	FlexRay 1 Terminal Resistor Connection
J35	J33	J33	FlexRay 1 Terminal Resistor Connection
J32	J36	J36	FlexRay Bus Driver 2 Enable
J33	J39	J39	FlexRay Bus Driver 2 Configuration
J38	J38	J38	FlexRay 2 Terminal Resistor Connection
J39	J37	J37	FlexRay 2 Terminal Resistor Connection
J18	J40	J40	POT Enable

3.1 Power Supplies

The xPC56XXMB obtains its power from the 12VDC Center Positive input barrel connector. The following jumpers are used to configure the power supply output:

J3 – VBat low voltage detection (Revisions A & B only)

Jumper Setting	Effect
On	Low battery detection is enabled
Off (default)	Low battery detection is disabled

J3 – Slew Rate Select (Revision C only)

Jumper Setting	Effect
1+2	Regulator configured for fast slew rate
2+3	Regulator configured for slow slew rate
Off (default)	Regulator configured for medium slew rate

J4 – VIO Peripherals Logic Level

Jumper Setting	Effect
1+2	Onboard peripherals are configured for 3.3V logic
2+3 (default)	Onboard peripherals are configured for 5V logic

J5 – IGN Control (Revisions A & B only)

Jumper Setting	Effect
On (default)	The power regulator is always on
Off	If 5+6 is also OFF on J6, the power regulator is in standby

J5 – Power Reset Pullup Voltage Select (Revision C only)

Jumper Setting	Effect

1+2	If J41 is ON, regulator output reset is pulled up to 5V
2+3	If J41 is ON, regulator output reset is pulled up to 3.3V

J6 – Regulators Enable & Standby (Revisions A & B only)

Jumper Setting	Position	Effect
1+2	On	The ST L9758 tracking regulator VSA tracks the input voltage at its TRACK_REF pin.
	Off (default)	The ST L9758 tracking regulator VSA tracks 5V
3+4	On	VSB, VSC, and VSD tracking regulators are disabled
	Off (default)	VSB, VSC, and VSD tracking regulators are enabled
5+6	On (default)	The power regulator is always on
	Off	The power regulator is in standby if jumpers 1+2 are also in the “off” position
7+8	On	VDLL and VCORE regulators are disabled
	Off (default)	VDLL and VCORE regulators are enabled

J6 – Power Reset Output Enable (Revision C only)

Jumper Setting	Effect

On (default)	If regulator voltages fall below threshold, a reset is sent to the microprocessor
Off	No reset is sent to the microprocessor

J7 – VPROG Regulators Control (Revisions A & B)

Jumper Setting	Position	Effect
1+2	On	VKAM regulator output is programmed to 1V
	Off (default)	VKAM regulator output is programmed to 1.5V
3+4	On	VSTBY regulator output is programmed to 2.6V
	Off (default)	VSTBY regulator output is programmed to 3.3V
5+6	On	VDLL regulator output is programmed to 2.6V
	Off (default)	VDLL regulator output is programmed to 3.3V

J7 – VPROG Regulators Control (Revision C only)

Jumper 1+2	Jumper 3+4	Jumper 5+6	VDD3	VDDL	VKAM
Off	Off	Off	3.3 V	2.6 V	2.6 V
Off	Off	On	3.3 V	3.3 V	3.3 V
Off	On	Off	3.3 V	1.5 V	1.0 V

Off	On	On	3.3 V	3.3 V	1.0 V
On	Off	Off	3.3V standby	3.3 V	1.0 V
On	Off	On	2.0 V	3.15 V	5.0 V
On	On	Off	2.6 V standby	3.3 V	1.0 V
On	On	On	2.6 V standby	3.3 V	1.5 V

J37 – VBat low voltage detection

Jumper Setting	Effect
On	Low battery detection is enabled
Off (default)	Low battery detection is disabled

J41 – Power Reset Pullup Enable (Revision C only)

Jumper Setting	Effect
On	Regulator output reset is pulled up
Off (default)	Regulator output reset is not pulled up

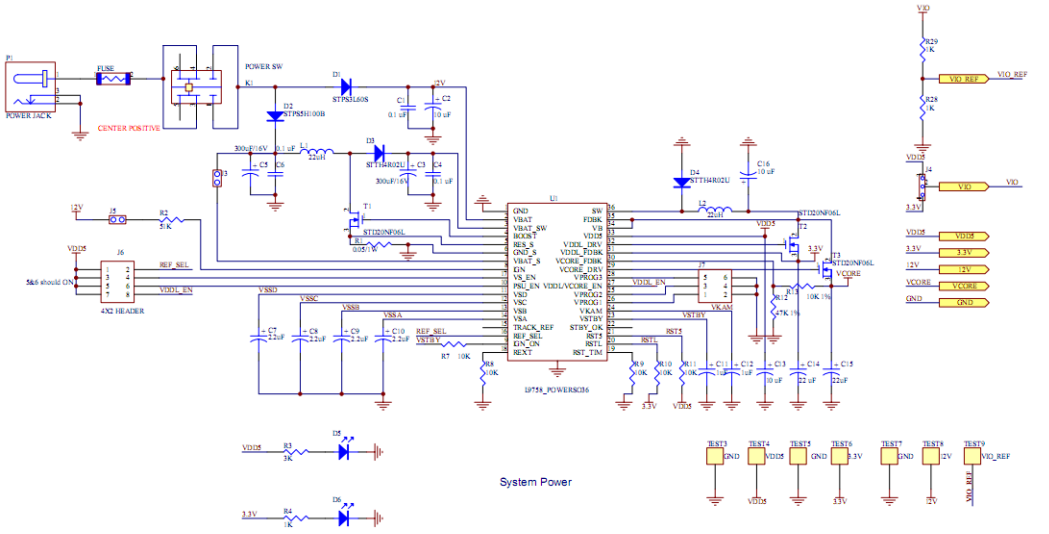

Figure 3-1: Power Supply circuitry schematic (Revisions A & B only)

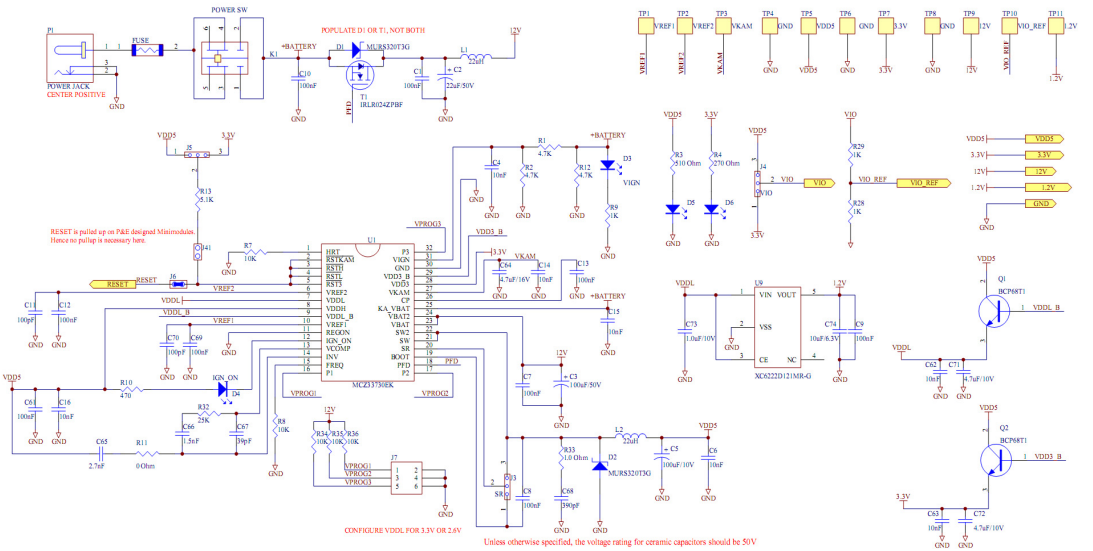

Figure 3-2: Power Supply circuitry schematic (Revision C only)

3.2 LEDs

There are four user LEDs available on the xPC56XXMB. All LEDs are active low.

J8 – LEDs Enable

Controls whether the LEDs on the xPC56XXMB motherboard are connected to I/O pins of the processor. The exact pins used are dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Jumper Setting	Effect
1+2 (default on)	LED1 connected to processor I/O pin
3+4 (default on)	LED2 connected to processor I/O pin
5+6 (default on)	LED3 connected to processor I/O pin
7+8 (default on)	LED4 connected to processor I/O pin

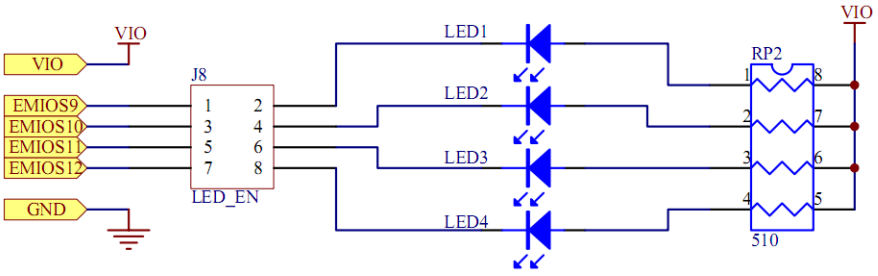

Figure 3-3: LEDs circuitry schematic

3.3 Buttons

There are four user buttons available on the xPC56XXMB.

J9 – Buttons Enable

Controls whether the buttons on the xPC56XXMB motherboard are connected to I/O pins of the processor. The exact pins used are dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Jumper Setting	Effect
1+2 (default on)	KEY1 connected to processor I/O pin
3+4 (default on)	KEY2 connected to processor I/O pin
5+6 (default on)	KEY3 connected to processor I/O pin
7+8 (default on)	KEY4 connected to processor I/O pin

J10 – Buttons Driving Configuration

Selects whether the buttons drive logic high or drive logic low when pressed.

Jumper Setting	Effect
1+2	When pressed, buttons will send logic high to the connected I/O pin
2+3 (default)	When pressed, buttons will send logic low to the connected I/O pin

J11 – Buttons Idle Configuration

Selects whether the I/O pins are pulled logic high or pulled logic low. This controls the defaultlogic level of the I/O pins when the buttons are not pressed.

Jumper Setting	Effect
1+2 (default)	I/O pins connected to the buttons are pulled up to logic high
2+3	I/O pins connected to the buttons are pulled down to logic low

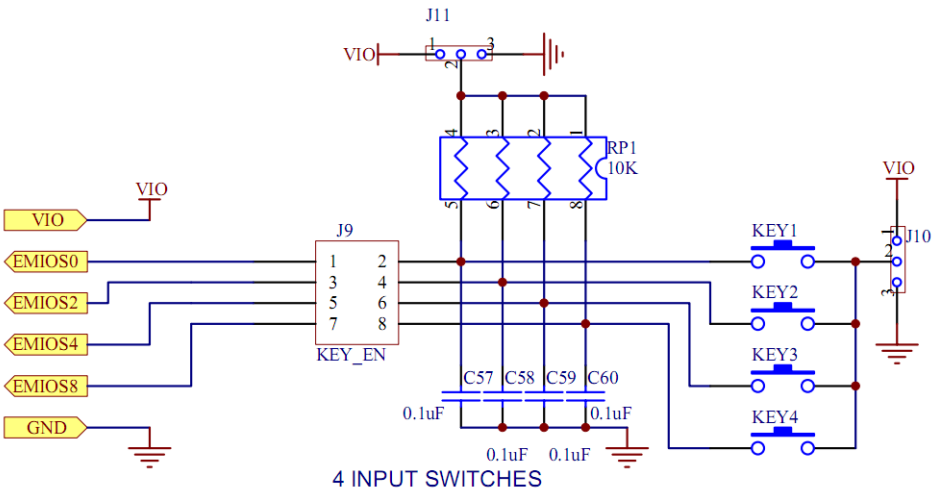

Figure 3-4: Buttons circuitry schematic

3.4 LIN

There are footprints for two LIN connections on the xPC56XXMB. By default,

one LIN circuit is assembled (LIN1) and the other circuit is left unpopulated (LIN2).

J15 – LIN1 VSUP configuration

Jumper Setting	Effect
On	LIN1 VSUP is connected to 12V
Off (default)	LIN1 VSUP is not connected to 12V

J13 – LIN1 enable

Jumper Setting	Effect
On (default)	Enables the LIN1 transceiver
Off	Disables the LIN1 transceiver

J16 – LIN1 master selection

Jumper Setting	Effect
On	LIN1 is configured as a master node
Off (default)	LIN1 is configured as a slave node

J14 – LIN1 VBUS configuration

Jumper Setting	Effect

On	LIN1 VBUS is connected to 12V
Off (default)	LIN1 VBUS is not connected to 12V

J25– LIN1/SCI TxD selection

Controls whether the TxD pin on LIN1 or SCI is connected to the default I/O pin on the processor. The exact pins used are dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Jumper Setting	Effect
1+2	The LIN1 TxD pin is connected to a processor I/O pin. This should be set if enabling LIN1.
2+3	The SCI TxD pin is connected to a processor I/O pin.

J22 – LIN1/SCI RxD selection

Controls whether the RxD pin on LIN1 or SCI is connected to the default I/O pin on the processor. The exact pins used are dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Jumper Setting	Effect
1+2	The LIN1 RxD pin is connected to a processor I/O pin. This should be set if enabling LIN1.
2+3	The SCI RxD pin is connected to a processor I/O pin.

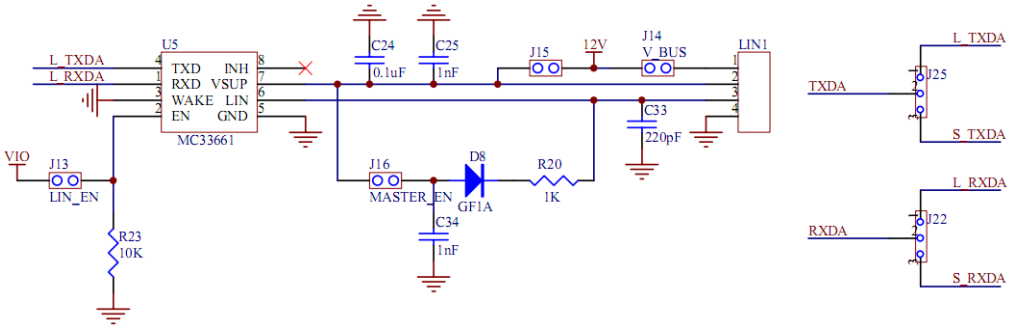

Figure 3-5: LIN1 Schematic

J20 – LIN2 VSUPconfiguration

Jumper Setting	Effect
On	LIN2 VSUP is connected to 12V
Off (default)	LIN2 VSUP is not connected to 12V

J17 – LIN2 enable

Jumper Setting	Effect
On	Enables the LIN2 transceiver
Off (default)	Disables the LIN2 transceiver

J21 – LIN2 master selection

Jumper Setting	Effect
On	LIN2 is configured as a master node
Off (default)	LIN2 is configured as a slave node

J18 – LIN2 VBUS configuration

Jumper Setting	Effect
On	LIN2 VBUS is connected to 12V
Off (default)	LIN2 VBUS is not connected to 12V

J19 – LIN2/SCI TxD selection

Controls whether the TxD pin on LIN2 or SCI is connected to the default I/O pin on the processor. The exact pins used are dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Jumper Setting	Effect
1+2	The LIN2 TxD pin is connected to a processor I/O pin. This should be set if enabling LIN2.
2+3	The SCI TxD pin is connected to a processor I/O pin.

J12 – LIN2/SCI RxD selection

Controls whether the RxD pin on LIN2 or SCI is connected to the default I/O pin on the processor. The exact pins used are dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Jumper Setting	Effect
1+2	The LIN2 RxD pin is connected to a processor I/O pin. This should be set if enabling LIN2.
2+3	The SCI RxD pin is connected to a processor I/O pin.

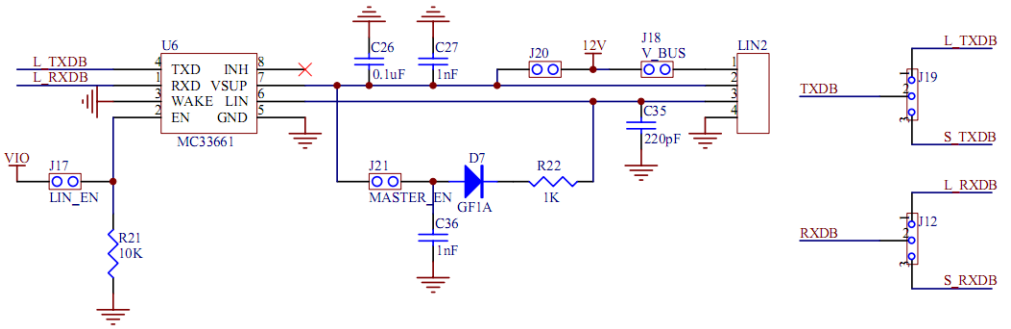

Figure 3-6: LIN2 schematic (Not populated by default)

3.5 SCI

One SCI interface is available on the xPC56XXMB.

J24 – SCI TxD Enable

Jumper Setting	Effect
On (default)	Enables SCI transmit
Off	Disables SCI transmit

J23 – SCI RxD Enable

Jumper Setting	Effect
On (default)	Enables SCI receive
Off	Disables SCI receive

J25 – LIN1/SCI TxD selection

Controls whether the TxD pin on LIN1 or SCI is connected to the default I/O pin on the processor. The exact pins used are dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Jumper Setting	Effect
1+2	The LIN1 TxD pin is connected to a processor I/O pin.

2+3	The SCI TxD pin is connected to a processor I/O pin. This should be set if enabling SCI.

J22 – LIN1/SCI RxD selection

Controls whether the RxD pin on LIN1 or SCI is connected to the default I/O pin on the processor. The exact pins used are dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Jumper Setting	Effect
1+2	The LIN1 RxD pin is connected a processor I/O pin.
2+3	The SCI RxD pin is connected to a processor I/O pin. This should be set if enabling SCI.

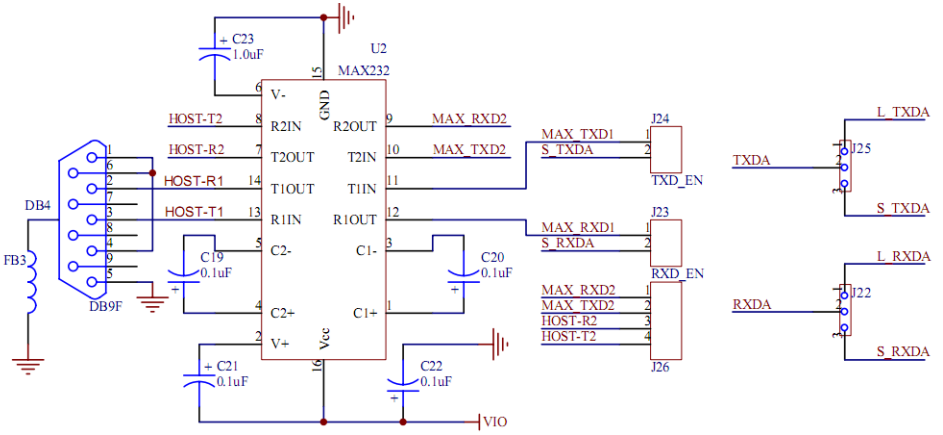

Figure 3-7: SCI schematic

3.6 CAN

Two CAN interfaces are implemented on the xPC56XXMB: a high-speed CAN interface and a low-speed CAN interface.

J28 – CAN (H) Transmit Enable

Jumper Setting	Effect
On	Enables CAN transmission
Off (default)	Disables CAN transmission

J27 – CAN (H) TxD/RxD Enable

Controls which I/O pins on the processor are connected to the TxD and RxD pins on CAN (H). The exact pins used are dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Jumper Setting	Effect
1+3 (default)	The RxD pin of the CAN (H) interface is connected to a processor I/O pin.
3+5	The RxD pin of the CAN (H) interface is connected to a processor I/O pin.
2+4 (default)	The TxD pin of the CAN (H) interface is connected to a processor I/O pin.
4+6	The TxD pin of the CAN (H) interface is connected to a processor I/O pin.

J30 – CAN (L) Enable

Jumper Setting	Effect
On (default)	Enables CAN (L) transceiver
Off	Disables CAN (L) transceiver

J31 – CAN (L) CTE

Jumper Setting	Effect
On	Enables CAN transmission
Off (default)	Disables CAN transmission

J29 – CAN (L) TxD/RxD Enable

Controls which I/O pins on the processor are connected to the TxD and RxD pins on CAN (L). The exact pins used are dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Jumper Setting	Effect
1+3	The RxD pin of the CAN (L) interface is connected to a processor I/O pin.
3+5 (default)	The RxD pin of the CAN (L) interface is connected to a processor I/O pin.

2+4	The TxD pin of the CAN (L) interface is connected to a processor I/O pin.
4+6 (default)	The TxD pin of the CAN (L) interface is connected to a processor I/O pin.

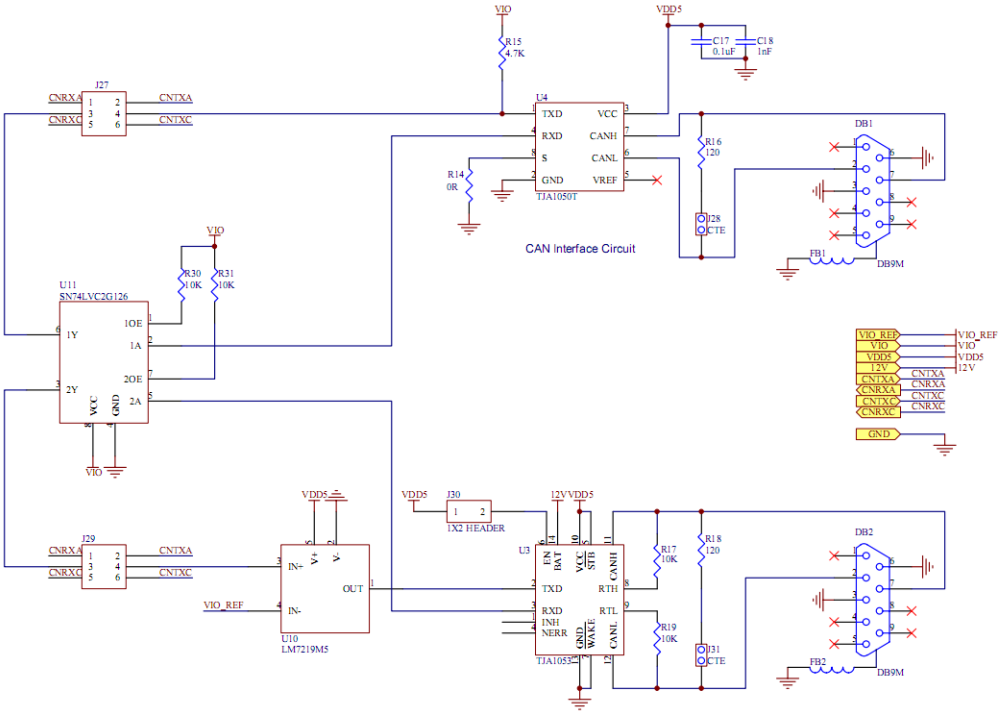

Figure 3-8: CAN schematic

3.7 FlexRay

The xPC56XXMB has footprints for two FlexRay interfaces. However, only one circuit is assembled by default. The FlexRay circuit is comprised of two DB9 connectors. DB3 contains signals for both FlexRay channels and is compatible with major FlexRay tools. DB5 contains the channel B signal,

thereby also allowing 2 separate FlexRay connectors for channel A and channel B operation.

J32 – FlexRay Bus Driver 1 Enable

Controls which I/O pins on the processor are connected to the TxD and RxD pins on FlexRay Bus Driver. The exact pins used are dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Jumper Setting	Effect
1+2 (default on)	The TXD pin on the FlexRay Bus Driver is connected to a processor I/O pin.
3+4 (default on)	The TXEN pin on the FlexRay Bus Driver is connected to a processor I/O pin.
5+6 (default on)	The RXD pin on the FlexRay Bus Driver is connected to a processor I/O pin.

J35 – FlexRay Bus Driver 1 Configuration

Controls which pins on the FlexRay Bus Driver are pulled up.

Jumper Setting	Effect
1+2	The BGE pin on the FlexRay Bus Driver is pulled up to 5V
3+4	The STBN pin on the FlexRay Bus Driver is pulled up to 5V

5+6 (default on)	The EN pin on the FlexRay Bus Driver is pulled down to GND
7+8 (default on)	The WAKE pin on the FlexRay Bus Driver is pulled down to GND

J33 & J34 FlexRay 1 Terminal Resistor Connection

Jumper Setting	Effect
On	Terminal resistors connected
Off (default)	Terminal resistors not connected

J36 – FlexRay Bus Driver 2 Enable

Controls which I/O pins on the processor are connected to the TxD and RxD pins on FlexRay Bus Driver. The exact pins used are dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Jumper Setting	Effect
1+2	The TXD pin on the FlexRay Bus Driver is connected to a processor I/O pin.
3+4	The TXEN pin on the FlexRay Bus Driver is connected to a processor I/O pin.
5+6	The RXD pin on the FlexRay Bus Driver is connected to a processor I/O pin.

J39 – FlexRay Bus Driver 2 Configuration

Controls which pins on the FlexRay Bus Driver are pulled up.

Jumper Setting	Effect
1+2	The BGE pin on the FlexRay Bus Driver is pulled up to 5V
3+4	The STBN pin on the FlexRay Bus Driver is pulled up to 5V
5+6	The EN pin on the FlexRay Bus Driver is pulled up to 5V
7+8	The WAKE pin on the FlexRay Bus Driver is pulled down to GND

J37 & J38 – FlexRay 2 Terminal Resistor Connection

Jumper Setting	Effect
On	Terminal resistors connected
Off (default)	Terminal resistors not connected

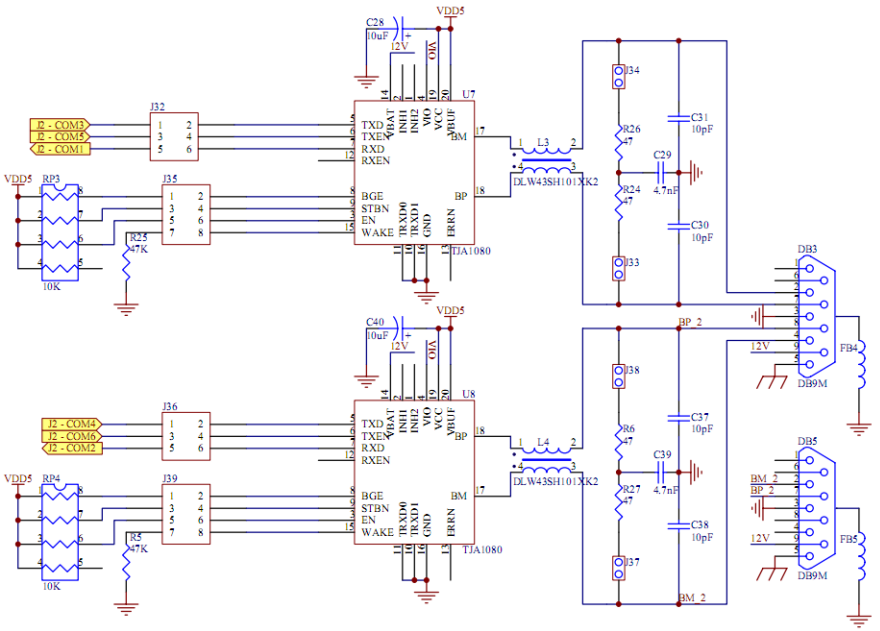

Figure 3-9: FlexRay schematic

3.8 Potentiometer

A potentiometer is available on the xPC56XXMB to allow an analog voltage input.

J40 – POT Enable

Jumper Setting	Effect
On	The potentiometer wiper terminal is connected to a processor I/O pin. The exact pin used is dependent on the specific Mini-Module plugged into the motherboard. Please refer to the Mini-Module hardware manual for more details.

Off (default)	The potentiometer wiper terminal is left disconnected.

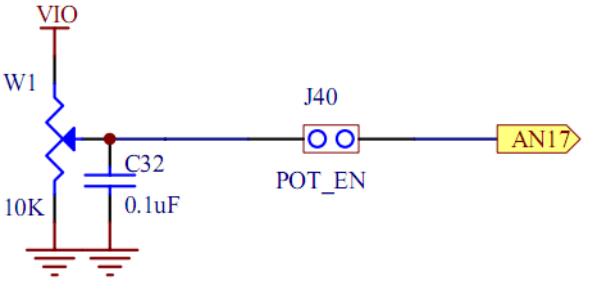

Figure 3-10: Potentiometer schematic

4 DEBUGGING/PROGRAMMING xPC56XX MOTHERBOARD

P&E provides hardware and software tools for debugging and programming the xPC56XXMB (with Mini-Module, sold separately).

P&E's Power Architecture USB Multilink and Cyclone MAX offer two effective hardware solutions, depending on your needs. The Power Architecture USB Multilink is a development tool that will enable you to debug your code and program it onto your target. The Cyclone MAX is a more versatile and robust development tool with advanced features and production programming capabilities, as well as Ethernet support.

More information is available below to assist you in choosing the appropriate development tool for your needs.

4.1 Hardware Solutions At A Glance

The Power Architecture USB Multilink offers an affordable and compact solution for your development needs, and allows debugging and programming to be accomplished simply and efficiently. Those doing rapid development will find the Multilink easy to use and fully capable of fast-paced debugging and programming.

The Cyclone MAX is a more complete solution designed for both development and production. The Cyclone MAX features multiple communications interfaces (including USB, Ethernet, and Serial), stand-alone programming functionality, high speed data transfer, a status LCD, and many other advanced capabilities.

Below is an overview of the features and intended use of the Power Architecture USB Multilink and Cyclone MAX.

4.2 Power Architecture USB Multilink Key Features

- Programming and debugging capabilities
- Compact and lightweight
- Communication via USB 2.0
- Supported by P&E software and Freescale's CodeWarrior

4.3 Cyclone MAX Key Features

- Advanced programming and debugging capabilities, including:

- PC-Controlled and User-Controlled Stand-Alone Operation
- Interactive Programming via Host PC
- In-Circuit Debugging, Programming, and Testing
- Compatible with Freescale's ColdFireV2/3/4, Power Architecture 5xx/8xx/55xx/56xx, and ARM7 microcontroller families
- Communication via USB, Serial, and Ethernet Ports
- Multiple image storage
- LCD screen menu interface
- Supported by P&E software and Freescale's CodeWarrior

4.4 Working With P&E's Power Architecture USB Multilink

Figure 4-1: P&E's Power Architecture USB Multilink

4.4.1 Product Features & Implementation

P&E's Power Architecture USB Multilink (part# USB-ML-PPCNEXUS) connects your target to your PC and allows the PC access to the debug mode on Freescale's Power Architecture 5xx/8xx/55xx/56xx microcontrollers. It connects between a USB port on a Windows 2000/XP/2003/Vista/7 machine and a standard 14-pin JTAG/Nexus connector on the target.

By using the Multilink, the user can take advantage of the background debug mode to halt normal processor execution and use a PC to control the processor. The user can then directly control the target's execution, read/write registers and memory values, debug code on the processor, and program internal or external FLASH memory devices. The Mukltilink enables you to debug, program, and test your code on your board.

4.4.2 Software

The Power Architecture USB Multilink works with Codewarrior as well as P&E's in-circuit debugger and flash programmer to allow debug and flash programming of the target processor. P&E's Power Architecture Development Packages come with the Power Architecture USB Multilink, as well as flash programming software, in-circuit debugging software, Windows IDE, and register file editor.

4.5 Working With P&E's Cyclone MAX

P&E's Cyclone MAX

4.5.1 Product Features & Implementation

P&E's Cyclone MAX is an extremely flexible tool designed for debugging, testing, and in-circuit flash programming of Freescale's ColdFireV2/3/4, Power Architecture 5xx/8xx/55xx/56xx, and ARM7 microcontrollers. The Cyclone MAX connects your target to the PC via USB, Ethernet, or Serial Port and enables you to debug your code, program, and test it on your board. After development is complete the Cyclone MAX can be used as a production tool on your manufacturing floor.

For production, the Cyclone MAX may be operated interactively via Windows-based programming applications as well as under batch or .dll commands from a PC. Once loaded with data by a PC it can be disconnected and operated manually in a stand-alone mode via the LCD menu and control buttons. The Cyclone MAX has over 3Mbytes of non-volatile memory, which allows the on-board storage of multiple programming images. When connected to a PC for programming or loading it can communicate via the ethernet, USB, or serial interfaces.

4.5.2 Software

The Cyclone MAX comes with intuitive configuration software and interactive programming software, as well as easy to use automated control software. The Cyclone MAX also functions as a full-featured debug interface, and is supported by Freescale's CodeWarrior as well as development software from P&E.

P&E's Cyclone MAX is also available bundled with additional software as part of various Development Packages. In addition to the Cyclone MAX, these Development Packages include in-circuit debugging software, flash programming software, a Windows IDE, and register file editor.

Freescale Controller Continuum

68HC08/S08/RS08/(S)12(X) ColdFire® V1 ColdFire® V2/V3/V4 Power Architecture® ARM®

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