

DEVKIT-MPC5748G

Revision Information

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Caution:

These schematics are provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

Notes:

- All components and board processes are to be ROHS compliant
- All small capacitors are 0402 unless otherwise stated
- All resistors are 0603 5% 0.1w unless otherwise stated. All zero ohm links are 0603
- All connectors and headers are denoted Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.

3 Different test points used in design:

TPVx - Through Hole Pad small

TPHx - Through Hole Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)

TPX - Surface Mount Wire Loop

TPV?


TPH5

TP?

User notes are given throughout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

Rev	Date	Designer	Comments
X1	23 Sep 2015	Catalin Neacsu	Initial release
X2	24 Sep 2015	Catalin Neacsu	Further changes. Decreased component size where possible.
X3	29 Sep 2015	Catalin Neacsu	Changed ethernet page. Changed caps around Q50 Rearranged GPIOs on page 15. Added more LEDs on page 14
X4	02 Oct 2015	Catalin Neacsu	Changed U50, USB connectors, ETH Connector, BOM optimization
X5	05 Oct 2015	Catalin Neacsu	Changed PN of U11 and C23
X6	07 Oct 2015	Catalin Neacsu	Small visual updates
X7	08 Oct 2015	Catalin Neacsu	Add separation resistors for USB interface, U50
X8	12 Oct 2015	Catalin Neacsu	Changed 3V3 converter, minor BOM optimization
X9	14 Oct 2015	Catalin Neacsu	Changed 3V3 converter, minor BOM optimization, better cost
X10	21 Oct 2015	Catalin Neacsu	Updated IO connections per Jesus Sanchez's request Added TP on page 3 per Ruiz Ricardo's request
X11	27 Oct 2015	Catalin Neacsu	Changed Power Supply page Added one user led
X12	28 Oct 2015	Catalin Neacsu	Changed PN for P2 and P7
X13	30 Oct 2015	Catalin Neacsu	Changed Power Supply page to allow supply selection
X14	02 Nov 2015	Catalin Neacsu	BOM Optimization
X15	03 Nov 2015	Catalin Neacsu	PN change for L1
X16	23 Dec 2015	Catalin Neacsu	Added Open SDA block Implemented other feedback
X17	06 Jan 2016	Catalin Neacsu	Implemented OpenSDA feedback
X18	08 Jan 2016	Catalin Neacsu	Changed some ICs to their NXP equivalent
X19	15 Jan 2016	Catalin Neacsu	P12, Y50 add GND connections. JTAG connector 14 pins
A	26 Jan 2016	Catalin Neacsu	Prototype Release
A1	13 Jun 2016	Jun Qiao	Update with Flexray, OpenSDA, Ethernet, LED, Buttons, GPIO.
A2	20 Jun 2016	Jun Qiao	Update with OpenSDA, GPIO connectors.
B	24 Jun 2016	Jun Qiao	Pilot Release
BX1	03 Nov 2017	Sendhil kumar	Update Ethernt & USB connection...etc
C	29 Nov 2017	Sendhil kumar	Pilot Release
D	03 Apr 2018	Sendhil kumar	Ethernet Section - replaced from Rev B KSZ8081RNACA schematics J2,J3,J4, J9,J12,J13&J14 are changed.

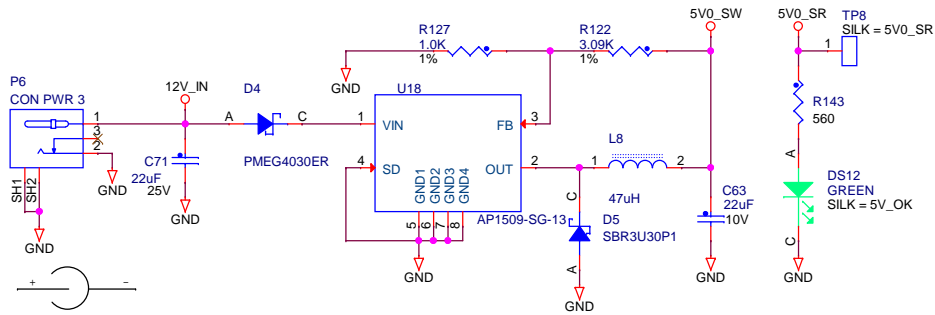
		Automotive Product Group 6501 William Cannon Drive West Austin, TX 78735-8598	
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ICAP Classification:		CP:	IUO: X
PUBI:			
Designer: C Neacsu	Drawing Title: DEVKIT-MPC5748G		
Drawn by: C Neacsu	Page Title: Index and Title Page		
Approved: Pissas Philip	Size B	Document Number SCH-29030	PDF: SPF-29030
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Power Input and Voltage Regulators

12V Power Supply Input

5V Switching Regulator

Input Voltage 12V, Output 5V at 1800mA

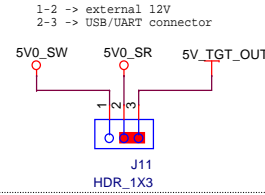


LAYOUT NOTE:
ADD Graphical silk:

Layout note: follow IC datasheet recommendations for PCB layout and thermal dissipation

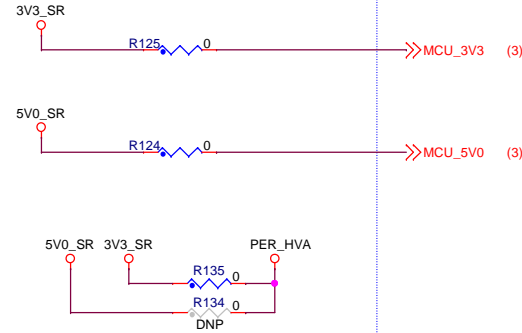
Board supply selection

Select between USB and external 12V

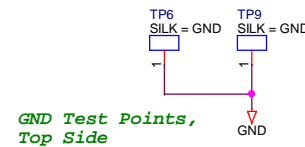


Power Control

Jumpers can be fitted to facilitate power measurements

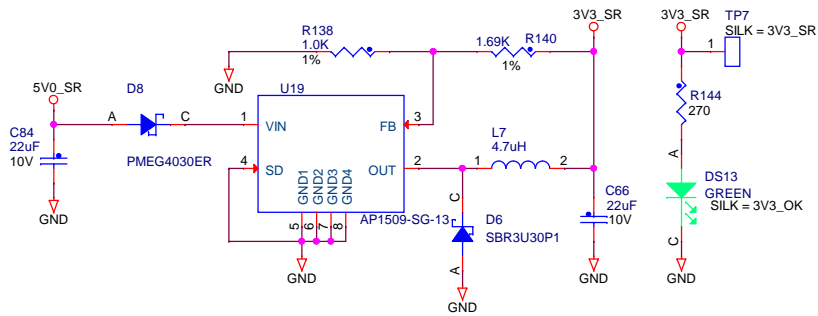


Test and reference points



3.3V Switching Regulator

Input Voltage 5V, Output 3.3V at 1600mA



Layout note: follow IC datasheet recommendations for PCB layout and thermal dissipation



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Drawing Title:

DEVKIT-MPC5748G

Page Title:

Power Input, 5V, 3.3V Reg

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Calypto MCU Power Connections

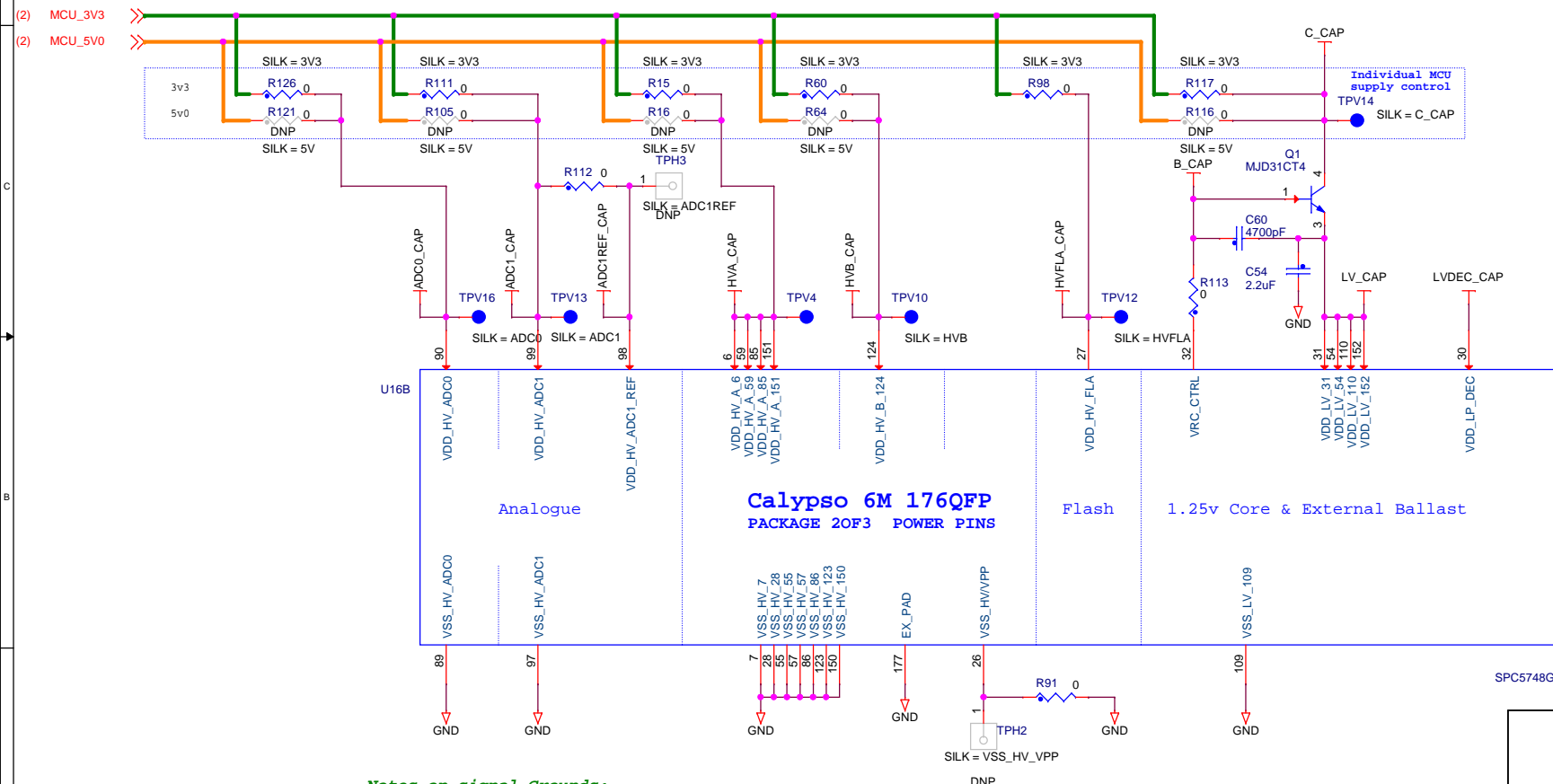
Power Supply Constraints:

- If VDD_HV_A is driven from 3.3V, VDD_HV_FL_A must also be supplied from 3.3V
- If VDD_HV_A is driven from 5V, the VDD_HV_FL_A pin must be disconnected from 3.3V
- Don't attempt to over drive an analogue pad to 5V when the digital VDD_HV_x supply is set to 3.3V. This will trigger the ESD protection on that pad. For example if VDD_HV_A is set to 3.3V and the analogue supplies are set to 5V, you cannot drive 5V into a pad in the VDD_HV_A domain

Default Configuration:

- ALL MCU supply voltages are set to 3.3V (ADC0, ADC1, VDD_HV_A, VDD_HV_B, VDD_HV_C, VBallast)
- VDD_HV_FL_A = External 3.3V supplied (jumper fitted)


The analogue pins can only be driven to the same voltage as the VDD_HV_x domain they are situated in (ie max 3.3V) so makes sense for the analogue supply and reference to be 3.3V



SPC5748GHK0AMKU6

Notes on signal Grounds:

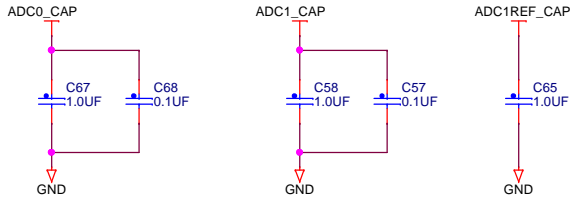
- The scheme shown has the analogue and digital grounds connected to the same plane
- This results in better ADC performance than using an analogue ground plane with single entry point (or ferrite) to digital ground plane.



ICAP Classification: CP: ___ IUC: X PUB: ___			
Drawing Title: DEVKIT-MPC5748G			
Page Title: Calypto MCU Power			
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Calypso MCU Decoupling and bulk storage

ADC

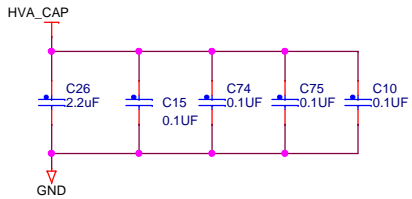


Place small Caps as close as possible to MCU pins

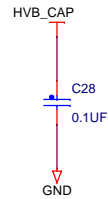
Flash



VDD_HVA

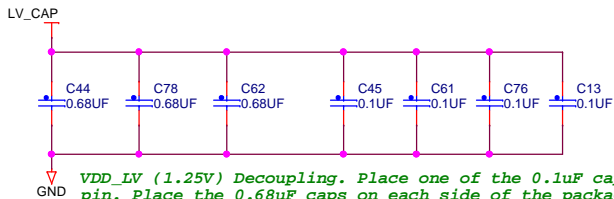


VDD_HVB



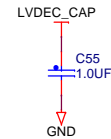
One 0.1uF cap per VDD_HV_x pin. Place as close as possible to pin

VDD_LV



VDD_LV (1.25V) Decoupling. Place one of the 0.1uF caps close to each VDD_LV pin. Place the 0.68uF caps on each side of the package such that there is no cap on the side with the ballast transistor
(For regulator stability the total capacitance should be around 2.2uF).

LP Internal Reg Cap



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Calypso MCU Decoupling

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Reset and External Clock In

Reset is in the VDD_HVA domain.

Reset Input / Output

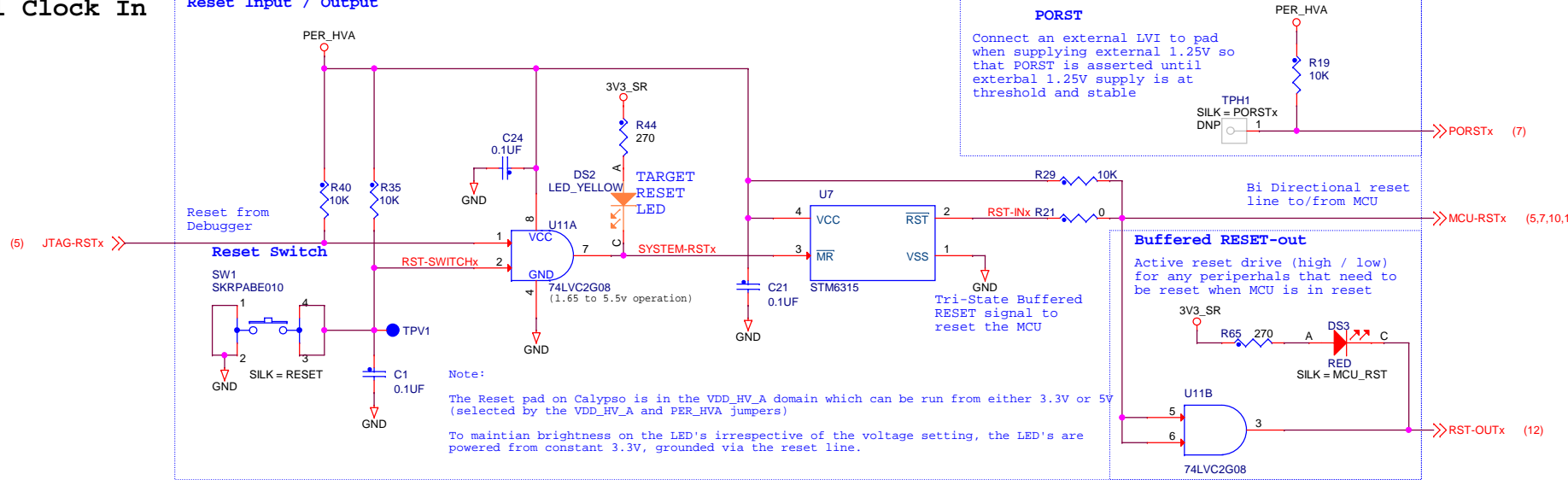
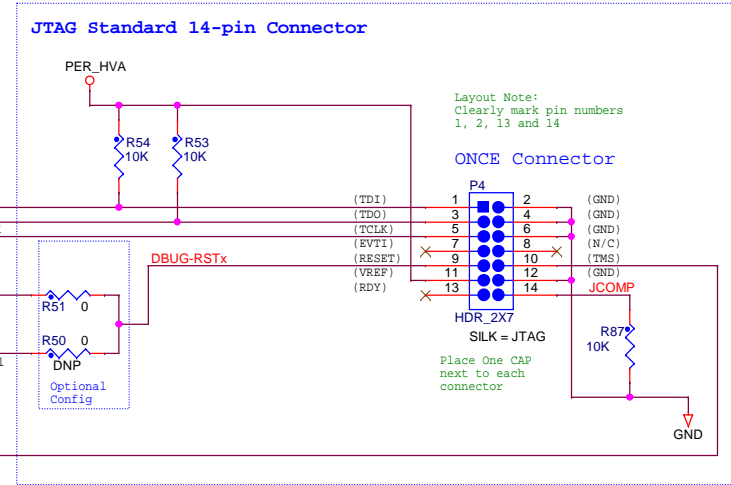



Table 13-3. Functional terminal state during power-up and reset

TERMINAL TYPE ¹	POWERUP pad state ²	RESET pad state	DEFAULT pad state ³	Comments
RESET	strong pull-down	strong pull-down	weak pull-up	functional reset pad.
PORST ⁴	Weak pull down	Weak pull up	weak pull-up	power on reset pad.
GPIO	high impedance	high impedance	high impedance	by default, but configurable for STANDBY exit
ANALOG	high impedance	high impedance	high impedance	-
EOUT0, EOUT1	high impedance	high impedance	high impedance	-
TCK	high impedance	weak pull-up	weak pull-up	-
TMS	high impedance	weak pull-up	weak pull-up	-
TDI	high impedance	weak pull-up	weak pull-up	-
TDO	high impedance	high impedance	high impedance	-
TCK_ALT	high impedance	weak pull-up	weak pull-up	-
TMS_ALT	high impedance	weak pull-up	weak pull-up	-
TDI_ALT	high impedance	weak pull-up	weak pull-up	-
TDO_ALT	high impedance	high impedance	high impedance	-





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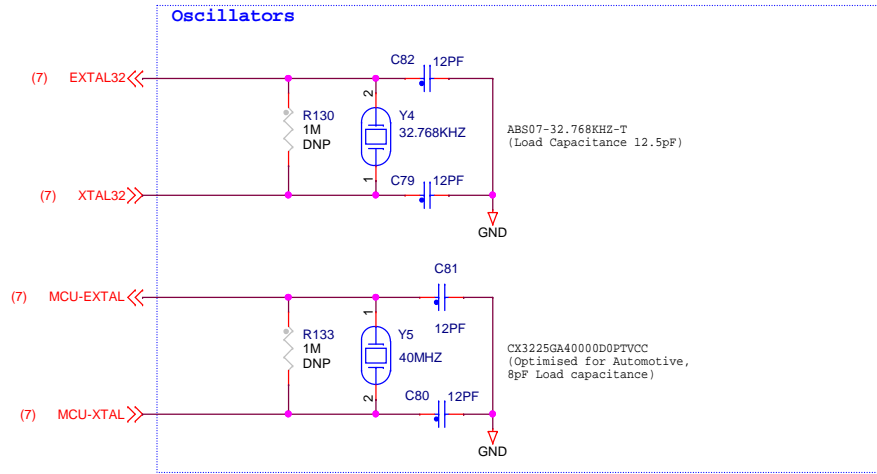
Drawing Title: **DEVKIT-MPC5748G**

Page Title: **Reset Circuitry & External Clock In, JTAG**

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Clocks




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Pin	Signal	Function	Pin	Signal	Function	
(14) PA0	(LEB2)	24	PA0/GPIO0/EUCL_0_XCLKOUT0/EUCL_13_HWKP19/CAN1RX	18	(GPIO)	PE0/GPIO6/EUCL_16_XSCL1/WKP6/CAN5RX/LIN1RX
(14) PA1	(GPIO)	19	PA1/GPIO1/EUCL_1_GWKP20/MDC0/CANRX	20	(GPIO)	PE1/GPIO7/EUCL_17_YCANSTX/S241
(14) PA2	(GPIO)	17	PA2/GPIO2/EUCL_2_GE2UC_0_XIADC0_MA2/WKP13	156	(PE_A_TX_EN)	PE2
(14) PA3	(LEB4)	51	PA3/GPIO3/EUCL_3_GLIN2TX/ACS4_1/ADC1_S0/EIRO0/M1_0_RX_CLK	157	(GPIO)	PE3
(14) PA4	(GPIO)	146	PA4/GPIO4/EUCL_4_GdCS0_1/E2UC_24_XWKP18/CMP1_13/LINRX/dSS_1	160	(GPIO)	PE4
(14) PA5	(GPIO)	147	PA5/GPIO5/EUCL_5_GLIN2TX/ULP10_STP	161	(GPIO)	PE5
(14) PA6	(LEB5)	128	PA6/GPIO6/EUCL_6_GdCS1_1/EIRO1/LINRX/ULP10_DIR	168	(GPIO)	PE6
(14) PA7	(LEB5)	129	PA7/GPIO7/EUCL_7_GLIN2TX/ADC1_S0/EIRO2/M1_0_RXD2	167	(GPIO)	PE7
(12) PA8	(SBI1_S0D1)	129	PA8/GPIO8/EUCL_8_X/EUCL_14_H/ADC1_S0/EIRO3/LINRX/M1_RMI_0_RXD1	21	(GPIO)	PE8
(14) PA10	(LEB3)	131	PA9/GPIO9/EUCL_9_HdCS2_1/ADC1_S10/M1_RMI_0_RXD0	22	(GPIO)	PE9
(12) PA11	(SBI1_S0D1)	132	PA10/GPIO10/EUCL_10_HSDA0/LIN2/M1_1_TXD1/ADC1_S11/SSIN_1/M1_0_COL	25	(GPIO)	PE10
(15) PA12	(GPIO)	52	PA11/GPIO11/EUCL_11_H/SCL0/M1_1_TXD0/ADC1_S12/EIRO16/LIN2RX/ULP10_FAULT/M1_RMI_0_RX_ER	23	(GPIO)	PE11
(15) PA13	(GPIO)	50	PA12/GPIO12/EUCL_28_YdCS0_1/E2UC_26_YCMP1_15/EIRO17/SSIN_0	133	(SBI1_CSB1)	PE12
(15) PA14	(GPIO)	50	PA13/GPIO13/HSOUT_0/EUCL_29_YE2UC_25_YCANTX/CMP1_14	127	(GPIO)	PE13
(15) PA15	(GPIO)	48	PA14/GPIO14/dSCLK_0/dCS0_0/EUCL_0_X/E2UC_23_XCMP1_12/EIRO4/dSS_0	136	(GPIO)	PE14
(15) PA15	(GPIO)	48	PA15/GPIO15/dCS0_0/dSCLK_0/EUCL_1_GE2UC_21_Y/WKP10/CMP1_10/CANRX/dSS_0	137	(SBI1_S1)	PE15
(9) PB0	(CAN0_TX)	39	PB0/GPIO16/CAN0TX/EUCL_30_Y/LIN2TX/E2UC_4_Y/CMP0_2	63	(GPIO)	PF0
(9) PB1	(CAN0_RX)	40	PB1/GPIO17/EUCL_31_YE2UC_5_Y/WKP4/CMP0_3/CANRX/LINRX	64	(GPIO)	PF1
(9) PB2	(GPIO)	176	PB2/GPIO18/LIN2TX/dSA0/EUCL_30_Y/SD_DAT7	65	(GPIO)	PF2
(9) PB3	(GPIO)	88	PB3/GPIO19/EUCL_31_Y/SCL0/E2UC_8_X/WKP11/LIN2RX/ULP10_FAULT	66	(GPIO)	PF3
(14,15) PB4	(ADC_VREF)	88	PB4/GPIO20/ADC1_P0	67	(GPIO)	PF4
(15) PB5	(GPIO)	92	PB5/GPIO21/ADC1_P1/M1_1_RX_DV	68	(GPIO)	PF5
(15) PB6	(GPIO)	93	PB6/GPIO22/ADC1_P2/M1_1_RXD3	69	(GPIO)	PF6
(15) PB7	(GPIO)	93	PB7/GPIO23/ADC1_P3/M1_1_RXD2	70	(GPIO)	PF7
(6) XTAL32		60	PB8/GPIO24/ADC0_S0/WKP25/dCS2K_XTAL	71	(GPIO)	PF8
(15) PB10	(GPIO)	62	PB8/GPIO25/ADC0_S1/WKP26/dCS2K_XTAL	72	(GPIO)	PF9
(15) PB11	(GPIO)	101	PB10/GPIO26/dSOUT_1/CAN3TX/CMP2_0/dSA0_SYNC/E2UC_29_Y/ADC0_S2/WKP8/CANRX	46	(GPIO)	PF10
(15) PB12	(GPIO)	103	PB11/GPIO27/EUCL_4_GdCS0_0/ADC0_S3/dSS_0/M1_1_RX_CLK	47	(GPIO)	PF11
(15) PB13	(GPIO)	103	PB12/GPIO28/EUCL_4_GdCS1_0/D01/ENET1_TMR0/ADC0_X0	48	(GPIO)	PF12
(15) PB14	(GPIO)	105	PB13/GPIO29/EUCL_5_GdCS2_0/ADC0_X1/M1_1_RX_DV	126	(SBI1_S0D1)	PF13
(15) PB15	(GPIO)	107	PB14/GPIO30/EUCL_6_GdCS3_0/FR_DBG1/ADC0_X2/M1_1_RXD2	125	(SBI1_CSB1)	PF14
(15) PB15	(GPIO)	107	PB15/GPIO31/EUCL_7_GdCS4_0/dLBSIG/ADC0_X3/M1_1_RXD0	125	(SBI1_CSB1)	PF15
(10) PC0	(TD1)	154	PC0/GPIO32/TD1	122	(SBI1_S0D1)	PG0
(5,10) PC1	(TD0)	148	PC1/GPIO33/TD0	121	(SBI1_S0D1)	PG1
(11) PC2	(SBI1_CSK)	145	PC2/GPIO34/dSCLK_1/CAN4TX/E2UC_22_Y/SSCM_DBG0/EIRO2/GULPH1_CLK	15	(GPIO)	PG2
(11) PC3	(SBI1_DSR)	144	PC3/GPIO35/dCS0_1/S0D1/WK/EUCL_23_X/SSCM_DBG1/EIRO3/CAN1RX/CANRX/ULP11_DIR/dSS_1	16	(GPIO)	PG3
(14) PC4	(LEB6)	159	PC4/GPIO36/EUCL_31_Y/FR_B_TX_EN/SD_DAT0/ULP10_D1/SSCM_DBG2/ERO18/CANRX/dSSN_1	14	(GPIO)	PG4
(15) PC5	(PE_A_TX)	159	PC5/GPIO37/HSOUT_1/CAN3TX/E2UC_24_X/FR_A_TX/dS_CLK/ULP10_D2/SSCM_DBG3/ERO7	13	(GPIO)	PG5
(15) PC6	(GPIO)	44	PC6/LIN1TX/EUCL_28_YE2UC_17_Y/SSCM_DBG4/CMP0_7	38	(GPIO)	PG6
(15) PC7	(GPIO)	45	PC7/GPIO38/EUCL_29_Y/CMP1_0/E2UC_18_Y/SSCM_DBG5/WKP12/LIN1RX	34	(GPIO)	PG7
(10) PC8	(SBI1_S1)	175	PC8/GPIO39/LIN2TX/EUCL_3_G/SD_DAT6/SSCM_DBG6	37	(GPIO)	PG8
(10) PC9	(SBI1_S1)	2	PC9/GPIO40/LIN2TX/EUCL_3_G/SD_DAT6/SSCM_DBG6	33	(GPIO)	PG9
(15) PC10	(GPIO)	36	PC10/GPIO41/EUCL_7_GE2UC_7_Y/SSCM_DBG7/WKP13/LIN2RX/ULP11_FAULT	138	(SBI1_S1)	PG10
(15) PC11	(GPIO)	35	PC10/GPIO42/CAN1TX/CAN4TX/ADC0_MAI/CMP0_0/LIN2TX	139	(SBI1_S1)	PG10
(15) PC12	(FR_DBG0)	173	PC11/GPIO43/ADC0_MAI/E2UC_1_Y/WKP5/CAN1RX/CANRX	116	(GPIO)	PG11
(15) PC13	(FR_DBG0)	174	PC12/GPIO44/EUCL_12_H/FR_DBG0/SD_DAT4/ERO18/dSSIN_2	115	(GPIO)	PG12
(15) PC14	(FR_DBG0)	3	PC13/GPIO45/EUCL_13_HdSOUT_2/FR_DBG1/SD_DAT5	134	(SBI1_S0)	PG13
(15) PC15	(FR_DBG0)	4	PC14/GPIO46/EUCL_14_HdSCLK_2/E2UC_5_Y/FR_DBG2/CAN4TX/EIRO8	135	(SBI1_S1)	PG14
(15) PC15	(FR_DBG0)	4	PC15/GPIO47/EUCL_15_HdCS0_2/E2UC_5_Y/FR_DBG3/ERO20/dSS_2/CANRX	135	(SBI1_S1)	PG15
(15) PD0	(GPIO)	77	PD0/GPIO48/ADC1_P4/WKP127	117	(SBI1_S0D1)	PH0
(15) PD1	(GPIO)	78	PD1/GPIO49/ADC1_P5/WKP128	118	(SBI1_S0D1)	PH1
(15) PD2	(GPIO)	79	PD2/GPIO50/ADC1_P6	119	(SBI1_S0D1)	PH2
(15) PD3	(GPIO)	80	PD3/GPIO51/ADC1_P7	120	(GPIO)	PH3
(15) PD4	(GPIO)	81	PD4/GPIO52/ADC1_P8	162	(GPIO)	PH4
(15) PD5	(GPIO)	82	PD5/GPIO53/ADC1_P9	163	(LEB8)	PH5
(15) PD6	(GPIO)	83	PD6/GPIO54/ADC1_P10	164	(GPIO)	PH6
(15) PD7	(GPIO)	84	PD7/GPIO55/ADC1_P11	165	(GPIO)	PH7
(15) PD8	(GPIO)	87	PD8/GPIO56/ADC1_P12	166	(GPIO_SBI)	PH8
(15) PD9	(GPIO)	94	PD9/GPIO57/ADC1_P13/M1_1_RXD1	155	(TX)	PH9
(15) PD10	(GPIO)	95	PD10/GPIO58/ADC1_P14/M1_1_RXD0	148	(TX)	PH10
(15) PD10	(GPIO)	100	PD10/GPIO59/dCS0_0/EUCL_24_X/D00/ENET1_TMR1/ADC0_S4	140	(SBI1_S0)	PH11
(15) PD11	(GPIO)	102	PD11/GPIO60/dCS0_1/EUCL_25_Y/ENET0_TMR0/ADC0_S5/dSS_1	141	(SBI1_S0)	PH12
(15) PD12	(GPIO)	104	PD12/GPIO61/dCS0_1/EUCL_26_Y/ENET0_TMR0/ADC0_S6/dSS_1	9	(LEB7)	PH13
(15) PD13	(GPIO)	104	PD13/GPIO62/dCS0_1/EUCL_26_Y/FR_DBG0/ADC0_S6/M1_1_RXD3	10	PH14	PH14
(15) PD14	(GPIO)	106	PD14/GPIO63/dCS2_1/EUCL_27_Y/FR_DBG1/MLBDAT/ADC0_S7/M1_1_RXD1	8	PH15	PH15
(5,10,15) MCU-Rstx	RESET	29				
(5) PORStx	PORST	153				
(6) MCU-XTAL	XTAL	56				
(6) MCU-EXTAL	EXTAL	56				

Calypso 176QFP
PACKAGE IOP3 GPIO PINS1

Key to text colours:
purple - Core Physical Interfaces
orange - Other Peripherals and I/O
blue - Debug (JTAG & Reset)
black - Clock, Reset and Control
red - I/O Matrix and other functions (eg LED)
green - I/O Matrix (dedicated)

SPC5748GH00AMK06



ICAP Classification: CP IUC X PUB:
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Key to text colours:
 Purple - Comms Physical Interfaces
 Orange - Other Peripherals and I/O
 Blue - Debug (JTAG & Nexus)
 Black - Clock, Reset and Control
 RED - I/O Matrix and other functions (eg LED)
 Green - I/O Matrix (dedicated)

(14,15)	P10	<<<	(GPIO)	P10	172
(14,15)	P11	<<<	(GPIO)	P11	171
(14,15)	P12	<<<	(GPIO)	P12	170
(14,15)	P13	<<<	(GPIO)	P13	169
(14,15)	P14	<<<	(USB1_STP)	P14	143
(11)	P15	<<<	(USB1_NXT)	P15	142
(15)	P16	<<<	(GPIO)	P16	11
(11,15)	P17	<<<	(USB1_RST)	P17	12
(15)	P18	<<<	(GPIO)	P18	108
(12,15)	PI11	<<<	(ENET_RST)	PI11	111
(15)	PI12	<<<	(GPIO)	PI12	112
(15)	PI13	<<<	(GPIO)	PI13	113
(15)	PI14	<<<	(GPIO)	PI14	76
(15)	PI15	<<<	(GPIO)	PI15	75
(15)	PJ0	<<<	(GPIO)		74
(15)	PJ1	<<<	(GPIO)		73
(15)	PJ2	<<<	(GPIO)		72
(15)	PJ3	<<<	(GPIO)		71
(14)	PJ4	<<<	(LED1)		5

U16C

PI0/GPIO128/E0UC_28_Y/LIN8TX/SDA1/SD_DAT3	
PI1/GPIO129/E0UC_29_Y/SCL1/SD_DAT2/WKPU24/LIN8RX	
PI2/GPIO130/E0UC_30_Y/LIN9TX/SDA2/SD_DAT1	
PI3/GPIO131/E0UC_31_Y/SCL2/SD_DAT0/WKPU23/LIN9RX	
PI4/GPIO132/E1UC_28_Y/SCOUT_0/ULP11_STP	
PI5/GPIO133/E1UC_29_Y/SCLK_0/CS2_1/CS2_2/ULP11_NXT	
PI6/GPIO134/E1UC_30_Y/CS0_0/CS0_1/CS0_2/DO0/SS_0/SS_1/SS_2	
PI7/GPIO135/E1UC_31_Y/CS1_0/CS1_1/CS1_2/DO1	
PI8/GPIO136/E2UC_15_Y/ADC0_S16/MLBCLK/MIL1_RX_CLK	
PI11/GPIO139/E2UC_14_Y/ENET0_TMR1/ADC0_S19/dSIN_3	
PI12/GPIO140/dCS0_3/dCS0_2/MIL1_TX_EN/ADC0_S20/dSS_2/dSS_3	
PI13/GPIO141/dCS1_3/dCS1_2/MIL1_TXD3/ADC0_S21	
PI14/GPIO142/SAI2_D0/ADC0_S22/SIN_0	
PI15/GPIO143/CS0_0/dCS2_2/SAI2_MCLK/ADC0_S23/SS_0	
PJ0/GPIO144/CS1_0/dCS3_2/SAI2_SYNC/E2UC_19_Y/ADC0_S24	
PJ1/GPIO145/SOUT_0/SAI2_BCLK/ADC0_S25/SIN_1	
PJ2/GPIO146/CS0_1/CS0_2/CS0_3/SAI1_D0/ADC0_S26/SS_1/SS_2/SS_3	
PJ3/GPIO147/CS1_1/CS1_2/CS1_3/SAI1_BCLK/ADC0_S27	
PJ4/GPIO148/SCLK_1/E1UC_18_Y/E2UC_4_Y/EIN_ERR	

Calypso 176QFP

PACKAGE 30F3 GPIO PINS2

SPC5748GHK0AMKU6



ICAP Classification: CP: ___ IUC: X PUB: ___

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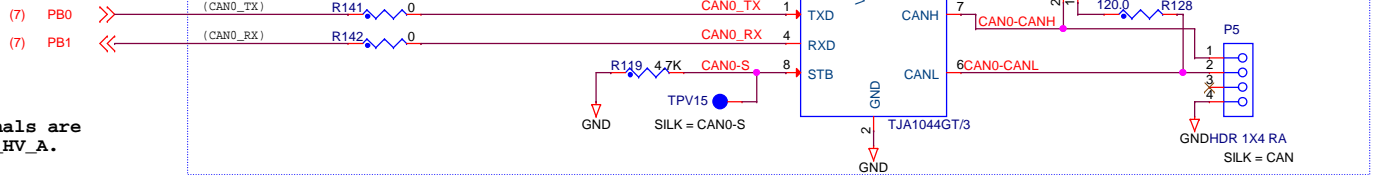
Date: Tuesday, April 03, 2018 Sheet 8 of 15

CAN & LIN Physical

CAN0 Physical Interface

VDD - 5.0V input supply for CAN transceiver (4.5 to 5.5V)
 VI/O - determines the signal level on MCU TX and RX pins and can range from 2.8 to 5.5V
 STB - High for Standby mode, pulled low for normal mode.

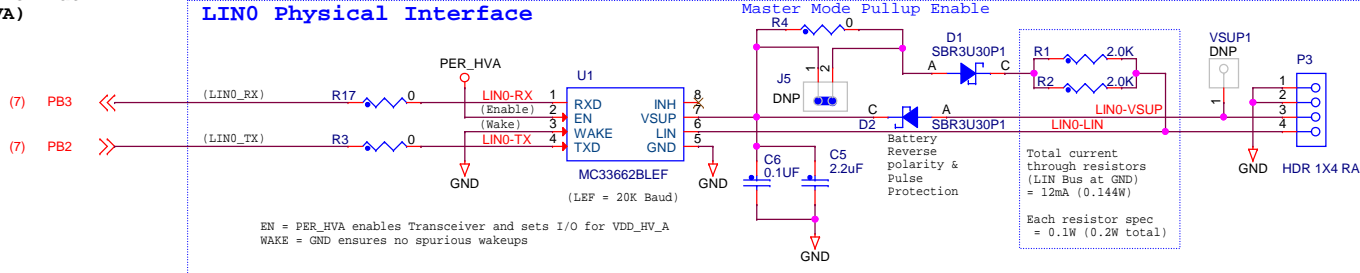
312-80788- MC33901WEF -> SO8_1P27_4X5
 IC INTERFACE CAN HS 60KB/S-1MB/S 4.5-5.5V SOIC8
 Replaced with TJA1044GT/3



All CAN and LIN signals are in power domain VDD_HV_A.

All interfaces will work at 3.3V or 5.0V (PER_HVA)

LINO Physical Interface



EN = PER_HVA enables Transceiver and sets I/O for VDD_HV_A
 WAKE = GND ensures no spurious wakeups

MC33662LEF LIN transceiver is newer version of 33661 offering:

- Full LIN compliance (33661 no longer compliant)
- Improved ESD protection on LIN pin up to 15KV
- Improved ESD on Wake and VSUP Pins
- Other EMC and performance improvements

See freescale.com for more details



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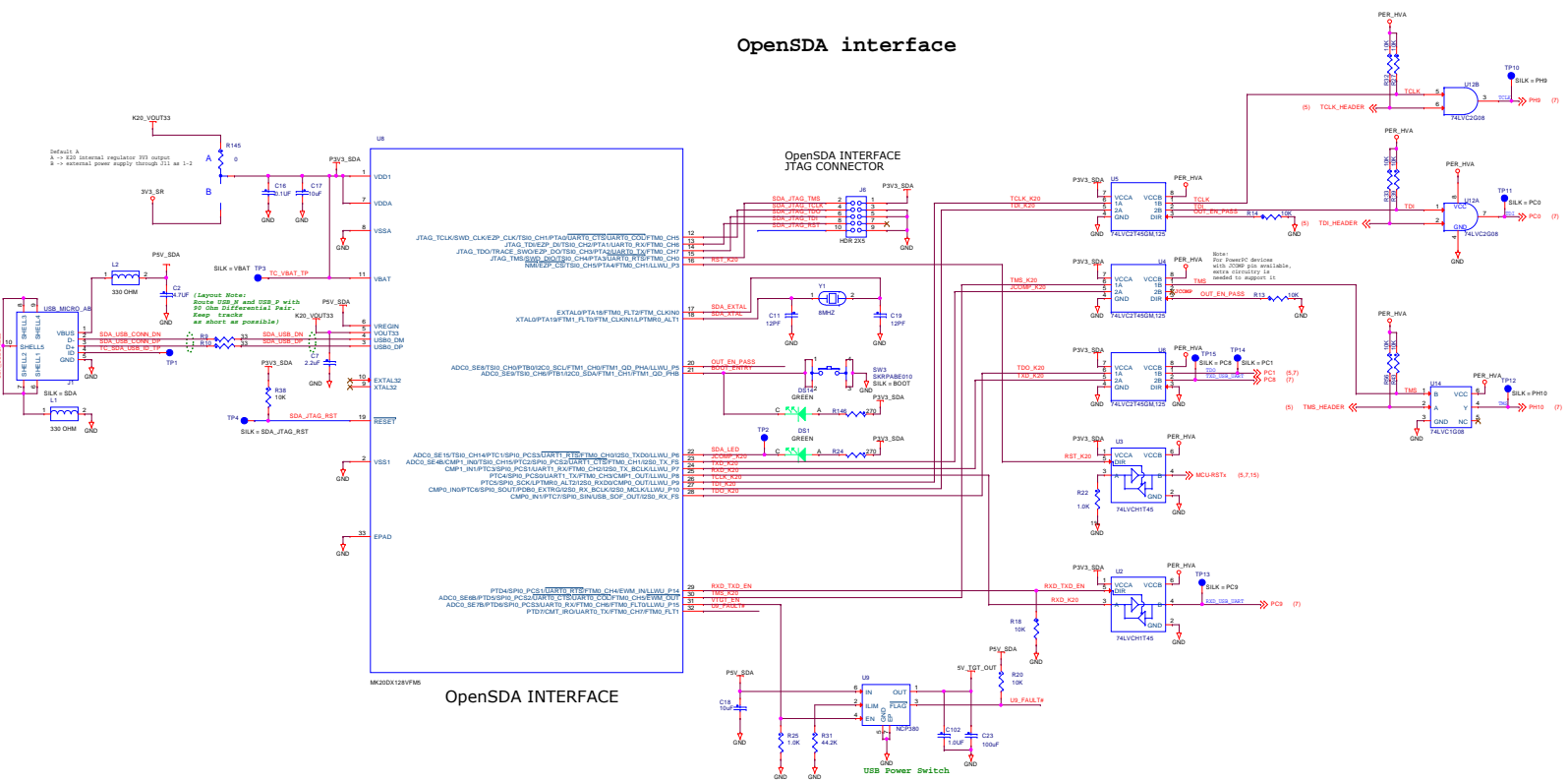
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CAN and LIN

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OpenSDA interface

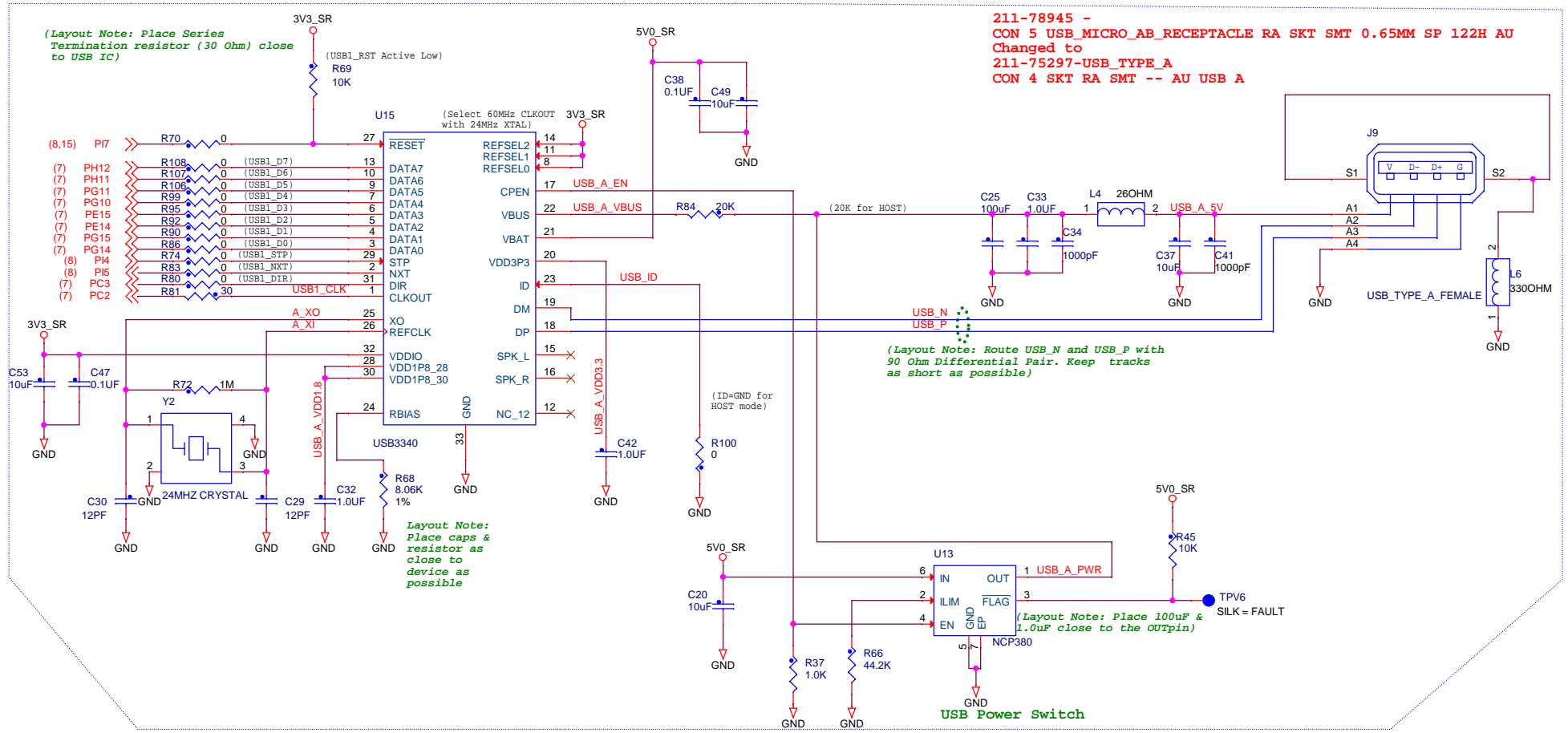



OpenSDA INTERFACE

USB (Type A Host and Type AB OTG)

USB Signals are in power domain VDD_HV_A

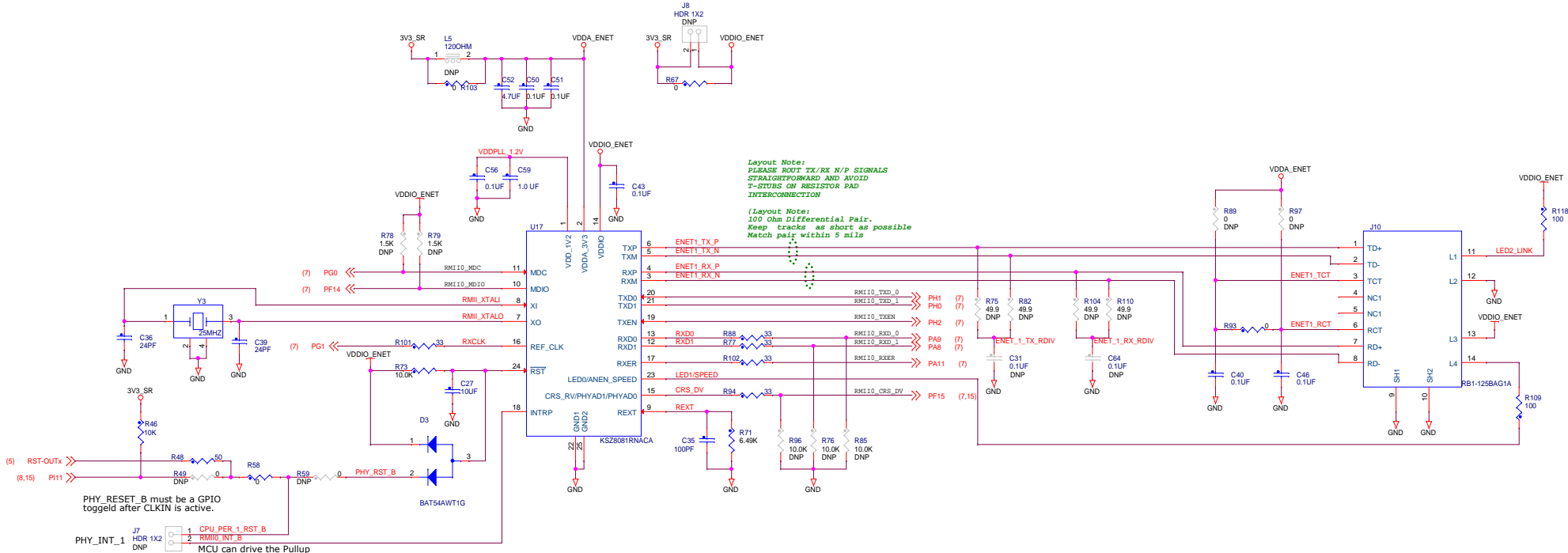
The USB interface only supports 3.3V operation. All I/O signals must be 3.3V. If VDD_HVA is set to 5V, USB MCU pads must be left as tri-state with no pullups or series resistors to be removed





ICAP Classification: CP: _____ IUO: X PUB: _____			
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Page Title: USB Type A / Type AB			
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Ethernet Physical Interface



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Drawing Title: DEVKIT-MPC5748G	
Page Title: Ethernet	
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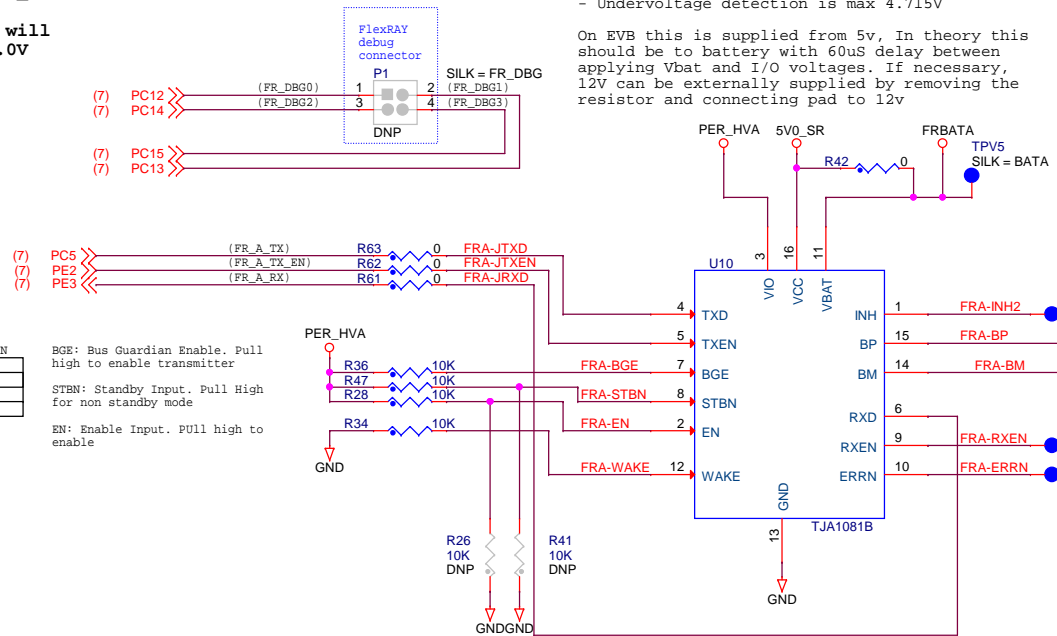
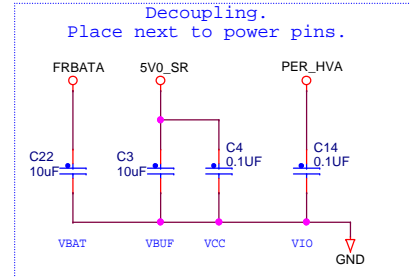
FlexRAY Physical Interface

All Signals are in power domain VDD_HV_A.

FlexRAY interface will work at 3.3V or 5.0V (PER_HVA)

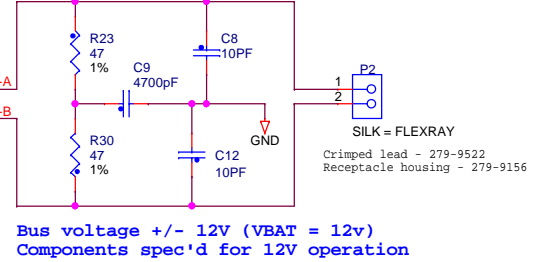
Note on VBAT:
 - Operational range is 4.45V to 60V
 - Undervoltage detection is max 4.715V


On EVB this is supplied from 5v, In theory this should be to battery with 60uS delay between applying Vbat and I/O voltages. If necessary, 12V can be externally supplied by removing the resistor and connecting pad to 12v



MODE	EN	STBN
Normal	1	1
Rec Only	0	1
Go to Sleep	1	0
Sleep	0	0

BGE: Bus Guardian Enable. Pull high to enable transmitter
 STBN: Standby Input. Pull High for non standby mode
 EN: Enable Input. Pull high to enable



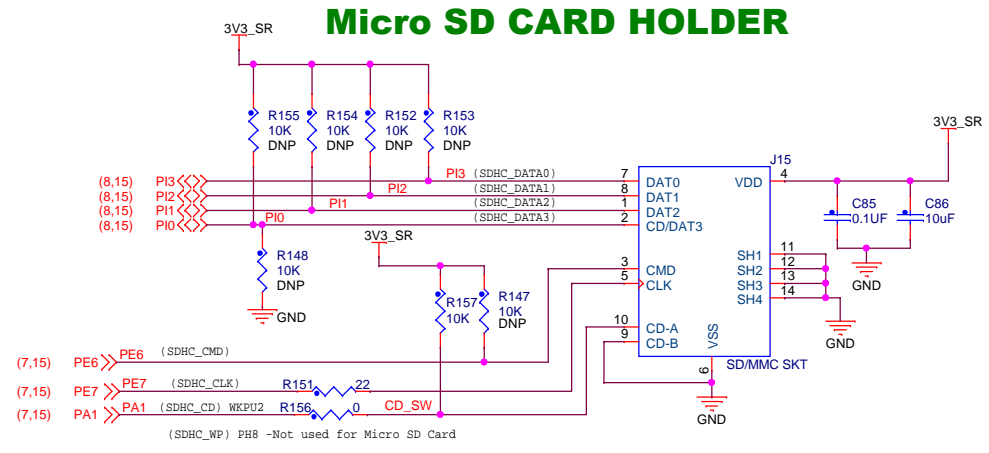
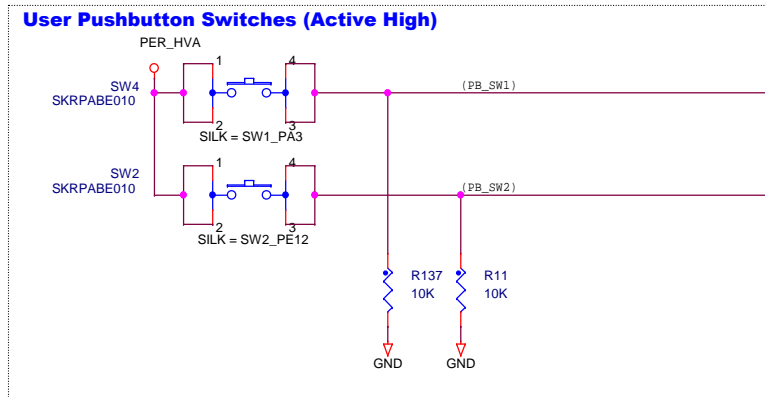
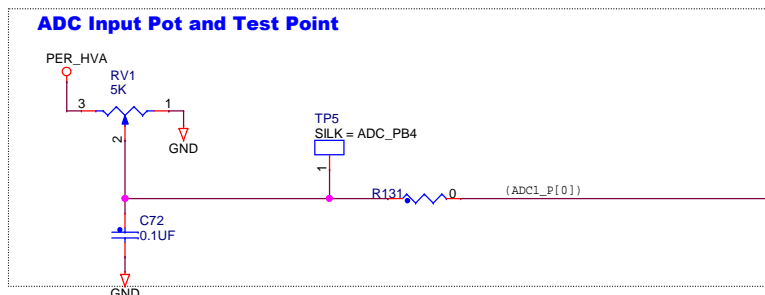
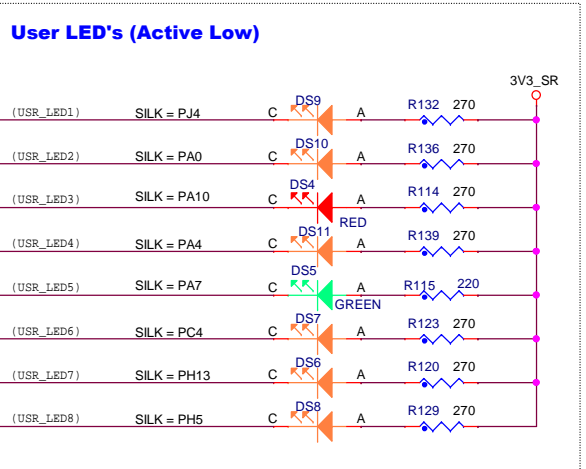


ICAP Classification: CP: ___ IUC: X PUB: ___
 Drawing Title: **DEVKIT-MPC5748G**
 Page Title: **FlexRAY Physical Interface**

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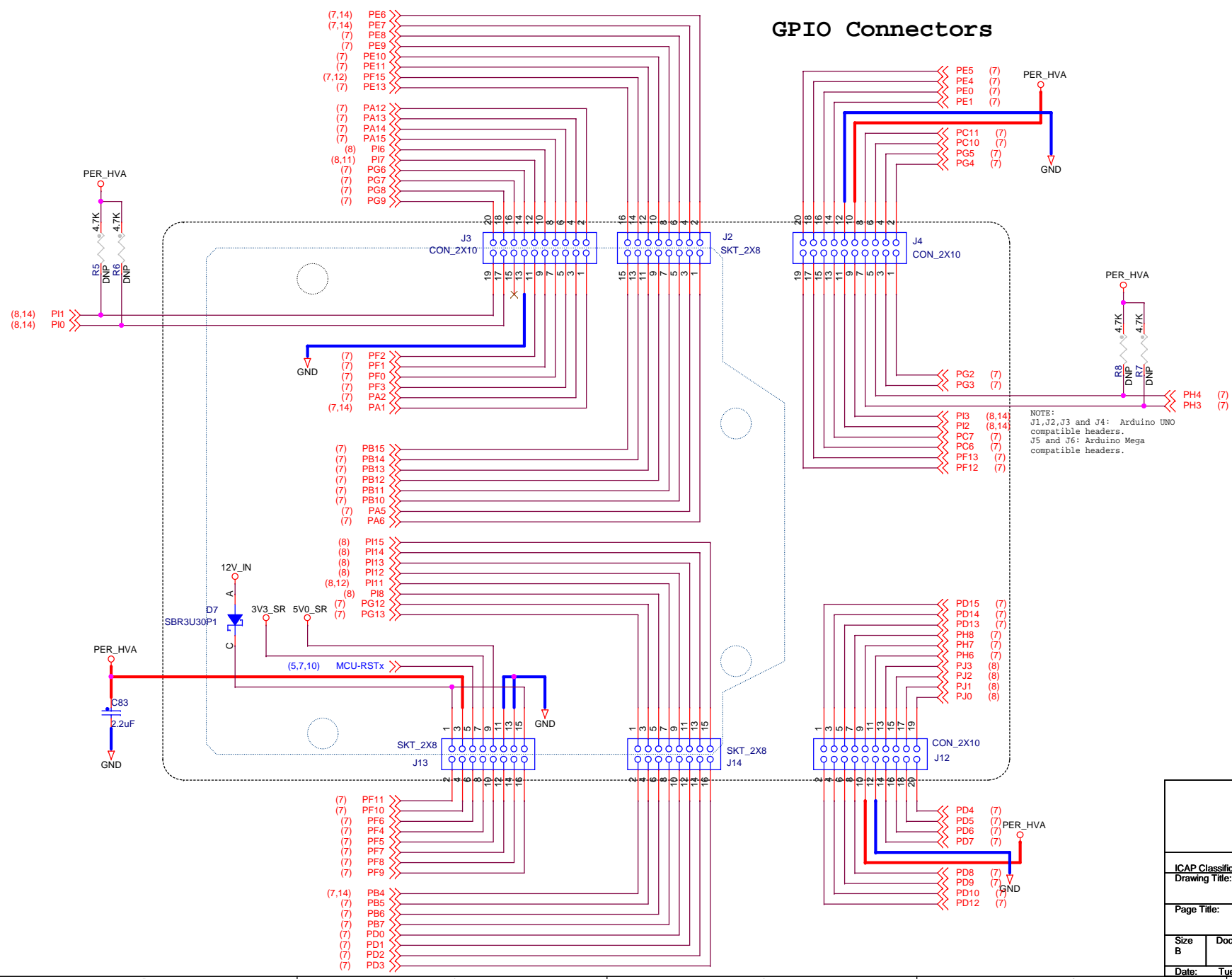
User Peripherals (Led's, Switches and ADC Pot)

Switches are hard wired to 3.3V rather than 5V so it's not possible to drive 5V into a 3.3V pad (which would cause damage)
 Similarly, the LED's are active low with 3.3v supply so can be safely coupled to pads on either 3.3V or 5V domains
 The ADC input is limited to 3.3V, again to prevent driving 5V into a 3.3V pad which would cause damage



ICAP Classification: CP: ___ IUO: X PUBt: ___			
Drawing Title: DEVKIT-MPC5748G			
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GPIO Connectors



NOTE:
 J1, J2, J3 and J4: Arduino UNO compatible headers.
 J5 and J6: Arduino Mega compatible headers.



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Drawing Title: DEVKIT-MPC5748G			
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