DEVKIT-MPC5744P

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Revision Information

Rev	Date	Designer	Comments
X1	6 July 2016	Jun Qiao	Initial
X2	12 July 2016	Jun Qiao	Update MCU decoupling, add boot section
X3	19 July 2016	Jun Qiao	Update MCU decoupling, update notes, rename nets
A	22 July 2016	Jun Qiao	Update J13 setting, update power to RV1, update notes
A1	26 Aug 2016	Jun Qiao	Update FRDM+ connection compatible to DEVKIT-MOTORGF
A2	5 Sept 2016	Jun Qiao	Add test points
A3	7 Sept 2016	Jun Qiao	Change U15 to NX5P2190UKZ, change R57 to 100K
A4	9 Sept 2016	Jun Qiao	Remove D8, add J39
A5	13 Sept 2016	Jun Qiao	Set power net 12V_IN at U1 pin 1, add R88
A6	20 Sept 2016	Jun Qiao	Change R56 from 10K to 20K, and connected to P3V3_SDA
A7	23 Sept 2016	Jun Qiao	Change U15 to MIC2005-0.8YM6, remove R57, change R56 to 10K, add C87.
B	28 Sept 2016	Jun Qiao	Release
B1	19 May 2017	Jun Qiao	Change R17 to 1K, add U30
C	2 June 2017	Jun Qiao	Release
CX1	1 Sept 2017	Jun Qiao	Add J40 and J41
D	8 Sept 2017	Jun Qiao	Release
E			

Notes:

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- All components and board processes are to be ROHS compliant
- All capacitors are 10% tolerance unless otherwise stated
- All resistors are 5% tolerance unless otherwise stated
- All zero ohm links are 0603
- All connectors and headers are denoted Px and are
  2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics.
  For 3 way jumpers, default is always posn 1-2
  2 Pin jumpers generally have the "source" on pin 1
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

 3 Different test points used in design:

 TPVx - Through Hole Pad small

 TPHx - Through Hile Pad Large (for standard 0.1" header).
 Also used on IO Matrix (IOMx)

 TPX  - Surface Mount Wire Loop
```

TPV?

1 TPH5

1 TP?

User notes are given throughtout the schematics.

Specific PCB LAYOUT notes are detailed in ITALICS

Caution:
These schematics are provided for reference purposes only. As such, NXP does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the NXP Calypso family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

Power & Ground Nets

EXTERNALLY SUPPLIED POWER

EXT_PWR	12V	External power supplied through the barrel connector to the System Basis Chip (SBC) - MC33FS6522LAE

SYSTEM BASIS CHIP (SBC) POWER NETS

VSUP3	12V	Power into the pre-regulator switching regulator in the SBC
V_PRE	6.5V	Power out of the pre-regulator switching regulator in the SBC
SB_VCORE	3.3V	Power out of the core switching regulator in the SBC
SB_VAUX	5V	Power out of the VAUX linear regulator in the SBC
SB_VCCA	3.3V	Power out of the VCCA linear regulator in the SBC
SB_VCAN	5V	Power out of the CAN linear regulator in the SBC

POWER TO THE MCU

VDD_LV_CORE	1.25V	Power to the core logic on the MCU
VDD_LV_PLL	1.25V	Power to the pll circuit on the MCU
VDD_HV_PMU	3.3V	Power to the pmu circuit on the MCU
VDD_HV_IO	3.3V	Power to the I/O circuits on the MCU
VDD_HV_OSC	3.3V	Power to the oscillator circuit on the MCU
VDD_HV_FLA	3.3V	Power to the flash memory circuit on the MCU
VDD_HV_ADV	3.3V	Power to the ADC circuit on the MCU
VDD_HV_ARE0	3.3V	Reference voltage to the ADC0 circuit on the MCU
VDD_HV_ARE1	3.3V	Reference voltage to the ADC1 circuit on the MCU

GROUND NETS

GND	0V

Automotive Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: PUBI: X

Designer: Jun Qiao	Drawing Title: DEVKIT-MPC5744P		
Drawn by: Jun Qiao	Page Title: Index, Rev, Notes		
Approved: Pesses Philip	Size C	Document Number SCH-29333 PDF: SPF-29333	Rev E
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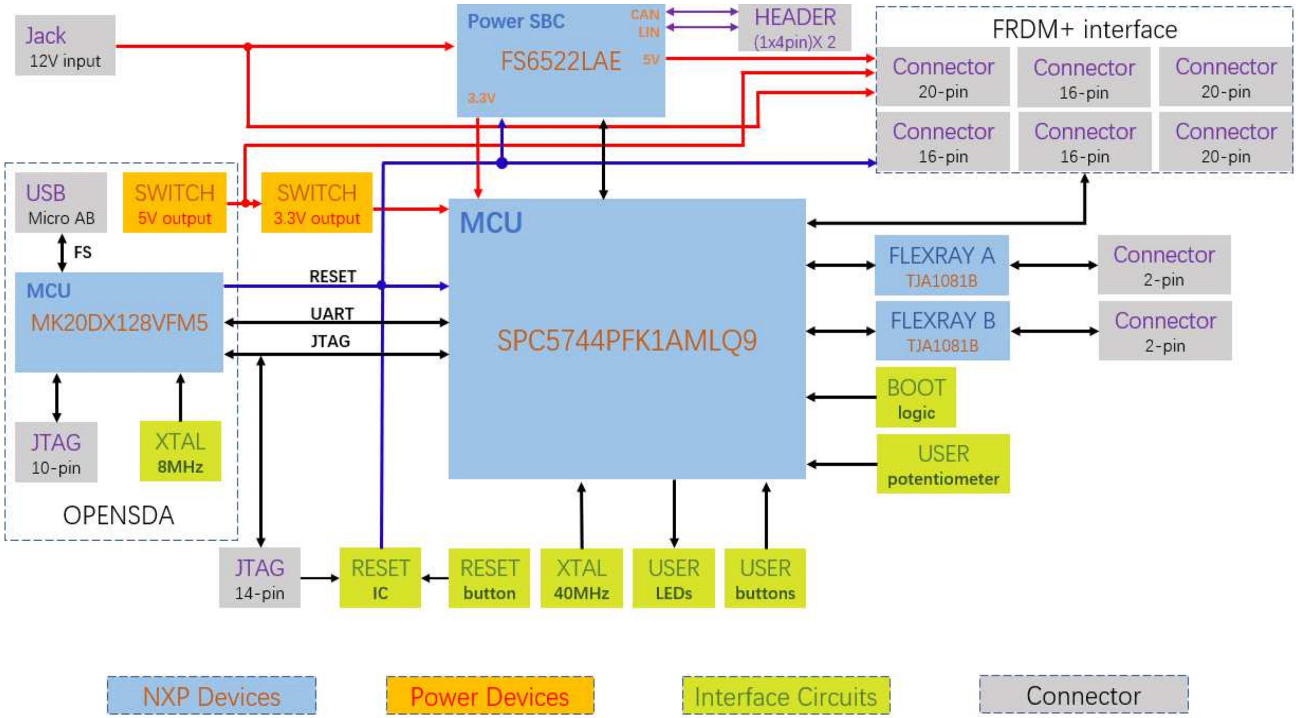
Block Diagram



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Drawing Title: DEVKIT-MPC5744P
Page Title: Block Diagram
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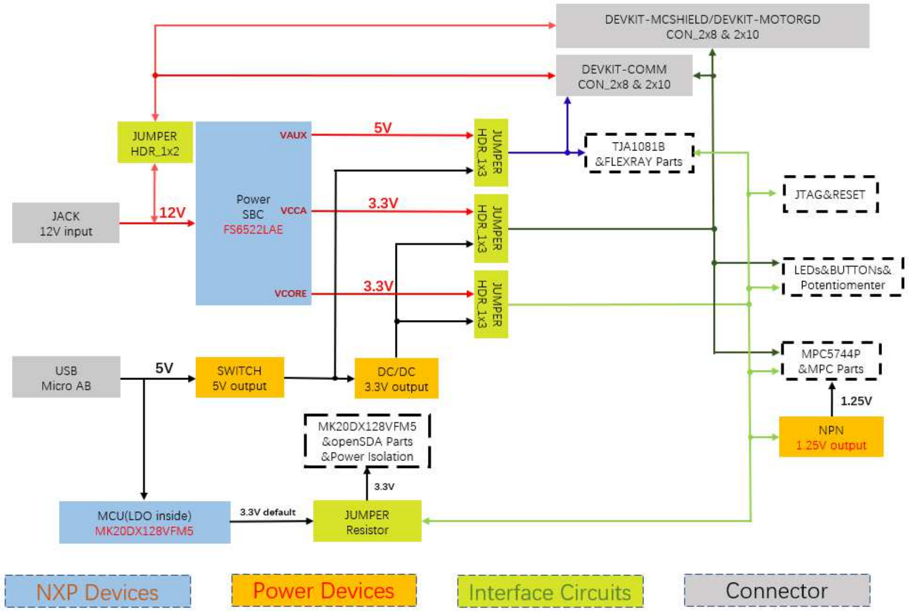
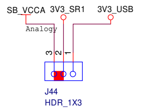
Board Power Block

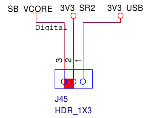


Board supply selection



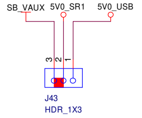
1-2 -> SBC Power Supply for analogy circuit

2-3 -> USB/UART Power Spply for analogy circuit



1-2 -> SBC Power Supply for digital circuit

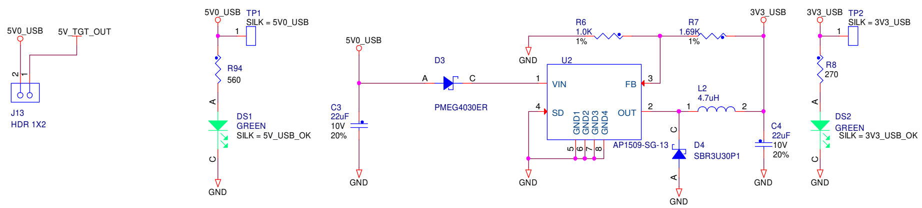
2-3 -> USB/UART Power Spply for digital circuit



1-2 -> SBC Power Supply for Devkit Comm and Flexray

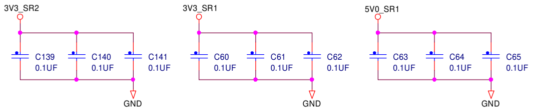
2-3 -> USB/UART Power Spply for Devkit Comm

USB Power Supply Connection   3.3V Switching Regulator with USB Power Supply



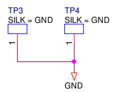
Layout note: follow IC datasheet recommandations for PCB layout and thermal dissipation

3.3V & 5V Power Decoupling



Layout note: Decoupling distributed uniformly

Test and reference points



Layout note: GND Test Points, Top Side

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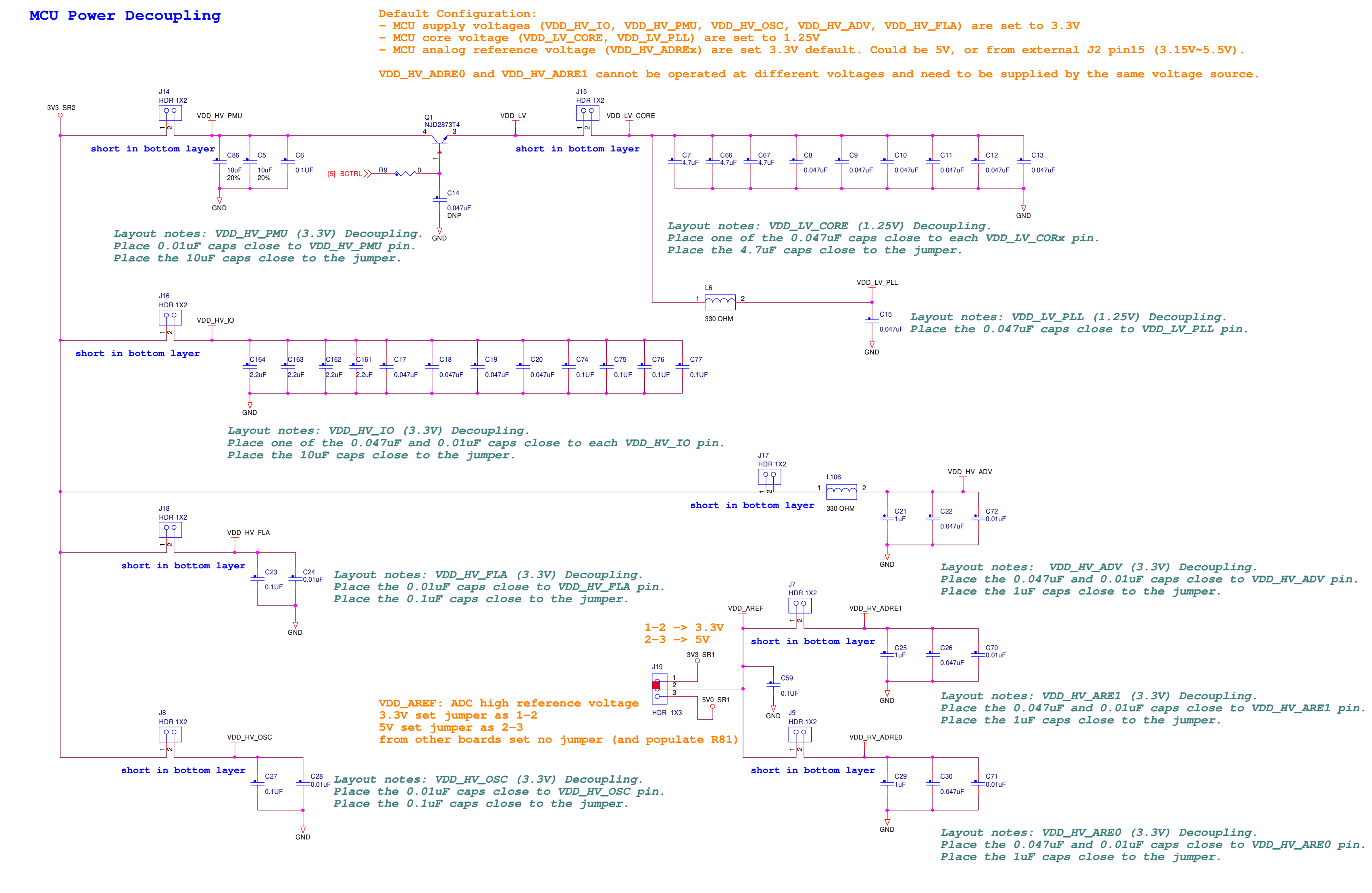
MCU Power



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Drawing Title: DEVKIT-MPC5744P

Page Title: MCU Power

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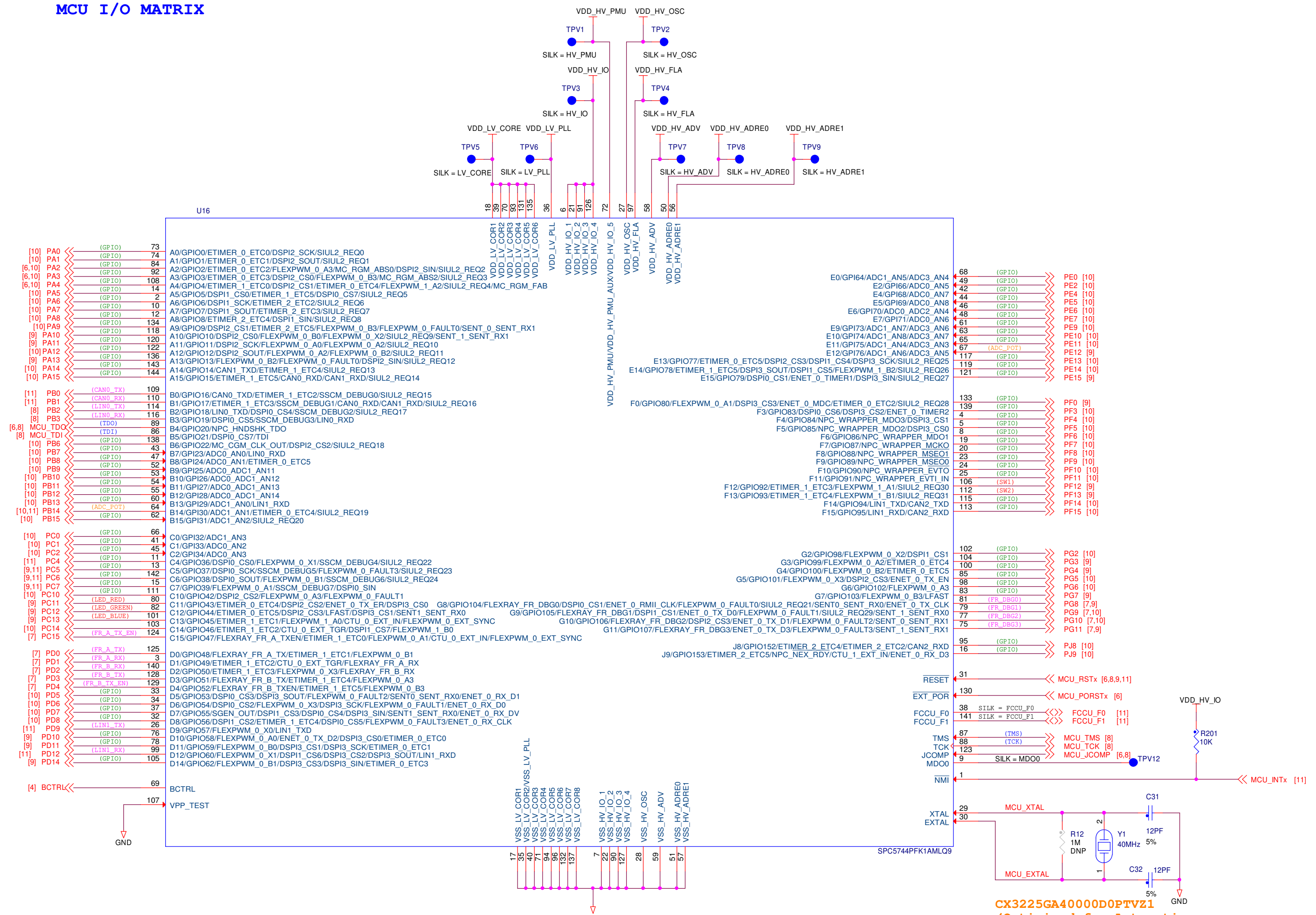
MCU Pins

MCU I/O MATRIX



Layout notes on signal Grounds:

- The scheme shown has the analogue and digital grounds connected to the same plane
- This results in better ADC performance than using an analogue grond plane with single entry point (or ferrite) to digital ground plane.

Key to text colours:

Purple - Comms Physical Interfaces
Orange - Other Peripherals and I/O
Blue - Debug (JTAG & Nexus)
Black - Clock, Reset and Control
RED - I/O Matrix and other functions (eg. LED, BUTTON)
Green - I/O Matrix (dedicated)

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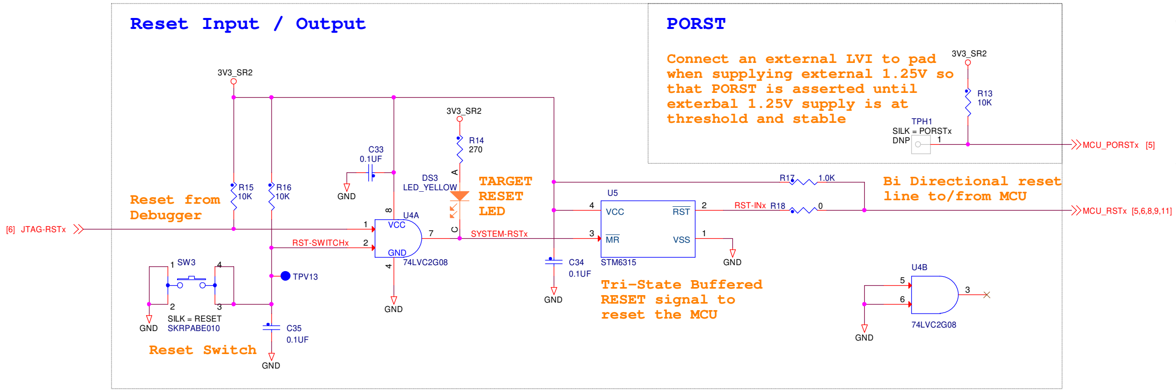
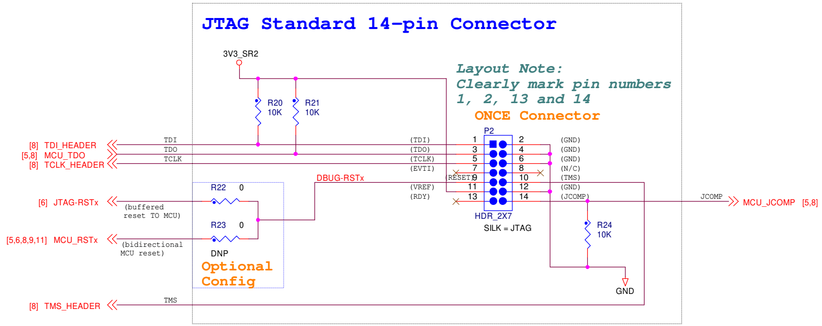
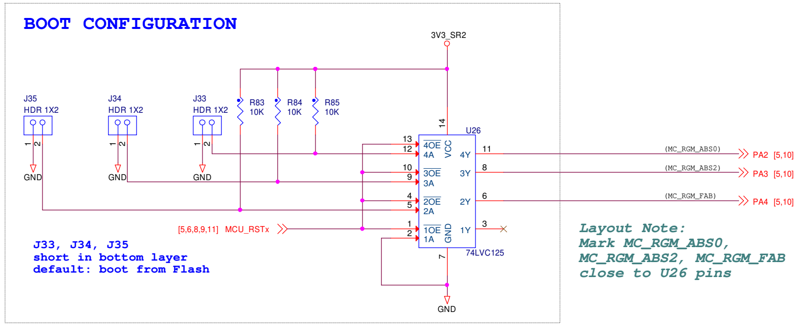
Boot, Reset & JTAG



Pin/ball startup and reset states

Pin/ball	Startup state	State during reset	State after reset
GPIOs	hi-z	hi-z	hi-z
Analog inputs	hi-z	hi-z	hi-z
JCOMP (TRST)	hi-z	input, weak pull-down	input, weak pull-down
TDI	hi-z	input, weak pull-up	input, weak pull-up
TDO	hi-z	output, hi-z	output, hi-z
TMS	hi-z	input, weak pull-up	input, weak pull-up
TCK	hi-z	input, weak pull-up	input, weak pull-up
XTAL/EXTAL	hi-z	hi-z	hi-z
FCCU_F[0]	hi-z	input, hi-z	output/input, hi-z
FCCU_F[1]	hi-z	input, hi-z	output/input, hi-z
EXT_POR_B	hi-z	input, weak pull-down	input, weak pull-down
RESET_B	hi-z	input, weak pull-down	input, weak pull-down
NMI_B	hi-z	input, weak pull-up	input,weak pull-up
FAB	hi-z	input, weak pull-down	input, weak pull-down
ABS[2]	hi-z	input, weak pull-down	input, weak pull-down
ABS[0]	hi-z	input, weak pull-down	input, weak pull-down





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Page Title: **Boot, Reset & JTAG**

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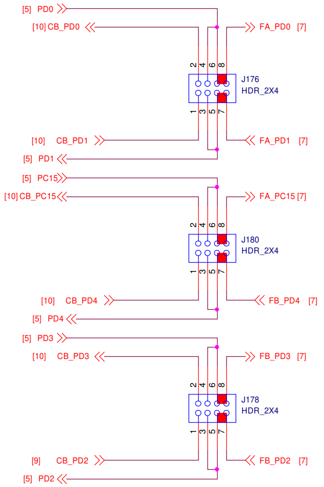
Flexray_A, Flexray_B

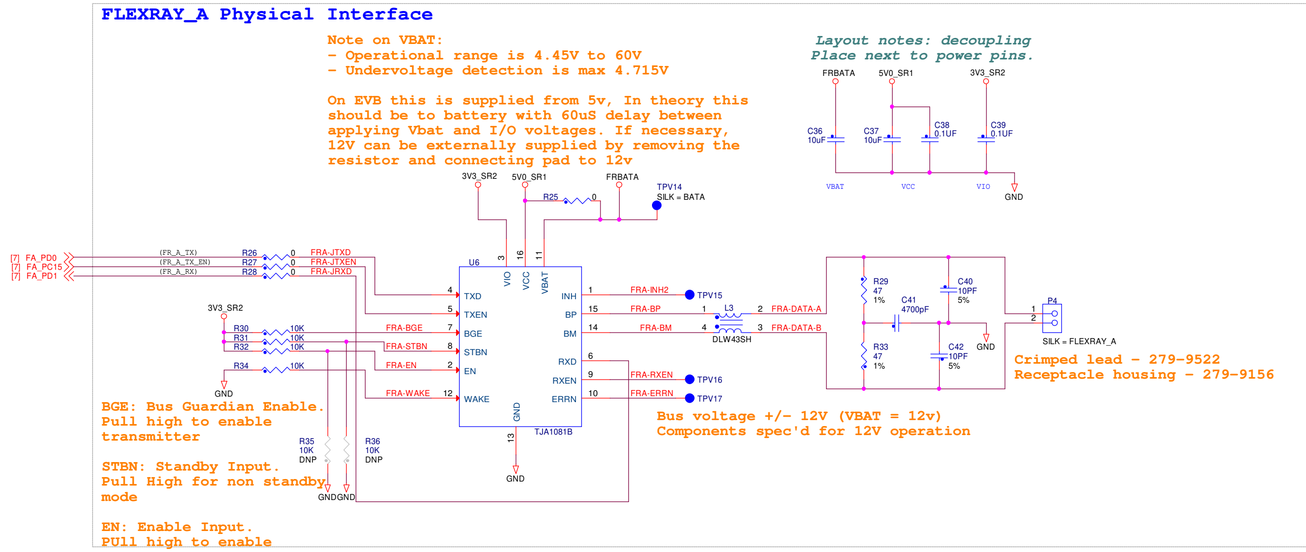
State transitions forced by EN and STBN

→ indicates the action that initiates a transaction

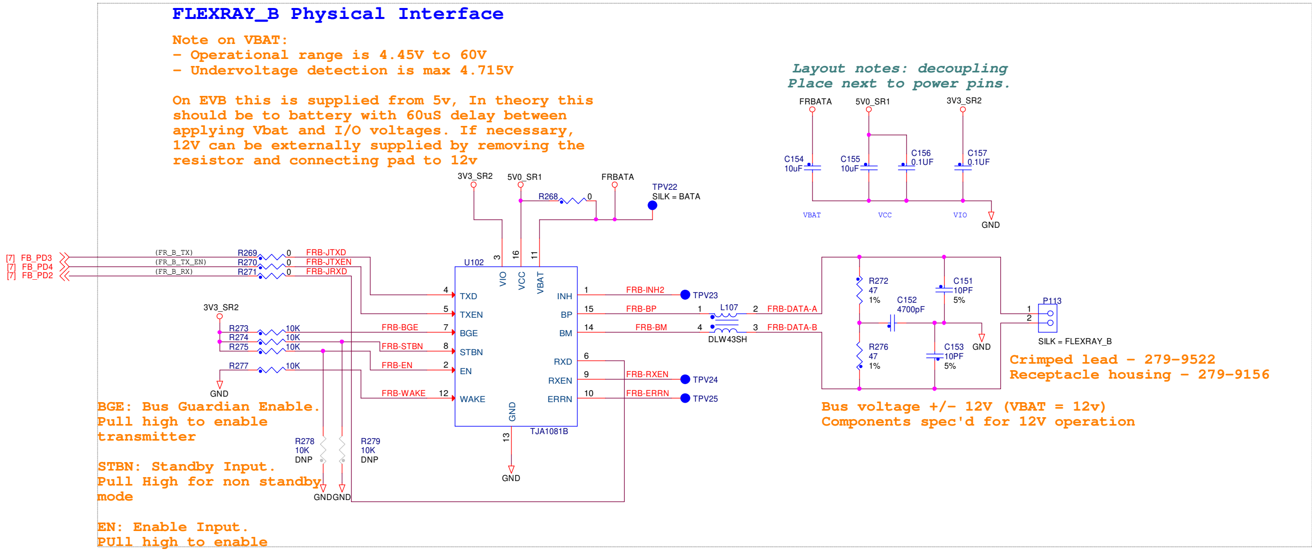
Transition from mode	Direction to mode	Transition number	Pin STBN	Pin EN
Normal	Receive-only	1	H	→L
	Go-to-sleep	2	→L	H
	Standby	3	→L	→L
Receive-only	Normal	4	H	→H
	Go-to-sleep	5	→L	→H
	Standby	6	→L	L
Standby	Normal	7	→H	→H
	Receive-only	8	→H	L
	Go-to-sleep	9	L	→H
Go-to-sleep	Normal	10	→H	H
	Receive-only	11	→H	→L
	Standby	12	L	→L
	Sleep	13	L	H
Sleep	Normal	14	→H	H
	Receive-only	15	→H	L
	Standby	16	→H	X



FLEXRAY_A Physical Interface



FLEXRAY_B Physical Interface



ICAP Classification:	CP: IUO: PUBI: X
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OpenSDA

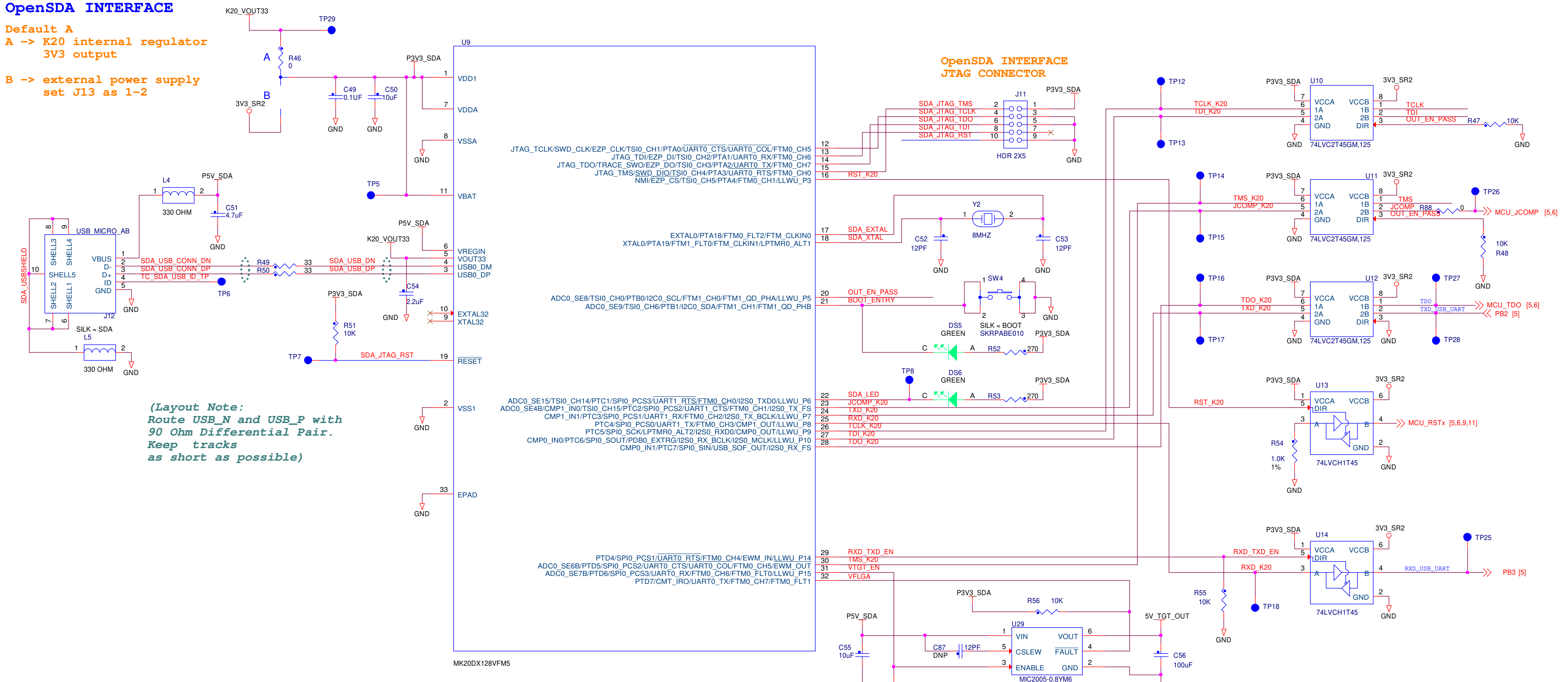
OpenSDA INTERFACE

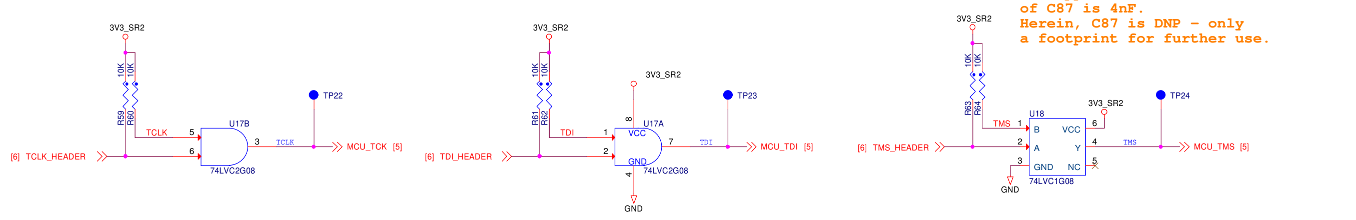
Default A
A -> K20 internal regulator
3V3 output

B -> external power supply
set J13 as 1-2

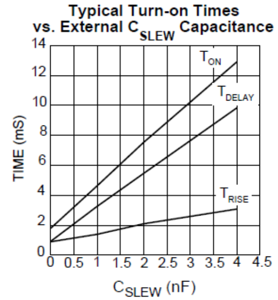
*(Layout Note:
Route USB_N and USB_P with
90 Ohm Differential Pair.
Keep tracks
as short as possible)*

OpenSDA INTERFACE
JTAG CONNECTOR





The CSLEW pin is provided to
increase control of the output
voltage ramp at turn-on.
The upper limit on the value
of C87 is 4nF.
Herein, C87 is DNP - only
a footprint for further use.



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Drawing Title: **DEVKIT-MPC5744P**

Page Title: **OpenSDA**

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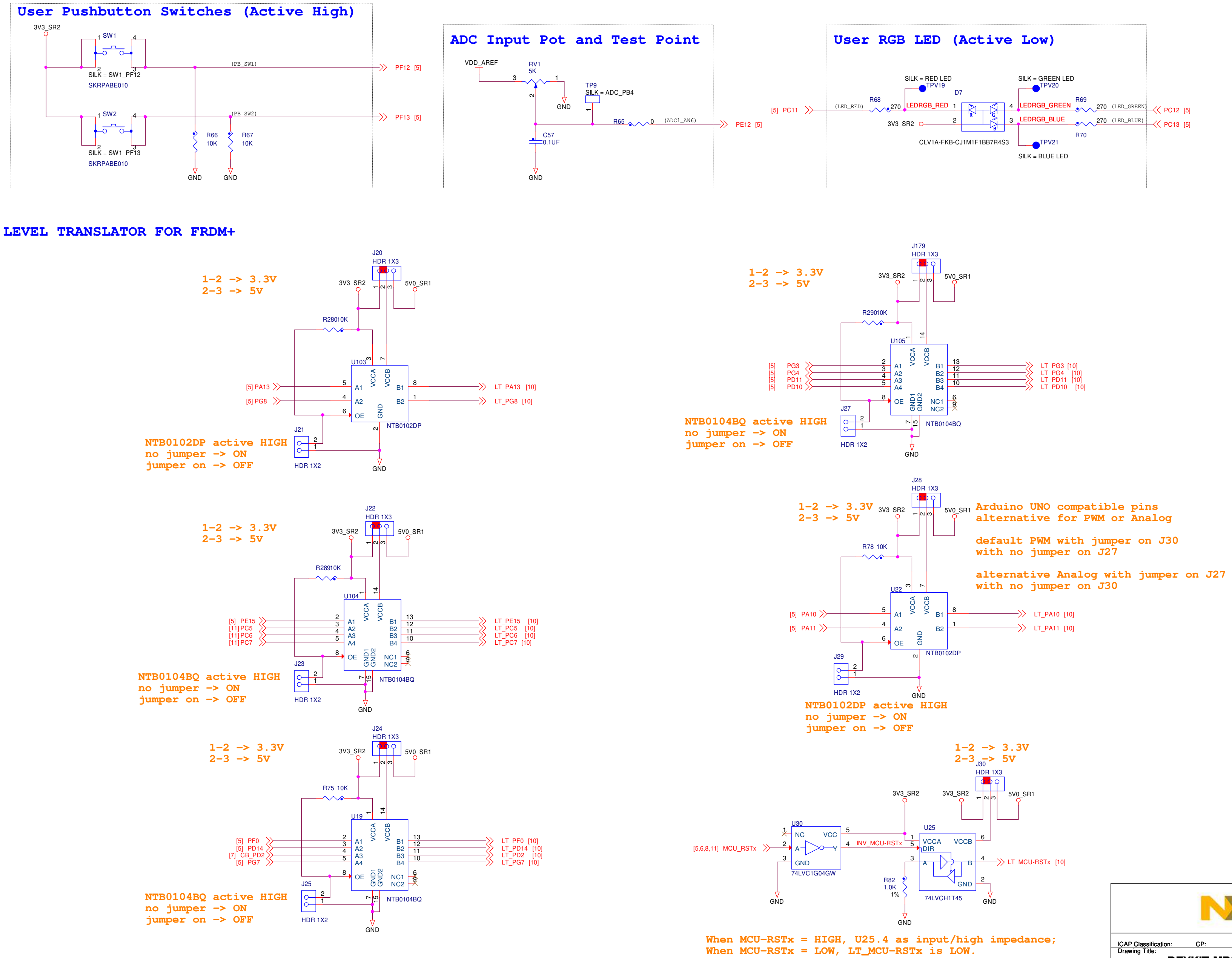
User Peripherals



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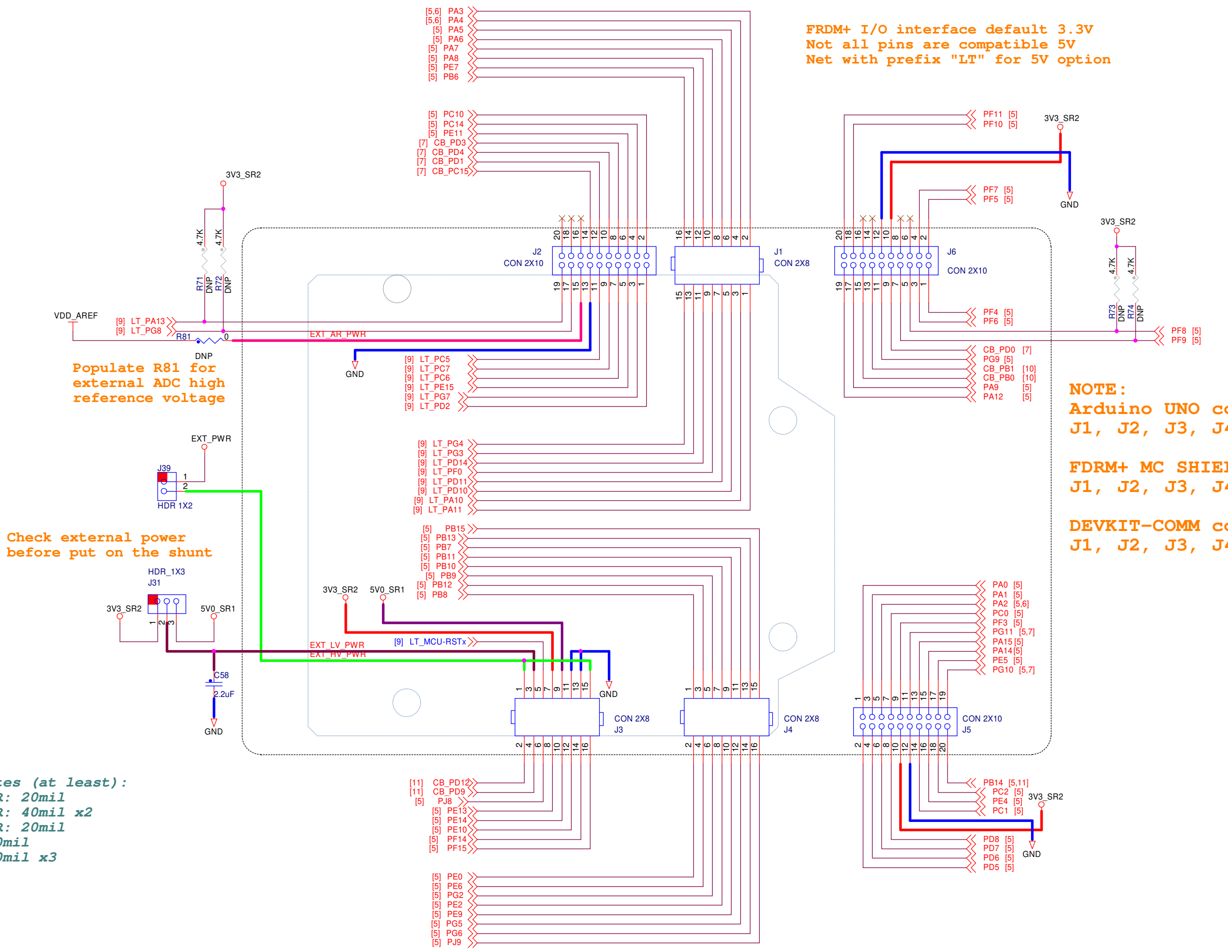
FRDM+ Connectors



NOTE:
Arduino UNO compatible headers:
J1, J2, J3, J4

FDRM+ MC SHIELD/DEVKIT-MOTORGD compatible headers:
J1, J2, J3, J4, J5

DEVKIT-COMM compatible headers:
J1, J2, J3, J4, J5, J6

Layout notes (at least):
EXT_LV_PWR: 20mil
EXT_HV_PWR: 40mil x2
EXT_AR_PWR: 20mil
5V0_SR: 20mil
3V3_SR: 20mil x3

ICAP Classification: CP: IUO: PUBI: X
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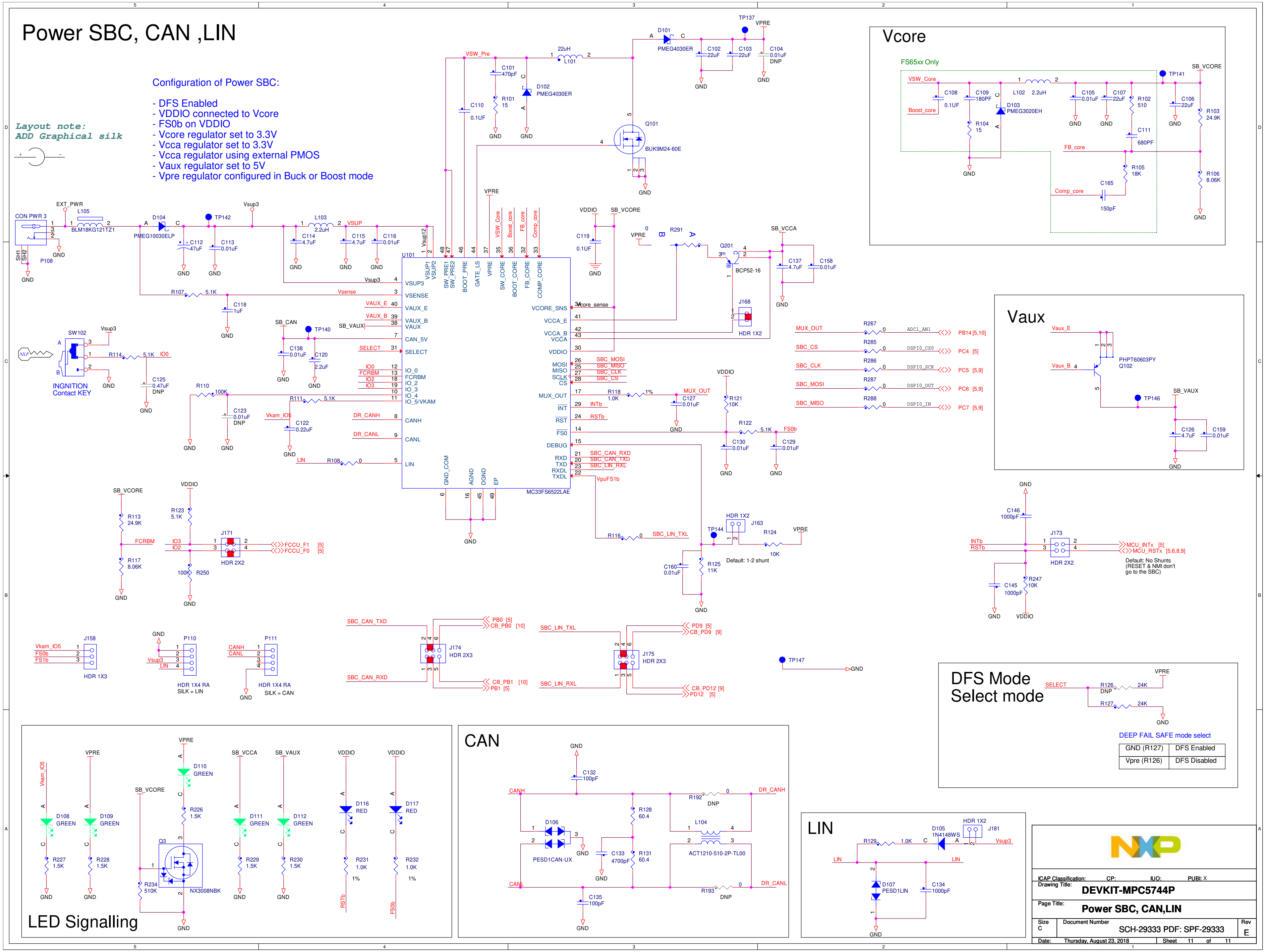
Power SBC, CAN ,LIN
Configuration of Power SBC:
- DFS Enabled
- VDDIO connected to Vcore
- FS0b on VDDIO
- Vcore regulator set to 3.3V
- Vcca regulator set to 3.3V
- Vcca regulator using external PMOS
- Vaux regulator set to 5V
- Vpre regulator configured in Buck or Boost mode
Layout note:
ADD Graphical silk
Vcore
FS65xx Only
Vaux
INGNITION
Contact KEY
MC33FS6522LAE
Default: 1-2 shunt
Default: No Shunts
(RESET & NMI don't
go to the SBC)
DFS Mode
Select mode
DEEP FAIL SAFE mode select
GND (R127) DFS Enabled
Vpre (R126) DFS Disabled
CAN
LIN
LED Signalling
Drawing Title: DEVKIT-MPC5744P
Page Title: Power SBC, CAN,LIN
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