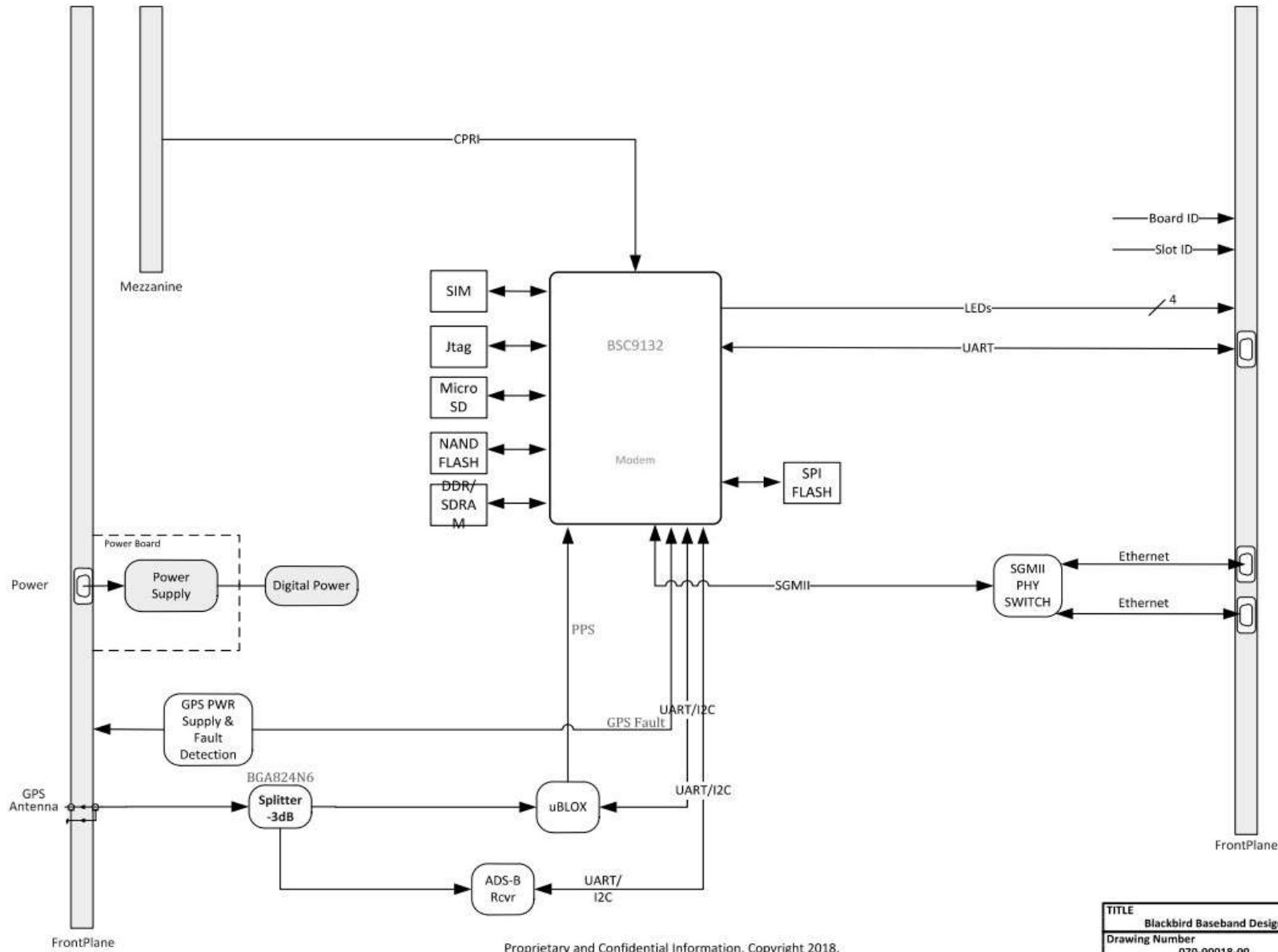


ABR_9132_MB

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03	POWER TREE
04	CORE_POWER&RESET
05	SYSTEM_POWER
06	POWER
07	DDR3_POWER&DDR_RST
08	SYS_CLK&LED
09	9132_POWER
10	9132_POWER_DECOUPLE
11	9132_DDR1
12	9132_DDR2
13	9132_IFC
14	9132_MISC
15	9132_SERDES
16	9132_ANT1&2_IF
17	9132_SPI&EMI&SIM&SD
18	POWER_UP_CONFIG
19	QCA8337
20	QCA8337_WAN_LAN
21	GPS
22	URAT_CONSOLE
23	ETHERNET PHY
24	RF_CARD_CLOCK&RESET
25	Front Plane Connectors
26	FRONT PANEL LED DRIVERS
27	HEATING
28	MACHINAL
29	RECORD

Blackbird Baseband DESIGN

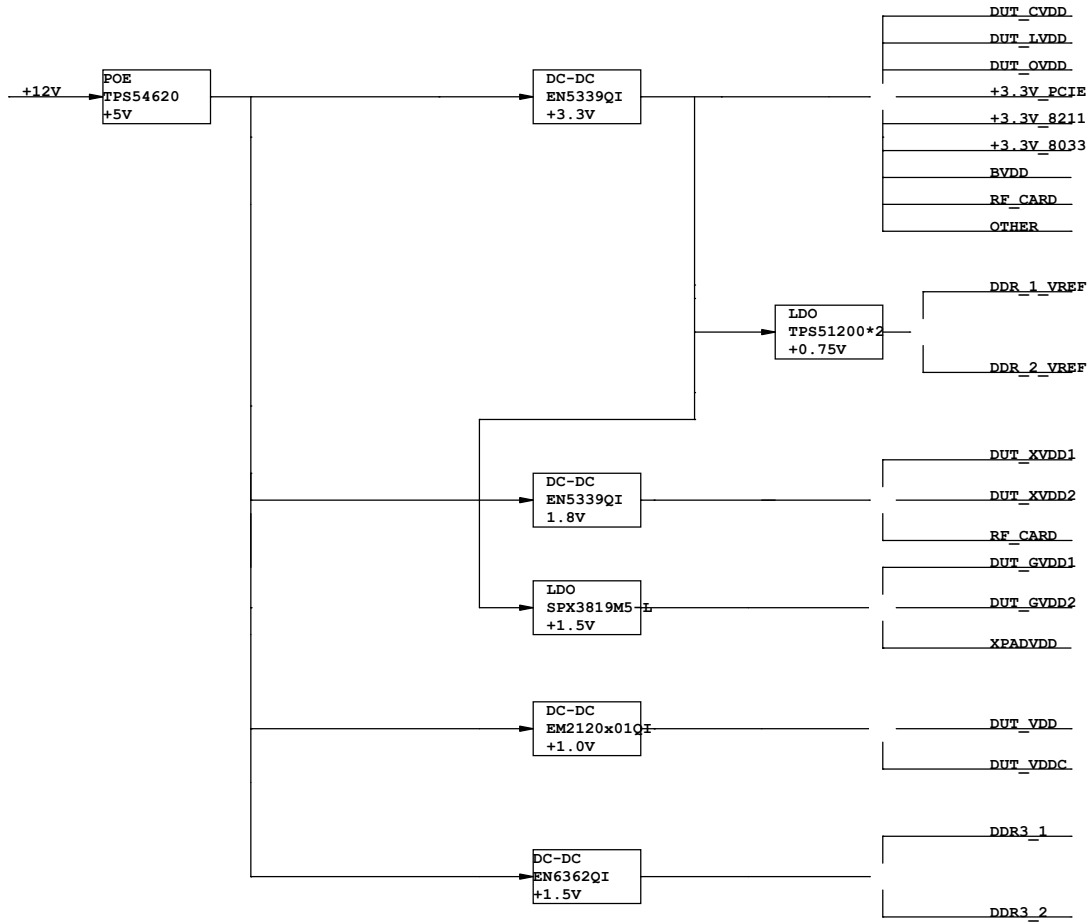


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TITLE			
Blackbird Baseband Design			
Drawing Number			
070-00018-00			
5/07/18	Size	PAGE	Rev
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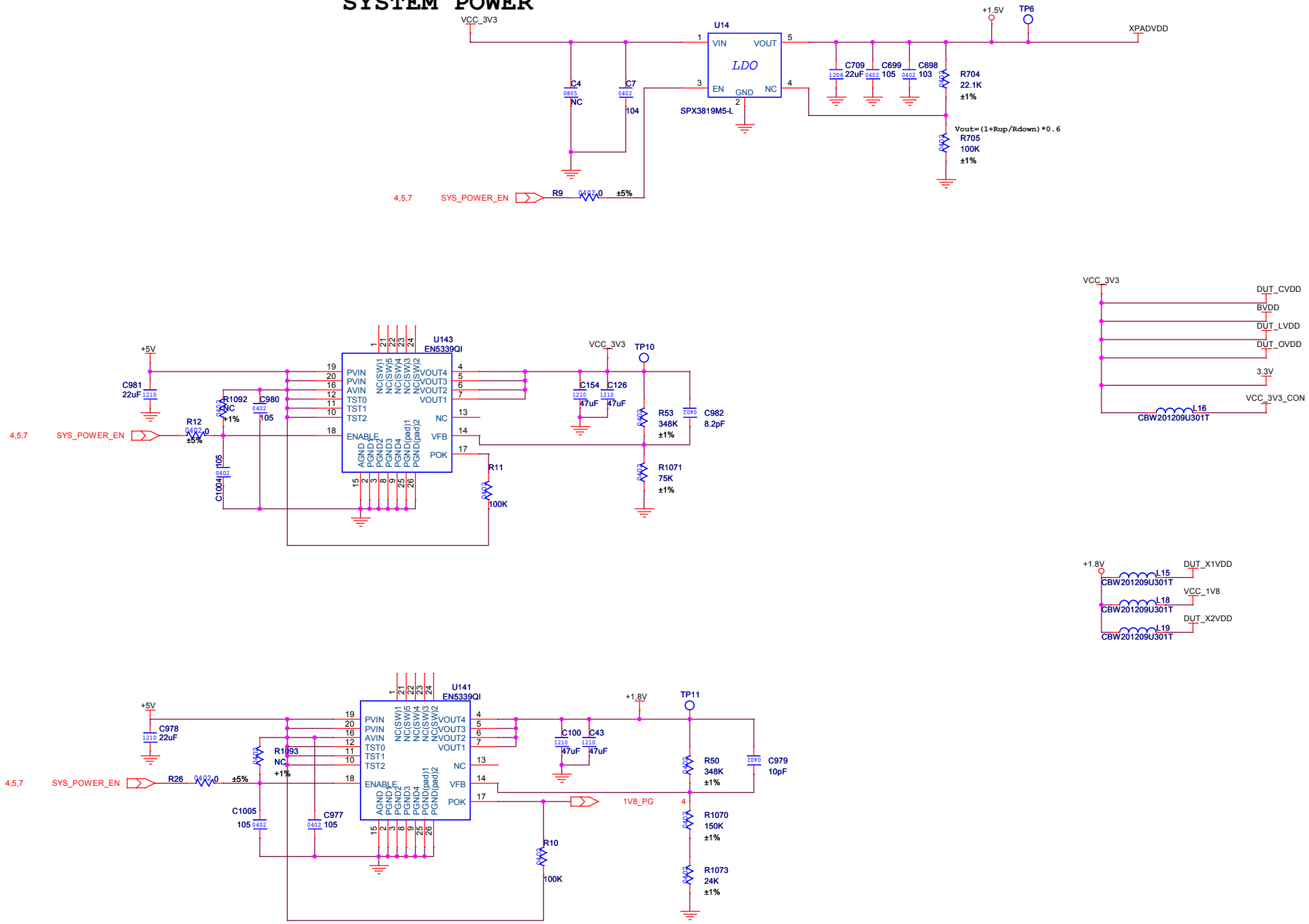
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ABR_9132_MB			
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POWER TREE



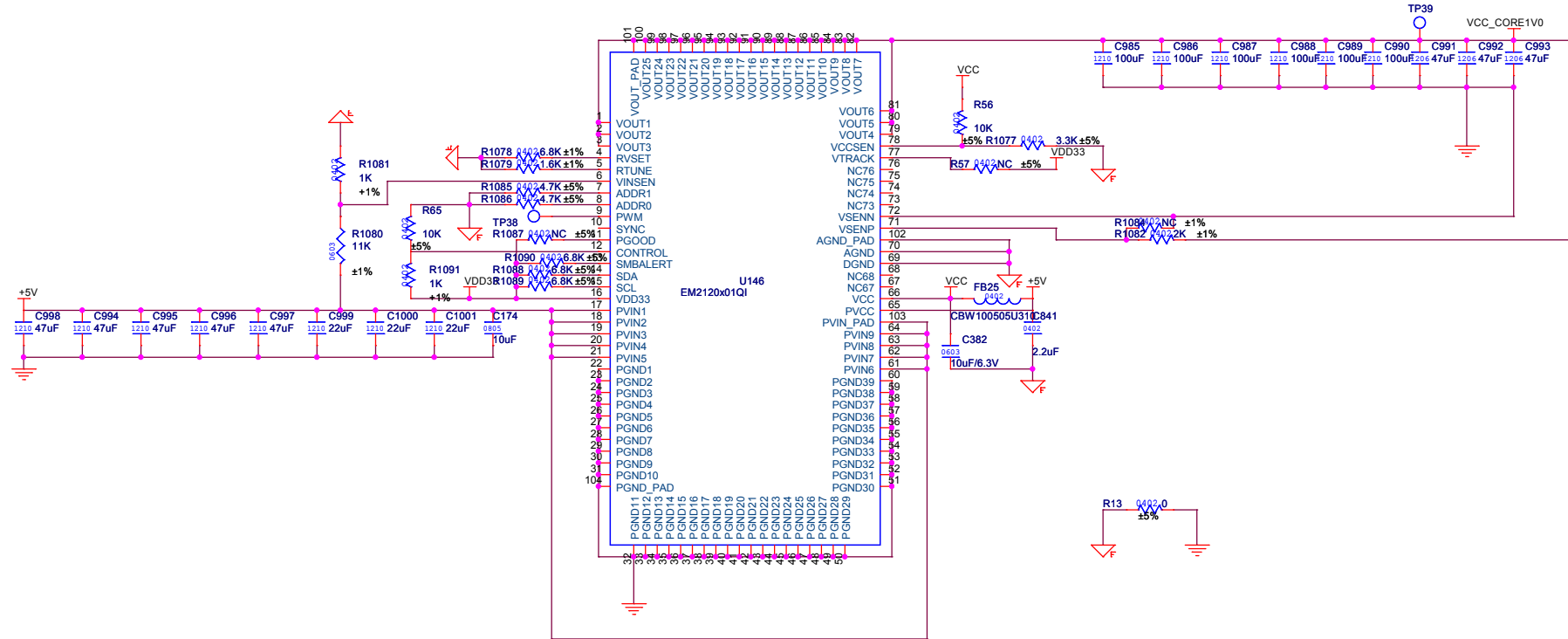
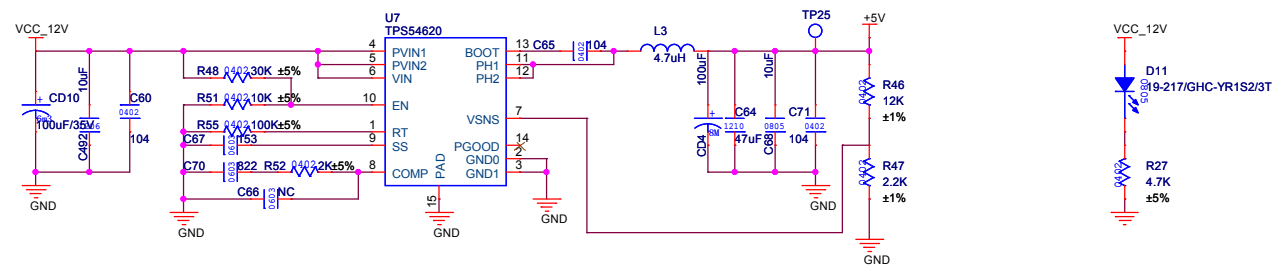
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A3	POWER TREE	V0.9	
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SYSTEM POWER

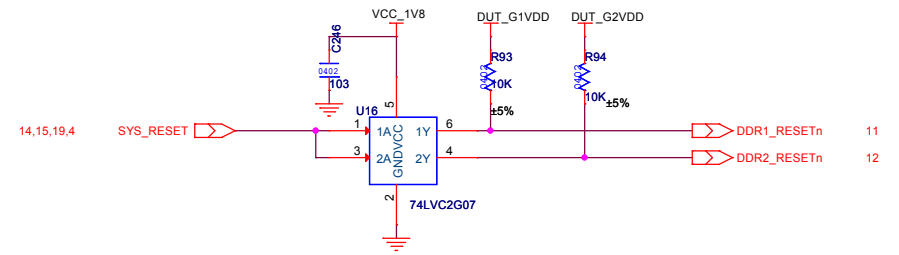
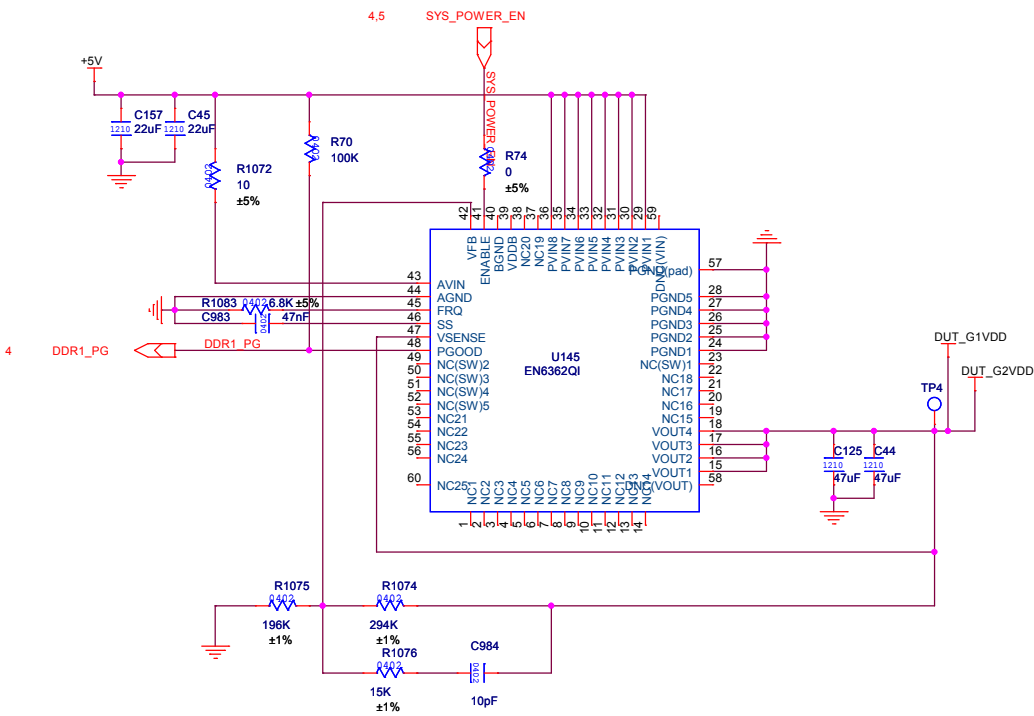
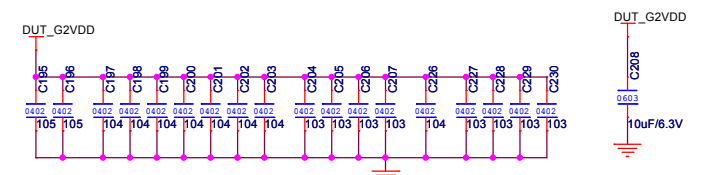
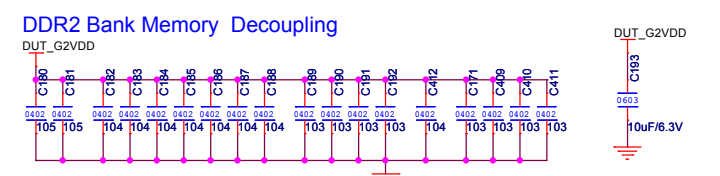
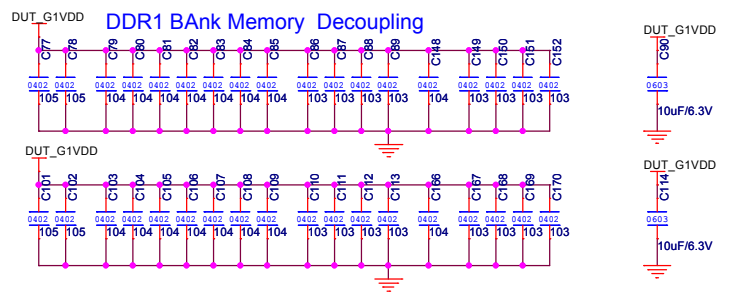
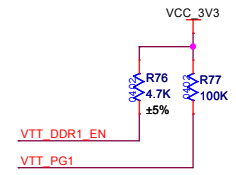
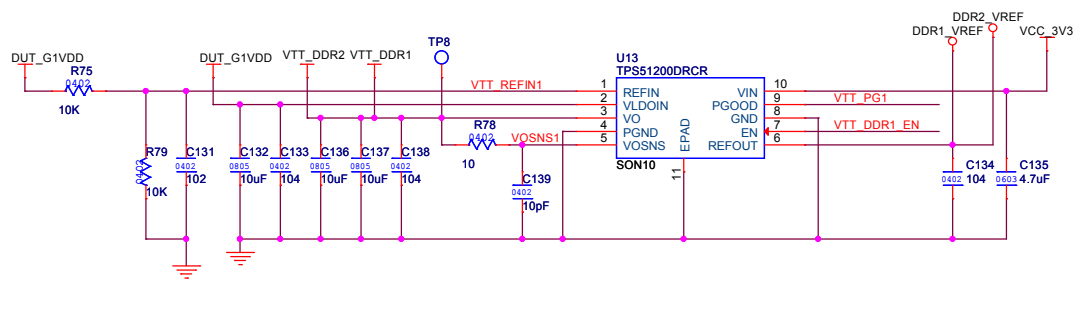


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A3	SYSTEM_POWER	V0.9	
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12V-5V

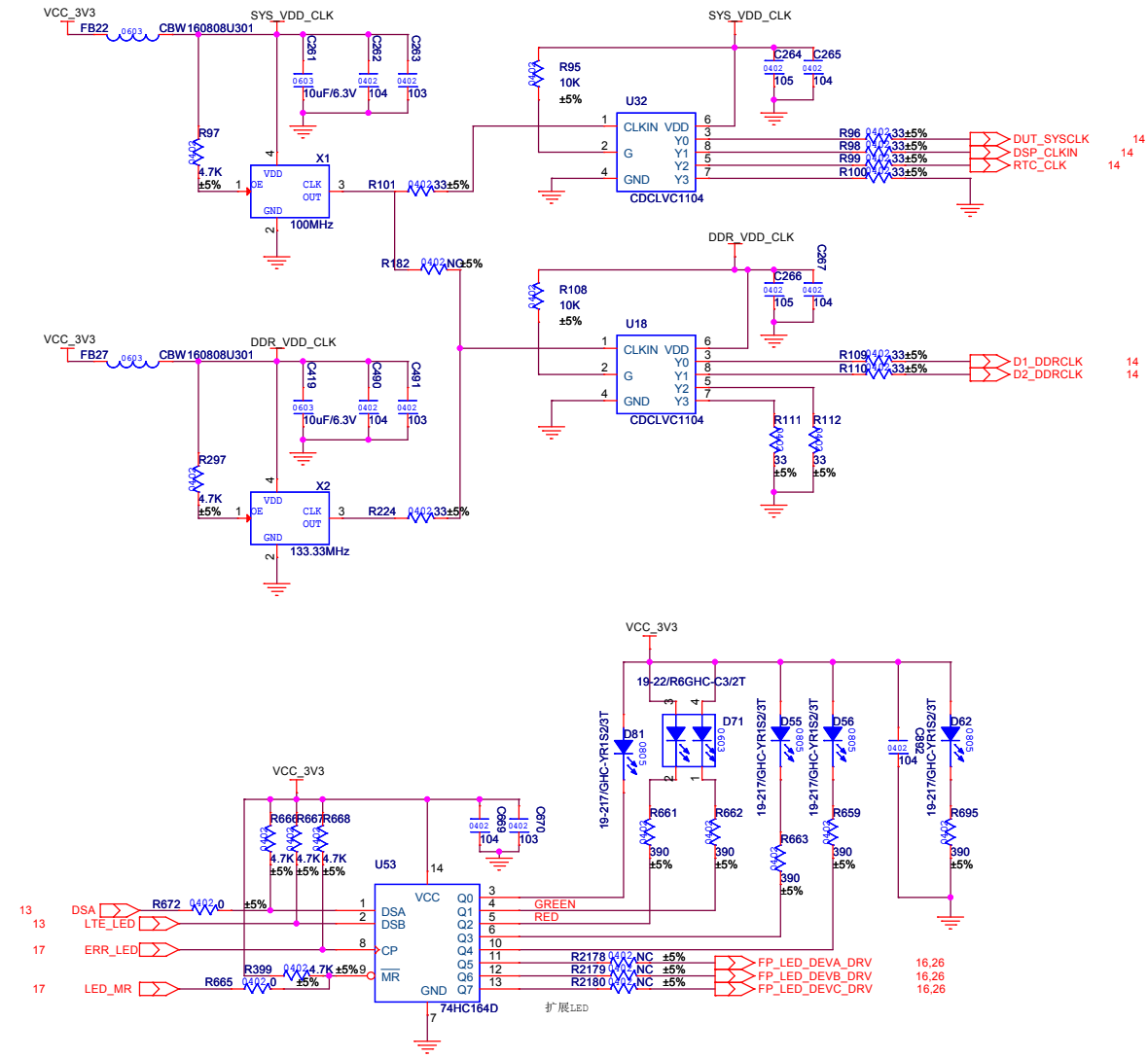


DDR3_POWER & DDR_RST



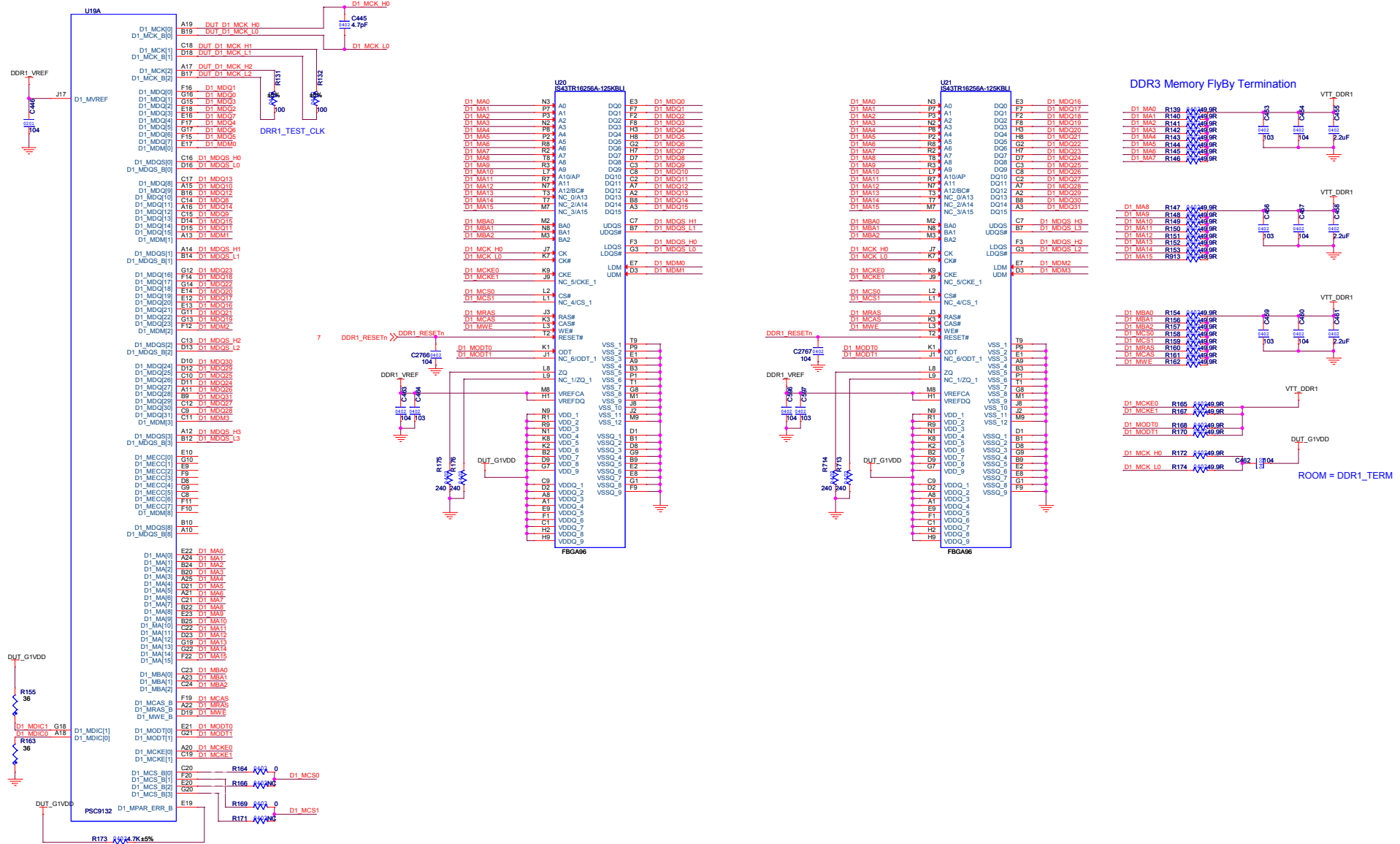
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Title	ABR_9132_MB		
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A3	DDR3_POWER&DDR_RST		
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SYSCLK, DDRCLK & DSPCLK SYNTHESIZERS & LED

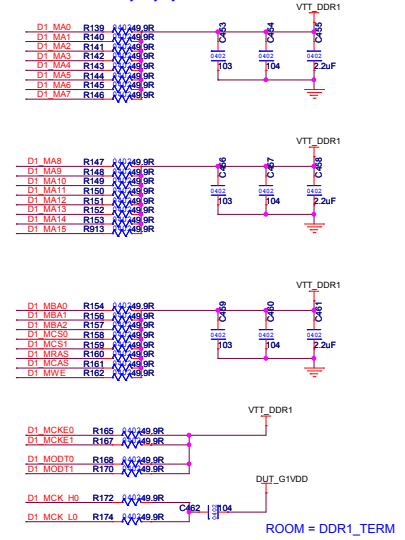


9132_DDR1

Place these caps close to DUT.



DDR3 Memory FlyBy Termination



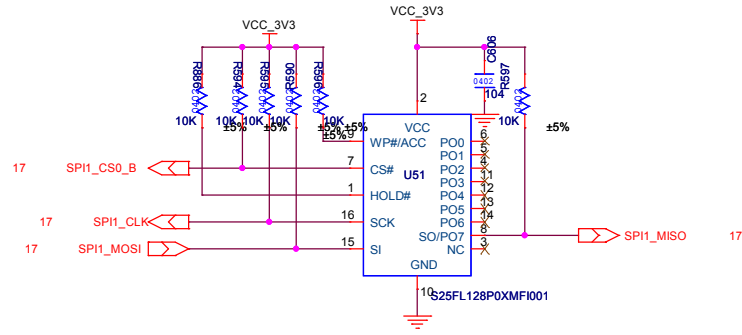
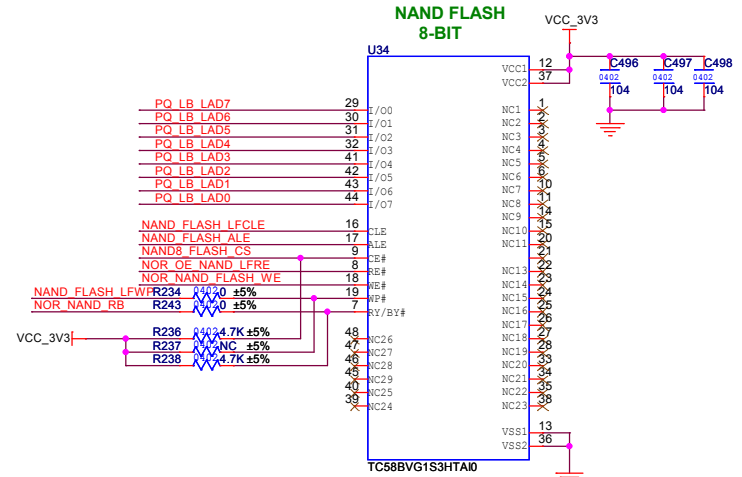
ROOM = DDR1_TERM

9132 IFC

U19E



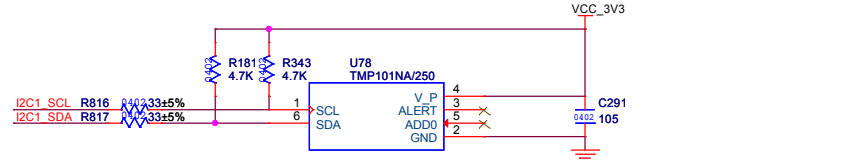
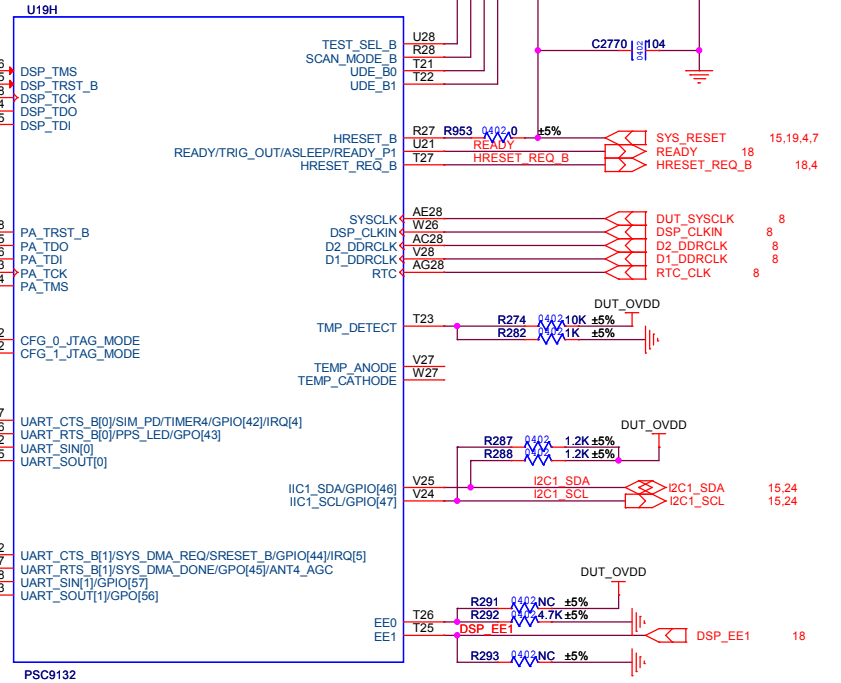
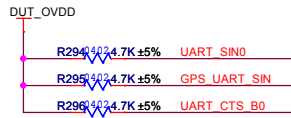
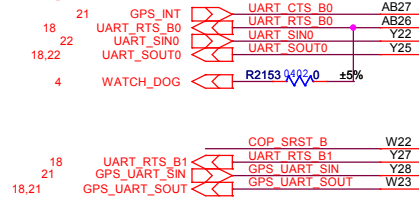
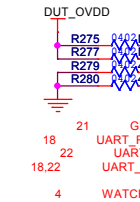
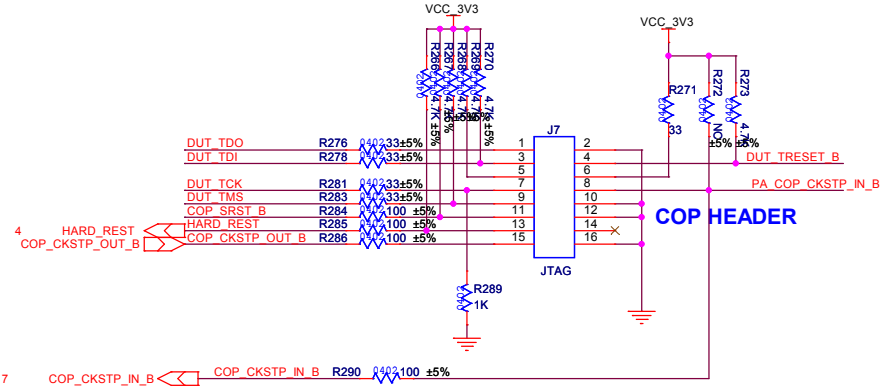
PSC9132



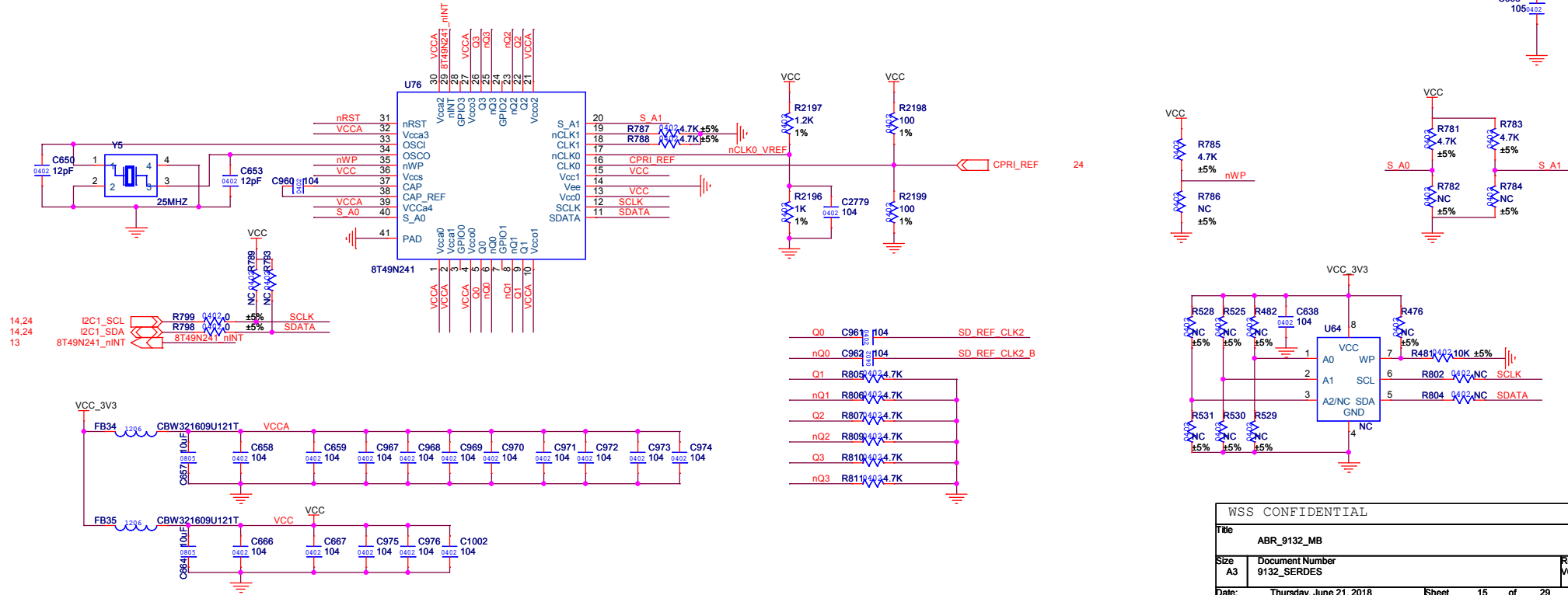
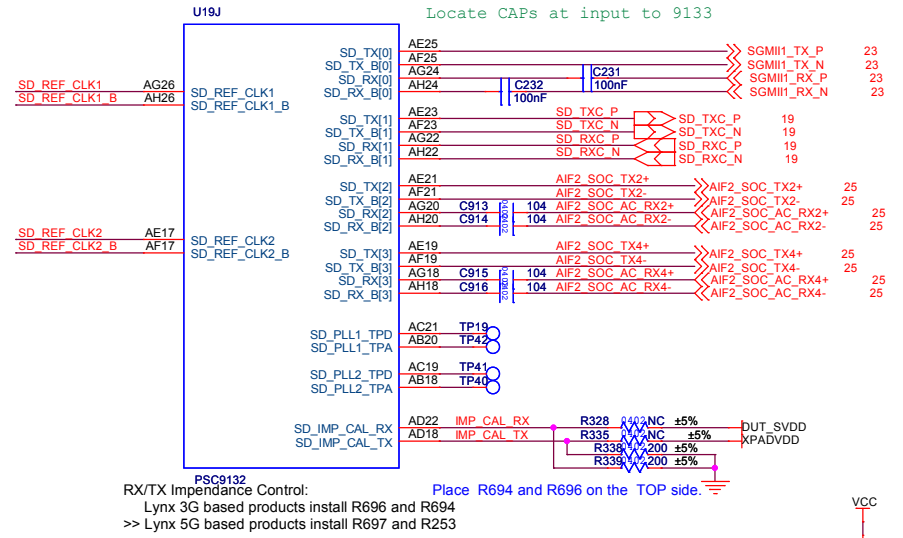
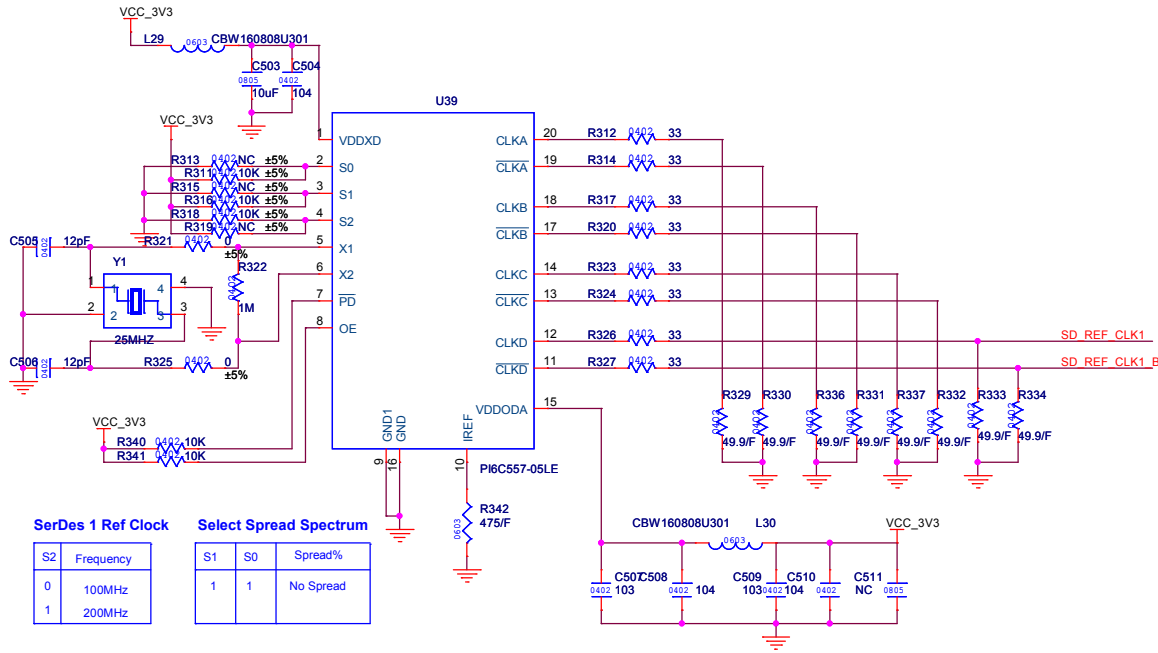
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Title	ABR_9132_MB		
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A3	9132_IFC&SPI	V0.9	
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9132 - MISC (OVDD)

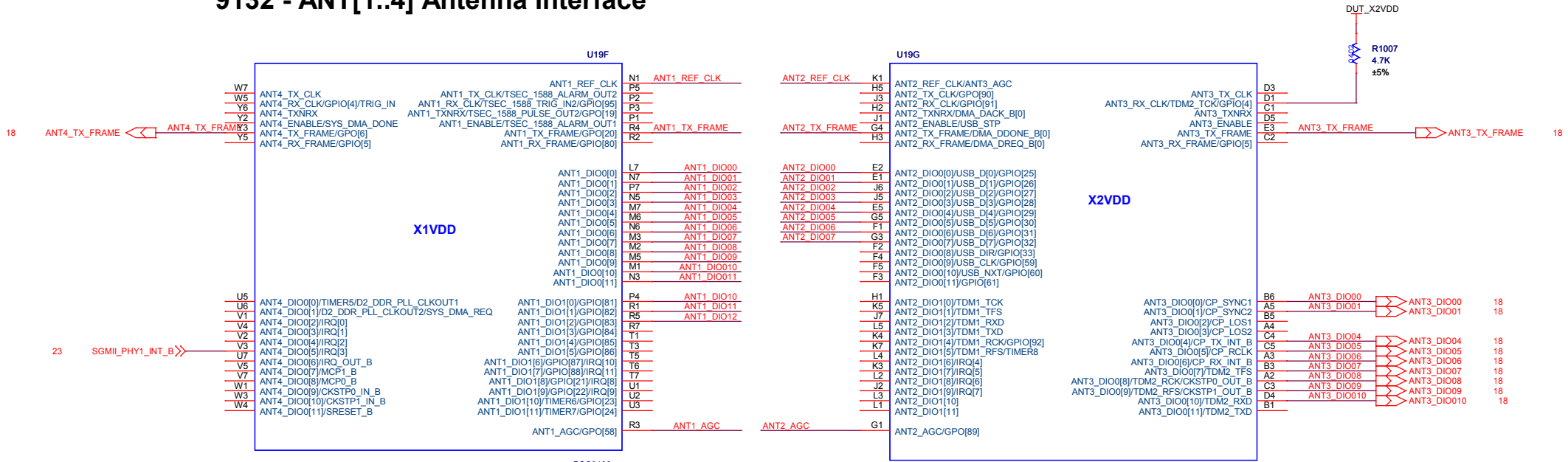
EONCE HEADER



PSC9132 SerDes



9132 - ANT[1..4] Antenna Interface



ANT1_TX_FRAME >> ANT1_TX_FRAME 18

ANT1_DIO10 R2181 4.7K ±5% >> FP_LED_DEVA_DRV 26.8
 ANT1_DIO11 R2182 4.7K ±5% >> FP_LED_DEVB_DRV 26.8
 ANT1_DIO12 R2183 4.7K ±5% >> FP_LED_DEVC_DRV 26.8

ANT1_REF_CLK >> ANT1_REF_CLK 24
 ANT1_AGC >> ANT1_AGC 18

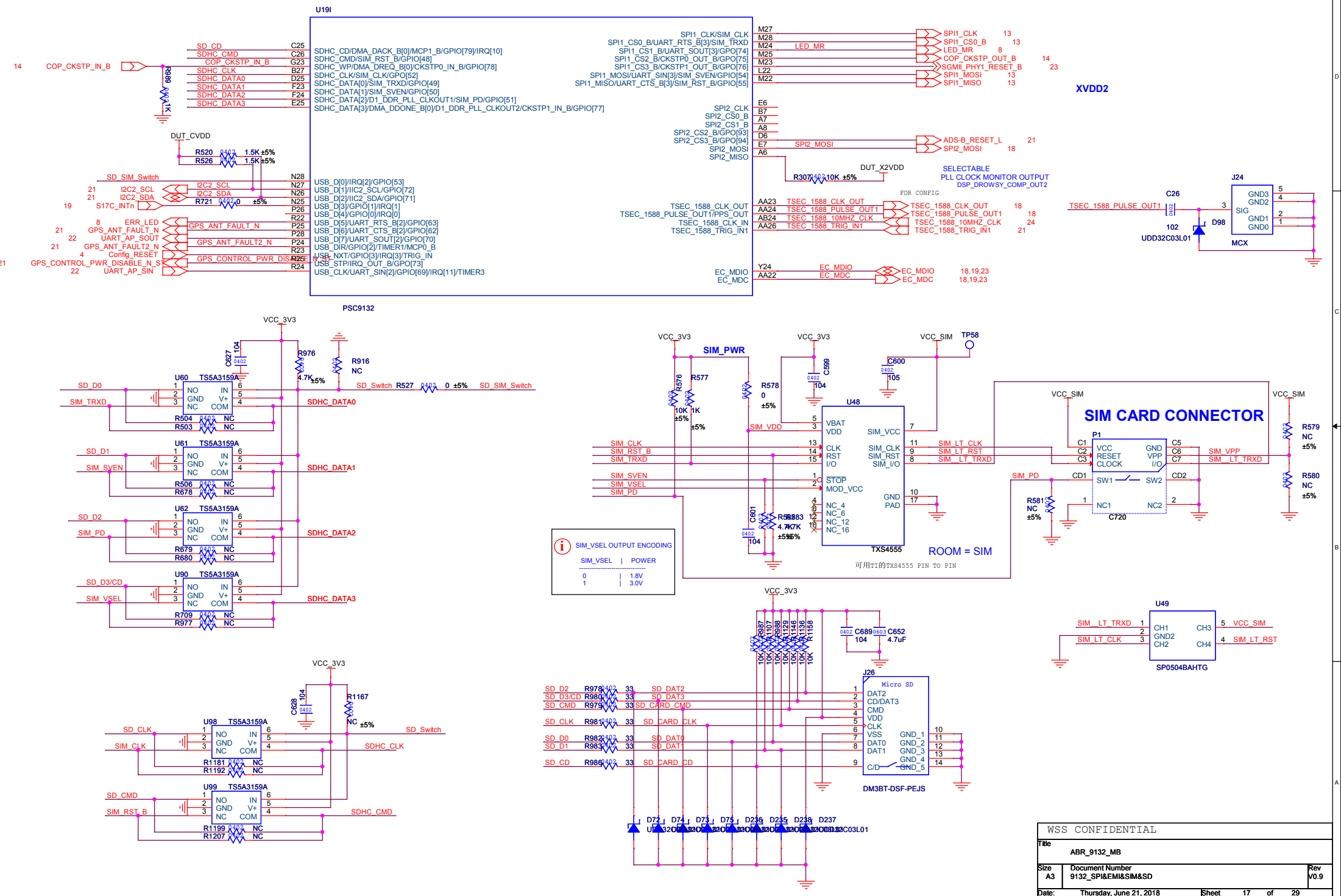
ANT2_REF_CLK >> ANT2_REF_CLK 18
 ANT2_AGC >> ANT2_AGC 18

ANT2_TX_FRAME >> ANT2_TX_FRAME 18

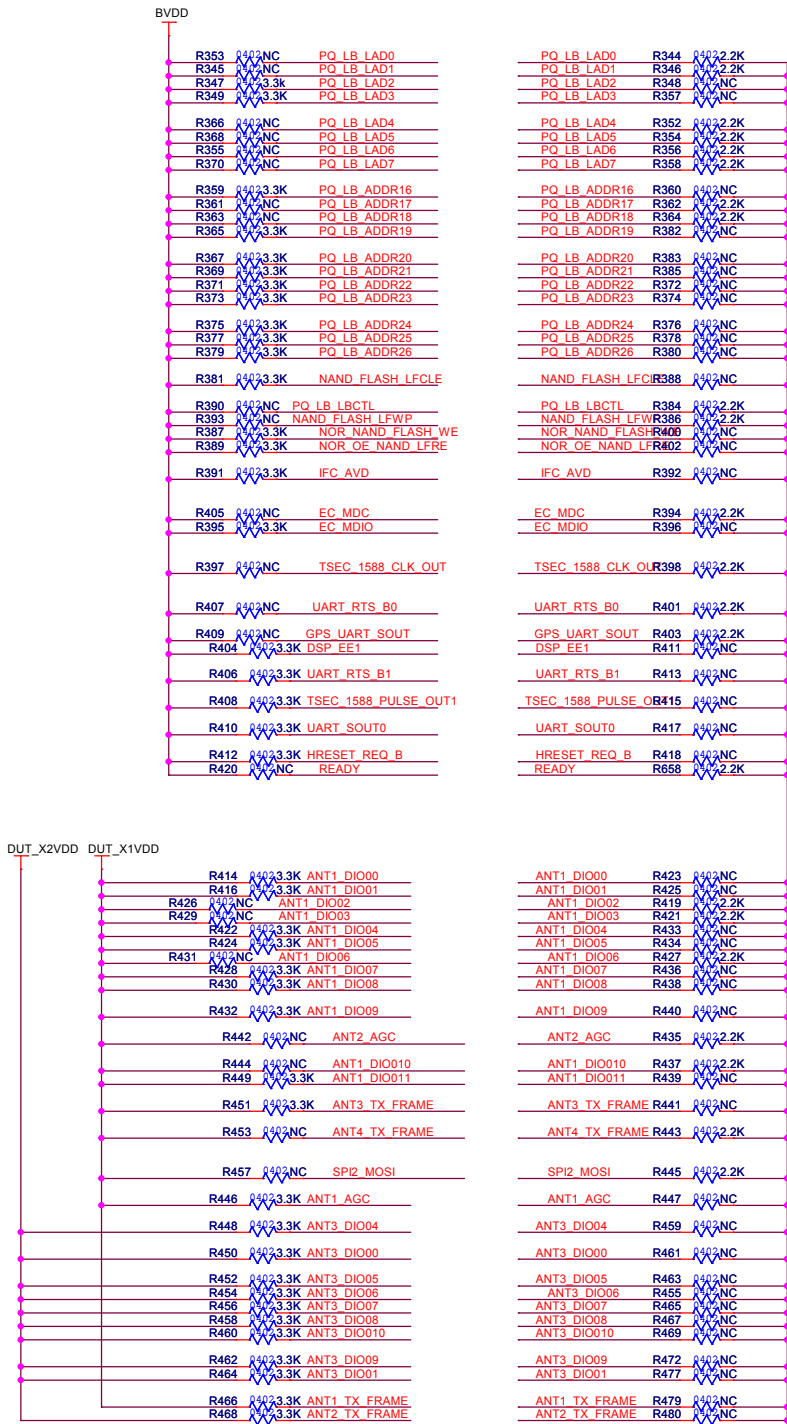
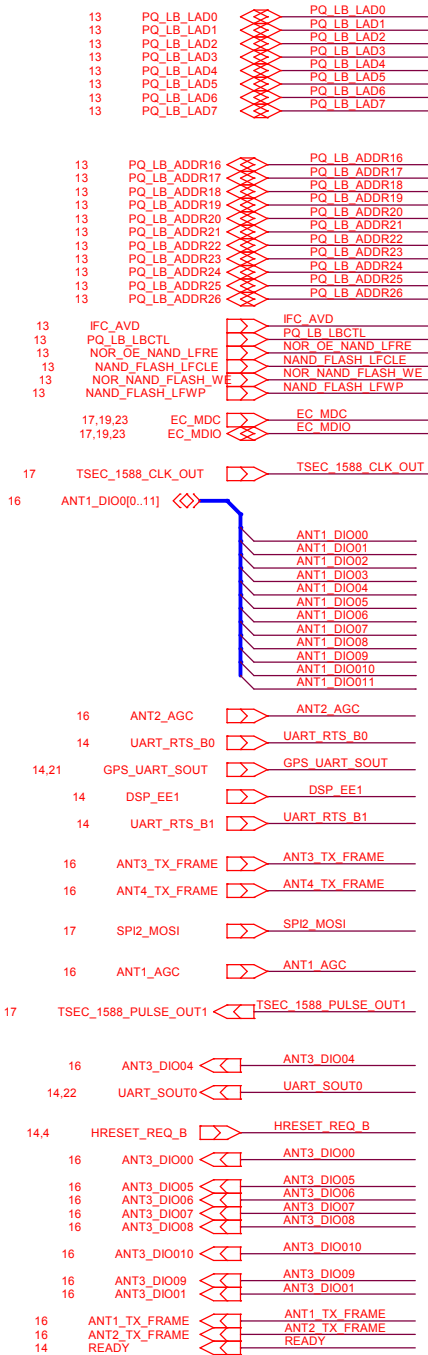
ANT2_DIO01 R2188 4.7K ±5% >> SLOT_ID_ID1_OUT 25
 ANT2_DIO06 R2189 4.7K ±5% >> SLOT_ID_ID2_OUT 25
 ANT2_DIO00 R2190 4.7K ±5% >> SLOT_ID_ID3_OUT 25
 ANT2_DIO04 R2191 4.7K ±5% >> SLOT_ID_ID4_OUT 25
 ANT2_DIO05 R2192 4.7K ±5% >> BOARD_ID0_BK_OUT 25
 ANT2_DIO07 R2193 4.7K ±5% >> BOARD_ID1_BK_OUT 25
 ANT2_DIO03 R2194 4.7K ±5% >> BOARD_ID2_BK_OUT 25
 ANT2_DIO02 R2195 4.7K ±5% >> BOARD_ID3_BK_OUT 25

ANT1_DIO00 >> ANT1_DIO0[0..11] 18
 ANT1_DIO01
 ANT1_DIO02
 ANT1_DIO03
 ANT1_DIO04
 ANT1_DIO05
 ANT1_DIO06
 ANT1_DIO07
 ANT1_DIO08
 ANT1_DIO09
 ANT1_DIO10
 ANT1_DIO11

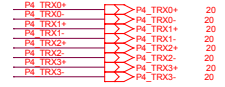
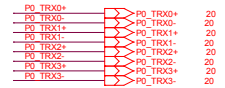
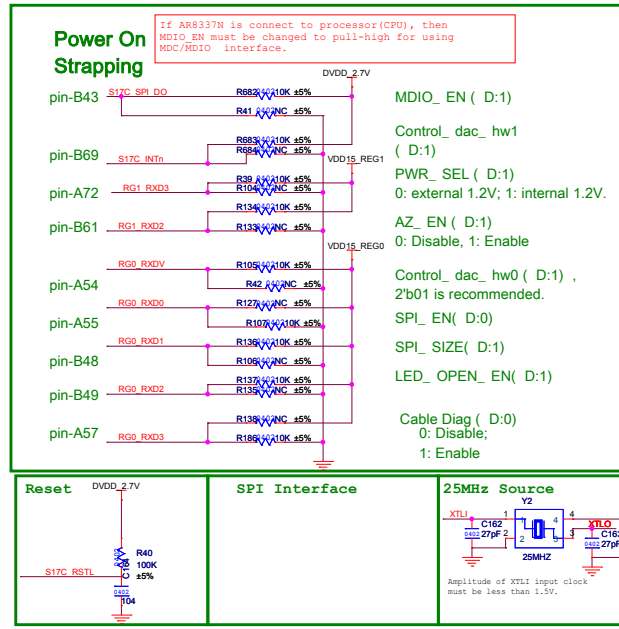
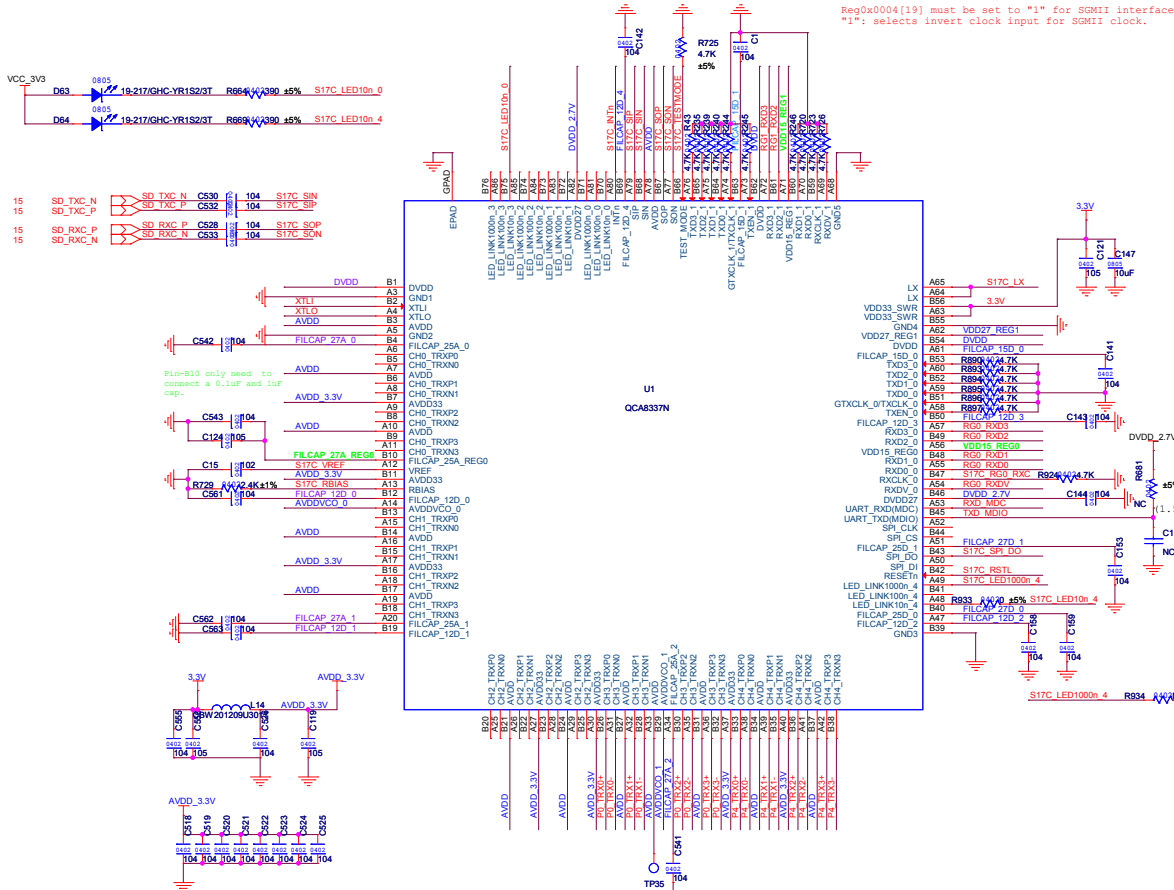
9132 - USB,SPI,SDHC,EMI



POWER_UP_CONFIG



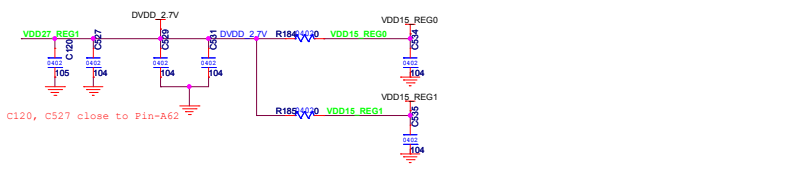
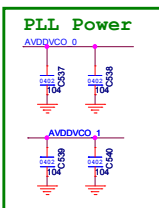
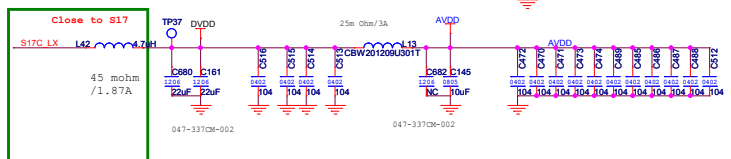
Reg0x0004[19] must be set to "1" for SGMII interface
 "1": selects invert clock input for SGMII clock.



- Notel:**
- If RGMII0_RGMII1 are 1.5V/1.8V level, then R172 and R170 are no load. And VDD15_REG 0 & VDD15_REG 1 will output 1.5V or 1.8V power.
 - If RGMII0_RGMII1 are 2.5V Level, then R172 and R170 load a 0 ohm resistor.
 - VDD15_REG 0 is connected to VDD15_IO_0 together at S17 chip inner. VDD15_REG 0 and VDD15_IO 0 only need a external 0.1uF.
 - VDD15_REG 1 is connected to VDD15_IO_1 together at S17 chip inner. VDD15_REG 1 and VDD15_IO_1 only need a external 0.1uF.
 - All FILCAP pins are connected to inner power, so these FILCAP only need a external 0.1uF.

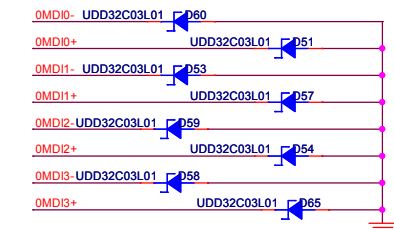
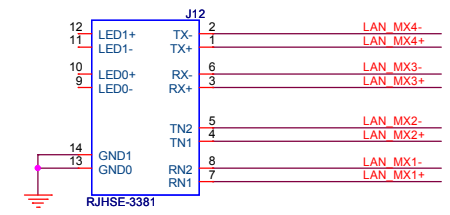
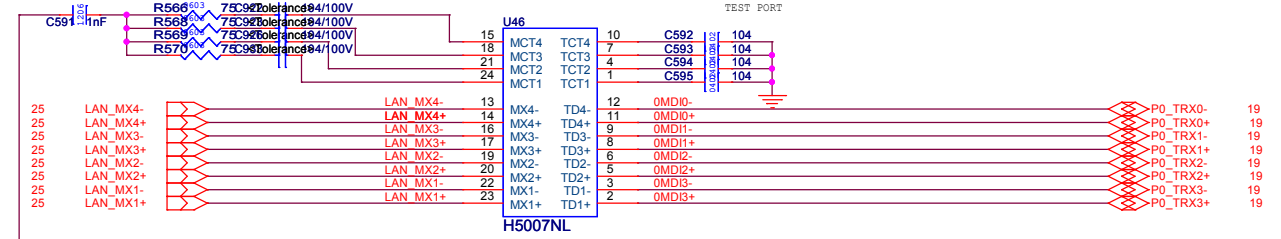
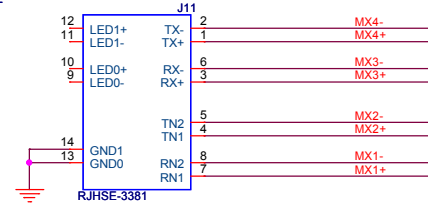
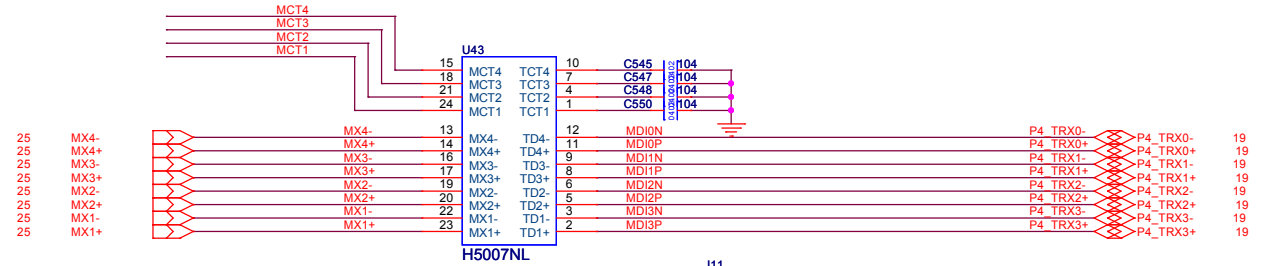
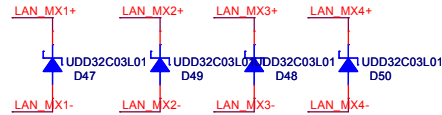
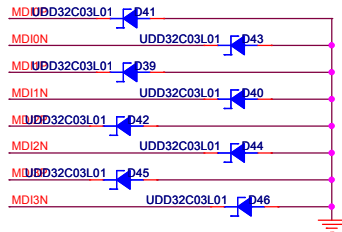
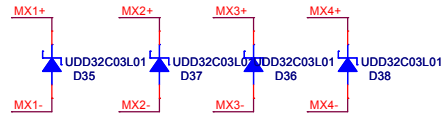
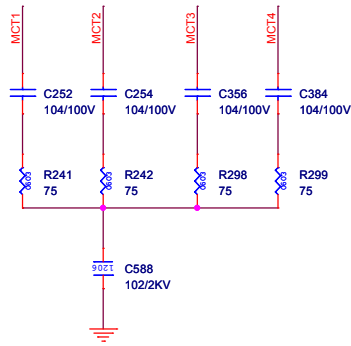
- Note 2:**
- For LX(Pin-A64/65) layout suggestion: (Please follow the below suggestion)
- LX trace doesn't change to any layer. So, please keep it at top-layer.
 - Lx trace length is as short as possible and a large area. L2's DVDD need also a large copper area.
 - Any trace, power and components don't close to LX trace in particular all 3.3V power.
 - Any trace, power and components don't rout under LX trace / pin.

- Note 3:**
- For VDD33 SVR(pin-A63/B56) layout suggestion: (Please follow the below suggestion)
- VDD33 SVR trace width >= 15mil.
 - The via of VDD33_SVR don't close to L2/LX trace.

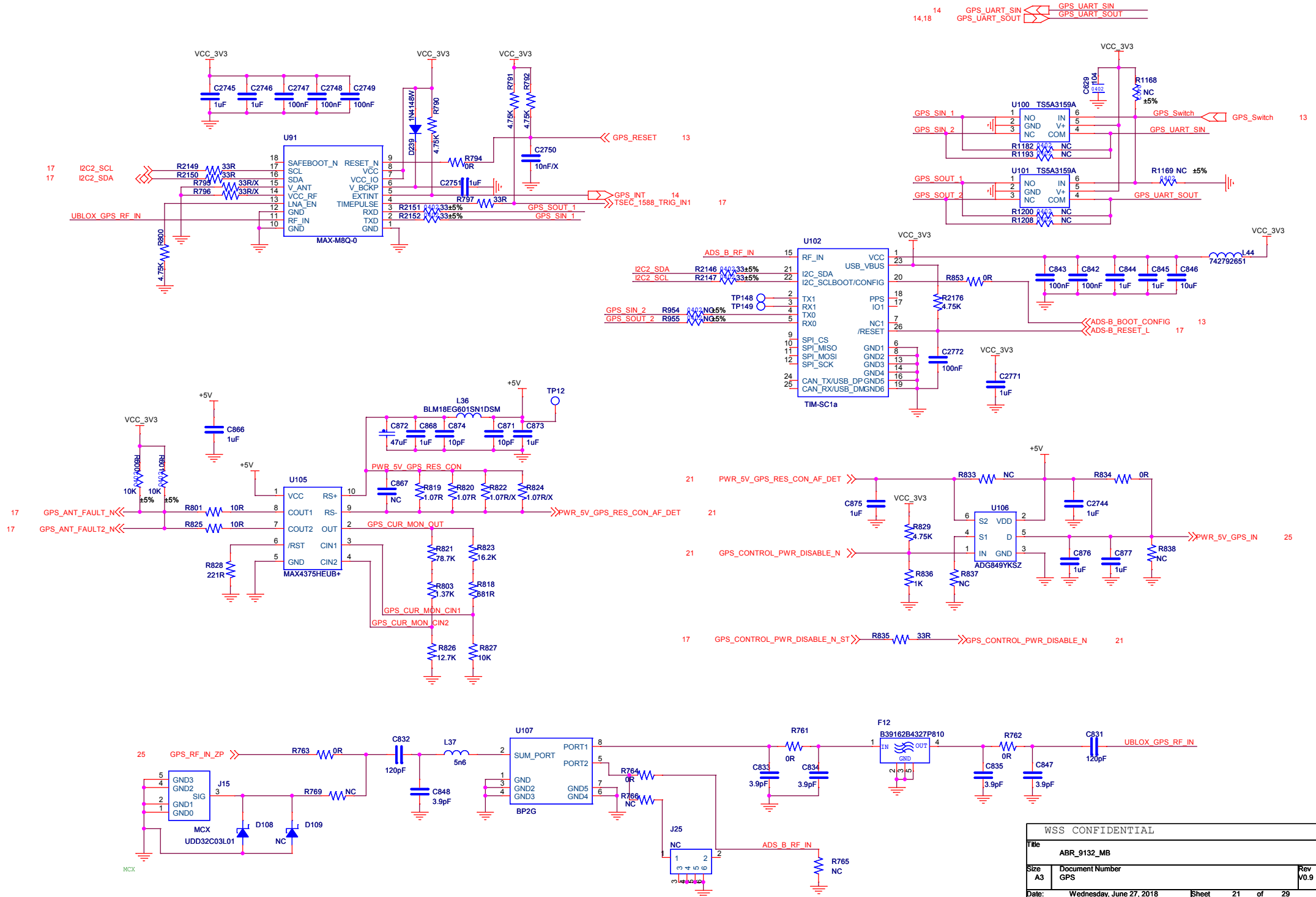


SYS_RESET	R603	10K	±5%	S17C_RSTL
EC_MDC	R604	10K	±5%	RG0_MDC
EC_MDIO	R605	10K	±5%	TXD_MDIO

QCA8337_Magnet



GPS & ADS-B

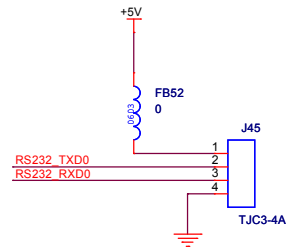
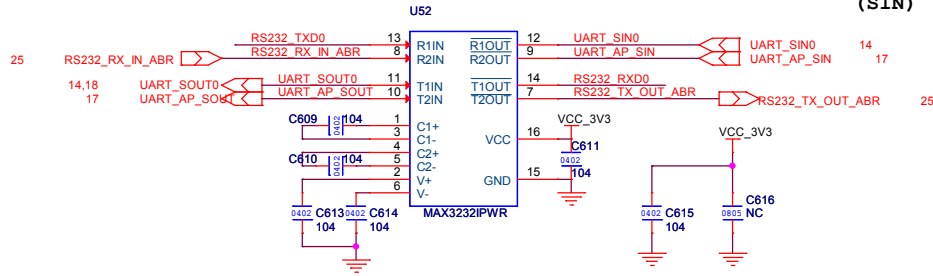


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UART

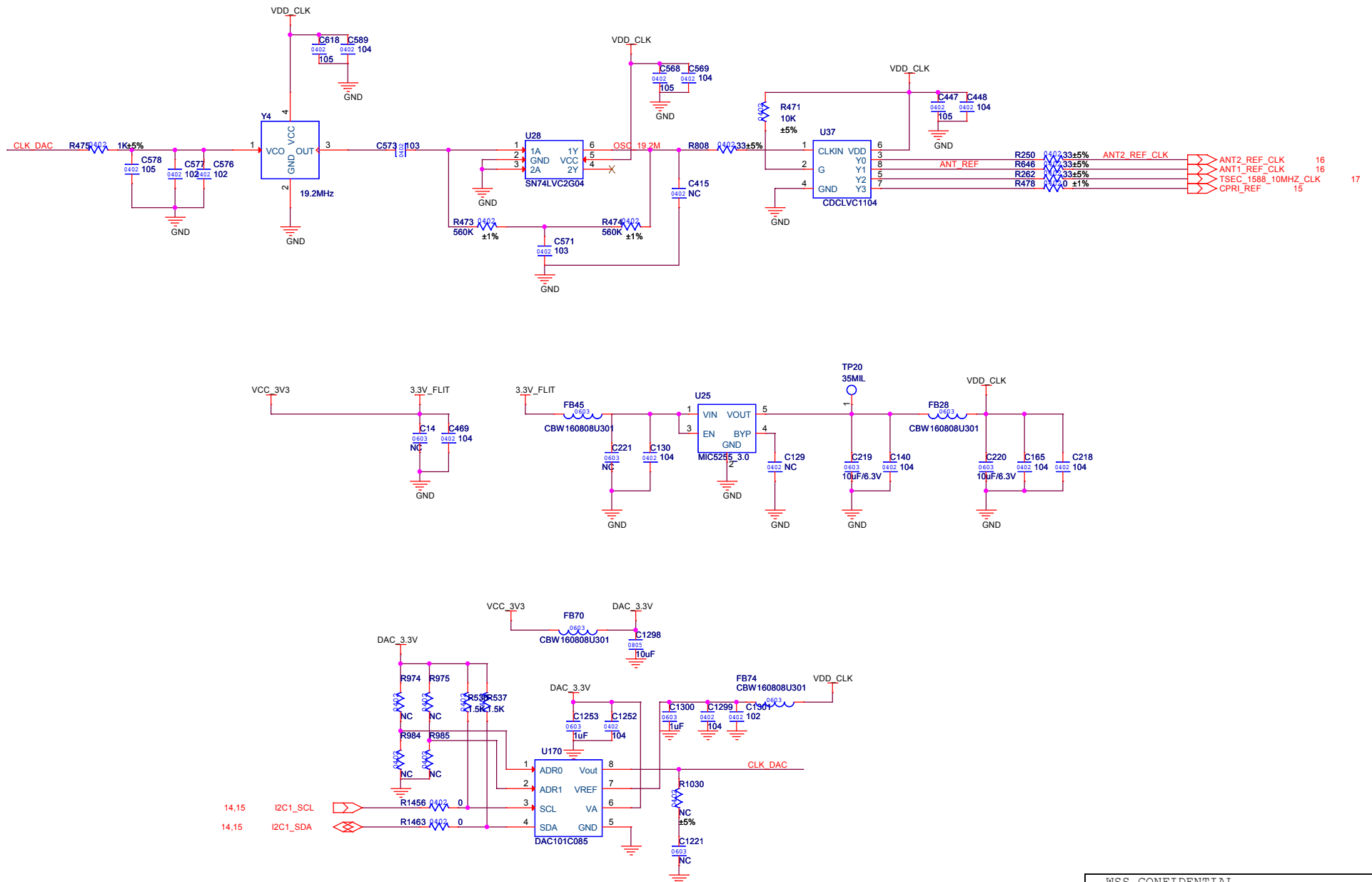
(SOUT)

(SIN)



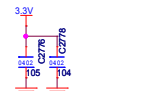
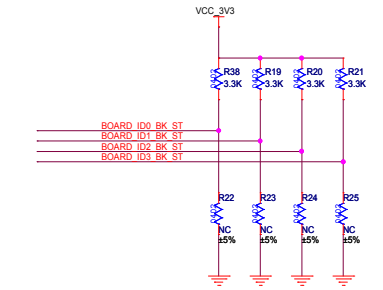
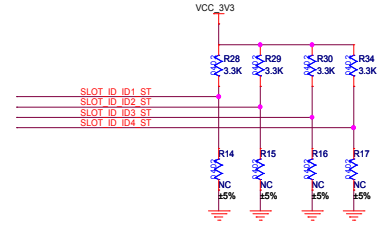
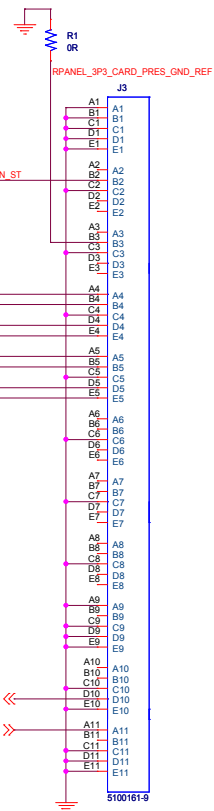
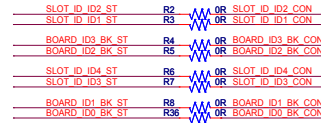
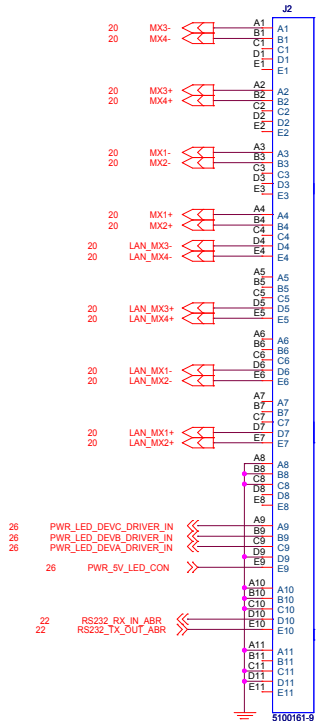
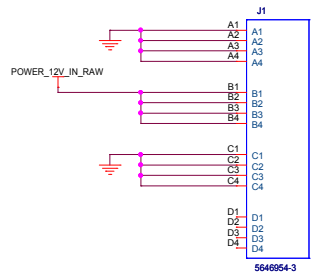
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RF_CARD_CLOCK&RESET

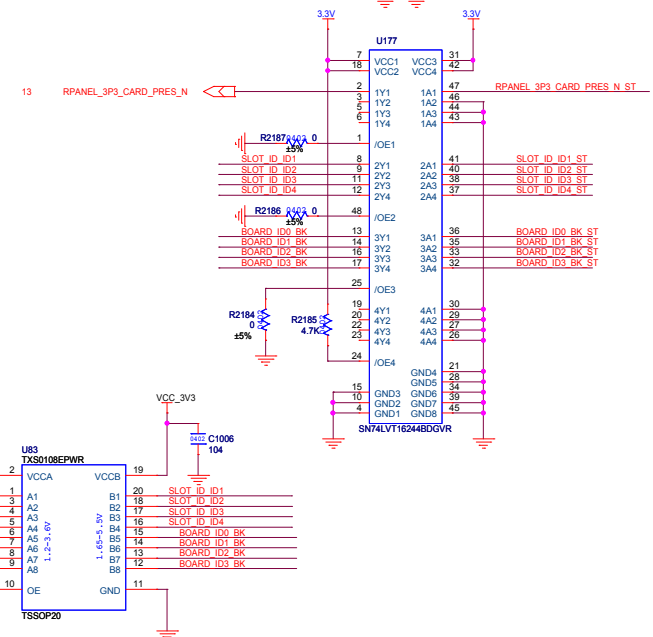
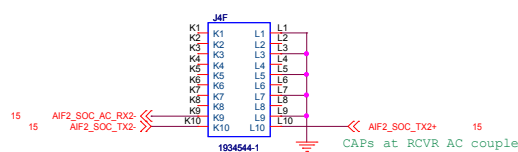
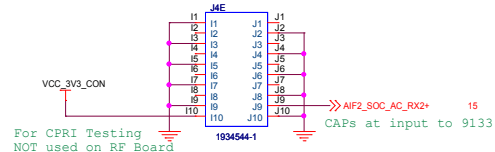
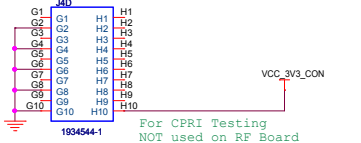
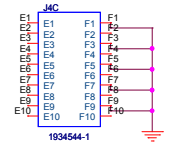
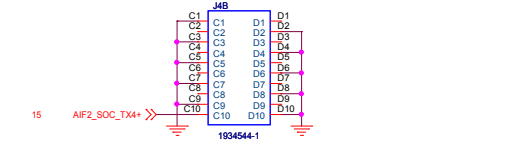
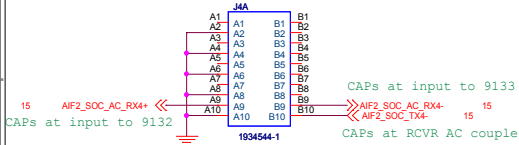


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Front Plane Connectors

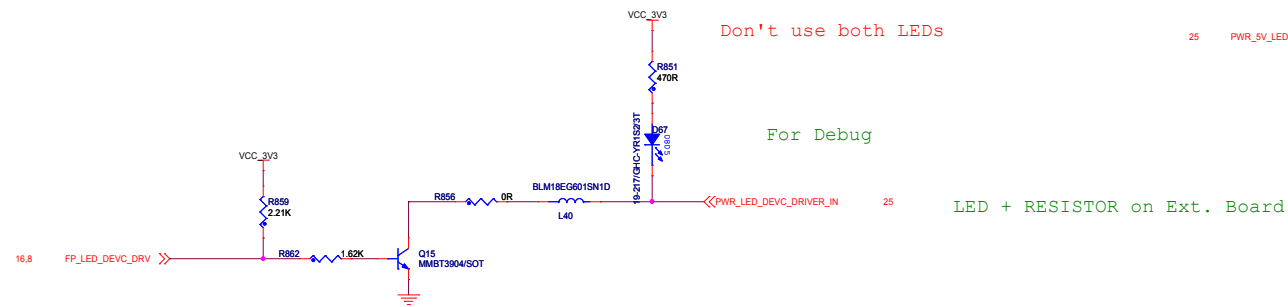
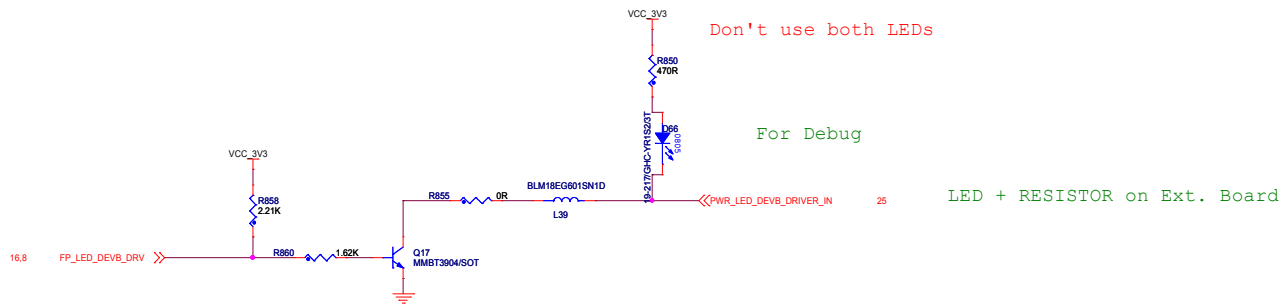
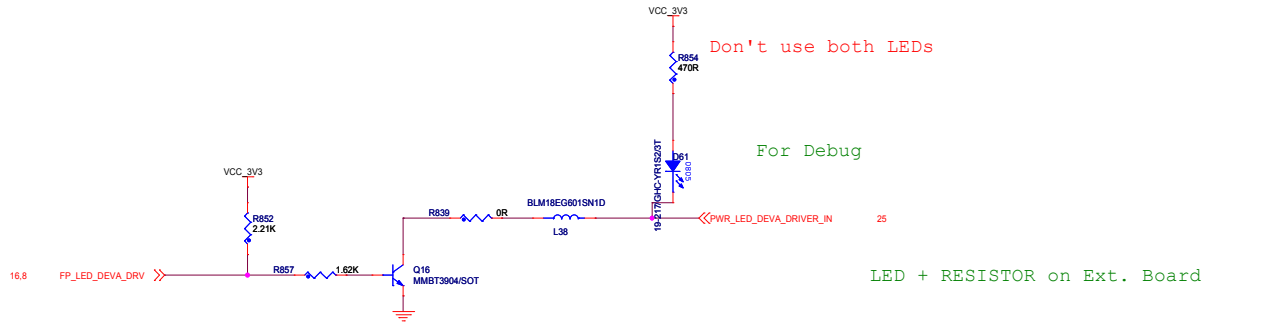


Mezzanine Connector

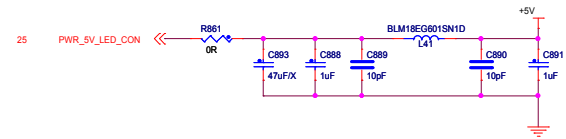


FRONT PANEL LED DRIVERS

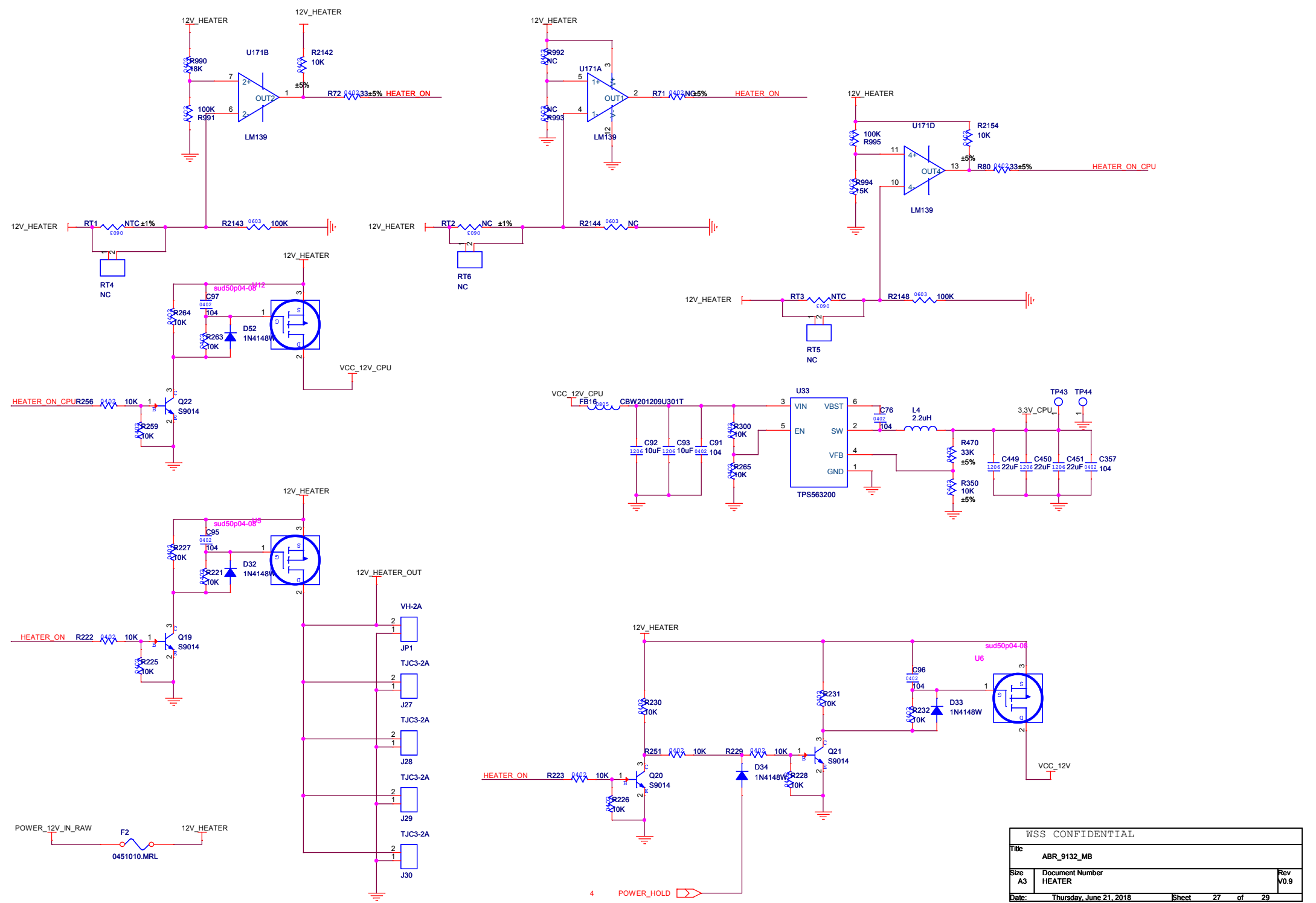
STATUS AND CONTROL LED'S



FRONTPLANE LED PWR SUPPLY



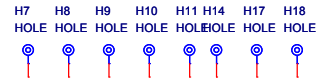
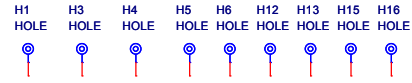
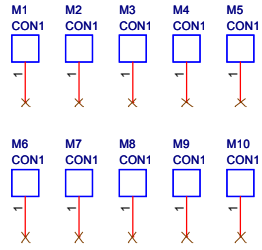
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MACHINAL

MARK POINT



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