Model Based Design Toolbox

User Manual

An Embedded Target for S32K Family of Processors
Version 2.0.0

Target Based Automatic Code Generation Tools
For MATLAB™/Simulink™/Stateflow™ Models working with Simulink Coder ™ and Embedded Coder®

Model Based Design Toolbox Users Manual is for use with the Model Based Design Toolbox, an embedded target and block set library for MATLAB/Simulink/Stateflow Modeling.

MATLAB, Simulink, Stateflow, Handle Graphics, and Real-Time Workshop are registered trademarks, and TargetBox is a trademark of The MathWorks, Inc.

Microsoft and .NET Framework are trademarks of Microsoft Corporation.

Flexera Software, Flexlm, and FlexNet Publisher are registered trademarks or trademarks of Flexera Software, Inc. and/or InstallShield Co. Inc. in the United States of America and/or other countries.

Other product or brand names are trademarks or registered trademarks of their respective holders.

1 Overview 1-16
2 Installation 2-17
2.1 Minimum Platform Requirements 2-17
2.2 Installation Steps 2-17
2.2.1 Run Setup.exe 2-17
2.2.2 Run FreeMASTER Installer 2-17
2.2.3 License Request & Installation 2-17
2.2.4 Setting the Path for Model Based Design Toolbox 2-18
2.2.5 Setting up the Target Compilers 2-18
2.2.6 Setting up the MCU for MBD Toolbox 2-18
2.3 Example Models 2-19
3 Processors Supported 3-20
4 Required and Recommended Products 4-21
4.1 MATLAB Required and Recommended Products 4-21
4.2 Compiler Specific Code 4-21
5 MBD Toolbox Integration into Simulink 5-22
5.1 Target Configuration Block 5-22
5.1.1.1 Block Name 5-22
5.1.1.2 Block Description 5-22
5.1.1.3 Block Image 5-22
5.1.1.4 Configuration Parameters Dialog target-specific Panes and Parameters: 5-22
5.1.1.5 Block Dialog and Parameters: 5-22
5.1.1.6 Block Dependency 5-30
5.1.1.7 Block Miscellaneous Details: 5-30
5.1.1.8 Block Details 5-30
5.1.1.9 Layout of Block GUIs 5-30
5.2 Motor Control Blocks 5-33
5.2.1 ADC Configuration Block 5-33
5.2.1.1 Block Name 5-33
5.2.1.2 Block Description 5-33
5.2.1.3 Block Image 5-33
5.2.1.4 Inputs: 5-34
5.2.1.5 Outputs: 5-34
5.2.1.6 Block Dialog and Parameters: 5-34
5.2.1.7 Block Dependency 5-41
5.2.1.8 Block Miscellaneous Details: 5-41
5.2.2 ADC Start Block 5-41
5.2.2.1 Block Name 5-41
5.2.2.2 Block Description 5-42
5.2.2.3 Block Image 5-42
5.2.2.4 Inputs: 5-42
5.2.2.5 Outputs: 5-42
5.2.2.6 Block Dialog and Parameters: 5-42
5.2.2.7 Block Dependency 5-44
5.2.2.8 Block Miscellaneous Details: 5-44

5.2.3 ADC ISR Block 5-44
5.2.3.1 Block Name 5-44
5.2.3.2 Block Description 5-44
5.2.3.3 Block Image 5-44
5.2.3.4 Inputs: 5-45
5.2.3.5 Outputs: 5-45
5.2.3.6 Block Dialog and Parameters: 5-45
5.2.3.7 Block Dependency 5-45
5.2.3.8 Block Miscellaneous Details: 5-45
5.2.4 CMP Configuration Block 5-46
5.2.4.1 Block Name 5-46
5.2.4.2 Block Description 5-46
5.2.4.3 Block Image 5-46
5.2.4.4 Inputs: 5-46
5.2.4.5 Outputs: 5-46
5.2.4.6 Block Dialog and Parameters: 5-46
5.2.4.7 Block Dependency 5-53
5.2.4.8 Block Miscellaneous Details: 5-53
5.2.5 CMP ISR Enable/Disable Block 5-53
5.2.5.1 Block Name 5-53
5.2.5.2 Block Description 5-54
5.2.5.3 Block Image 5-54
5.2.5.4 Inputs: 5-54
5.2.5.5 Outputs: 5-54
5.2.5.6 Block Dialog and Parameters: 5-54
5.2.5.7 Block Dependency 5-54
5.2.5.8 Block Miscellaneous Details: 5-55
5.2.6 CMP ISR Block 5-55
5.2.6.1 Block Name 5-55
5.2.6.2 Block Description 5-55
5.2.6.3 Block Image 5-55
5.2.6.4 Inputs: 5-55
5.2.6.5 Outputs: 5-55
5.2.6.6 Block Dialog and Parameters: 5-55
5.2.6.7 Block Dependency 5-56
5.2.6.8 Block Miscellaneous Details: 5-56
5.2.6.9 Block Name 5-56
5.2.6.10 Block Description 5-56
5.2.6.11 Block Image 5-56
5.2.6.12 Inputs: 5-56
5.2.6.13 Outputs: 5-57
5.2.6.14 Block Dialog and Parameters: 5-57
5.2.6.15 Block Dependency 5-58
5.2.6.16 Block Miscellaneous Details: 5-58
5.2.7 FTM Independent PWM Output Block 5-58
5.2.7.1 Block Name 5-58

5.2.7.2 Block Description 5-58
5.2.7.3 Block Image 5-58
5.2.7.4 Inputs: 5-59
5.2.7.5 Outputs: 5-59
5.2.7.6 Block Dialog and Parameters: 5-59
5.2.7.7 Block Dependency 5-63
5.2.7.8 Block Miscellaneous Details: 5-63
5.2.8 FTM Complementary PWM Output Block 5-64
5.2.8.1 Block Name 5-64
5.2.8.2 Block Description 5-64
5.2.8.3 Block Image 5-64
5.2.8.4 Inputs: 5-64
5.2.8.5 Outputs: 5-64
5.2.8.6 Block Dialog and Parameters: 5-64
5.2.8.7 Block Dependency 5-68
5.2.8.8 Block Miscellaneous Details: 5-69
5.2.9 FTM Three-phase PWM Output Block 5-69
5.2.9.1 Block Name 5-69
5.2.9.2 Block Description 5-69
5.2.9.3 Block Image 5-69
5.2.9.4 Inputs: 5-69
5.2.9.5 Outputs: 5-69
5.2.9.6 Block Dialog and Parameters: 5-69
5.2.9.7 Block Dependency 5-74
5.2.9.8 Block Miscellaneous Details: 5-75
5.2.10 FTM Frequency Update Block 5-75
5.2.10.1 Block Name 5-75
5.2.10.2 Block Description 5-75
5.2.10.3 Block Image 5-75
5.2.10.4 Inputs: 5-75
5.2.10.5 Outputs: 5-75
5.2.10.6 Block Dialog and Parameters: 5-75
5.2.10.7 Block Dependency 5-76
5.2.10.8 Block Miscellaneous Details: 5-76
5.2.11 FTM PWM Deadtime Update Block 5-76
5.2.11.1 Block Name 5-76
5.2.11.2 Block Description 5-76
5.2.11.3 Block Image 5-76
5.2.11.4 Inputs: 5-76
5.2.11.5 Outputs: 5-76
5.2.11.6 Block Dialog and Parameters: 5-77
5.2.11.7 Block Dependency 5-77
5.2.11.8 Block Miscellaneous Details: 5-77
5.2.12 FTM Channel ISR Block 5-77
5.2.12.1 Block Name 5-77
5.2.12.2 Block Description 5-77

5.2.12.3 Block Image 5-77
5.2.12.4 Inputs: 5-78
5.2.12.5 Outputs: 5-78
5.2.12.6 Block Dialog and Parameters: 5-78
5.2.12.7 Block Dependency 5-78
5.2.12.8 Block Miscellaneous Details: 5-78
5.2.13 FTM Input Edge Capture Block 5-78
5.2.13.1 Block Name 5-78
5.2.13.2 Block Description 5-79
5.2.13.3 Block Image 5-79
5.2.13.4 Inputs: 5-79
5.2.13.5 Outputs: 5-79
5.2.13.6 Block Dialog and Parameters: 5-79
5.2.13.7 Block Dependency 5-82
5.2.13.8 Block Miscellaneous Details: 5-82
5.2.14 FTM Dual Edge Capture Block 5-82
5.2.14.1 Block Name 5-82
5.2.14.2 Block Description 5-82
5.2.14.3 Block Image 5-83
5.2.14.4 Inputs: 5-83
5.2.14.5 Outputs: 5-83
5.2.14.6 Block Dialog and Parameters: 5-83
5.2.14.7 Block Dependency 5-85
5.2.14.8 Block Miscellaneous Details: 5-85
5.2.15 FTM Restart Dual Edge Capture Block 5-85
5.2.15.1 Block Name 5-85
5.2.15.2 Block Description 5-85
5.2.15.3 Block Image 5-86
5.2.15.4 Inputs: 5-86
5.2.15.5 Outputs: 5-86
5.2.15.6 Block Dialog and Parameters: 5-86
5.2.15.7 Block Dependency 5-86
5.2.15.8 Block Miscellaneous Details: 5-86
5.2.16 FTM Quadrature Decoder Block 5-87
5.2.16.1 Block Name 5-87
5.2.16.2 Block Description 5-87
5.2.16.3 Block Image 5-87
5.2.16.4 Inputs: 5-87
5.2.16.5 Outputs: 5-87
5.2.16.6 Block Dialog and Parameters: 5-87
5.2.16.7 Block Dependency 5-90
5.2.16.8 Block Miscellaneous Details: 5-90
5.2.17 FTM Timer Overflow Block 5-90
5.2.17.1 Block Name 5-90
5.2.17.2 Block Description 5-90
5.2.17.3 Block Image 5-90

5.2.17.4 Inputs: 5-90
5.2.17.5 Outputs: 5-91
5.2.17.6 Block Dialog and Parameters: 5-91
5.2.17.7 Block Dependency 5-91
5.2.17.8 Block Miscellaneous Details: 5-91
5.2.18 FTM ISR Enable/Disable Block 5-91
5.2.18.1 Block Name 5-91
5.2.18.2 Block Description 5-91
5.2.18.3 Block Image 5-92
5.2.18.4 Inputs: 5-92
5.2.18.5 Outputs: 5-92
5.2.18.6 Block Dialog and Parameters: 5-92
5.2.18.7 Block Dependency 5-92
5.2.18.8 Block Miscellaneous Details: 5-92
5.3 Communication Blocks 5-93
5.3.1 FCAN Configuration Block 5-93
5.3.1.1 Block Name 5-93
5.3.1.2 Block Description 5-93
5.3.1.3 Block Image 5-93
5.3.1.4 Inputs: 5-93
5.3.1.5 Outputs: 5-93
5.3.1.6 Block Dialog and Parameters: 5-93
5.3.1.7 Block Dependency 5-99
5.3.1.8 Block Miscellaneous Details: 5-99
5.3.2 FCAN Receive Data Block 5-99
5.3.2.1 Block Name 5-99
5.3.2.2 Block Description 5-99
5.3.2.3 Block Image 5-99
5.3.2.4 Inputs: 5-99
5.3.2.5 Outputs: 5-99
5.3.2.6 Block Dialog and Parameters: 5-99
5.3.2.7 Block Dependency 5-100
5.3.2.8 Block Miscellaneous Details: 5-100
5.3.3 FCAN Receive Data Trigger Block 5-100
5.3.3.1 Block Name 5-100
5.3.3.2 Block Description 5-100
5.3.3.3 Block Image 5-101
5.3.3.4 Inputs: 5-101
5.3.3.5 Outputs: 5-101
5.3.3.6 Block Dialog and Parameters: 5-101
5.3.3.7 Block Dependency 5-102
5.3.3.8 Block Miscellaneous Details: 5-102
5.3.4 FCAN Transmit Block 5-102
5.3.4.1 Block Name 5-102
5.3.4.2 Block Description 5-102
5.3.4.3 Block Image 5-102

5.3.4.4 Inputs:.....5-103
5.3.4.5 Outputs:.....5-103
5.3.4.6 Block Dialog and Parameters:.....5-103
5.3.4.7 Block Dependency.....5-103
5.3.4.8 Block Miscellaneous Details:.....5-103
5.3.5 FCAN ISR Block.....5-104
5.3.5.1 Block Name.....5-104
5.3.5.2 Block Description.....5-104
5.3.5.3 Block Image.....5-104
5.3.5.4 Inputs:.....5-104
5.3.5.5 Outputs:.....5-104
5.3.5.6 Block Dialog and Parameters:.....5-104
5.3.5.7 Block Dependency.....5-105
5.3.5.8 Block Miscellaneous Details:.....5-105
5.3.6 FCAN ISR Enable/Disable.....5-105
5.3.6.1 Block Name.....5-105
5.3.6.2 Block Description.....5-105
5.3.6.3 Block Image.....5-105
5.3.6.4 Inputs:.....5-105
5.3.6.5 Outputs:.....5-106
5.3.6.6 Block Dialog and Parameters:.....5-106
5.3.6.7 Block Dependency.....5-107
5.3.6.8 Block Miscellaneous Details:.....5-107
5.3.7 LPI2C Configuration Block.....5-107
5.3.7.1 Block Name.....5-107
5.3.7.2 Block Description.....5-107
5.3.7.3 Block Image.....5-107
5.3.7.4 Inputs:.....5-108
5.3.7.5 Outputs:.....5-108
5.3.7.6 Block Dialog and Parameters:.....5-108
5.3.7.7 Block Dependency.....5-110
5.3.7.8 Block Miscellaneous Details:.....5-110
5.3.8 LPI2C Transmit Block.....5-110
5.3.8.1 Block Name.....5-110
5.3.8.2 Block Description.....5-110
5.3.8.3 Block Image.....5-110
5.3.8.4 Inputs:.....5-110
5.3.8.5 Outputs:.....5-110
5.3.8.6 Block Dialog and Parameters:.....5-110
5.3.8.7 Block Dependency.....5-111
5.3.8.8 Block Miscellaneous Details:.....5-111
5.3.9 LPI2C Receive Block.....5-111
5.3.9.1 Block Name.....5-111
5.3.9.2 Block Description.....5-111
5.3.9.3 Block Image.....5-111
5.3.9.4 Inputs:.....5-111

5.3.9.5 Outputs: 5-112
5.3.9.6 Block Dialog and Parameters: 5-112
5.3.9.7 Block Dependency 5-112
5.3.9.8 Block Miscellaneous Details: 5-112
5.3.10 LPI2C ISR Block 5-113
5.3.10.1 Block Name 5-113
5.3.10.2 Block Description 5-113
5.3.10.3 Block Image 5-113
5.3.10.4 Inputs: 5-113
5.3.10.5 Outputs: 5-113
5.3.10.6 Block Dialog and Parameters: 5-113
5.3.10.7 Block Dependency 5-114
5.3.10.8 Block Miscellaneous Details: 5-114
5.3.11 LPI2C ISR Enable/Disable Block 5-115
5.3.11.1 Block Name 5-115
5.3.11.2 Block Description 5-115
5.3.11.3 Block Image 5-116
5.3.11.4 Inputs: 5-116
5.3.11.5 Outputs: 5-116
5.3.11.6 Block Dialog and Parameters: 5-116
5.3.11.7 Block Dependency 5-117
5.3.11.8 Block Miscellaneous Details: 5-117
5.3.12 LPSPI Configuration Block 5-117
5.3.12.1 Block Name 5-117
5.3.12.2 Block Description 5-117
5.3.12.3 Block Image 5-118
5.3.12.4 Inputs: 5-118
5.3.12.5 Outputs: 5-118
5.3.12.6 Block Dialog and Parameters: 5-118
5.3.12.7 Block Dependency 5-123
5.3.12.8 Block Miscellaneous Details: 5-123
5.3.13 LPSPI Transmit Block 5-123
5.3.13.1 Block Name 5-123
5.3.13.2 Block Description 5-123
5.3.13.3 Block Image 5-124
5.3.13.4 Inputs: 5-124
5.3.13.5 Outputs: 5-124
5.3.13.6 Block Dialog and Parameters: 5-124
5.3.13.7 Block Dependency 5-124
5.3.13.8 Block Miscellaneous Details: 5-124
5.3.14 LPSPI Receive Block 5-124
5.3.14.1 Block Name 5-124
5.3.14.2 Block Description 5-125
5.3.14.3 Block Image 5-125
5.3.14.4 Inputs: 5-125
5.3.14.5 Outputs: 5-125

5.3.14.6 Block Dialog and Parameters: 5-125
5.3.14.7 Block Dependency 5-125
5.3.14.8 Block Miscellaneous Details: 5-125
5.3.14.9 5-125
5.3.14.10 Block Name 5-126
5.3.14.11 Block Description 5-126
5.3.14.12 Block Image 5-126
5.3.14.13 Inputs: 5-126
5.3.14.14 Outputs: 5-126
5.3.14.15 Block Dialog and Parameters: 5-126
5.3.14.16 Block Dependency 5-127
5.3.14.17 Block Miscellaneous Details: 5-127
5.3.15 LPSPI ISR Block 5-127
5.3.15.1 Block Name 5-127
5.3.15.2 Block Description 5-127
5.3.15.3 Block Image 5-127
5.3.15.4 Inputs: 5-127
5.3.15.5 Outputs: 5-127
5.3.15.6 Block Dialog and Parameters: 5-127
5.3.15.7 Block Dependency 5-128
5.3.15.8 Block Miscellaneous Details: 5-128
5.3.16 LPSPI Receive Trigger Block 5-130
5.3.16.1 Block Name 5-130
5.3.16.2 Block Description 5-130
5.3.16.3 Block Image 5-130
5.3.16.4 Inputs: 5-130
5.3.16.5 Outputs: 5-130
5.3.16.6 Block Dialog and Parameters: 5-130
5.3.16.7 Block Dependency 5-131
5.3.16.8 Block Miscellaneous Details: 5-131
5.3.17 LPSPI ISR Enable/Disable Block 5-131
5.3.17.1 Block Name 5-131
5.3.17.2 Block Description 5-131
5.3.17.3 Block Image 5-131
5.3.17.4 Inputs: 5-131
5.3.17.5 Outputs: 5-131
5.3.17.6 Block Dialog and Parameters: 5-131
5.3.17.7 Block Dependency 5-132
5.3.17.8 Block Miscellaneous Details: 5-133
5.3.18 LPUART Configuration Block 5-133
5.3.18.1 Block Name 5-133
5.3.18.2 Block Description 5-133
5.3.18.3 Block Image 5-133
5.3.18.4 Inputs: 5-133
5.3.18.5 Outputs: 5-133
5.3.18.6 Block Dialog and Parameters: 5-133

5.3.18.7 Block Dependency 5-140
5.3.18.8 Block Miscellaneous Details: 5-140
5.3.19 LPUART Transmit Block 5-140
5.3.19.1 Block Name 5-140
5.3.19.2 Block Description 5-140
5.3.19.3 Block Image 5-141
5.3.19.4 Inputs: 5-141
5.3.19.5 Outputs: 5-141
5.3.19.6 Block Dialog and Parameters: 5-141
5.3.19.7 Block Dependency 5-141
5.3.19.8 Block Miscellaneous Details: 5-141
5.3.20 LPUART Receive Block 5-141
5.3.20.1 Block Name 5-141
5.3.20.2 Block Description 5-142
5.3.20.3 Block Image 5-142
5.3.20.4 Inputs: 5-142
5.3.20.5 Outputs: 5-142
5.3.20.6 Block Dialog and Parameters: 5-142
5.3.20.7 Block Dependency 5-142
5.3.20.8 Block Miscellaneous Details: 5-142
5.3.21 LPUART Receive/Transmit ISR Block 5-143
5.3.21.1 Block Name 5-143
5.3.21.2 Block Description 5-143
5.3.21.3 Block Image 5-143
5.3.21.4 Inputs: 5-143
5.3.21.5 Outputs: 5-143
5.3.21.6 Block Dialog and Parameters: 5-143
5.3.21.7 Block Dependency 5-144
5.3.21.8 Block Miscellaneous Details: 5-144
5.3.22 LPUART Error ISR Block 5-145
5.3.22.1 Block Name 5-145
5.3.22.2 Block Description 5-145
5.3.22.3 Block Image 5-145
5.3.22.4 Inputs: 5-145
5.3.22.5 Outputs: 5-145
5.3.22.6 Block Dialog and Parameters: 5-145
5.3.22.7 Block Dependency 5-146
5.3.22.8 Block Miscellaneous Details: 5-146
5.3.23 LPUART ISR Enable/Disable Block 5-147
5.3.23.1 Block Name 5-147
5.3.23.2 Block Description 5-147
5.3.23.3 Block Image 5-147
5.3.23.4 Inputs: 5-147
5.3.23.5 Outputs: 5-147
5.3.23.6 Block Dialog and Parameters: 5-147
5.3.23.7 Block Dependency 5-149

5.3.23.8 Block Miscellaneous Details: 5-149
5.4 Peripheral Interface Blocks 5-149
5.4.1 GPIO Digital Input Block 5-149
5.4.1.1 Block Name 5-149
5.4.1.2 Block Description 5-149
5.4.1.3 Block Image 5-150
5.4.1.4 Inputs: 5-150
5.4.1.5 Outputs: 5-150
5.4.1.6 Block Dialog Parameters: 5-150
5.4.1.7 Block Dependency 5-151
5.4.1.8 Block Miscellaneous Details: 5-151
5.4.2 GPIO Digital Output Block 5-151
5.4.2.1 Block Name 5-151
5.4.2.2 Block Description 5-151
5.4.2.3 Block Image 5-151
5.4.2.4 Inputs: 5-151
5.4.2.5 Outputs: 5-152
5.4.2.6 Block Dialog and Parameters: 5-152
5.4.2.7 Block Dependency 5-152
5.4.2.8 Block Miscellaneous Details: 5-152
5.4.3 GPIO Digital Input ISR Block 5-152
5.4.3.1 Block Name 5-152
5.4.3.2 Block Description 5-152
5.4.3.3 Block Image 5-153
5.4.3.4 Inputs: 5-153
5.4.3.5 Outputs: 5-153
5.4.3.6 Block Dialog and Parameters: 5-153
5.4.3.7 Block Dependency 5-154
5.4.3.8 Block Miscellaneous Details: 5-154
5.4.4 GPIO Digital Input ISR Enable/Disable Block 5-154
5.4.4.1 Block Name 5-154
5.4.4.2 Block Description 5-154
5.4.4.3 Block Image 5-154
5.4.4.4 Inputs: 5-154
5.4.4.5 Outputs: 5-155
5.4.4.6 Block Dialog and Parameters: 5-155
5.4.4.7 Block Dependency 5-155
5.4.4.8 Block Miscellaneous Details: 5-155
5.4.5 GPIO Glitch Filter Block 5-156
5.4.5.1 Block Name 5-156
5.4.5.2 Block Description 5-156
5.4.5.3 Block Image 5-156
5.4.5.4 Inputs: 5-156
5.4.5.5 Outputs: 5-156
5.4.5.6 Block Dialog and Parameters: 5-156
5.4.5.7 Block Dependency 5-157

5.4.5.8 Block Miscellaneous Details: 5-157
5.4.6 Programmable Delay Configuration Block 5-157
5.4.6.1 Block Name 5-157
5.4.6.2 Block Description 5-157
5.4.6.3 Block Image 5-157
5.4.6.4 Inputs: 5-158
5.4.6.5 Outputs: 5-158
5.4.6.6 Block Dialog and Parameters: 5-158
5.4.6.7 Block Dependency 5-164
5.4.6.8 Block Miscellaneous Details: 5-164
5.4.7 PDB Interrupt Block 5-164
5.4.7.1 Block Name 5-164
5.4.7.2 Block Description 5-165
5.4.7.3 Block Image 5-165
5.4.7.4 Inputs: 5-165
5.4.7.5 Outputs: 5-165
5.4.7.6 Block Dialog and Parameters: 5-165
5.4.7.7 Block Dependency 5-166
5.4.7.8 Block Miscellaneous Details: 5-166
5.4.8 PDB Interrupt Enable/Disable Block 5-166
5.4.8.1 Block Name 5-166
5.4.8.2 Block Description 5-166
5.4.8.3 Block Image 5-166
5.4.8.4 Inputs: 5-167
5.4.8.5 Outputs: 5-167
5.4.8.6 Block Dialog and Parameters: 5-167
5.4.8.7 Block Dependency 5-168
5.4.8.8 Block Miscellaneous Details: 5-168
5.4.9 PDB Start Soft Trigger Block 5-168
5.4.9.1 Block Name 5-168
5.4.9.2 Block Description 5-168
5.4.9.3 Block Image 5-168
5.4.9.4 Inputs: 5-168
5.4.9.5 Outputs: 5-168
5.4.9.6 Block Dialog and Parameters: 5-168
5.4.9.7 Block Dependency 5-169
5.4.9.8 Block Miscellaneous Details: 5-169
5.4.10 PDB Update Block 5-169
5.4.10.1 Block Name 5-169
5.4.10.2 Block Description 5-169
5.4.10.3 Block Image 5-169
5.4.10.4 Inputs (if selected): 5-169
5.4.10.5 Outputs: 5-170
5.4.10.6 Block Dialog and Parameters: 5-170
5.4.10.7 Block Dependency 5-172
5.4.10.8 Block Miscellaneous Details: 5-172

5.5 Utility Blocks 5-172
5.5.1 Periodic Interrupt Timer Block 5-172
5.5.1.1 Block Name 5-172
5.5.1.2 Block Description 5-172
5.5.1.3 Block Image 5-173
5.5.1.4 Inputs: 5-173
5.5.1.5 Outputs: 5-173
5.5.1.6 Block Dialog and Parameters: 5-173
5.5.1.7 Block Dependency 5-174
5.5.1.8 Block Miscellaneous Details: 5-174
5.5.2 PIT ISR Enable/Disable Block 5-174
5.5.2.1 Block Name 5-174
5.5.2.2 Block Description 5-174
5.5.2.3 Block Image 5-174
5.5.2.4 Inputs: 5-174
5.5.2.5 Outputs: 5-175
5.5.2.6 Block Dialog and Parameters: 5-175
5.5.2.7 Block Dependency 5-175
5.5.2.8 Block Miscellaneous Details: 5-175
5.5.3 Memory Read Block 5-175
5.5.3.1 Block Name 5-175
5.5.3.2 Block Description 5-175
5.5.3.3 Block Image 5-176
5.5.3.4 Inputs: 5-176
5.5.3.5 Outputs: 5-176
5.5.3.6 Block Dialog and Parameters: 5-176
5.5.3.7 Block Dependency 5-177
5.5.3.8 Block Miscellaneous Details: 5-177
5.5.4 Memory Write Block 5-177
5.5.4.1 Block Name 5-177
5.5.4.2 Block Description 5-177
5.5.4.3 Block Image 5-177
5.5.4.4 Inputs: 5-177
5.5.4.5 Outputs: 5-177
5.5.4.6 Block Dialog and Parameters: 5-177
5.5.4.7 Block Dependency 5-178
5.5.4.8 Block Miscellaneous Details: 5-178
5.5.5 Profiler Function Block 5-178
5.5.5.1 Block Name 5-179
5.5.5.2 Block Description 5-179
5.5.5.3 Block Image 5-179
5.5.5.4 Inputs: 5-179
5.5.5.5 Outputs: 5-179
5.5.5.6 Block Dialog and Parameters: 5-179
5.5.5.7 Block Dependency 5-180
5.5.5.8 Block Miscellaneous Details: 5-180

5.5.6 FreeMASTER Data Recorder Block 5-180
5.5.6.1 Block Name 5-180
5.5.6.2 Block Description 5-180
5.5.6.3 Block Image 5-180
5.5.6.4 Inputs: 5-180
5.5.6.5 Outputs: 5-181
5.5.6.6 Block Dialog and Parameters: 5-181
5.5.6.7 Block Dependency 5-181
5.5.6.7.1 Block Miscellaneous Details: 5-181
5.5.6.8 Initialization Call Insertion Block 5-181
5.5.6.9 Block Name 5-181
5.5.6.10 Block Description 5-181
5.5.6.11 Block Image 5-181
5.5.6.12 Inputs: 5-181
5.5.6.13 Outputs: 5-182
5.5.6.14 Block Dialog and Parameters: 5-182
5.5.6.15 Block Dependency 5-182
5.5.6.16 Block Miscellaneous Details: 5-182
6 Embedded Targets 6-183
6.1 User-Specific Files Needed for Build 6-183
6.2 Using Interrupt Service Routine (ISR) Blocks 6-183
7 FreeMASTER Interface 7-184
8 Bootloader 8-186
9 PIL/SIL Operational Mode 9-187
9.1 PIL & SIL Automatic Configuration 9-187
9.2 PIL & SIL Manual Configuration 9-188
10 S32DS for ARM Project File Generation 10-190

1 Overview

The Model Based Design Toolbox is a development toolbox to allow controls engineers to move quickly from the modeling and simulation environment to the target processor environment with ease. The toolbox contains peripheral driver interface blocks, a code generation target for the S32K14x family of processors, optimized target code blocks for the S32K14x processor, and support for model reference Software-In-the-Loop (SIL) / Processor-In-the-Loop (PIL) code generation and co-simulation testing. It works well in conjunction with the NXP Automotive Math and Motor Control Library which are used for Field Oriented Control applications.

Using the Model Based Design Toolbox the user can move from the modeling and simulation environment quickly to the target processor environment. The user can then profile execution in the target environment and quickly build and prototype new functions and features understanding the performance and memory cost of the implementation through automatic code generation technology. The toolbox allows the user to perform experiments on determination of best silicon configuration on target for the prototyped application.

2 Installation

Installing the Model Based Design Toolbox is your first step to getting up and running on the target processor. Please follow the installation steps below, and then explore the examples.

2.1 Minimum Platform Requirements

The minimum recommended PC platform is:

- *Windows® OS*: Intel® Pentium® 4 processor, 2 GHz or faster, Intel® Xeon™, Intel® Core™, AMD Athlon™ 64, AMD Opteron™, or later
- At least 4 GB of RAM
- At least 3 GB of free disk space.
- Internet connectivity for web downloads.

Operating System Hosts

Windows			
Host OS	**SP Level**	**32-bit**	**64-bit**
Windows 7	SP1	X	X
Windows 8.1	U1	X	X
Windows 10		X	X

2.2 Installation Steps

1. Run setup.exe
2. Run FreeMASTER Installer from Model Based Development Toolbox Menu
3. Request and Install license file
4. Setup the MATLAB path for Model Based Development Toolbox
5. Set the Target Compiler Environment Variables
6. Setup the MCU for MBD Toolbox

2.2.1 Run Setup.exe

Install the Model Based Design Toolbox by running the Setup.exe; this will activate the installer. Click through the dialogs entering in the appropriate location for the installation. It is best if this is NOT installed on a network drive.

2.2.2 Run FreeMASTER Installer

1. START->Programs->Model Based Design Toolbox for S32K MCUs ->FreeMASTER Installer->FreeMASTER v2.0 Installer

2.2.3 License Request & Installation

Please refer to *Model_Based_Design_Toolbox_License_Installation.pdf* for more information on how to request and install the license.

2.2.4 Setting the Path for Model Based Design Toolbox

In the toolbox the path needs to be setup in the MATLAB environment. This is done by navigating the MATLAB Current Directory to the MBD Toolbox/mbdtbx_S32K installation directory and running the "`mbd_s32k_path`" script.

```
>> mbd_s32k_path
Treating 'c:\MBDToolbox\mbdt_s32k' as MBD Toolbox installation root.
MBD Toolbox path prepended.
Successful.
>>
```

2.2.5 Setting up the Target Compilers

The target compiler for Model Based Design Toolbox to use will need to be configured. The GCC compiler has been included in the installation of MBD Toolbox, and the environment variable has been set for you. However, if you choose to use the IAR compiler or perhaps a different version of the GCC compiler, you will either need to add or update the compiler environment variable.

Ensure a system environment variable called <COMPILER_STRING>_TOOL is defined to value as shown below:

GCC_S32K_TOOL = c:\NXP\S32DS_ARM_v1.3\Cross_Tools\gcc-arm-none-eabi-4_9
IAR_TOOL = C:\IAR_Systems\EW_7_5
GHS_TOOL = C:\ghs\comp_201516

Note: Once Environmental variables are setup you will need to restart MATLAB for the environment to see these.

2.2.6 Setting up the MCU for MBD Toolbox

To prepare the MCU to accept download requests from the MBD Toolbox a boot loader needs to be loaded into flash memory by a programmer/debugger tool. Once this is done the MBD Toolbox will be able to download the application code generated from the model to perform PIL operations or to execute in stand-alone. The s-record file that needs to be manually programmed into the MCU is SK144_Bootloader.rbf. This s-record contains the code for the boot loader that communicates with the MBD Toolbox. It is located in the MBD Toolbox installation directory under: ...\tools\BootLoader\RBF_Files. Once the boot loader is programmed and the MCU is reset, it is ready to receive application code from the Toolbox. The boot loader will stay resident until erased by the user.

If the user prefers to program the application code generated by toolbox with a separate programmer or debugger then the boot loader is not required. To perform PIL operation, however, the boot loader is required.

2.3 Example Models

The Model Based Design Toolbox includes many demonstration models showing many different uses of the target peripheral blocks and optimized code blocks. All models have been saved in MATLAB version R2015b.

In mbdtbx_s32k14 directory all examples are grouped by functionality in subfolders e.g. adc, ftm or gflib. To open an example, go to the following path “Model Based Design Toolbox for S32K Series->S32K->S32K14x Examples” using “Simulink Library Browser”.

3 Processors Supported

The Model Based Design Toolbox for S32K MCUs Version 2.0.0 supports the S32K14x Processor. Testing has been completed on pre-production qualified parts.

4 Required and Recommended Products

The required products are those that are a minimum for the Model Based Design Toolbox to work. The recommended products are those that the toolbox has been tested with and would fit within the use case of embedded controls development for on-target rapid prototyping.

4.1 MATLAB Required and Recommended Products

Product	*Version Compatibility*	*Required or Recommended*
MATLAB	R2015B - R2017A	Required
Simulink	R2015B - R2017A	Required
MATLAB Coder	R2015B - R2017A	Required
Embedded Coder	R2015B - R2017A	Required
Simulink Coder	R2015B - R2017A	Required
Stateflow	R2015B - R2017A	Recommended
IEC Certification Kit (for ISO 26262)	R2015B - R2017A	Recommended

4.2 Compiler Specific Code

Model Based Design Toolbox supports code generation for the GCC, GHS and IAR. The C and assembly code generated is specific to these compilers.

Compiler	Versions Tested
GNU Tools for ARM Embedded Processors	V4.9.3
IAR for ARM	V7.50.3.10732/W32 for ARM
GHS	V2015.1.4

5 MBD Toolbox Integration into Simulink

5.1 Target Configuration Block

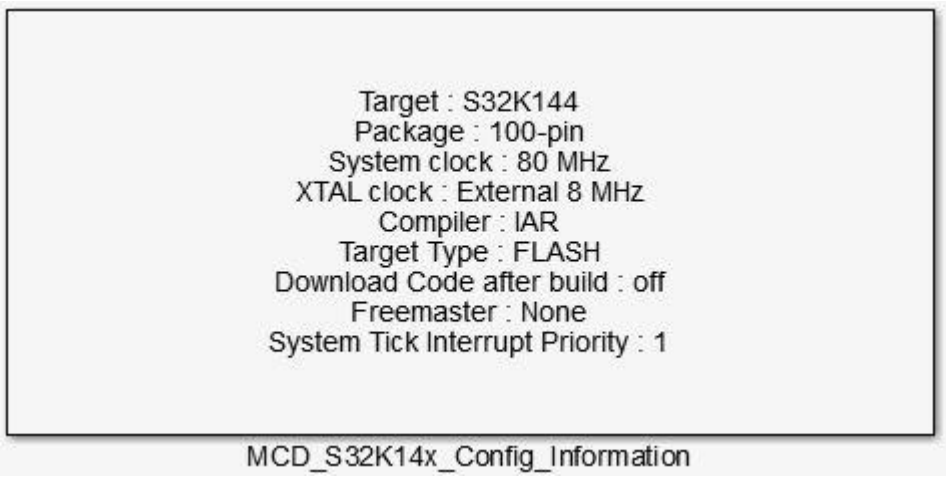
5.1.1.1 Block Name

Target Configuration Block

5.1.1.2 Block Description

The main functionality of the block is to configure the MCU target by opening Configuration Parameters Dialog.

5.1.1.3 Block Image



5.1.1.4 Configuration Parameters Dialog target-specific Panes and Parameters:

The Configuration Parameters dialog contains the following target-specific panes:

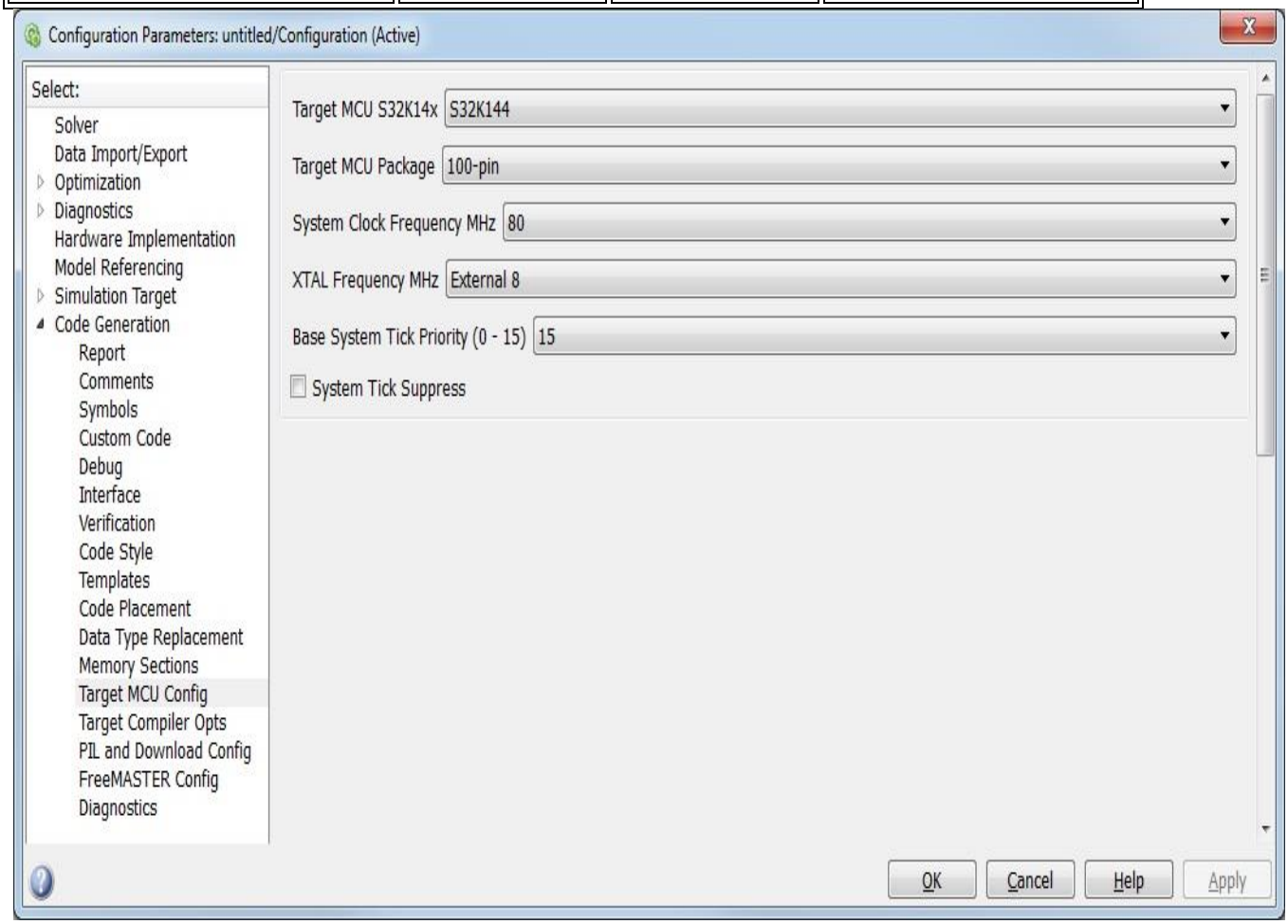
- Target MCU
- Target Compiler Opts
- PIL and Download Config
- FreeMASTER Config
- Diagnostics

- The Target MCU Pane contains the following parameters:

5.1.1.5 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Target MCU S32K14x	List-box	S32K142 S32K144 S32K146	

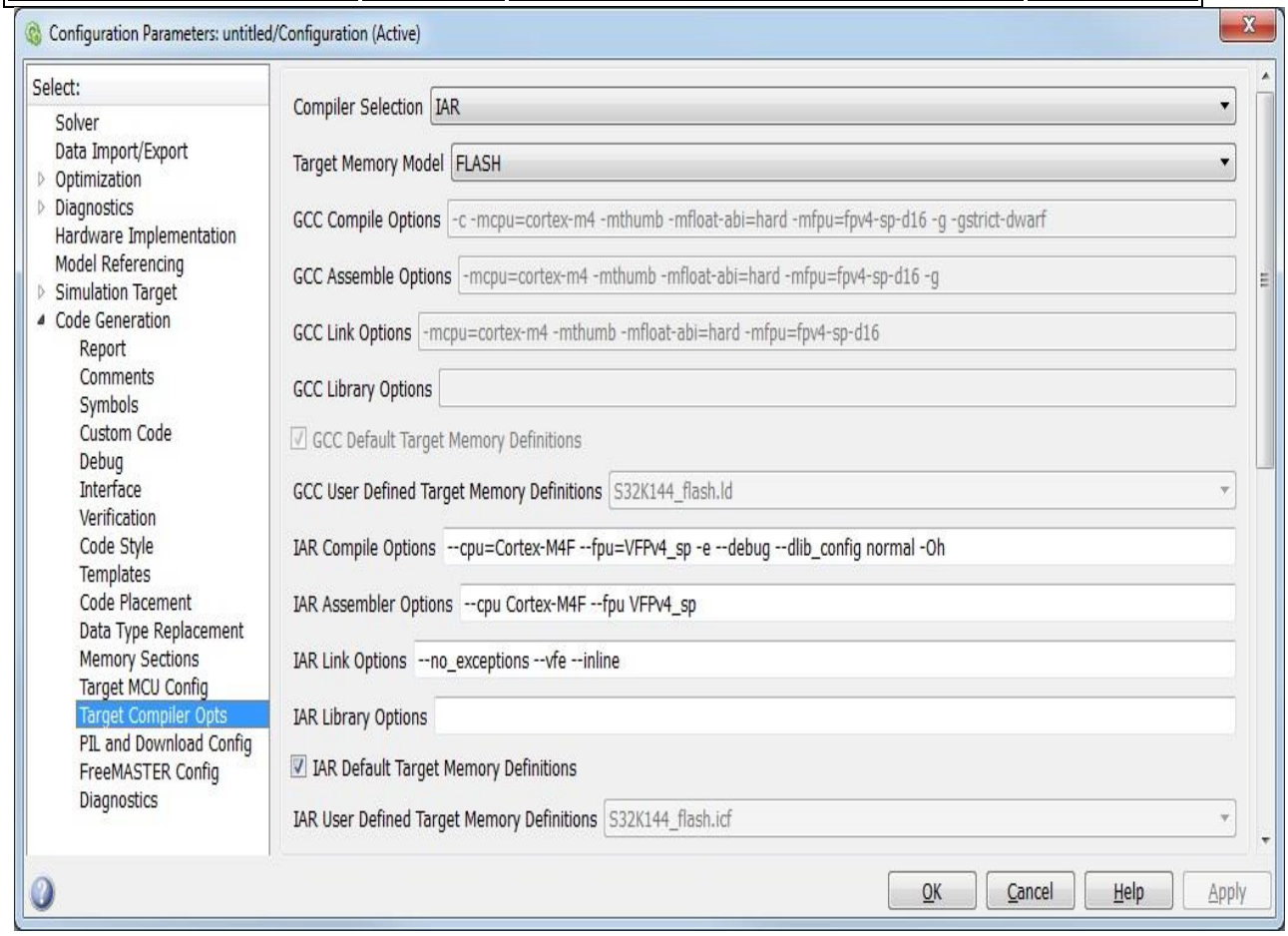
		S32K148	
Target MCU Package	Pop-up	64=pin 100-pin 144-pin 176-pin	
System Clock Frequency MHz	List-box	80 112	System Clock Value
XTAL Frequency MHz	List-box	External 8 External 40	External Crystal clock
Base System Tick Priority	List-box	0 – 15	Priority level of System Tick interrupt
System Tick Suppress	Check-box	Enable/Disable	



- The Target Compiler Opts Pane contains the following parameters:

Names	Selection Types	Range	Description
Generate S32 Design Studio ProjectInfo.xml file	Check-box	Enable/Disable	This enables the generation of a S32 Design Studio project file, when building a model. This option is only available when GCC is selected compiler.
Compiler Selection	List-box	IAR GCC	
Target Memory Model	Pop-up	FLASH	
GCC Compile Options	Text-box	-c -mcpu=cortex-m4 -mthumb -mfloat-abi=hard -mfpu=fpv4-sp-d16 -g -gstrict-dwarf	Default Compile Options
GCC Assemble Options	Text-box	-mcpu=cortex-m4 -mthumb -mfloat-abi=hard -mfpu=fpv4-sp-d16 -g	Default Assemble Options
GCC Link Options	Text-box	-mcpu=cortex-m4 -mthumb -mfloat-abi=hard -mfpu=fpv4-sp-d16	Default Link Options
GCC Library Options	Text-box	None	Default Library Options
IAR Compile Options	Text-box	--cpu=Cortex-M4F --fpu=VFPv4_sp -e --debug --dlib_config normal -Oh	Default Compile Options
IAR Assemble Options	Text-box	--cpu Cortex-M4F --fpu VFPv4_sp	Default Assemble Options
IAR Link Options	Text-box	--no_exceptions --vfe --inline	Default Link

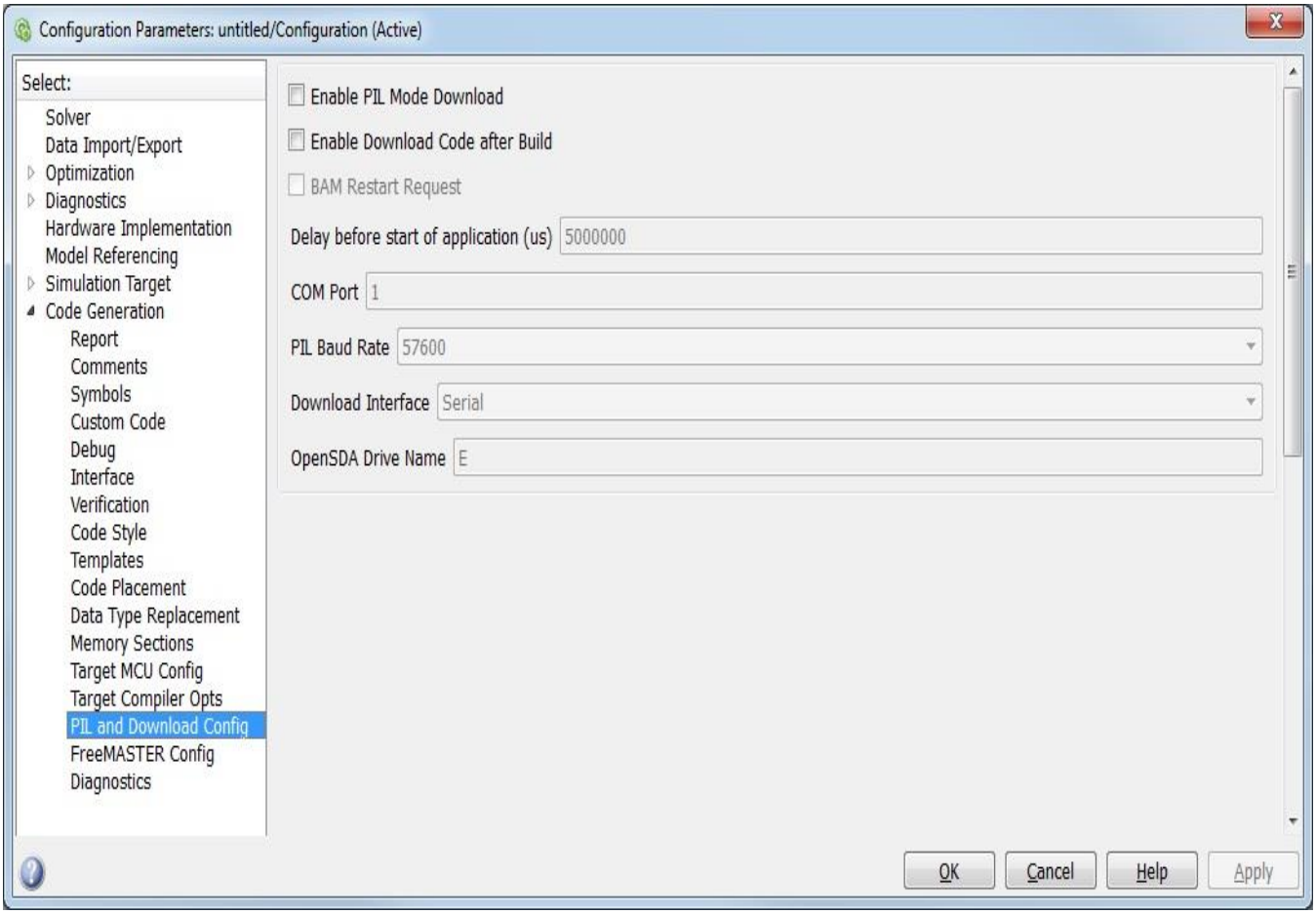
			Options
IAR Library Options	Text-box	None	Default Library Options
IAR Default Target Memory Definitions	Check-box	On/Off	
IAR User Defined Target Memory Definitions	List-box	List of available .icf files in iar_specific_files folder	



- The PIL and Download Config Pane contains the following parameters:

Names	Selection Types	Range	Description
Enable PIL Mode Download	Check-box	On/Off	If PIL simulation mode should be supported.
Enable Download Code after Build	Check-box	On/Off	If application code should be downloaded into target after

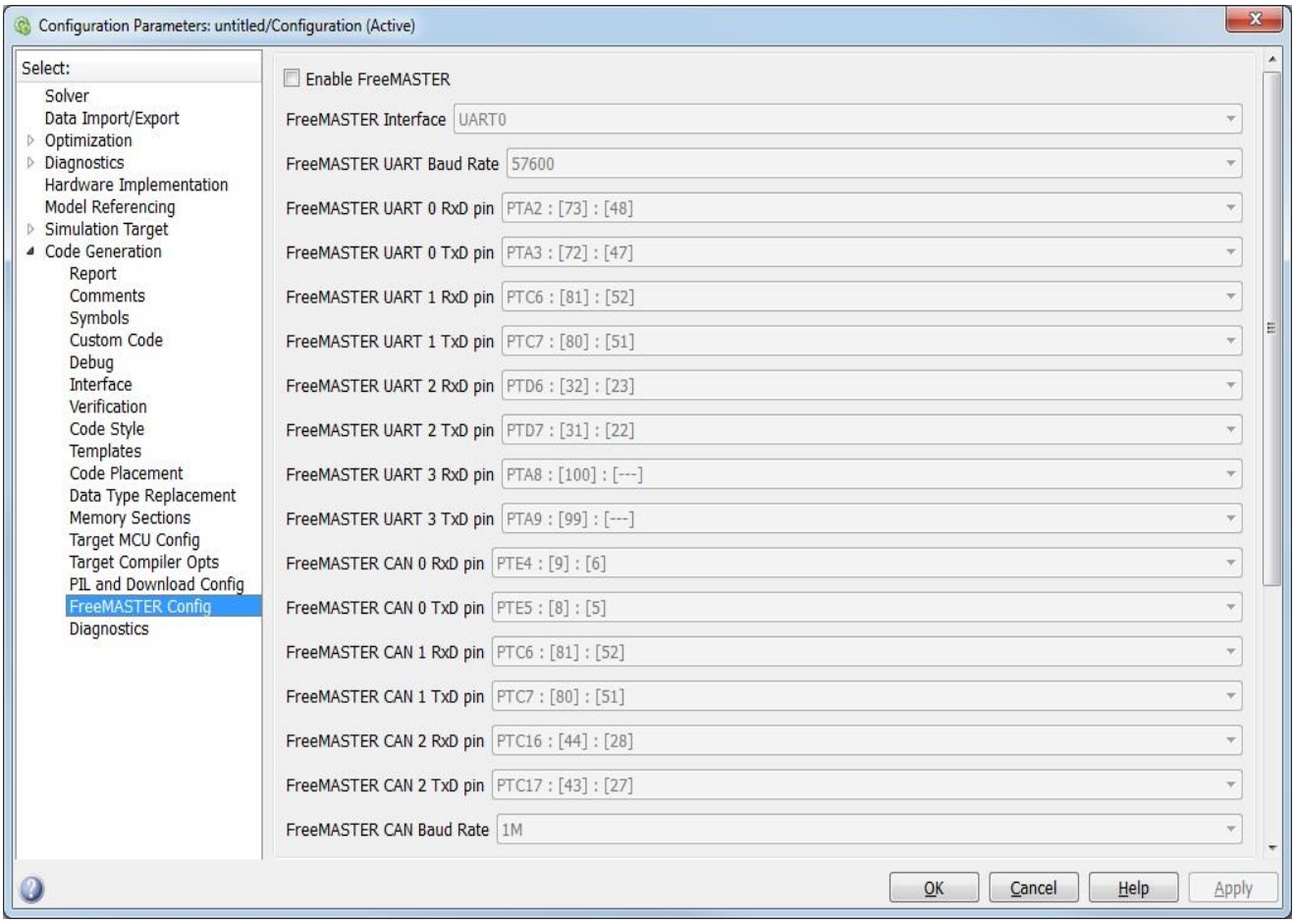
			build
BAM Restart Request	Check-box	On/Off	If Prompt Dialog should be shown before target reset
Delay before start application	Text-box		Delay in milliseconds before application start
COM Port	Text-box		COM port for PIL and BootLoader communication
PIL Baud Rate	List-box	9600 14400 19200 38400 56000 57600 115200	Baud rate for PIL and Bootloader communication
Download Interface	List-box	Serial OpenSDA	Choose Download method for application Serial (uses bootloader) or OpenSDA (no bootloader)
OpenSDA Drive Name	Text-box	Drive Letter	Drive letter that shows up on computer when OpenSDA connection is connected.



- The FreeMASTER Config Pane contains the following parameters:

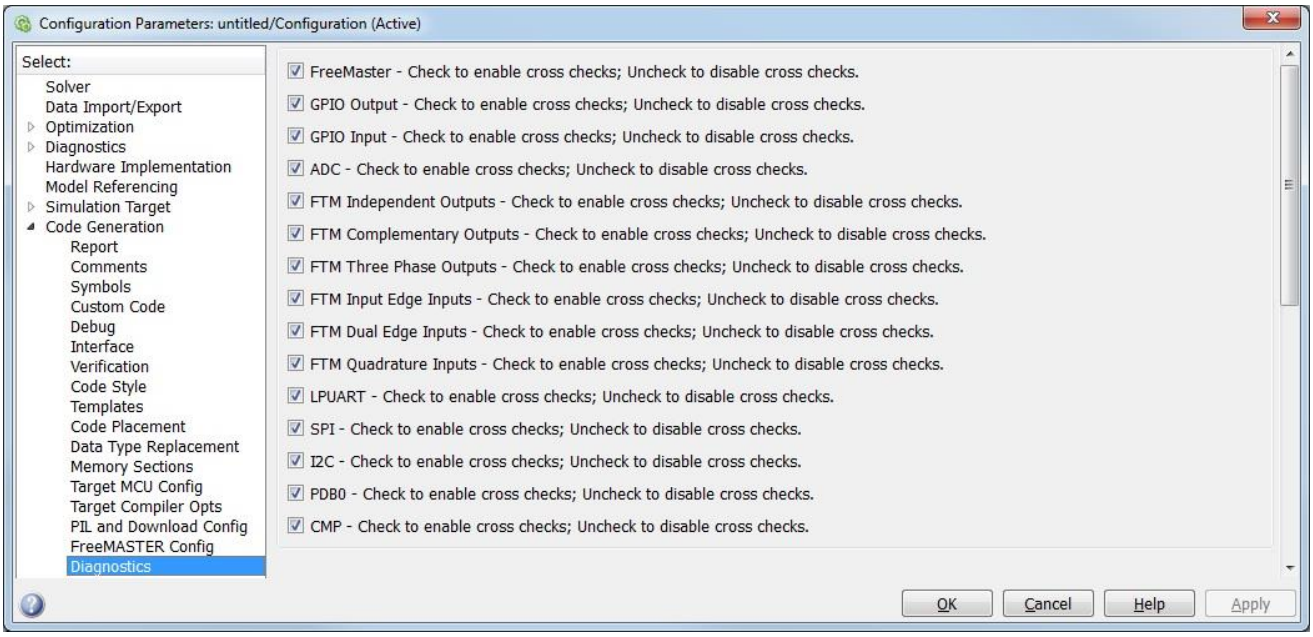
Names	Selection Types	Range	Description
Enable FreeMASTER	Check-box	Enable/Disable	
FreeMASTER Interface	List-box	UART 0 UART 1 UART 2 UART 3 CAN 0 CAN 1 CAN 2	
FreeMASTER UART Baud Rate	List-box	1200 2400 4800 9600 14400 19200	

		38400 56000 57600 115200 128000 256000	
FreeMASTER UART 0 RxD Pin	List-box	PTA2 PTB0	
FreeMASTER UART 0 TxD Pin	List-box	PTA3 PTB1	
FreeMASTER UART 1 RxD Pin	List-box	PTC6 PTC8	
FreeMASTER UART 1 TxD Pin	List-box	PTC7 PTC9	
FreeMASTER UART 2 RxD Pin	List-box	PTD6 PTD17	
FreeMASTER UART 2 TxD Pin	List-box	PTD7 PTE12	
FreeMASTER UART 3 RxD Pin	List-box	PTA8 PTD13	
FreeMASTER UART 3 TxD Pin	List-box	PTA9 PTD14	
FreeMASTER CAN 0 RxD Pin	List-box	PTE4 PTC2	
FreeMASTER CAN 0 TxD Pin	List-box	PTE5 PTC3	
FreeMASTER CAN 1 RxD Pin	List-box	PTC6 PTA12	
FreeMASTER CAN 1 TxD Pin	List-box	PTC7 PTA13	
FreeMASTER CAN 2 RxD Pin	List-box	PTC16 PTB12	
FreeMASTER CAN 2 TxD Pin	List-box	PTC17 PTB13	
FreeMASTER CAN Baud Rate	List-box	1M	



- The Diagnostic Pane contains the following parameters:

Names	Selection Types	Range	Description
Enable/Disable Cross Checks	Check-box	Enable/Disable	Several check boxes available to Enable/Disable cross checks.



5.1.1.6 Block Dependency

None

5.1.1.7 Block Miscellaneous Details:

Required System Target File is set automatically by adding Target Configuration Block into the model. If no Target Configuration Block in the model then System Target File should be set manually.

5.1.1.8 Block Details

Model Based Design Toolbox provides an easy to use graphic interface allowing configuration of individual peripherals. Each peripheral can be configured by selecting its block on the Model Based Design Toolbox startup screen. When a block is selected, that peripheral's GUI will be displayed. When finished, click OK and the peripheral's GUI will be saved and closed. More detailed information about specific blocks is found in the tutorial for that block.

5.1.1.9 Layout of Block GUIs

In the Model Based Design Toolbox library there are two types of block GUIs: NXP Application Motor Control Library (application blocks) and Model Based Design Toolbox for S32K14 (peripheral blocks). The NXP Application Motor Control Library contains independent blocks to be used in your motor control application model. The Model Based Design Toolbox contains configuration-dependent blocks for controlling the low level drivers and I/O of the target. These blocks are considered configuration-dependent because the MBD_S32K14x_Config_Information block **must** be used when any of the other blocks in the library is used within the model. In some cases, there are additional Config blocks that must be used as well, for example, CAN Config, SPI Config and ADC Config. The blocks within the Model Based Design Toolbox library are not all supported in all modes. Please use the following table to determine the support of each block.

Library Block Support by Mode

Note: Support means the block will not generate an error in the supported mode, but may or may not be functional.

Block	Simulation	SIL	PIL	Target
NXP Automotive Math and Motor Control Library	All Blocks	All Blocks	All Blocks	All Blocks
MBD_S32K14x_Config_Information	X	X	X	X
CAN Configuration				X
CAN Receive Data				X
CAN Receive Data Trigger				X
CAN Transmit				X
CAN ISR				X
LINSCI Configuration				X
LINSCI Transmit				X
LINSCI Receive				X
LINSCI ISR				X
SPI Configuration				X
SPI Receive				X
SPI Receive Trigger				X
SPI Transmit				X
SPI Transmit Trigger				X
SPI MODF				X
Digital Input	X	X	X	X
Digital Output	X	X	X	X
GDU Configuration				X
GDU ISR				X
GDU Desaturation ISR				X
GDU Status				X
PTU Generator				X
PTU ISR				X
ADC Configuration				X
ADC Command List				X
ADC Individual Command				X
ADC Start Sequence				X
ADC Restart Sequence				X
ADC Read	X	X	X	X
ADC Abort ISR				X
ADC Error ISR				X
ADC Complete ISR				X
Complementary PMF Output	X	X	X	X
Complementary PMF 3 Sync Pair Output	X	X	X	X
PWM Independent Output	X	X	X	X
PMF Reload ISR				X
Hall Sensor Port				X
Timer Interrupt Module				X
Timer Interrupt Module Overflow ISR				X
Memory Read				X
Memory Write				X

Profiler Function			X	X
FreeMASTER Data Recorder Block				X

5.2 Motor Control Blocks

A large part of moving from the modeling and simulation environment is connecting to real world sensors and actuators. A major portion of this is using hardware peripherals integrated with the application in a straight forward and simplistic manner. The Model Based Design Toolbox provides these interface blocks with the objective of allowing the user to do minimal configuration of the peripheral with the ability to completely configure the peripheral as desired. Certain configuration items are assumed in order to have a straight forward method of configuring the peripheral with the application; these constraints are spelled out in the use case of the peripheral.

5.2.1 ADC Configuration Block

Analog to Digital Converter is a complex device that utilizes Direct Memory Access for processing at maximum speed with minimal CPU loading. The peripheral block for this assumes the user has configured the conversion command queues for the channels desired and the conversion trigger source type in MBD_S32K14x_Config_Information.

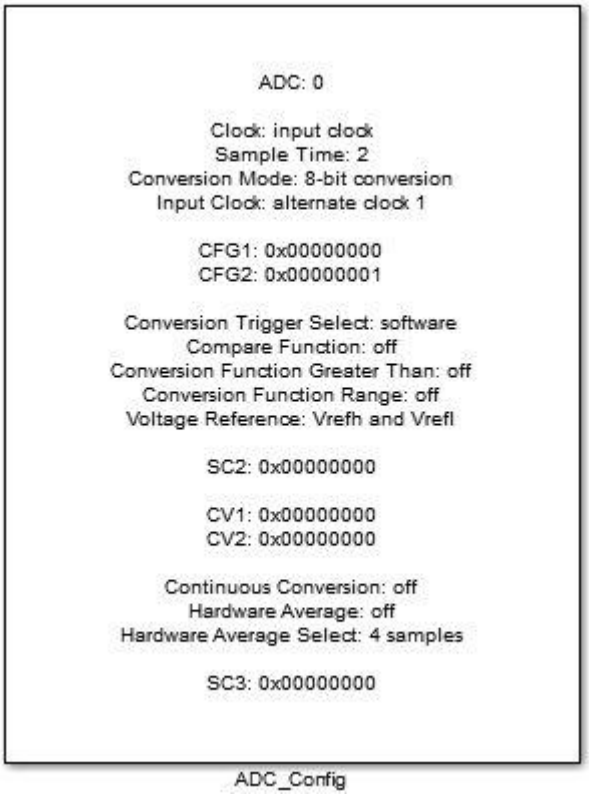
5.2.1.1 Block Name

ADC Configuration Block

5.2.1.2 Block Description

This block is used to configure the parameters of the ADC.

5.2.1.3 Block Image



5.2.1.4 Inputs:

- None

5.2.1.5 Outputs:

- None

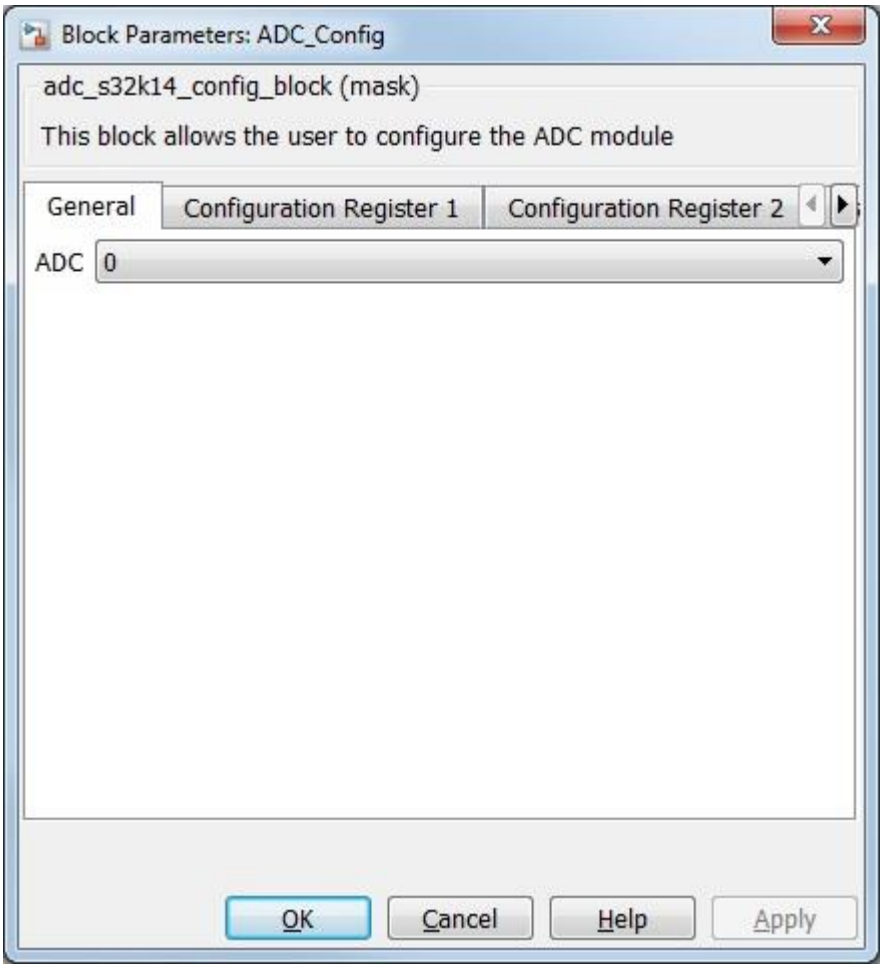
5.2.1.6 Block Dialog and Parameters:

The block dialog consists of the following tabs:

- General
- Configuration Register 1
- Configuration Register 2
- Status and Control Register 2
- Status and Control Register 3

- The General tab contains the following parameters:

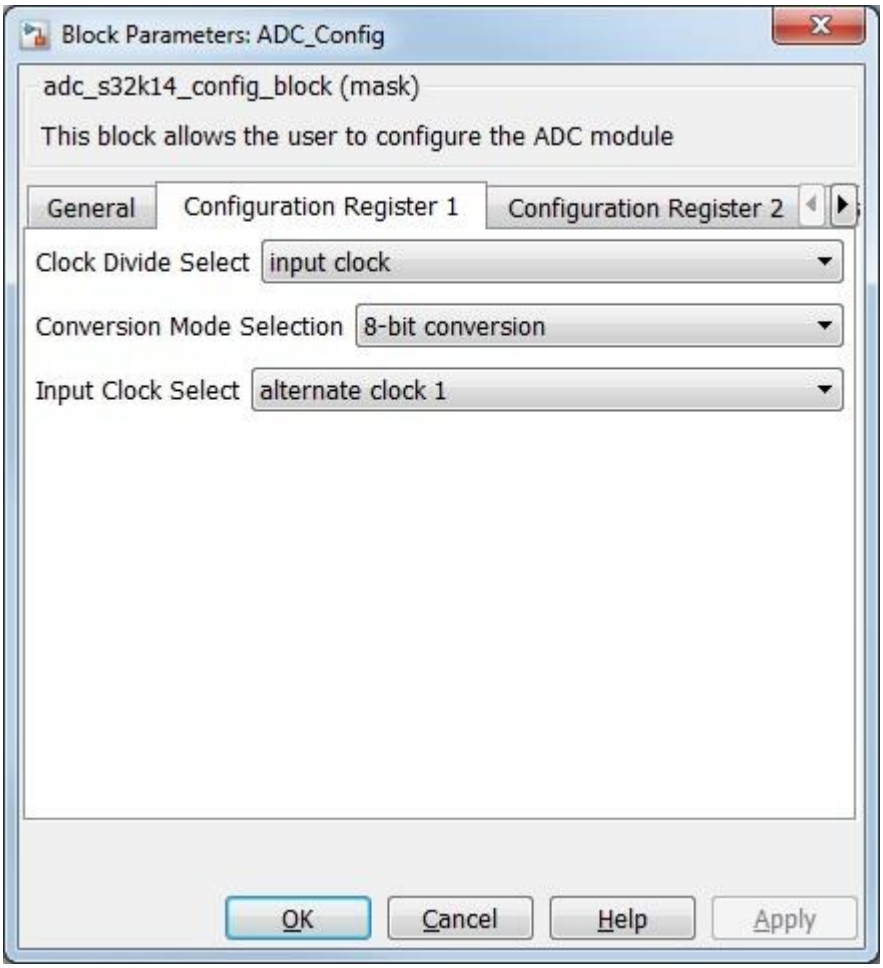
Names	Selection Types	Range	Description
ADC converter number	Pop-up	0 – 1	Select the ADC converter number



- Configuration Register 1 contains the following parameters:

Names	Selection Types	Range	Description
Clock Divide Select	List-box	input clock input clock / 2 input clock / 4 input clock / 8	Selects the divide ratio used by the ADC to generate the internal clock ADCK.*
Conversion Mode	List-box	8-bit conversion 12-bit conversion 10-bit conversion	Selects the ADC resolution mode.*
Input Clock Select	List-box	alternate clock 1 alternate clock 2 alternate clock 3 alternate clock 4	Selects the input clock source to generate the internal clock, ADCK.*

* Read Hardware Manual documentation to get more information.



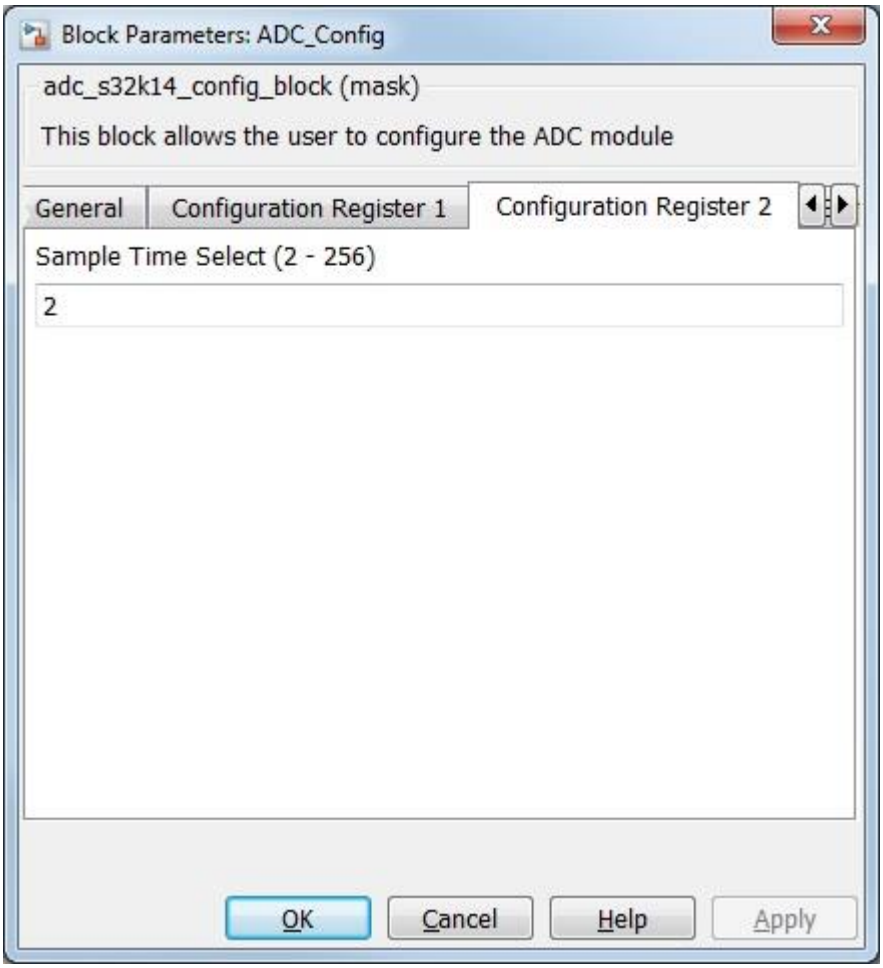
- Configuration Register 2 contains the following parameters:

Names	Selection Types	Range	Description
Sample Time Select (2 - 256)	Text-box	2 – 256	Selects a sample time of 2 to 256 ADCK clock cycles. The value written to this register is the desired sample time minus 1. A sample time of 1 is not supported. Allows higher impedance inputs to be accurately sampled or to maximize conversion speed for lower impedance inputs. Longer sample times can also be used to lower overall power consumption when continuous conversions are enabled if high conversion rates are not required.*

* Read Hardware Manual documentation to get more information.

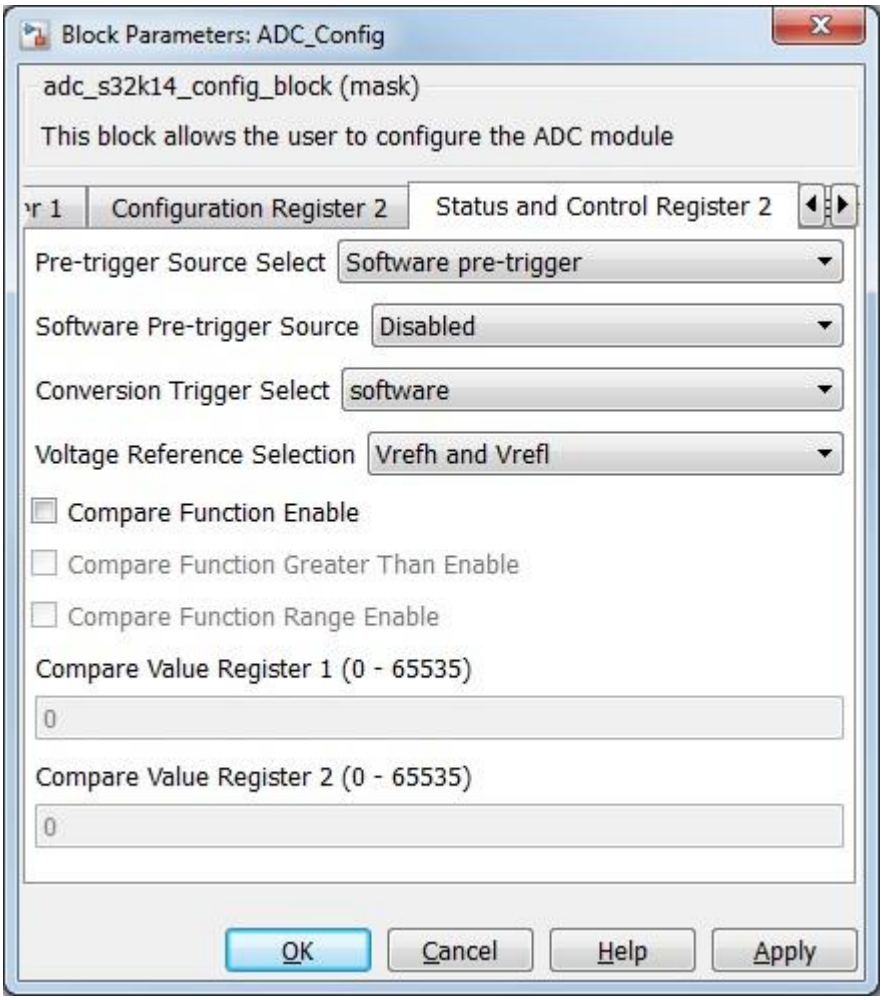
Names	Selection Types	Range	Description
Pre-trigger Source Select	List-box	PDB pre-trigger TRGMUX pre-trigger Software pre-trigger	Selects pre-trigger source for ADC.*
Software Pre-trigger Source	List-box	Disabled Software pre-trigger 0 Software pre-trigger 1 Software pre-trigger 2 Software pre-trigger 3	Selects pre-trigger source for ADC.*
Conversion Trigger Select	List-box	software hardware	Selects the type of trigger used for initiating a conversion.* Two types of trigger are selectable: • Software trigger: When software trigger is selected, a conversion is initiated following a write to SC1A. • Hardware trigger: When hardware trigger is selected, a conversion is initiated following the assertion of the ADHWT input after a pulse of the ADHWTSn input.
Voltage Reference Selection	List-box	Vrefh and Vrefl Valth and Valtl	Selects the voltage reference source used for conversions.*

Compare Function Enable	Check-box	Unchecked - Compare function disabled. Checked - Compare function enabled.	Enables the compare function. *
Compare Function Greater Than Enable	Check-box	Unchecked - Configures less than threshold, outside range not inclusive and inside range not inclusive; functionality based on the values placed in CV1 and CV2. Checked - Configures greater than or equal to threshold, outside and inside ranges inclusive; functionality based on the values placed in CV1 and CV2.	Configures the compare function to check the conversion result relative to the CV1 and CV2 based upon the value of ACREN. ACFE must be set for ACFGT to have any effect. *
Compare Function Range Enable	Check-box	Unchecked - Range function disabled. Only CV1 is compared. Checked - Range function enabled. Both CV1 and CV2 are compared.	Configures the compare function to check if the conversion result of the input being monitored is either between or outside the range formed by CV1 and CV2 determined by the value of ACFGT. ACFE must be set for ACFGT to have any effect. *
Compare Value Register 1 (0 - 65535)	Text-box	0 – 65535	Compare Value.*
Compare Value Register 2 (0 - 65535)	Text-box	0 – 65535	Compare Value.*



- Status and Control Register 2 contains the following parameters:

*Read Hardware Manual documentation to get more information.

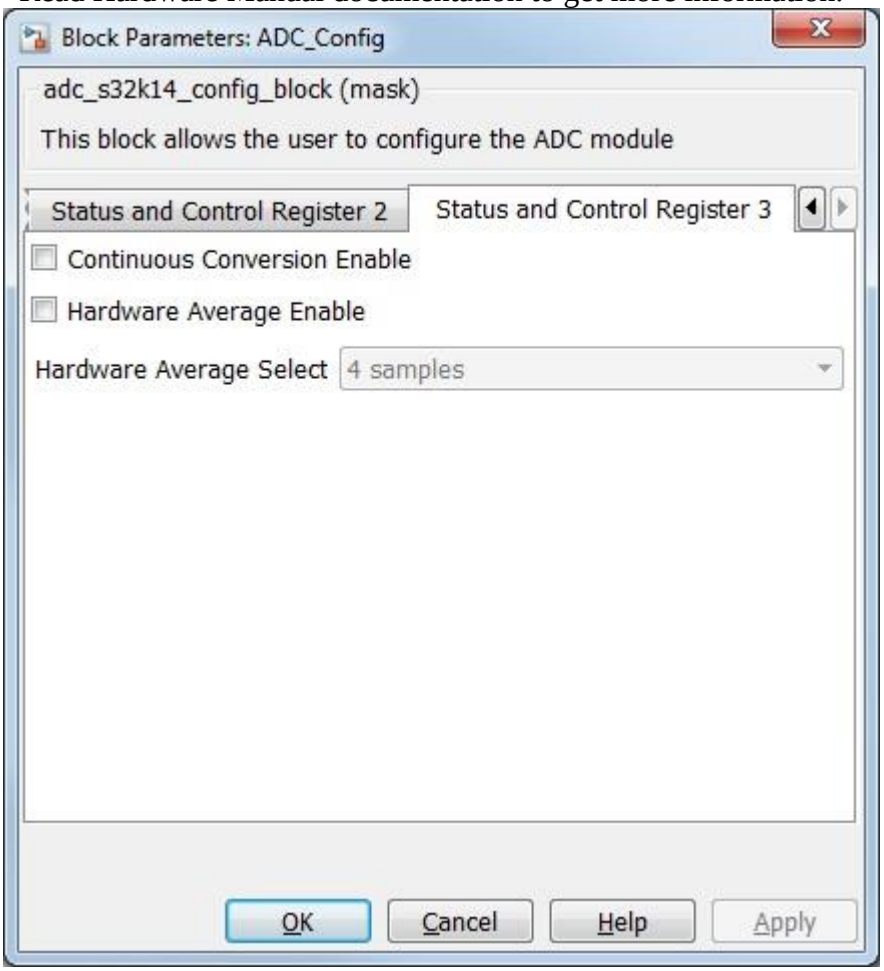


- Status and Control Register 3 contains the following parameters:

Names	Selection Types	Range	Description
Continuous Conversion Enable	Check-box	Unchecked - One conversion or one set of conversions if the hardware average function is enabled, that is, AVGE=1, after initiating a conversion. Checked - Continuous conversions or sets of conversions if the hardware average function is enabled, that is, AVGE=1, after initiating a conversion.	Enables the compare function. *
Hardware Average Enable	Check-box	Unchecked - Hardware average function disabled. Checked - Hardware average function enabled.	Enables the hardware average function of the ADC. *
Hardware Average Select	List-box	4 samples 8 samples 16 samples	Determines how many ADC

		32 samples	conversions will be averaged to create the ADC average result.*

*Read Hardware Manual documentation to get more information.



5.2.1.7 Block Dependency

5.2.1.8 Block Miscellaneous Details:

5.2.2 ADC Start Block

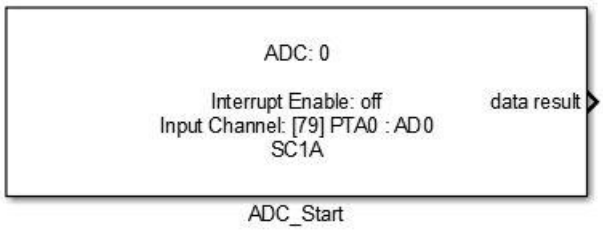
5.2.2.1 Block Name

ADC Start Block

5.2.2.2 Block Description

This block allows to configure channel parameters, start the conversion and get the result when interrupt is not configured.

5.2.2.3 Block Image



5.2.2.4 Inputs:

- None

5.2.2.5 Outputs:

- Function-call
- data result (uint32)
- channel (uint8)

5.2.2.6 Block Dialog and Parameters:

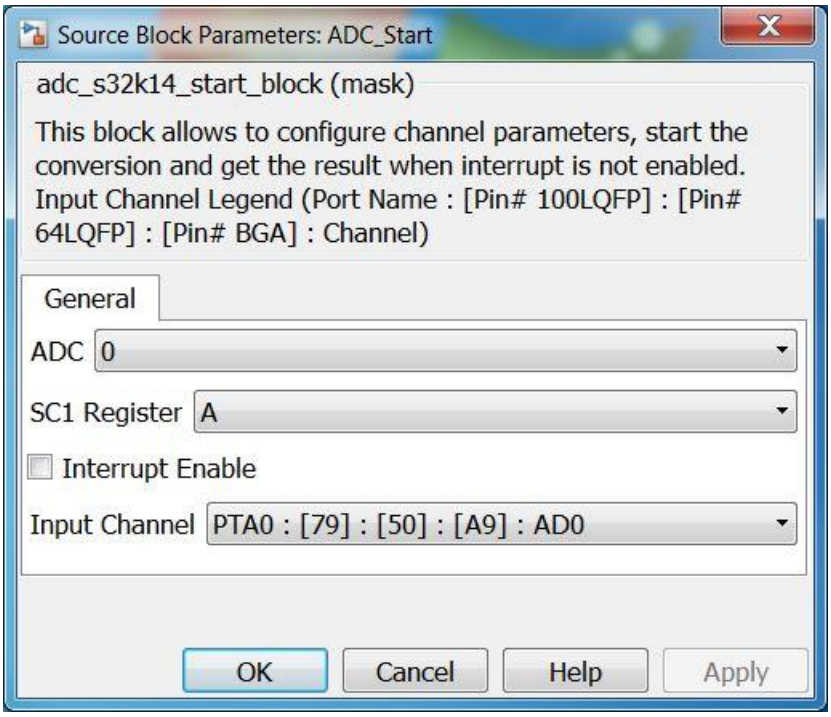
Names	Selection Types	Range	Description
ADC	List-box	0 – 1	Select the ADC converter number.
SC1 Register	List-box	A – P	Select which SC1 Register is the source for the trigger.
Interrupt Enable	Check-box	Enable/Disable	Enables conversion complete interrupts.
Input Channel	List-box	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13	Selects one of the input channels. See the next **Table 1** for the exact number of external ADC channels present on a specific deviece.

		AD14 AD15 ... AD31 Temp Sensor Band Gap VREFSH VREFSL Module is disabled	

* To get more information refer to Hardware Manual documentation.

Table 1. ADC external channels per package

Chip	Package	ADC0	ADC1
S32K142	64 LQFP	16	11
	100 LQFP	16	16
S32K144	64 LQFP	16	11
	100 LQFP	16	16
	100 MAPBGA	16	16
S32K148	144 LQFP	32	32
	100 MAPBGA	16	16
	176 LQFP	32	32



5.2.2.7 Block Dependency

Please do the following:

1. Configure the ADC Config block.

5.2.2.8 Block Miscellaneous Details:

None

5.2.3 ADC ISR Block

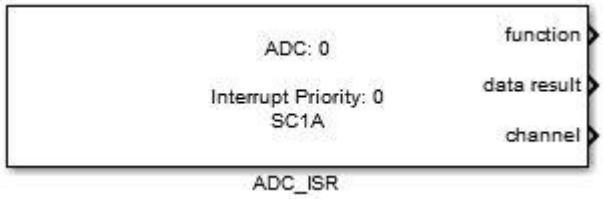
5.2.3.1 Block Name

ADC ISR Block

5.2.3.2 Block Description

This block allows user to call a function on ADC conversion events, get result and channel of the conversion.

5.2.3.3 Block Image



5.2.3.4 Inputs:

- None

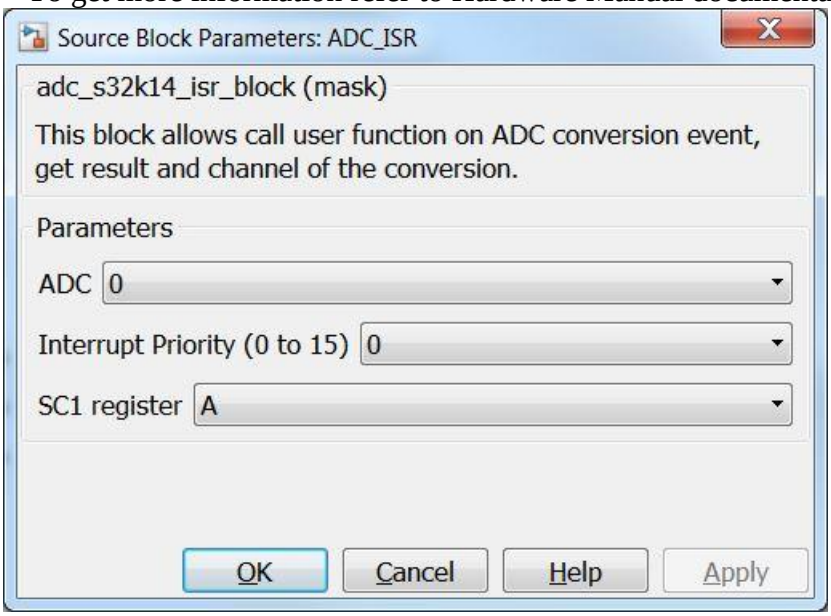
5.2.3.5 Outputs:

- Function-call
- data result (uint32)
- channel (uint8)

5.2.3.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
ADC	List-box	0 – 1	Select the ADC converter number.
Interrupt Priority (0 to 15)	List-box	0 – 15	Global ISR Priority.
SC1 Register	List-box	A – P	Select which SC1 Register is the source for the trigger.

* To get more information refer to Hardware Manual documentation.



5.2.3.7 Block Dependency

Please do the following:

1. Configure the ADC Config block.

5.2.3.8 Block Miscellaneous Details:

None

5.2.4 CMP Configuration Block

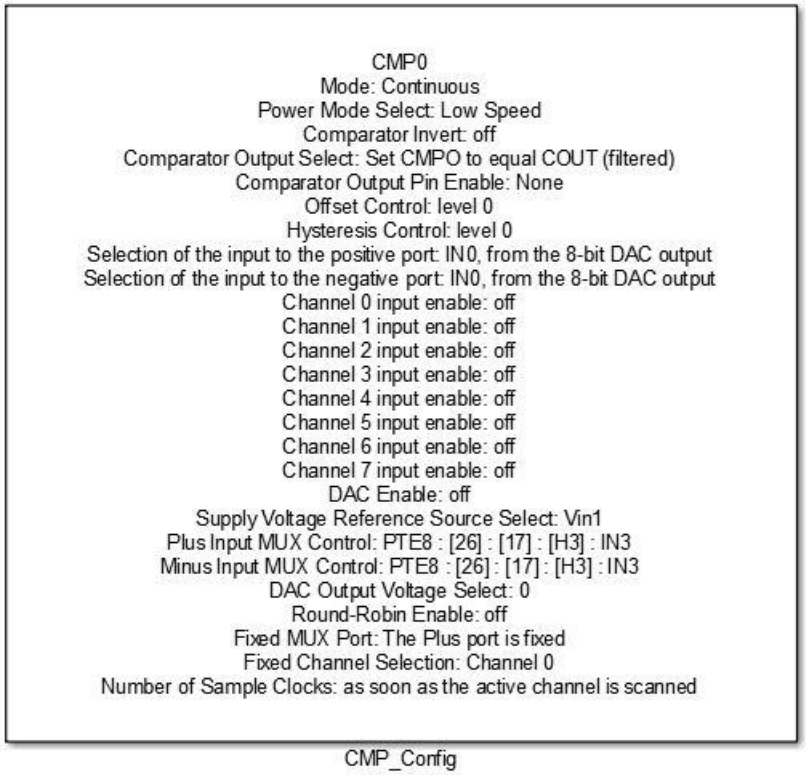
5.2.4.1 Block Name

CMP Configuration Block

5.2.4.2 Block Description

This block is used to configure the CMP module.

5.2.4.3 Block Image



5.2.4.4 Inputs:

- None

5.2.4.5 Outputs:

- None

5.2.4.6 Block Dialog and Parameters:

The block dialog consists of the following tabs:

- Control Register 0

- Control Register 1
- Control Register 2

- The Control Register 0 tab contains the following parameters:

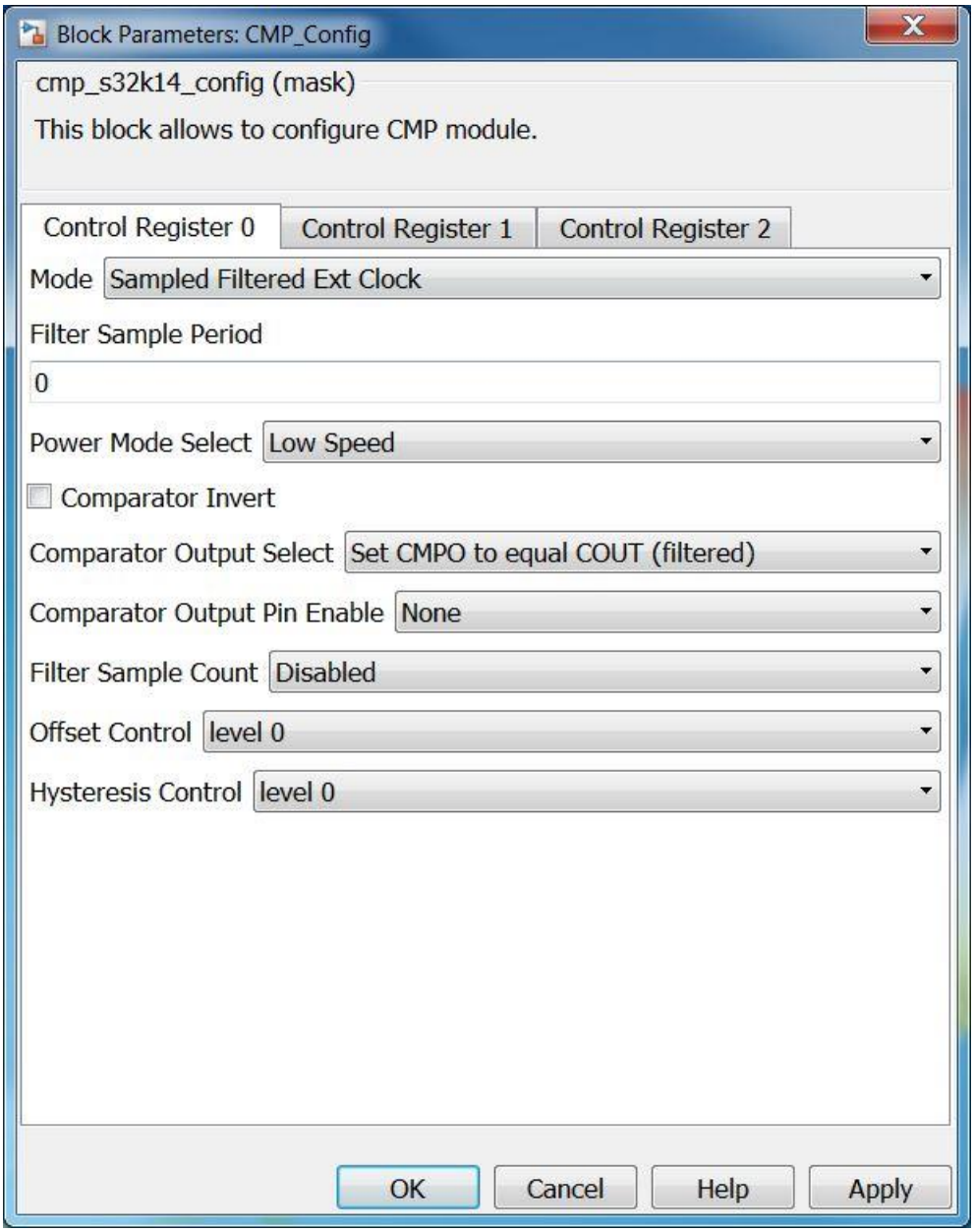
Names	Selection Types	Range	Description
Comparator Mode	List-box	Continuous Sampled Non-Filtered Int Clock Sampled Non-Filtered Ext Clock Sampled Filtered Int Clock Sampled Filtered Ext Clock Window Windowed Resampled Windowed Filtered	Select which functional mode to use. See table below.
Filter Sample Period	Text-box	0 – 255	Specifies the sampling period, in bus clock cycles, of the comparator output filter, when C1[SE] = 0. Setting FPR to 0x0 disables the filter. Filter programming and latency details are provided in the CMP functional description. This field has no effect when C0[SE]= 1. In that case, the external SAMPLE signal is used to determine the sampling period.
Power Mode Select	List-box	Low Speed High Speed	Select which power mode to use.
Comparator INVERT	List-box	Enable/Disable	Allows selection of the polarity of the analog comparator function. It is also driven to the COUT output, on both the device pin and as SCR[COUT], when OPE=0.
Comparator Output Select	List-box	Set CMPO to equal COUT (filtered) Set CMPO to equal COUTA (unfiltered)	Select the Comparator Output.
Comparator Output Pin Enable	List-box	None PTE3	The OPE bit enables the path from the comparator output to a selected pin.
Filter Sample Count	List-box	1 - 7	Represents the number of consecutive samples that must

			agree prior to the comparator ouput filter accepting a new output state.
Offset Control	List-box	level 0 level 1	Comparator hard block offset control. See chip data sheet to get the actual offset value with each level.
Hysteresis Control	List-box	00 - Level 0 01 - Level 1 10 - Level 2 11 - Level 3	Defines the programmable hysteresis level. The hysteresis values associated with each level are device specific. See the Data Sheet of the device for the exact values.

* Read Hardware Manual documentation to get more information.

Comparator functional modes

Mode #	C0[EN]	C0[WE]	C0[FILTER_CNT]	C0[FPR]	Operation	
1	0	x	x	x	x	Disabled
2A	0	x	x	0x00	x	Continuous Mode
2B	0	x	x	x	0x00	
3A	1	0	1	0x01	x	Sampled Non-Filtered External Clock
3B	1	0	0	0x01	> 0x00	Sampled Non-Filtered Internal Clock
4A	1	0	1	> 0x01	x	Sampled Filtered External Clock
4B	1	0	1	> 0x01	> 0x04	Sampled Filtered Internal Clock
5A	1	1	0	0x00	x	Windowed
5B	1	1	0	x	0x00	
6	1	1	0	0x01	0x01-0xFF	Windowed Resampled
7	1	1	0	> 0x01	0x01-0xFF	Windowed Filtered
All other combinations of C0[EN], C0[WE], C0[SE], C0[Filter_CNT], and C0[FPR] are illegal.						



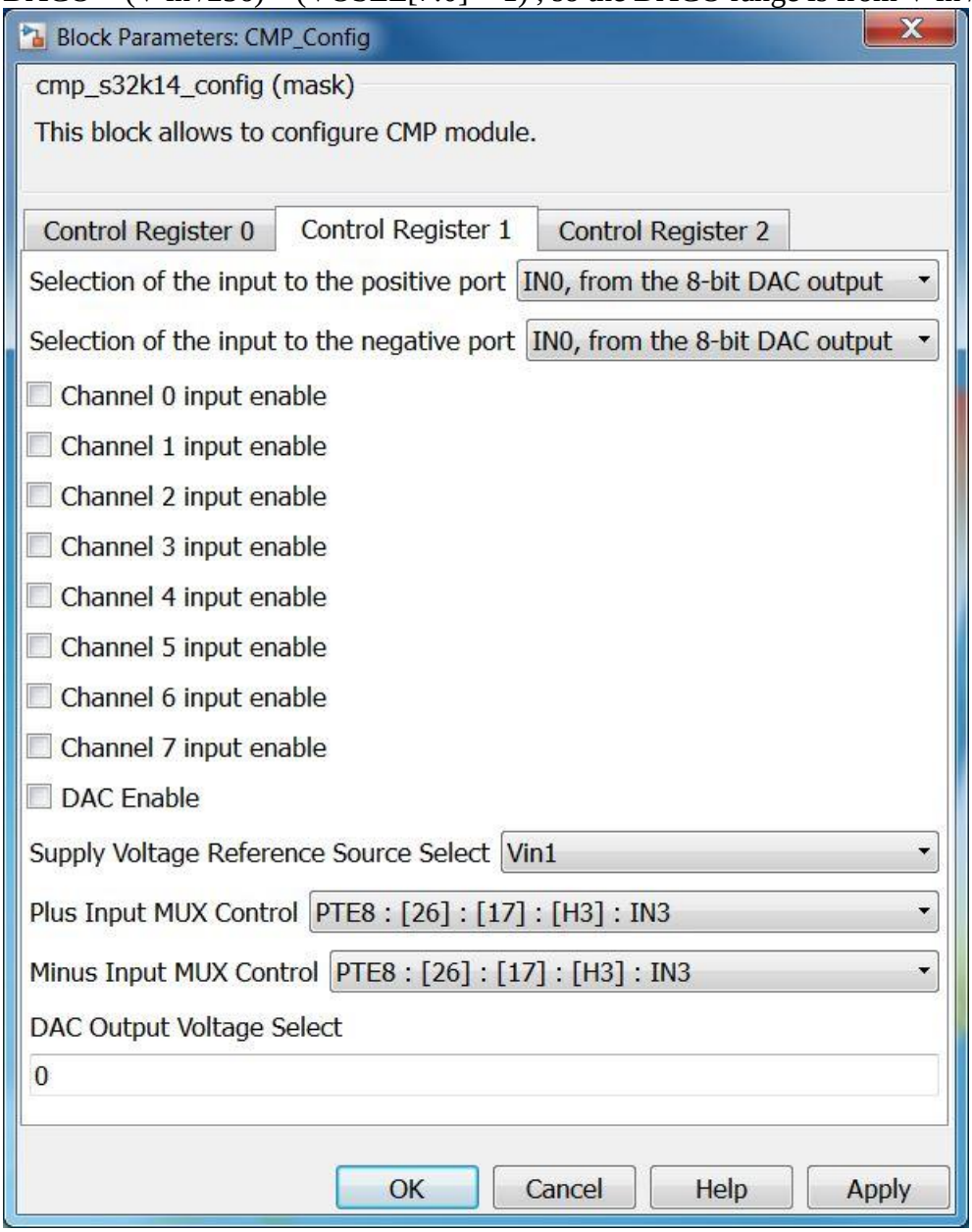
- The Control Register 1 tab contains the following parameters:

Names	Selection Types	Range	Description
Selection of the input to the positive port	List-box	IN0, from the 8-bit DAC output IN1, from the analog 8-1 mux	Selection of the input to the positive port of the comparator Determines which input is selected for the plus input of the comparator

Selection of the input to the positive port	List-box	IN0, from the 8-bit DAC output IN1, from the analog 8-1 mux	Selection of the input to the negative port of the comparator Determines which input is selected for the plus input of the comparator.
Channel 0 input enable	Check-box	Enable/Disable	Channel 0 of the input enable for the round-robin checker.
Channel 1 input enable	Check-box	Enable/Disable	Channel 1 of the input enable for the round-robin checker.
Channel 2 input enable	Check-box	Enable/Disable	Channel 2 of the input enable for the round-robin checker.
Channel 3 input enable	Check-box	Enable/Disable	Channel 3 of the input enable for the round-robin checker.
Channel 4 input enable	Check-box	Enable/Disable	Channel 4 of the input enable for the round-robin checker.
Channel 5 input enable	Check-box	Enable/Disable	Channel 5 of the input enable for the round-robin checker.
Channel 6 input enable	Check-box	Enable/Disable	Channel 6 of the input enable for the round-robin checker.
Channel 7 input enable	Check-box	Enable/Disable	Channel 7 of the input enable for the round-robin checker.
DAC Enable	Check-box	Enable/Disable	This bit is used to enable the DAC. When the DAC is disabled, it is powered down to conserve power.
Supply voltage Ref Source	List-box	0 - Vin1 1 - Vin2	selected resistor ladder network supply reference.*
Plus Input MUX Control	List-box	PTA0 : IN0 PTA1 : IN1 PTC4 : IN2 PTE8 : IN3 PTC3 : IN4 PTC2 : IN5 PTD7 : IN6 PTD6 : IN7	Determines which input is selected for the plus mux.*
Minus Input MUX Control	List-box	PTA0 : IN0 PTA1 : IN1 PTC4 : IN2 PTE8 : IN3 PTC3 : IN4 PTC2 : IN5	Determines which input is selected for the minus mux.*

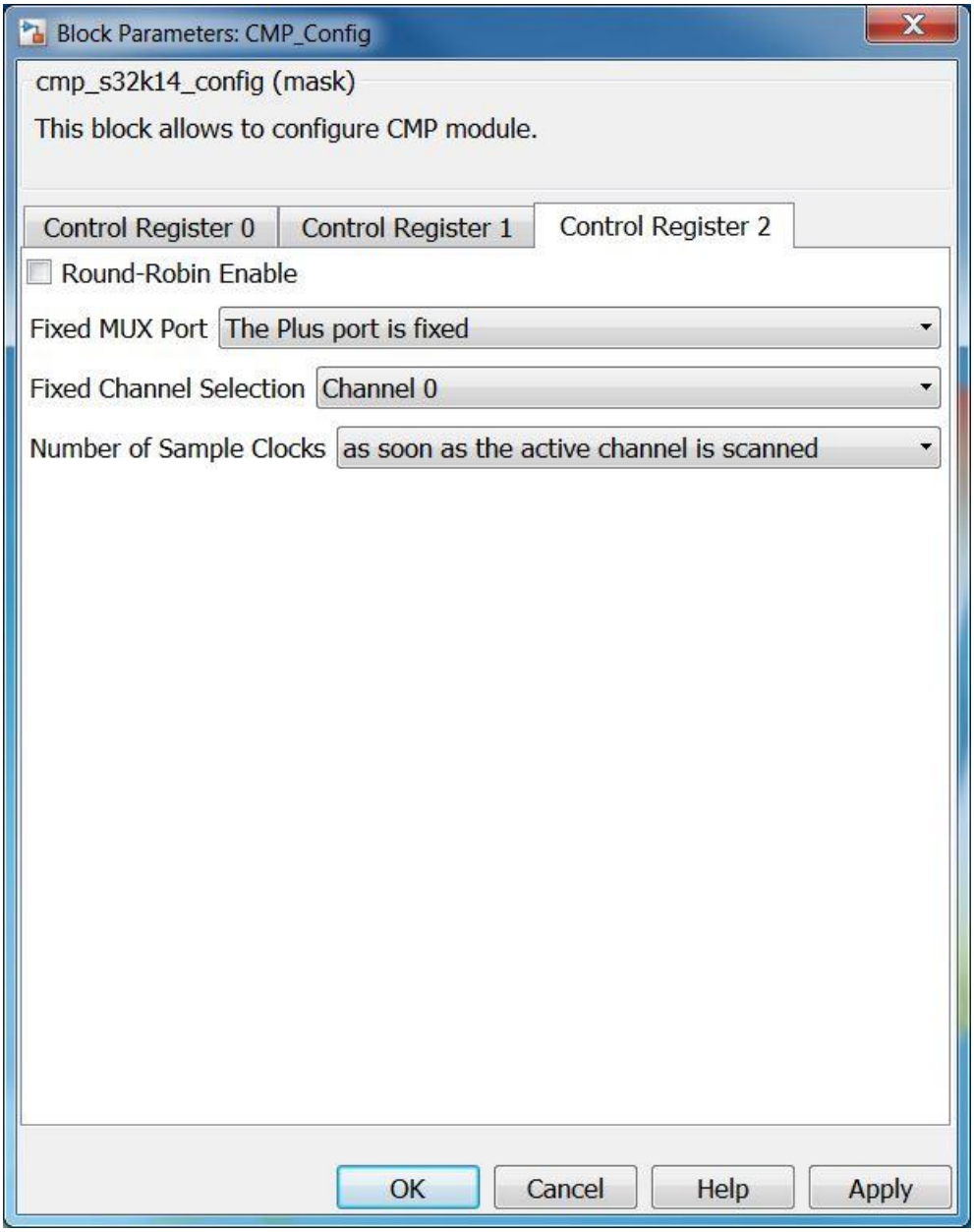
		PTD7 : IN6 PTD6 : IN7	
DAC Output Voltage	Text-box	0 – 256	Selects an output voltage from one of 256 distinct levels. See below for formula.

* Read Miscellaneous Details below or Hardware Manual documentation to get more information.
DACO = (V in /256) * (VOSEL[7:0] + 1) , so the DACO range is from V in /256 to V in .



- The Control Register 2 tab contains the following parameters:

Names	Selection Types	Range	Description
Round-Robin Enable	Check-box	Enable/Disable	This bit enables the round-robin operation.
Fixed MUX Port	List-box	The Plus port is fixed The Minus port is fixed	Selects the source for the Sample/Window input
Fixed Channel Selection	List-box	Channel 0 Channel 1 Channel 2 Channel 3 Channel 4 Channel 5 Channel 6 Channel 7	This field indicates which channel in the mux port is fixed in a given round-robin mode. If FXDACI is set, FXMXCH has no effect.
Number of Sample Clocks	List-box	as soon as the active channel is scanned 1 round-robin clock cycle after the next cycle 2 round-robin clock cycles after the next cycle 3 round-robin clock cycles after the next cycle	For a given channel, this field specifies how many round-robin clock cycles later the sample takes place.



5.2.4.7 Block Dependency

None

5.2.4.8 Block Miscellaneous Details:

None

5.2.5 CMP ISR Enable/Disable Block

5.2.5.1 Block Name

CMP ISR Enable Disable Block

5.2.5.2 Block Description

The main functionality of the block is to allow the user to Enable/Disable CMP ISRs.

5.2.5.3 Block Image

5.2.5.4 Inputs:

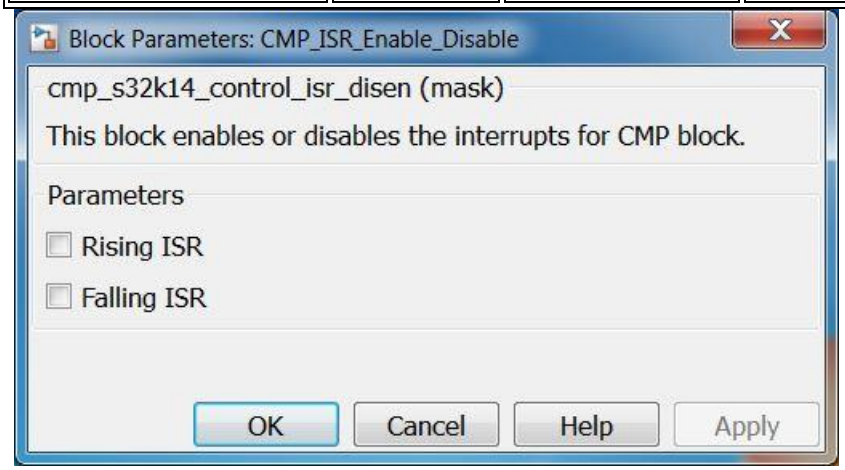
- None

5.2.5.5 Outputs:

- None

5.2.5.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Rising Interrupt Enable	Check-box	Enable/Disable	Enables the CFR interrupt from the CMP. When this field is set, an interrupt will be asserted when CFR is set.
Falling Interrupt Enable	Check-box	Enable/Disable	Enables the CFF interrupt from the CMP. When this field is set, an interrupt will be asserted when CFF is set.



5.2.5.7 Block Dependency

Please do the following:

1. Configure Comparator

5.2.5.8 Block Miscellaneous Details:

None

5.2.6 CMP ISR Block

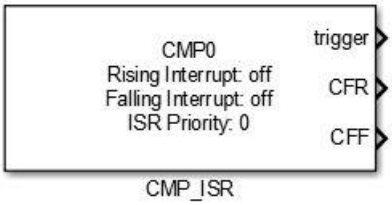
5.2.6.1 Block Name

CMP Interrupt Block

5.2.6.2 Block Description

The main functionality of the block is to configure CMP interrupts

5.2.6.3 Block Image



5.2.6.4 Inputs:

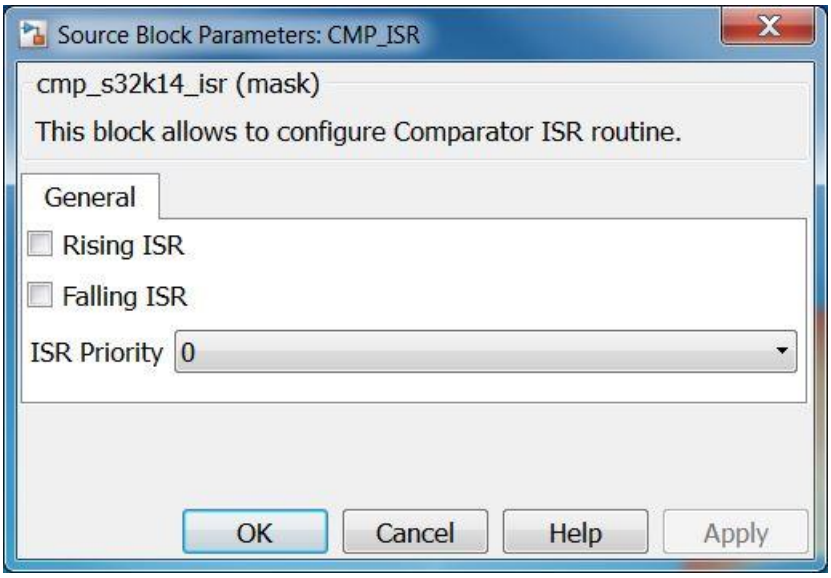
- None

5.2.6.5 Outputs:

- Function-Call
- CFR (boolean)
- CFF (boolean)

5.2.6.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Rising ISR	Check-box	Enable/Disable	Comparator Interrupt Enable Rising
Falling ISR	List-box	Enable/Disable	Comparator Interrupt Enable Falling
ISR Priority	Check-box	0 – 15	ISR Level



5.2.6.7 Block Dependency

Please do the following:

1. Configure Comparator

5.2.6.8 Block Miscellaneous Details:

None

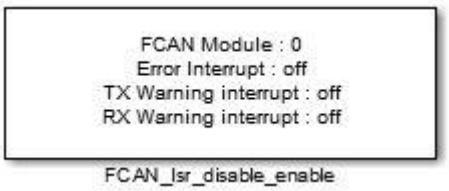
5.2.6.9 Block Name

FCAN Interrupt Enable/Disable Block

5.2.6.10 Block Description

The main functionality of the block is to enable/disable FCAN interrupts

5.2.6.11 Block Image



5.2.6.12 Inputs:

- None

5.2.6.13 Outputs:

- None

5.2.6.14 Block Dialog and Parameters:

Names	Selection Types	Range	Description
CAN Bus	Pop-up	0 - 2	CAN Module
Error interrupt	Check-box	Enable/Disable	This bit provides a mask for the Error Interrupt ERRINT in the CAN_ESR1 register.
Tx Warning interrupt	Check-box	Enable/Disable	This bit provides a mask for the Tx Warning Interrupt associated with the TWRNINT flag in the Error and Status Register 1 (ESR1). This bit is read as zero when CAN_MCR[WRNEN] bit is negated. This bit can be written only if CAN_MCR[WRNEN] bit is asserted.
Rx Warning interrupt	Check-box	Enable/Disable	This bit provides a mask for the Rx Warning Interrupt associated with the RWRNINT flag in the Error and Status Register 1 (ESR1). This bit is read as zero when CAN_MCR[WRNEN] bit is negated. This bit can be written only if CAN_MCR[WRNEN] bit is asserted.

5.2.6.15 Block Dependency

Please do the following:

1. Configure respective FCAN and its interrupts

5.2.6.16 Block Miscellaneous Details:

None

5.2.7 FTM Independent PWM Output Block

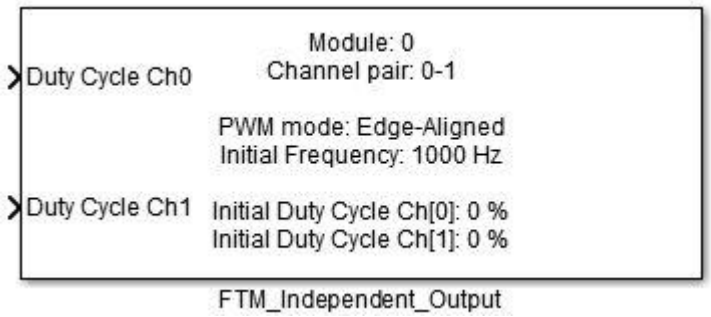
5.2.7.1 Block Name

Independent PWM Output Block

5.2.7.2 Block Description

The main functionality of the block is to generate a simple center-aligned or edge-aligned, PWM output signals on A and B outputs using the FTM 0 – 3 modules. Please see Block Miscellaneous Details for other information on using this block.

5.2.7.3 Block Image



5.2.7.4 Inputs:

- Duty Cycle Ch0 (uint32)
- Duty Cycle Ch1 (uint32)

5.2.7.5 Outputs:

- Duty Cycle Ch0 (double) - if "Duty Cycle Simulation Output" is On
- Duty Cycle Ch1 (double) - if "Duty Cycle Simulation Output" is On

5.2.7.6 Block Dialog and Parameters:

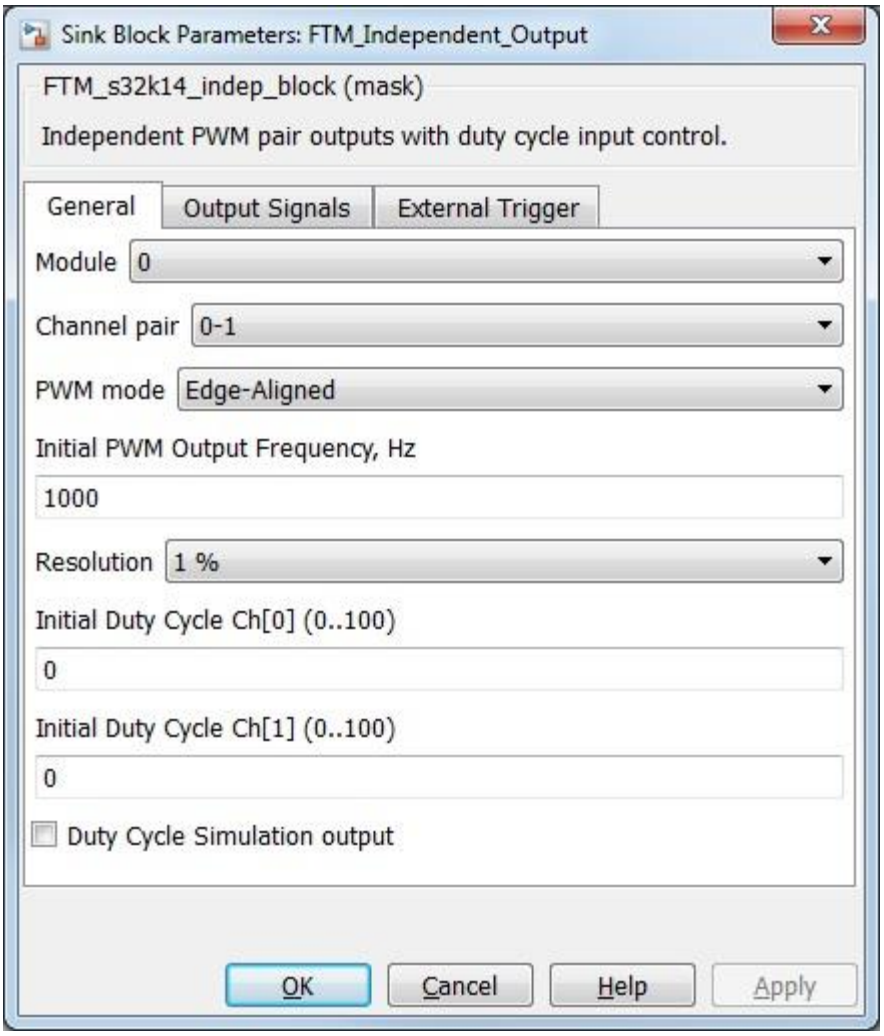
The block dialog consists of the following tabs:

- General
- Output Signals
- External Triggers

- The General tab contains the following parameters:

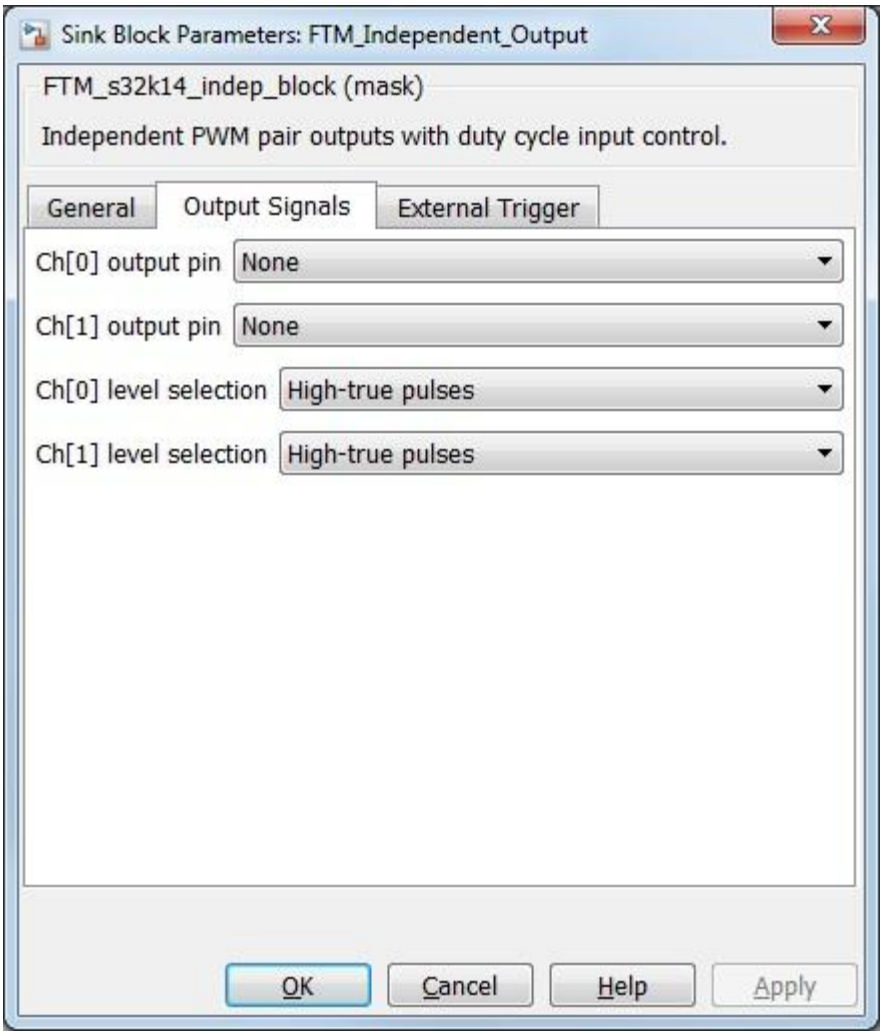
Names	Selection Types	Range	Description
FTM Module	List-box	0 – 3	Select which FTM module to use.
Channel Pair	List-box	0 – 1 2 – 3 4 – 5 6 – 7	PWM channel pair
PWM mode	List-box	Edge–Aligned Center–Aligned	Specifying PWM alignment in one Period
Initial PWM Output Frequency (Hz)	Text-box	Depends on Motor Control Clock value	Initial frequency of PWM output signals
Resolution	List-box	1 % 0.1 % 0.01 %	Duty cycle resolution: actual Duty

		0.001 %	cycle is equal to Duty cycle parameter or input value multiplied by resolution
Initial DutyCycle for Ch0	Text-box	0 – 100/resolution	Initial Duty Cycle of channel pair output
Initial DutyCycle for Ch1	Text-box	0 – 100/resolution	Initial Duty Cycle of channel pair output
Duty Cycle Simulation Output	Check-box	On/Off	If DutyCycle simulation output is used



- The Output Signals tab contains the following parameters:

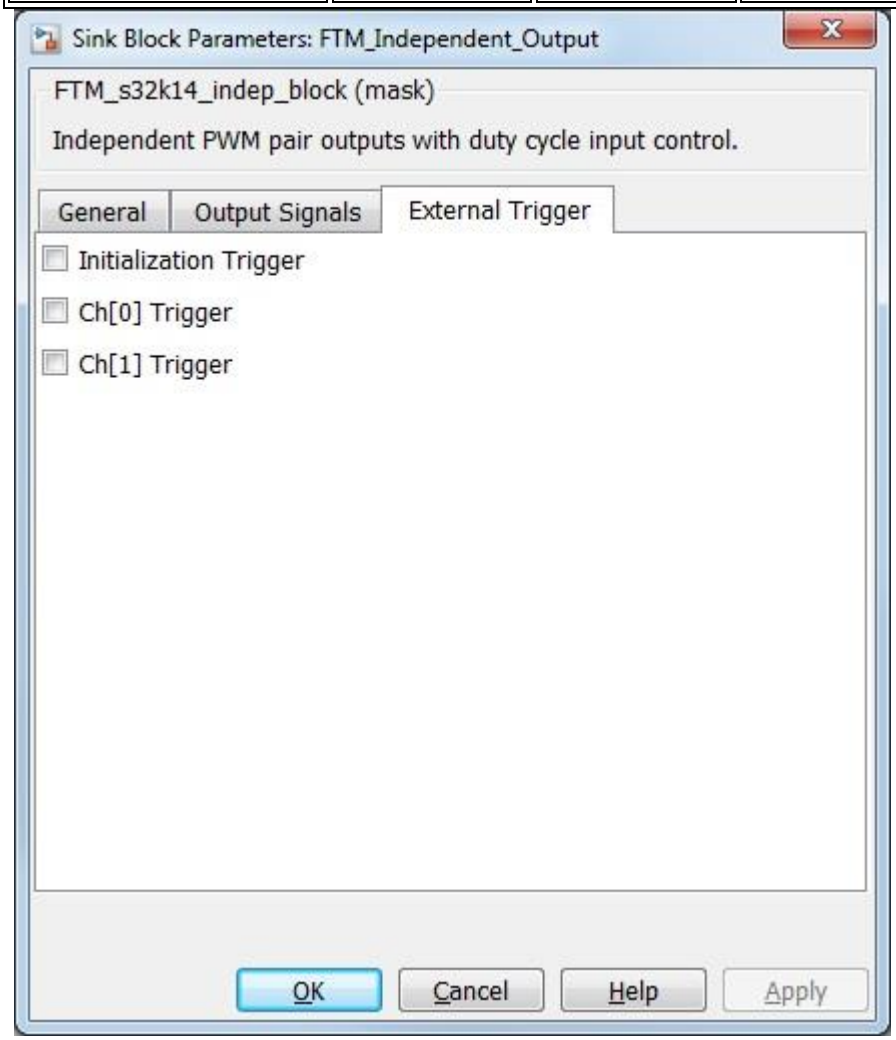
Names	Selection Types	Range	Description
Ch0 output pin	List-box	The list of available pins depends on the selected Channel.	pin selection
Ch1 output pin	List-box	The list of available pins depends on the selected Channel.	pin selection
Ch0 Output Polarity	List-box	High-true pulses Low-true pulses	
Ch1 Output Polarity	List-box	High-true pulses Low-true pulses	



- The External Triggers tab contains the following parameters:

Names	Selection Types	Range	Description
Initialization Trigger	Check-box	On/Off	Enable generation of Output Trigger signal based on the counter value matching of register value or initialization of FTM counter.
Ch[0] Trigger	Check-box	On/Off	Enable generation of Output Trigger signal based on the counter value matching of register value or initialization of FTM counter.
Ch[1] Trigger	Check-box	On/Off	Enable generation of Output

			Trigger signal based on the counter value matching of register value or initialization of FTM counter.



5.2.7.7 Block Dependency

None

5.2.7.8 Block Miscellaneous Details:

1. Duty Cycle output signal needed for simulation purpose only.
2. If it is desired to only use one of the output pair than select None for the pin selection of the unused output and tie the block input for the unused output to a constant value or tie it to the same input as the other output that is used.
3. Dedicate a FTM module for either PWM function or Input capture function. Do not share the same FTM Module b/t PWM blocks and FTM Input capture blocks.

5.2.8 FTM Complementary PWM Output Block

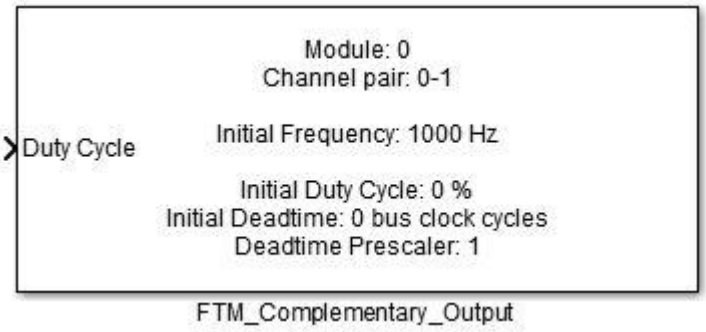
5.2.8.1 Block Name

Complementary PWM Output Block

5.2.8.2 Block Description

The main functionality of the block is to generate a complementary Center Aligned PWM signals on pair of outputs of the selected PWM Channel pair of the FTM module.

5.2.8.3 Block Image



5.2.8.4 Inputs:

- Duty Cycle A,B (uint32)

5.2.8.5 Outputs:

- Duty Cycle (double) - if "Duty Cycle Simulation Output" is On

5.2.8.6 Block Dialog and Parameters:

The block dialog consists of the following tabs:

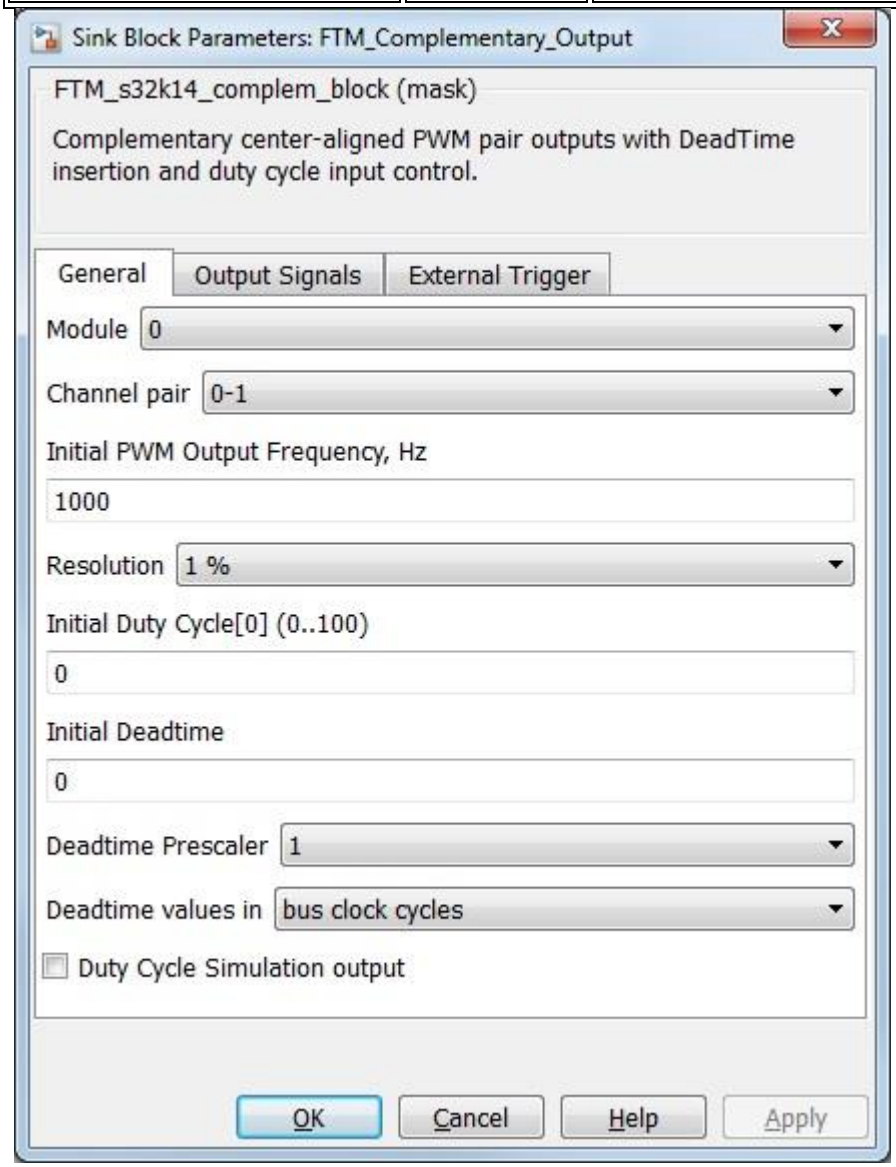
- General
- Output Signals
- External Triggers

- The General tab contains the following parameters:

Names	Selection Types	Range	Description
FTM Module	List-box	0 – 3	Select which FTM module to use.

Channel Pair	List-box	0 – 1 2 – 3 4 – 5 6 – 7	PWM channel pair
Initial PWM Output Frequency (Hz)	Text-box	Depends on Motor Control Clock value	Initial frequency of PWM output signals
Resolution	List-box	1 % 0.1 % 0.01 % 0.001 %	Duty cycle resolution: actual Duty cycle is equal to Duty cycle parameter or input value multiplied by resolution
Initial DutyCycle for Pair	Text-box	0 – 100/resolution	Initial Duty Cycle of channel pair output
Initial Deadtime	Text-box	0 – 63 IPBus clock cycles	Deadtime during 0 to 1 transitions of the PWM channel pair output
Deadtime Prescaler	List-box	1 4 16	Only available when using clock cycles for Deadtime
Deadtime values in	List-box	– IPBus clock cycles – nanoseconds	Units used for Deadtime
Duty Cycle Simulation Output	Check-box	On/Off	If DutyCycle simulation

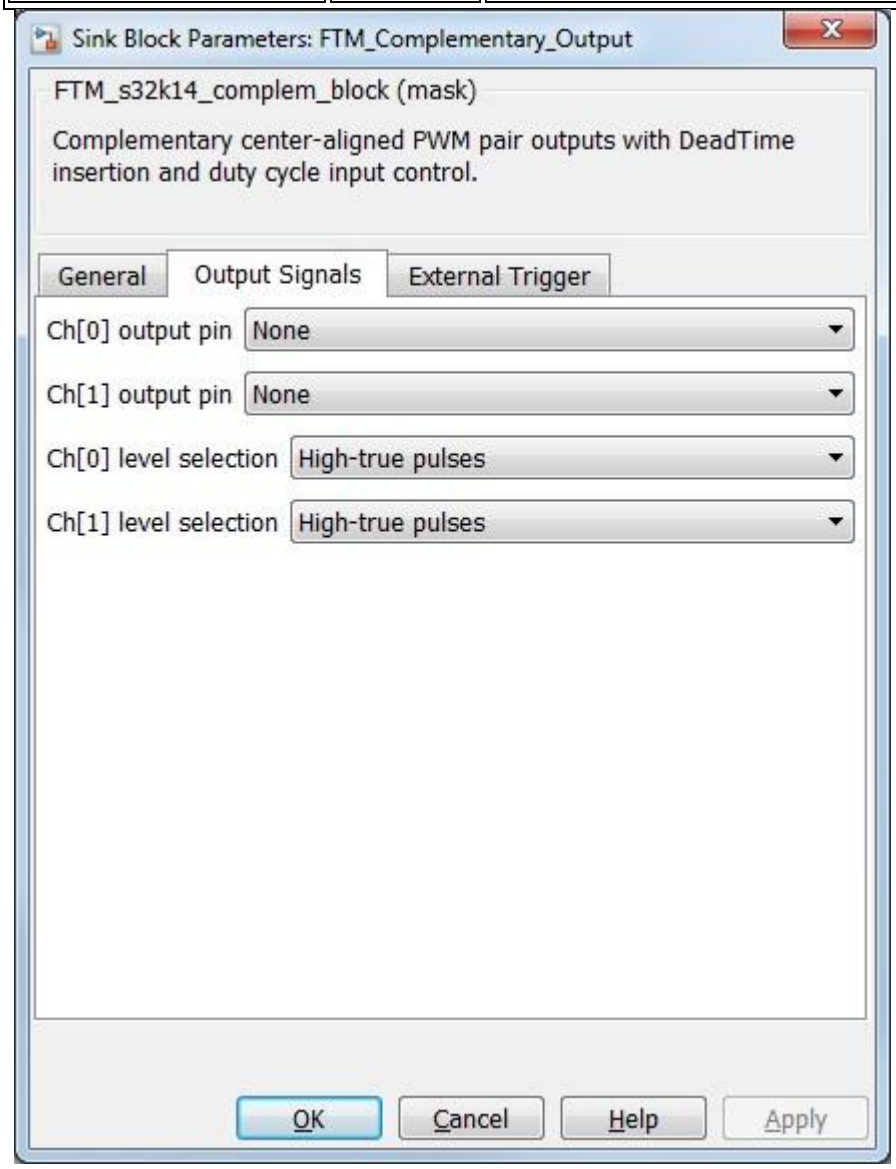
			output is used



- The Output Signals tab contains the following parameters:

Names	Selection Types	Range	Description
Ch0 output pin	List-box	The list of available pins depends on the selected Channel.	pin selection
Ch1 output pin	List-box	The list of available pins depends on the selected Channel.	pin selection
Ch0 level selection	List-box	High-true pulses	Level

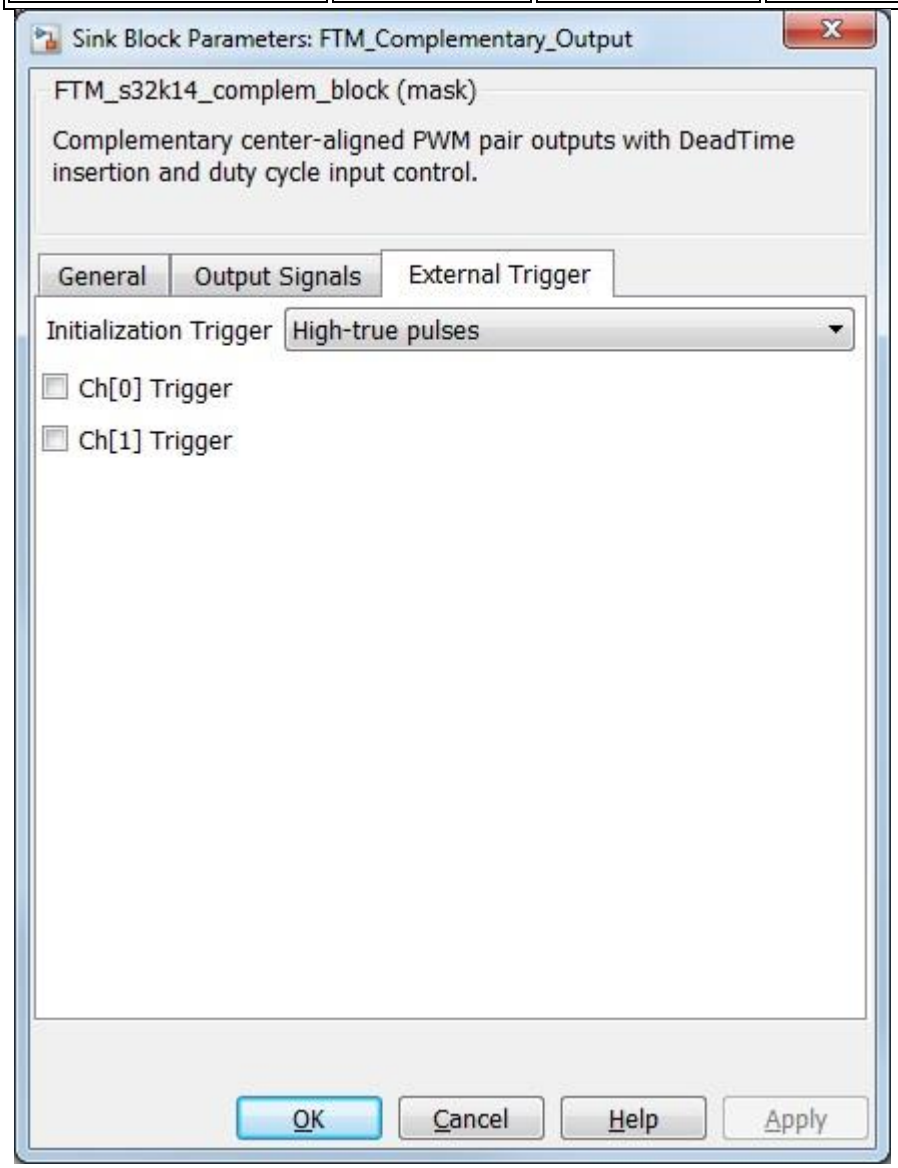
		Low-true pulses	Select
Ch1 level selection	List-box	High-true pulses Low-true pulses	Level Select



- The External Triggers tab contains the following parameters:

Names	Selection Types	Range	Description
Initialization Trigger	List-box	High-true pulses Low-true pulses	Level Select
Ch[0] Trigger	Check-box	On/Off	Enable generation of Output Trigger signal based on the

			counter value matching of register value or initialization of FTM counter.
Ch[1] Trigger	Check-box	On/Off	Enable generation of Output Trigger signal based on the counter value matching of register value or initialization of FTM counter.



5.2.8.7 Block Dependency

None

5.2.8.8 Block Miscellaneous Details:

1. Duty Cycle output signal needed for simulation purpose only.
2. Dedicate a FTM module for either PWM function or Input capture function. Do not share the same FTM Module b/t PWM blocks and FTM Input capture blocks.

5.2.9 FTM Three-phase PWM Output Block

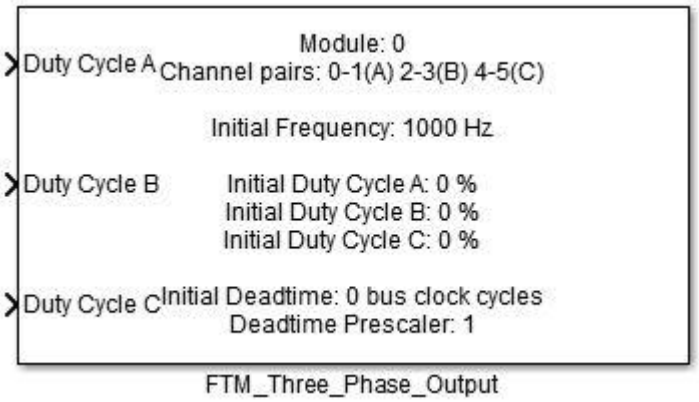
5.2.9.1 Block Name

Three-phase PWM Output Block

5.2.9.2 Block Description

The main functionality of the block is to generate a three-phase complementary center-aligned PWM signal pair outputs using the FTM module.

5.2.9.3 Block Image



5.2.9.4 Inputs:

- Duty Cycle A (uint32)
- Duty Cycle B (uint32)
- Duty Cycle C (uint32)

5.2.9.5 Outputs:

- Duty Cycle A (double) - if "Duty Cycle Simulation Output" is On
- Duty Cycle B (double) - if "Duty Cycle Simulation Output" is On
- Duty Cycle C (double) - if "Duty Cycle Simulation Output" is On

5.2.9.6 Block Dialog and Parameters:

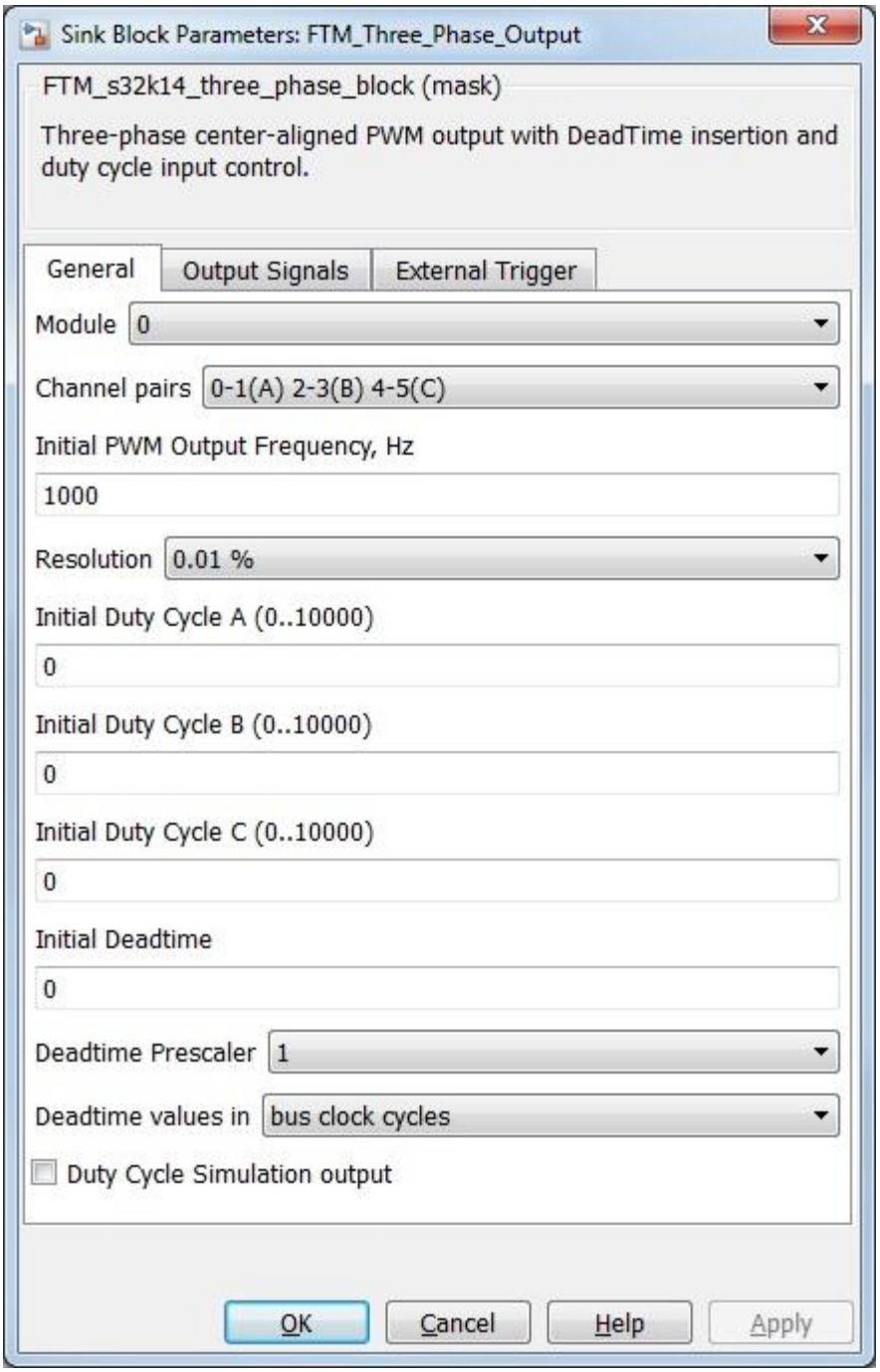
The block dialog consists of the following tabs:

- General
- Output Signals
- External Triggers

- The General tab contains the following parameters:

Names	Selection Types	Range	Description
FTM Module	List-box	0 – 3	Select which FTM module to use.
Channel Pair	List-box	0-1(A) 2-3(B) 4-5(C) 0-1(A) 2-3(B) 6-7(C) 0-1(A) 4-5(B) 6-7(C) 2-3(A) 4-5(B) 6-7(C)	PWM channel pair
Initial PWM Output Frequency (Hz)	Text-box	Depends on Motor Control Clock value	Initial frequency of PWM output signals
Resolution	List-box	1 % 0.1 % 0.01 % 0.001 %	Duty cycle resolution: actual Duty cycle is equal to Duty cycle parameter or input value multiplied by resolution
Initial DutyCycle for Phase A Pair	Text-box	0 – 100/resolution	Initial Duty Cycle of channel pair output
Initial DutyCycle for Phase B Pair	Text-box	0 – 100/resolution	Initial Duty Cycle of channel pair output
Initial DutyCycle for Phase	Text-box	0 – 100/resolution	Initial Duty

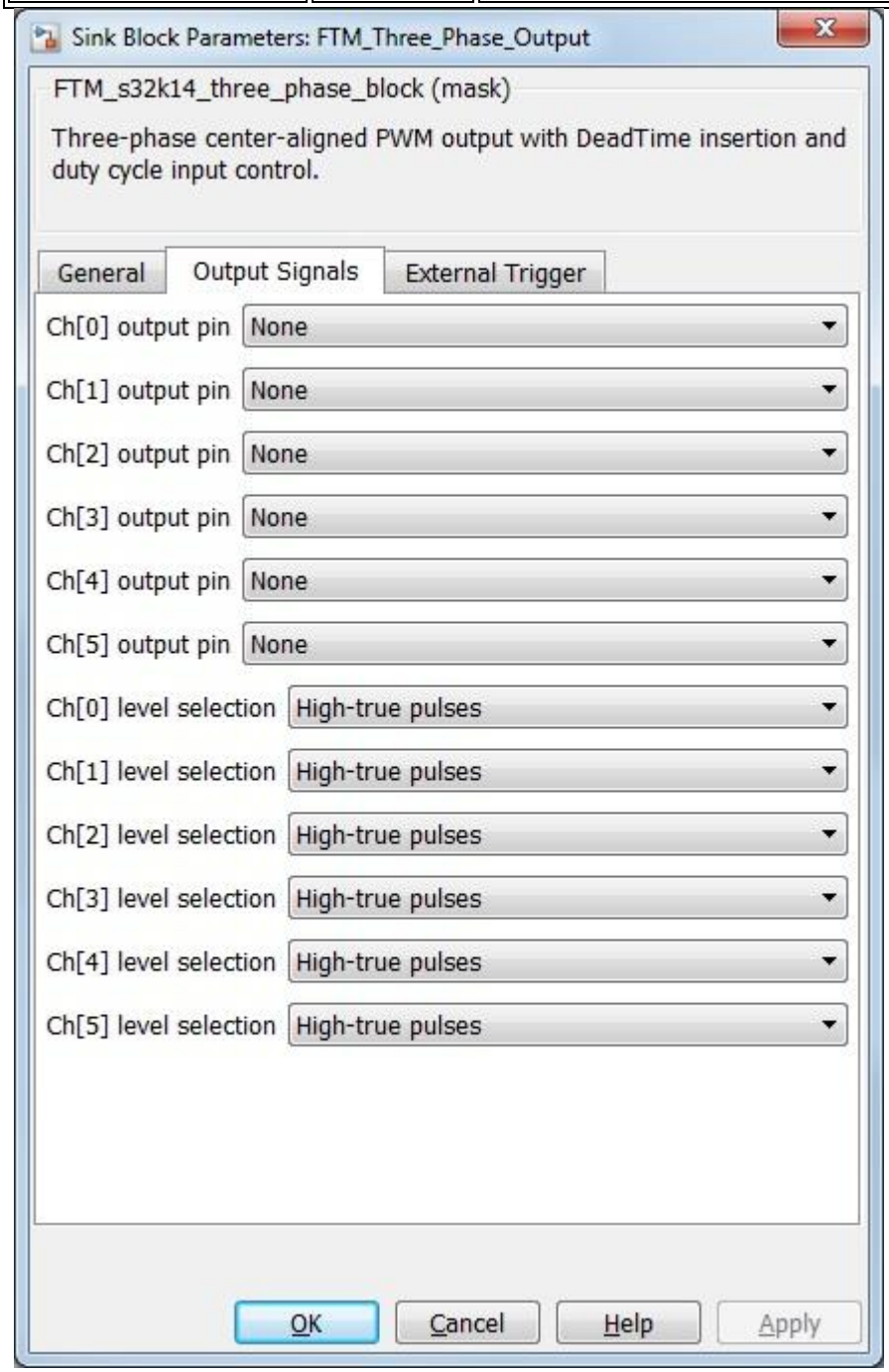
C Pair			Cycle of channel pair output
Initial Deadtime	Text-box	0 – 63 IPBus clock cycles	Deadtime during 0 to 1 transitions of the PWM channel pair output
Deadtime Prescaler	List-box	1 4 16	Only available when using clock cycles for Deadtime
Deadtime values in	List-box	– IPBus clock cycles – nanoseconds	Units used for Deadtime
Duty Cycle Simulation Output	Check-box	On/Off	If DutyCycle simulation output is used



- The Output Signals tab contains the following parameters:

Names	Selection Types	Range	Description
Ch[x] output pin	List-box	The list of available pins depends on the selected Channel.	pin selection

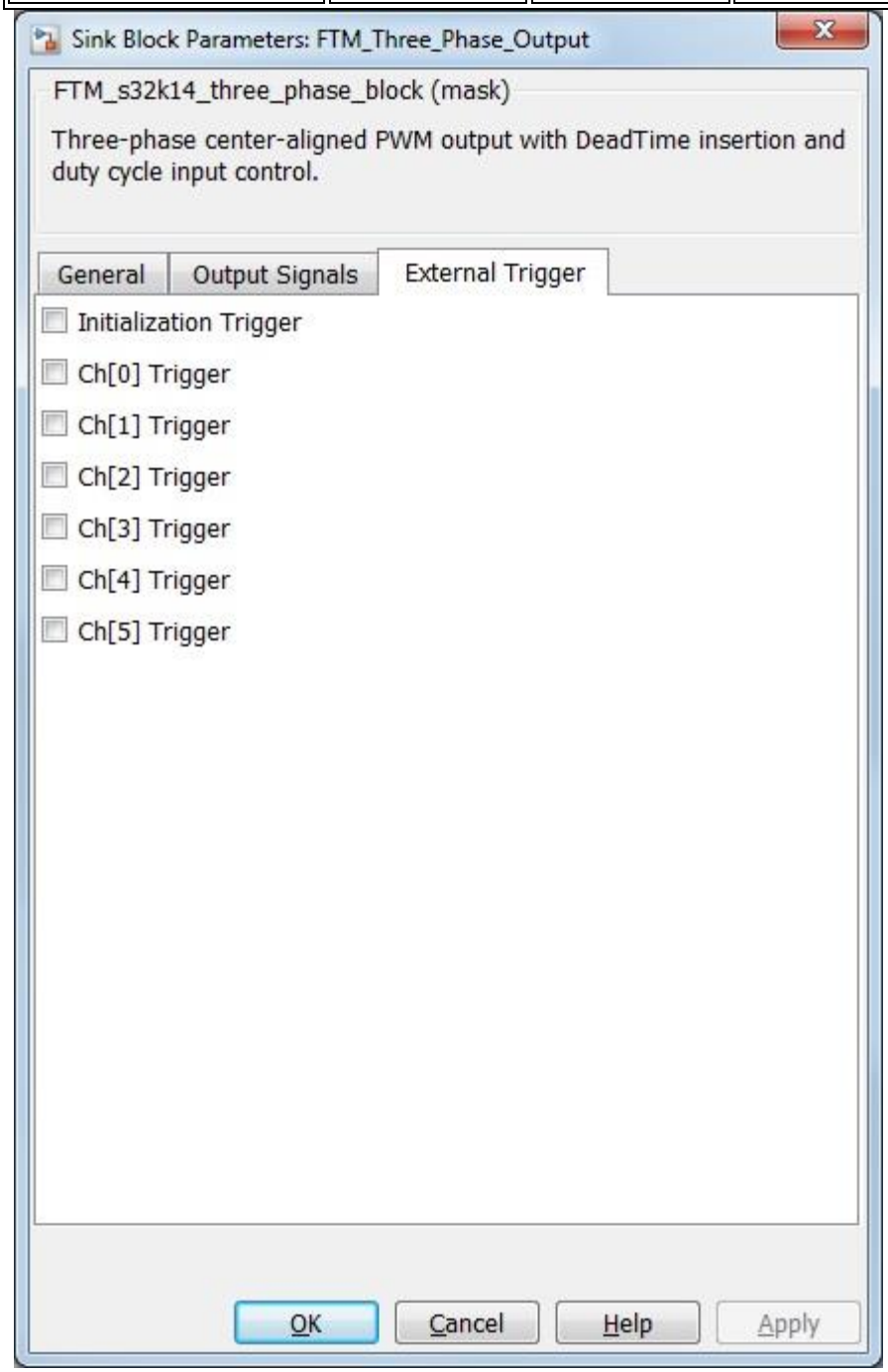
Ch[x] Output Polarity	Check-box	High-true pulses Low-true pulses	



- The External Triggers tab contains the following parameters:

Names	Selection Types	Range	Description

Initialization Channel x Trigger	Check-box	On/Off	Enable generation of Output Trigger signal based on the counter value matching of register value or initialization of FTM counter.



5.2.9.7 Block Dependency

None

5.2.9.8 Block Miscellaneous Details:

Duty Cycle output signal needed for simulation purpose only.

5.2.10 FTM Frequency Update Block

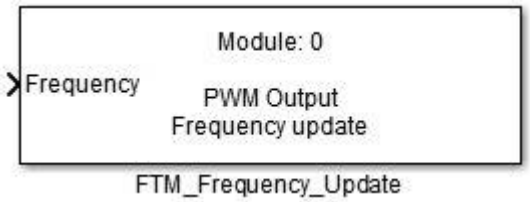
5.2.10.1 Block Name

PWM Frequency Update Block

5.2.10.2 Block Description

The functionality of the block is to update the PWM Frequency for FTM during runtime.

5.2.10.3 Block Image



5.2.10.4 Inputs:

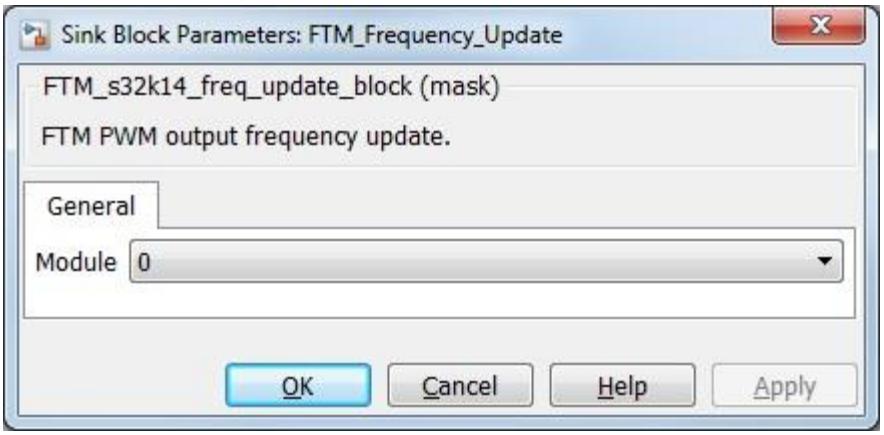
- Frequency (uint32)

5.2.10.5 Outputs:

- None

5.2.10.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
FTM Module	List-box	0 – 3	Select which FTM module to use.



5.2.10.7 Block Dependency

A PWM output block needs to be configured.

5.2.10.8 Block Miscellaneous Details:

1. The resolution of the input signal is dependent upon the configuration of the PWM Output block.

5.2.11 FTM PWM Deadtime Update Block

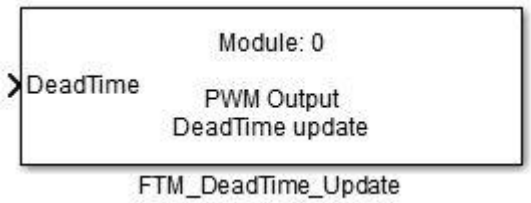
5.2.11.1 Block Name

PWM Deadtime Update Block

5.2.11.2 Block Description

The functionality of the block is to update the PWM Deadtime for FTM during runtime.

5.2.11.3 Block Image



5.2.11.4 Inputs:

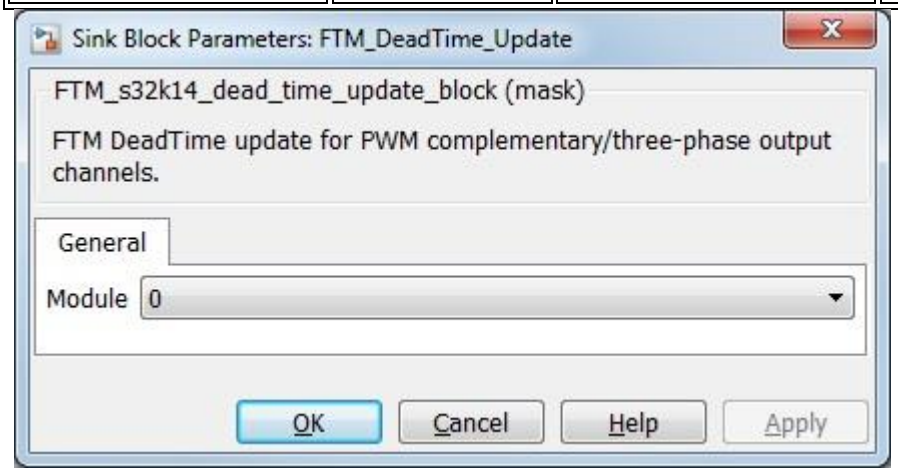
- Deadtime (uint32)

5.2.11.5 Outputs:

- None

5.2.11.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
FTM Module	List-box	0 – 3	Select which FTM module to use.



5.2.11.7 Block Dependency

Before using this block a FTM Complementary Output Block or FTM Three Phase Output Block needs to be configured.

5.2.11.8 Block Miscellaneous Details:

1. The resolution of the input signal is dependent upon the configuration of the PWM Output block.

5.2.12 FTM Channel ISR Block

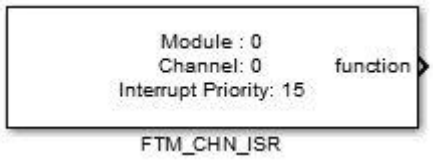
5.2.12.1 Block Name

FTM Channel ISR Block

5.2.12.2 Block Description

The main functionality of the block is to generate a function call if an event occurs on the selected module/channel.

5.2.12.3 Block Image



5.2.12.4 Inputs:

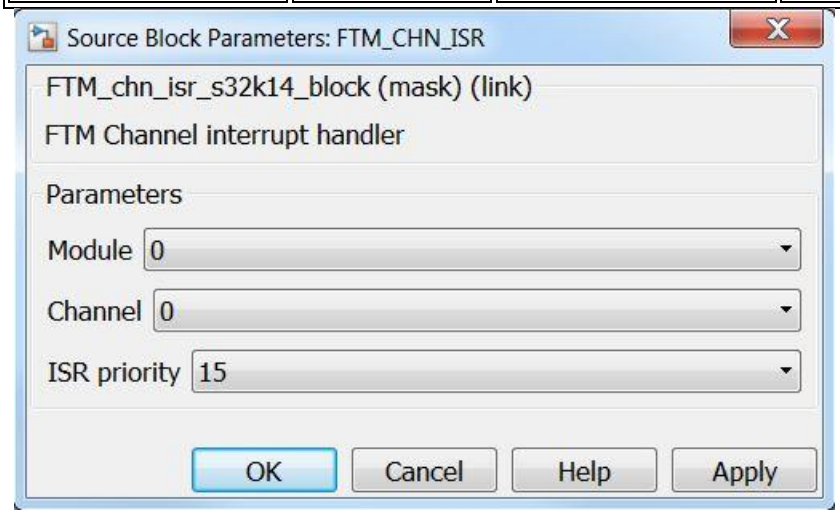
- None

5.2.12.5 Outputs:

- Function-call

5.2.12.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Module	List-box	0 – 3	Module selection
Channel	List-box	0 – 7	Channel selection
ISR Priority	List-box	0 – 15	Interrupt priority level. A lower priority value indicates a higher ISR priority



5.2.12.7 Block Dependency

None

5.2.12.8 Block Miscellaneous Details:

Channel(2n) and Channel(2n+1) with n=0..3 are using the same interrupt source. For more details refer to FTM Interrupts chapter in the Reference Manual

5.2.13 FTM Input Edge Capture Block

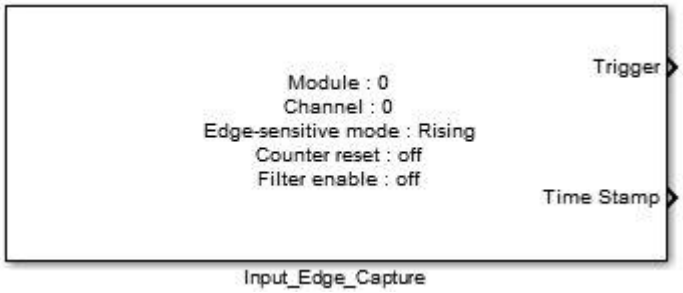
5.2.13.1 Block Name

Input Edge Capture Block

5.2.13.2 Block Description

The main functionality of the block is to generate a function call and get time stamp of the channel input event.

5.2.13.3 Block Image



5.2.13.4 Inputs:

- None

5.2.13.5 Outputs:

- Function-call
- Time in System Clock Ticks (uint16)

5.2.13.6 Block Dialog and Parameters:

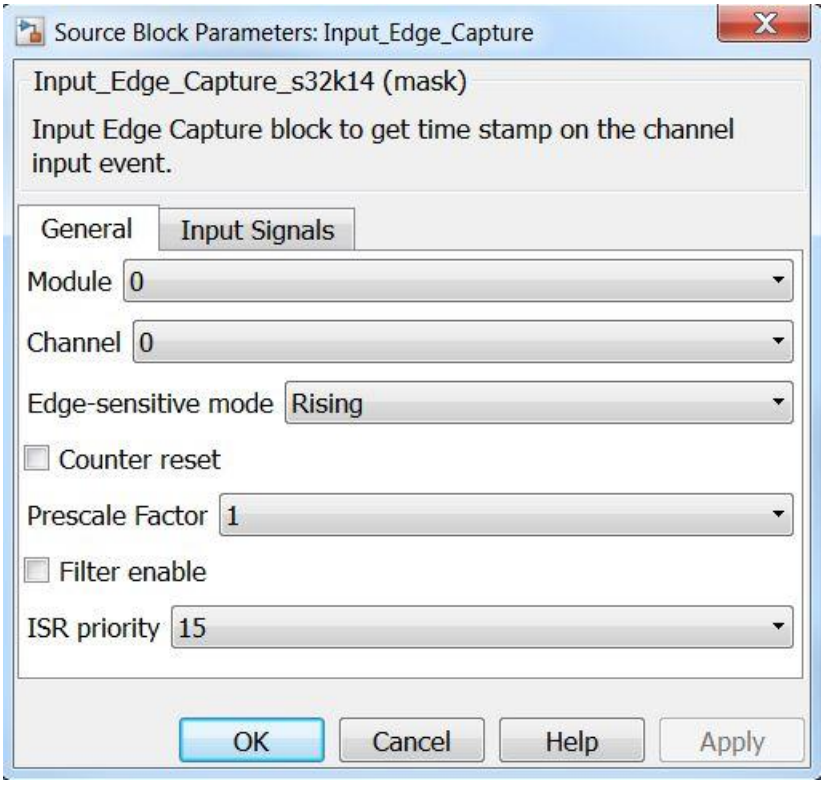
The block dialog consists of the following tabs:

- General
- Input Signals

- The General tab contains the following parameters:

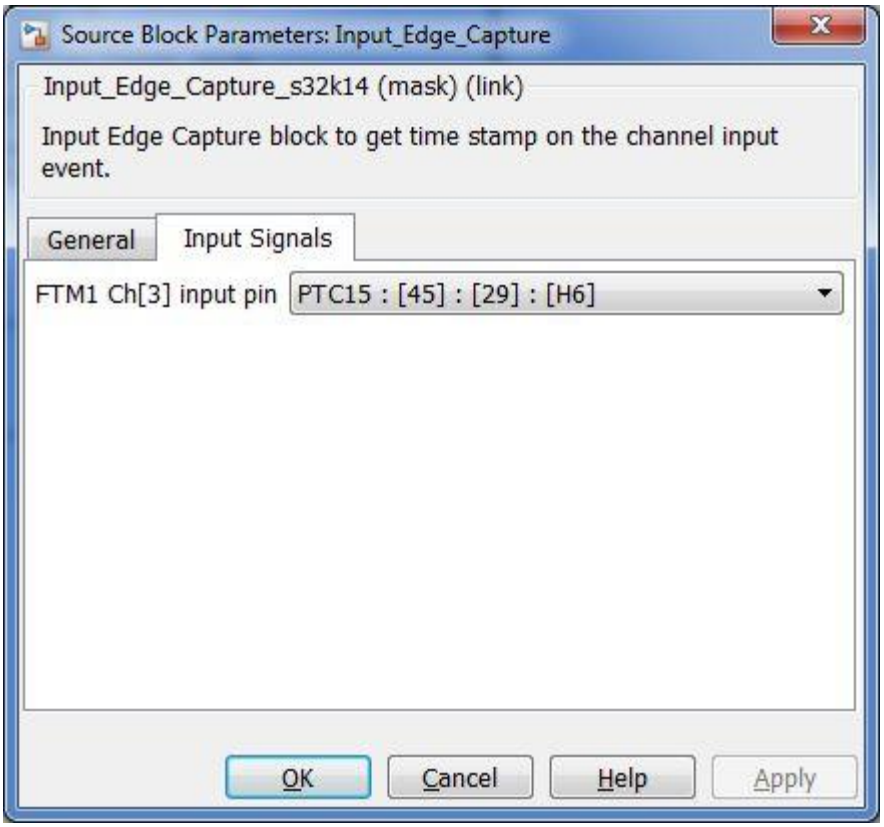
Names	Selection Types	Range	Description
Module	List-box	0 – 3	Module selection
Channel	List-box	0 - 7	Channel selection
Edge Selection	List-box	Rising Falling Rising or Falling	Get the time stamp on the event chosen
Counter Reset	Check-box	Enable/Disable	Reset the counter

			after each detected event.
Prescale factor for Time Stamp	List-box	1 2 4 8 16 32 64 128	The selected prescale factor for the time stamp
Filter Enable	Check-box	Enable/Disable	When enabled will show value field
ISR Priority	List-box	0 – 15	Interrupt priority level
FTM1/2 Ch0/1 Input Src. Only for Module 1 Channel 0, Module 2 Channels 0 and 1.	List-box	- FTM1_CH0 input / FTM2_CH0 input / FTM2_CH1 input - CMP0 output / Exclusive OR of FTM2_CH0 FTM2_CH1 and FTM1_CH1	Choose Input source for FTM1/2 Ch0/1



- The Input signal tab contains the following parameters:

Names	Selection Types	Range	Description
Input pin	List-box	Several Pins	Defines which input pin the signal to be measured is on.



5.2.13.7 Block Dependency

None

5.2.13.8 Block Miscellaneous Details:

None

5.2.14 FTM Dual Edge Capture Block

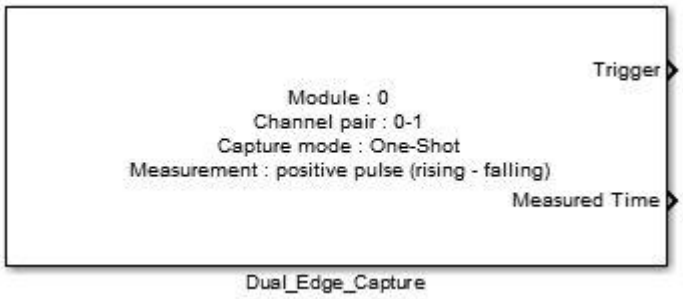
5.2.14.1 Block Name

Dual Edge Capture Block

5.2.14.2 Block Description

Dual Edge Capture block for signal pulse or period measurement on the even channel input.

5.2.14.3 Block Image



5.2.14.4 Inputs:

- None

5.2.14.5 Outputs:

- Function-call
- Time in System Clock Ticks (uint16)

5.2.14.6 Block Dialog and Parameters:

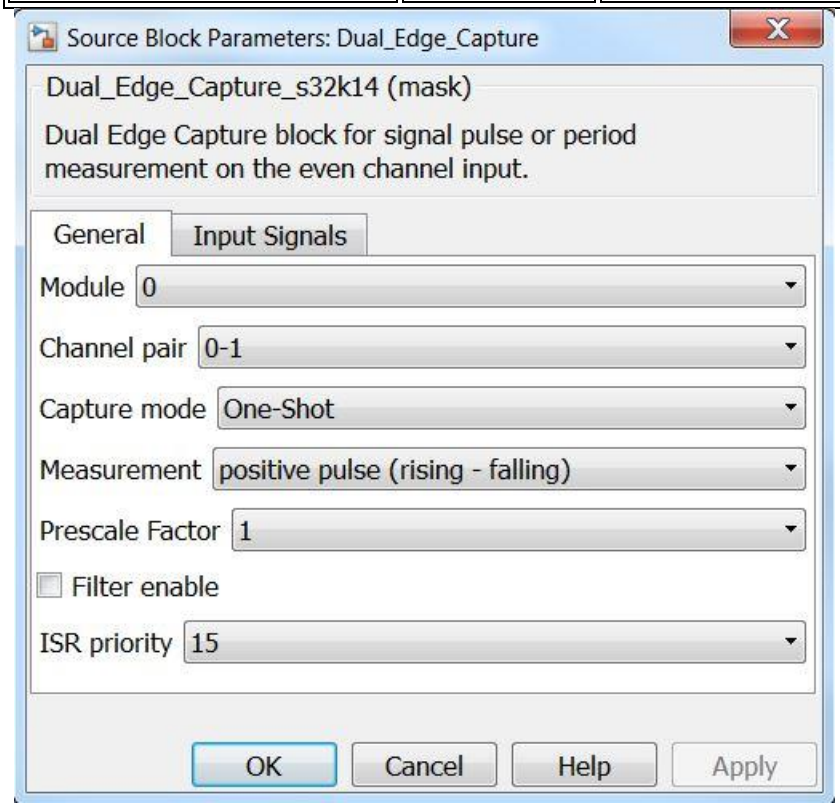
The block dialog consists of the following tabs:

- General
- Input Signals

- The General tab contains the following parameters:

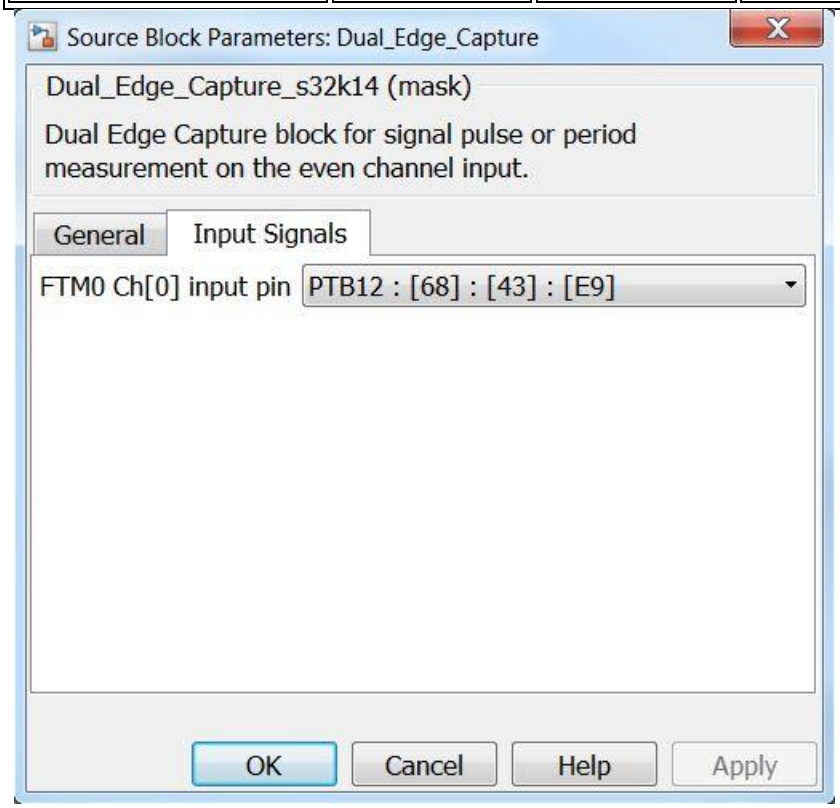
Names	Selection Types	Range	Description
Module	List-box	0 – 3	Module selection
Channel pair	List-box	0-1 2-3 4-5 6-7	Enables the Dual Edge Capture mode in the channels (n) and (n+1).
Capture Mode	List-box	One-Shot Continuous	Capture selection
Measurement	List-box	Positive Pulse (Rising to Falling) Negative Pulse (Falling to	Select edges to use

		Rising) Period (Rising to Rising) Period (Falling to Falling)	
Prescale factor for Time Stamp	List-box	1 2 4 8 16 32 64 128	The selected prescale factor for the time stamp
Filter Enable	Check-box	Enable/Disable	When enabled will show value field
ISR Priority	List-box	0 – 15	Interrupt priority level



- The Input signal tab contains the following parameters:

Names	Selection Types	Range	Description
Input pin	List-box	Several Pins	Defines which input pin the signal to be measured is on.



5.2.14.7 Block Dependency

None

5.2.14.8 Block Miscellaneous Details:

None

5.2.15 FTM Restart Dual Edge Capture Block

5.2.15.1 Block Name

Restart Dual Edge Capture Block

5.2.15.2 Block Description

The main functionality of the block is to restart the dual edge capture when operating in one-shot mode.

5.2.15.3 Block Image

5.2.15.4 Inputs:

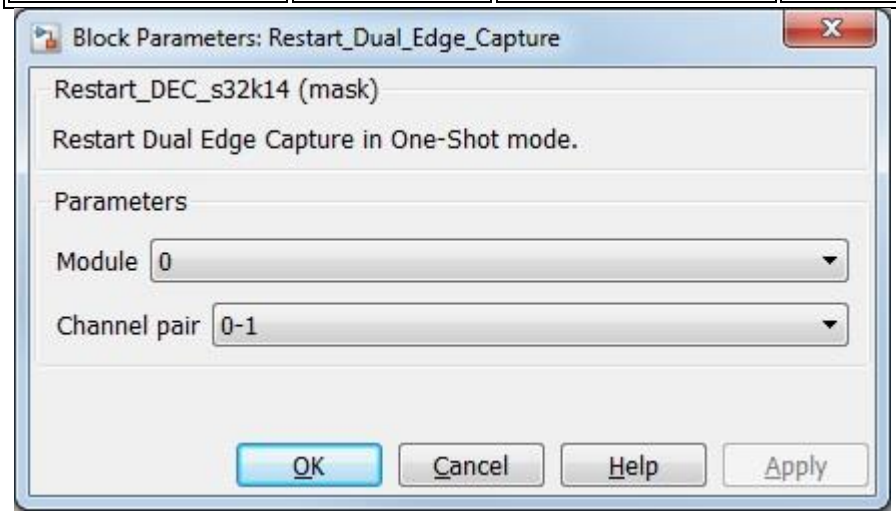
- None

5.2.15.5 Outputs:

- None

5.2.15.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Module	List-box	0 – 3	Module selection
Channel Pair	List-box	0 – 1 2 – 3 4 – 5 6 – 7	PWM channel pair



5.2.15.7 Block Dependency

Dual edge capture block must present and configured for one-shot mode.

5.2.15.8 Block Miscellaneous Details:

None

5.2.16 FTM Quadrature Decoder Block

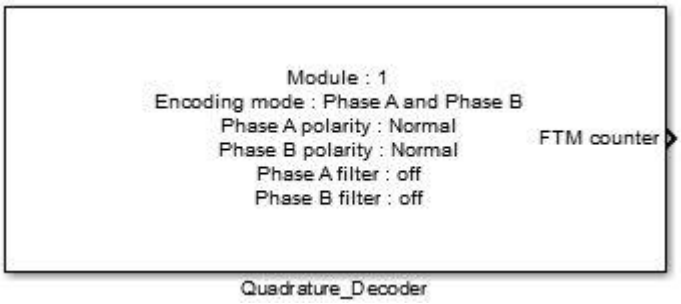
5.2.16.1 Block Name

Quadrature Decoder Block

5.2.16.2 Block Description

The main functionality of the block is to take input signals phase A and phase B to control the FTM counter increment and decrement.

5.2.16.3 Block Image



5.2.16.4 Inputs:

- None

5.2.16.5 Outputs:

- FTM Counter value (sint16)

5.2.16.6 Block Dialog and Parameters:

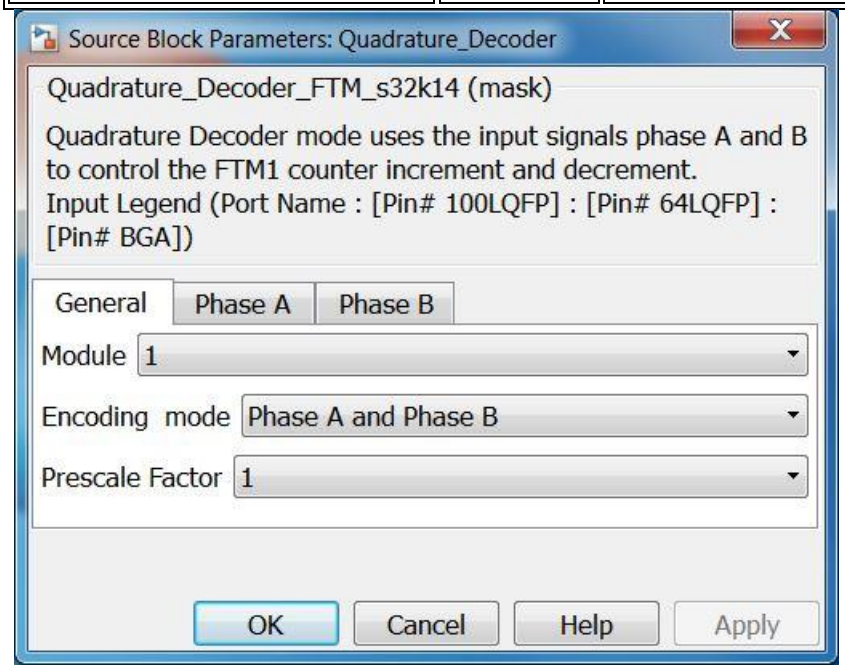
The block dialog consists of the following tabs:

- General
- Phase A
- Phase B

- The General tab contains the following parameters:

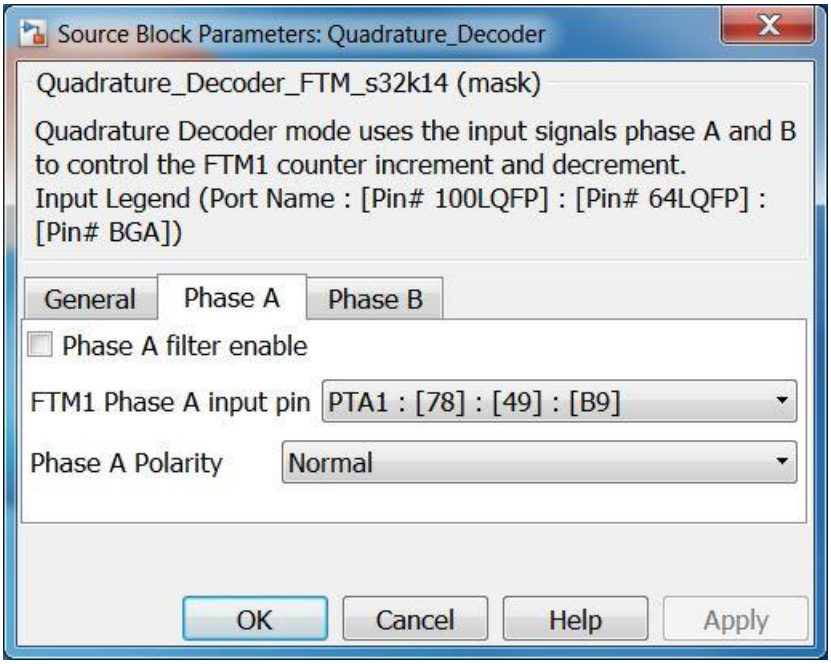
Names	Selection Types	Range	Description
Module	List-box	1 – 2	eFlexTimer module
Encoding Mode	List-box	Phase A and Phase B Count and Direction	Initial frequency of PWM output signals
Prescale factor to apply on input	List-box	1	The selected prescale factor for

		2 4 8 16 32 64 128	input



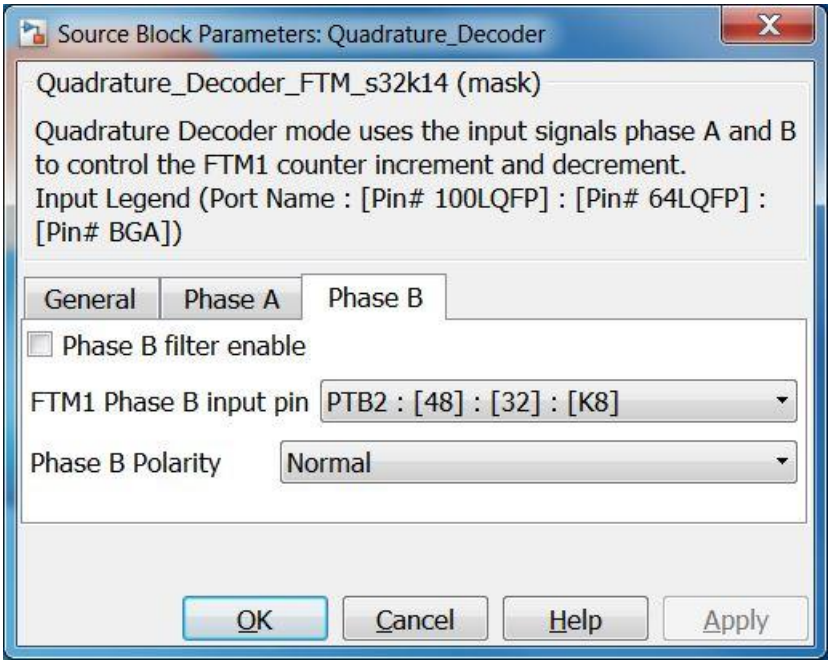
- The Phase A tab contains the following parameters:

Names	Selection Types	Range	Description
Phase A Filter Enable	Check-box	Enable/Disable	When enabled will show value field
Phase A input pin	List-box	The list of available pins depends on the selected module.	Pin selection
Phase Polarity	List-box	Normal Inverted	



- The Phase B tab contains the following parameters:

Names	Selection Types	Range	Description
Phase B Filter Enable	Check-box	Enable/Disable	When enabled will show value field
Phase B input pin	List-box	The list of available pins depends on the selected module.	Pin selection
Phase Polarity	List-box	Normal Inverted	



5.2.16.7 Block Dependency

None

5.2.16.8 Block Miscellaneous Details:

None

5.2.17 FTM Timer Overflow Block

5.2.17.1 Block Name

FTM Timer Overflow Block

5.2.17.2 Block Description

The main functionality of the block is to generate a function call on a timer overflow.

5.2.17.3 Block Image

5.2.17.4 Inputs:

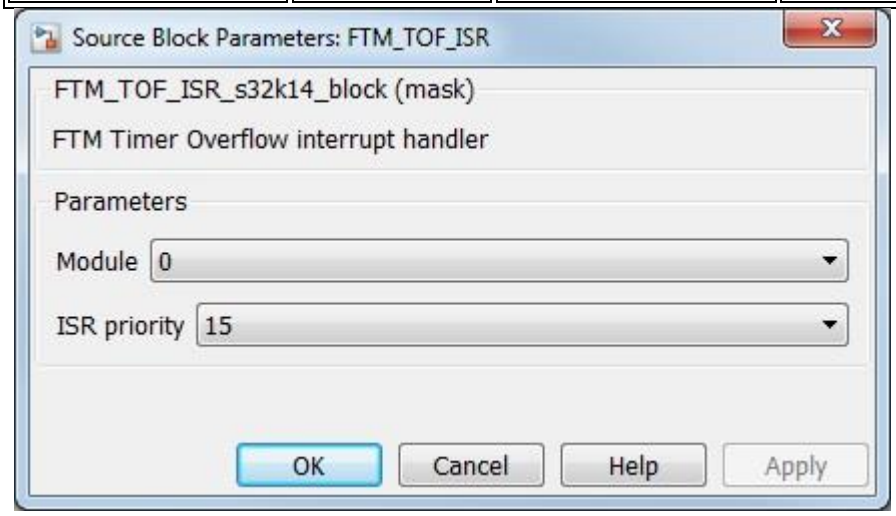
- None

5.2.17.5 Outputs:

- Function-call

5.2.17.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Module	List-box	0 – 3	Module selection
ISR Priority	List-box	0 – 15	Interrupt priority level. A lower priority value indicates a higher ISR priority



5.2.17.7 Block Dependency

None

5.2.17.8 Block Miscellaneous Details:

None

5.2.18 FTM ISR Enable/Disable Block

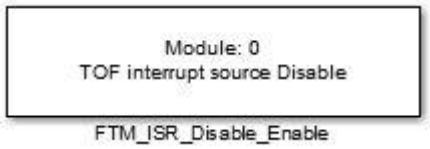
5.2.18.1 Block Name

FTM ISR Enable Disable Block

5.2.18.2 Block Description

The main functionality of the block is to allow the user to Enable/Disable FTM Timer Overflow and Channel ISRs.

5.2.18.3 Block Image



5.2.18.4 Inputs:

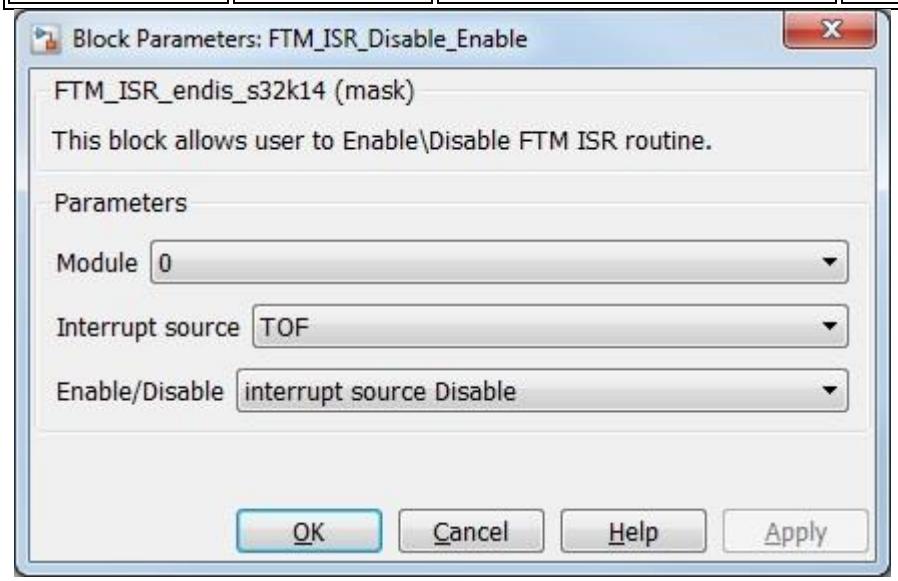
- None

5.2.18.5 Outputs:

- None

5.2.18.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Module	List-box	0 – 3	Module selection
Interrupt Source	List-box	TOF; Channel 0-7	Select interrupt source
Enable/Disable	List-box	Enable/Disable	



5.2.18.7 Block Dependency

None

5.2.18.8 Block Miscellaneous Details:

None

5.3 Communication Blocks

5.3.1 FCAN Configuration Block

Flexible CAN interface to CAN network message transmission and reception.

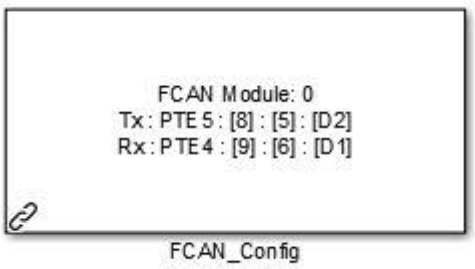
5.3.1.1 Block Name

FCAN Configuration Block

5.3.1.2 Block Description

The main functionality of the block is to configure FCAN module.

5.3.1.3 Block Image



5.3.1.4 Inputs:

- None

5.3.1.5 Outputs:

- None

5.3.1.6 Block Dialog and Parameters:

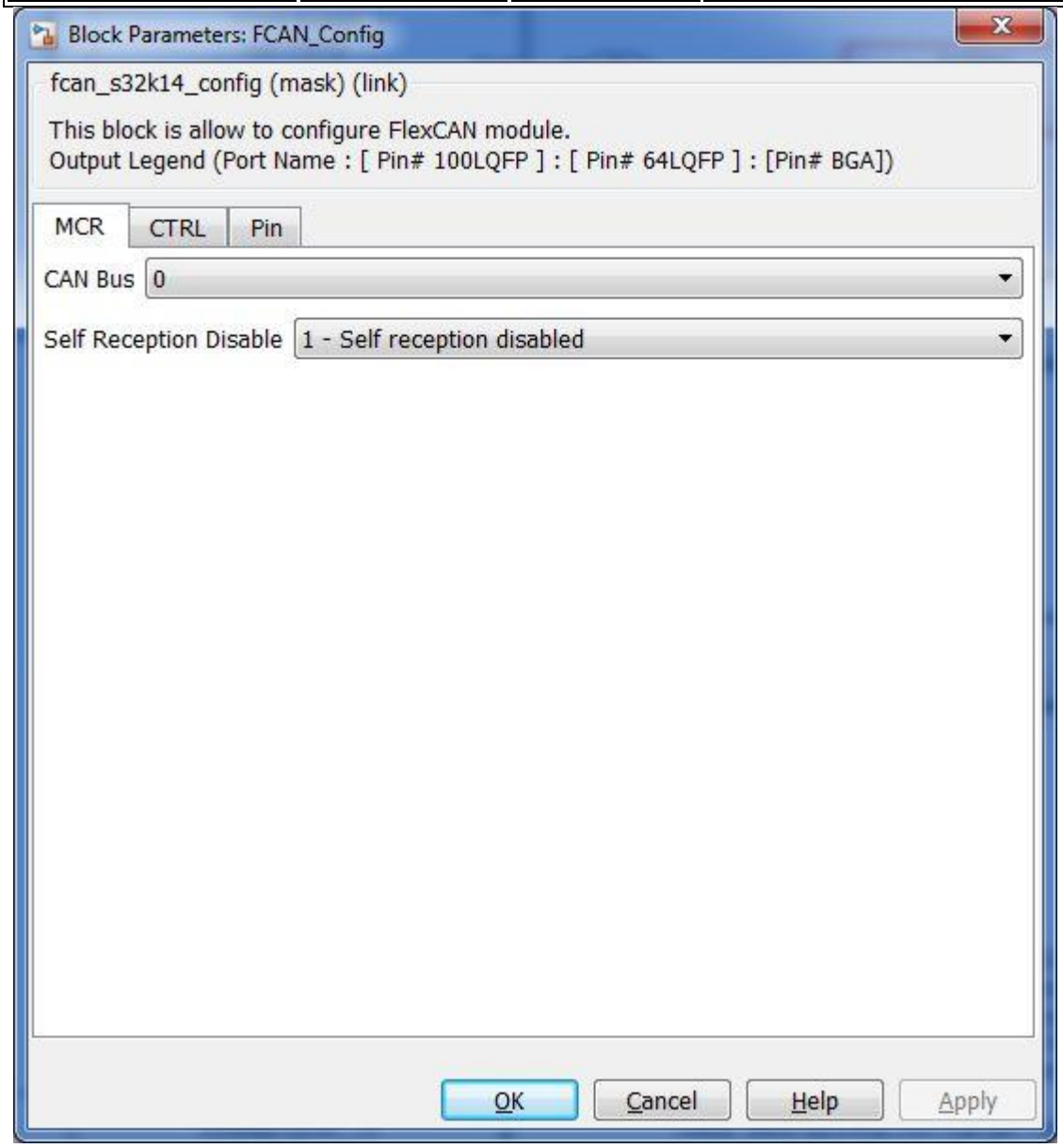
The block dialog consists of the following tabs:

- MCR
- CTRL
- Pin

- The MCR tab contains the following parameters:

Names	Selection Types	Range	Description
CAN Bus	List-Box	0 - 2	Select the CAN Bus name
Self Reception Disable	List-Box	0 – 1	0 – Self reception enabled

			1 – Self reception disabled



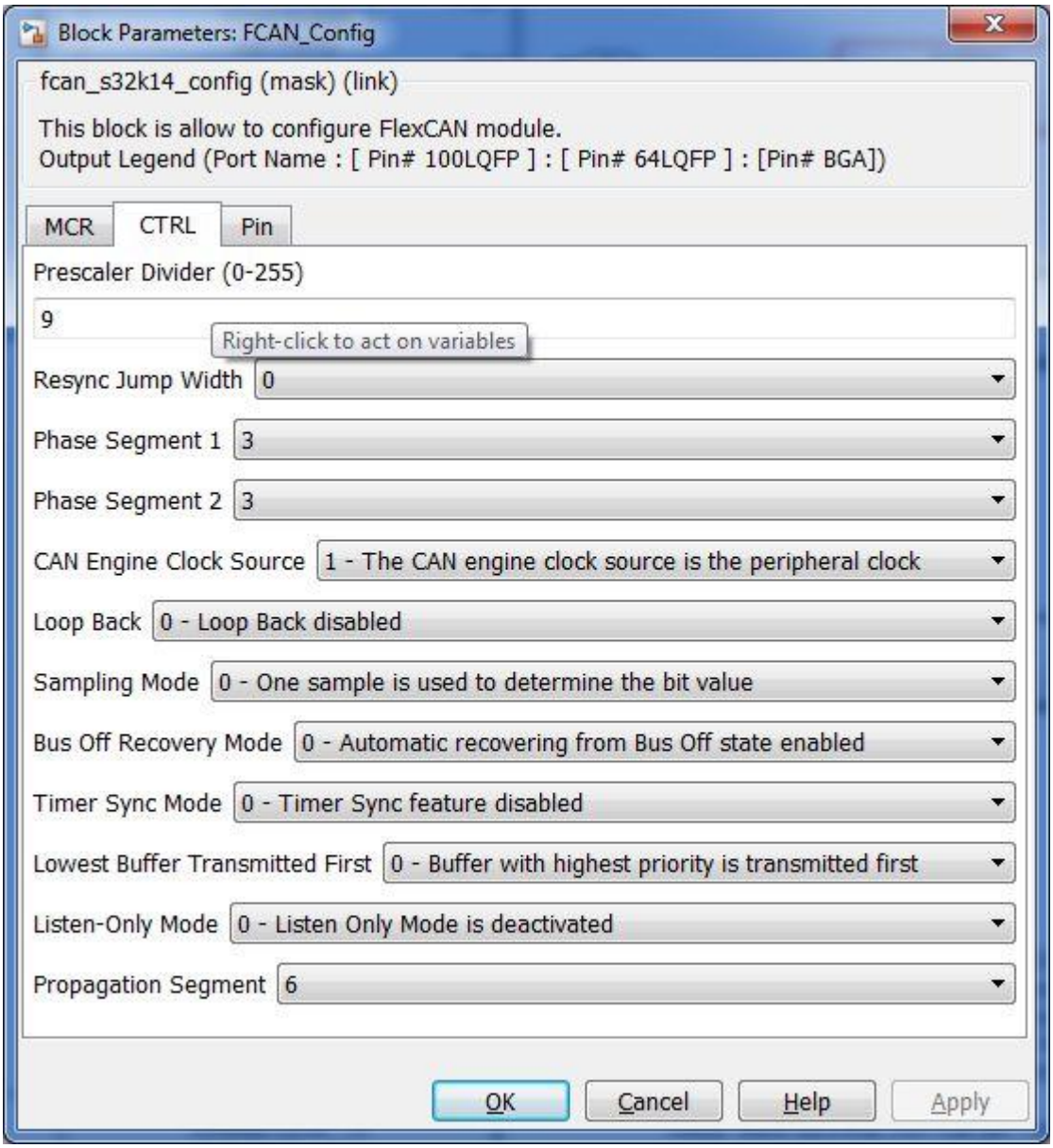
- The CTRL tab contains the following parameters:

Names	Selection Types	Range	Description
Prescaler Divider (0-255)	Text-box	0 – 255	This 8-bit field defines the ratio between the CPI clock frequency and the Serial Clock (Sclock) frequency. The Sclock period defines the time quantum of the

			CAN protocol. For the reset value, the Sclock frequency is equal to the CPI clock frequency. The Maximum value of this register is 0xFF, that gives a minimum Sclock frequency equal to the CPI clock frequency divided by 256
Resync Jump Width	List-Box	0 – 3	This 2-bit field defines the maximum number of time quanta1 that a bit time can be changed by one re-synchronization
Phase Segment 1	List-Box	0 – 7	This 3-bit field defines the length of Phase Buffer Segment 1 in the bit time. The valid programmable values are 0–7.
Phase Segment 2	List-Box	0 – 7	This 3-bit field defines the length of Phase Buffer Segment 2 in the bit time. The valid programmable values are 0–7.
CAN Engine Clock Source	List-Box	0 – The CAN Engine Clock Source is the oscillator clock 1 – The CAN Engine Clock Source is the peripheral bus clock	This bit selects the clock source to the CAN Protocol Interface (CPI) to be either the peripheral clock (driven by the FMPLL) or the crystal oscillator clock. The selected clock is the one fed to the prescaler to generate the Serial Clock (Sclock)
Loop Back	List-Box	0 – Loop Back disabled 1 – Loop Back enabled	This bit configures FlexCAN to operate in Loop-Back Mode. In this mode, FlexCAN performs an internal loop back that can be used for self test operation
Samplig Mode	List-Box	0 – One sample is used to determine the value of the received bit	This bit defines the sampling mode of CAN bits at the Rx input

		1 – Three samples are used to determine the value of the received bit	
Bus Off Recovery Mode	List-Box	0 – Automatic recovery from Bus Off state enabled 1 – Automatic recovery from Bus Off state disabled	This bit defines how FlexCAN recovers from Bus Off state
Timer Sync Mode	List-Box	0 – Timer Sync feature disabled 1 – Timer Sync feature enabled	This bit enables a mechanism that resets the free-running timer each time a message is received in Message Buffer 0
Lowest Buffer Transmitted First	List-Box	0 – Buffer with highest priority is transmitted first 1 – Lowest number buffer is transmitted first	This bit defines the ordering mechanism for Message Buffer transmission
Listen-Only Mode	List-Box	0 – Listen Only Mode is deactivated 1 – FlexCAN module operates in Listen Only Mode	This bit configures FlexCAN to operate in Listen Only Mode. In this mode, transmission is disabled, all error counters are frozen and the module operates in a CAN Error Passive mode
Propagation Segment	List-Box	0 – 7	This 3-bit field defines the length of the Propagation Segment in the bit time. The valid programmable values are 0–7.

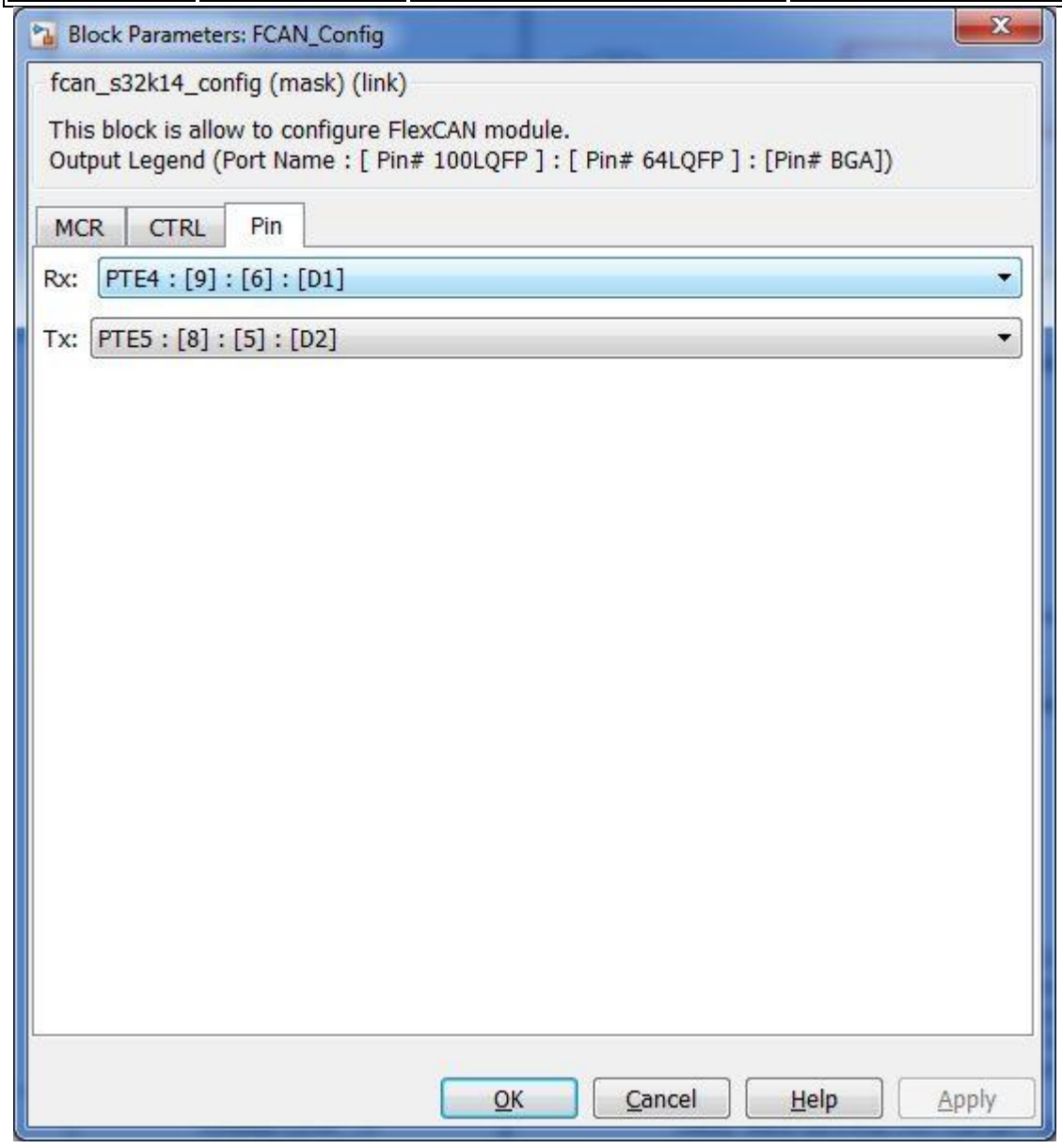
* Read Hardware Manual documentation to get more information.



- The Pin tab contains the following parameters:

Names	Selection Types	Range	Description
Rx	List-Box	For CAN0: PTE4 : [9] : [6] : [D1] PTC2 : [30] : [21] : [J3] PTB0 : [54] : [34] : [J10] For CAN1: PTC6 : [81] : [52] : [C7] PTA12 : [90] : [56] : [A5]	Rx Pin Selection

		For CAN2: PTC16 : [44] : [28] : [J7] PTB12 : [68] : [43] : [E9]	
Tx	List-Box	For CAN0: PTE5 : [8] : [5] : [D2] PTC3 : [29] : [20] : [J2] PTB1 : [53] : [33] : [J9] For CAN1: PTC7 : [80] : [51] : [B8] PTA13 : [89] : [55] : [A6] For CAN2: PTC17 : [43] : [27] : [K7] PTB13 : [67] : [42] : [E8]	Tx Pin Selection



5.3.1.7 Block Dependency

None

5.3.1.8 Block Miscellaneous Details:

None

5.3.2 FCAN Receive Data Block

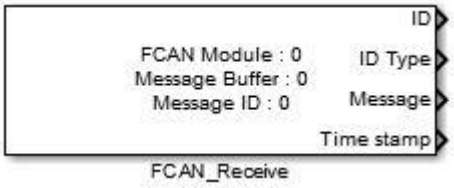
5.3.2.1 Block Name

FCAN Receive Data Block

5.3.2.2 Block Description

The main functionality of the block is to read a FlexCAN message.

5.3.2.3 Block Image



5.3.2.4 Inputs:

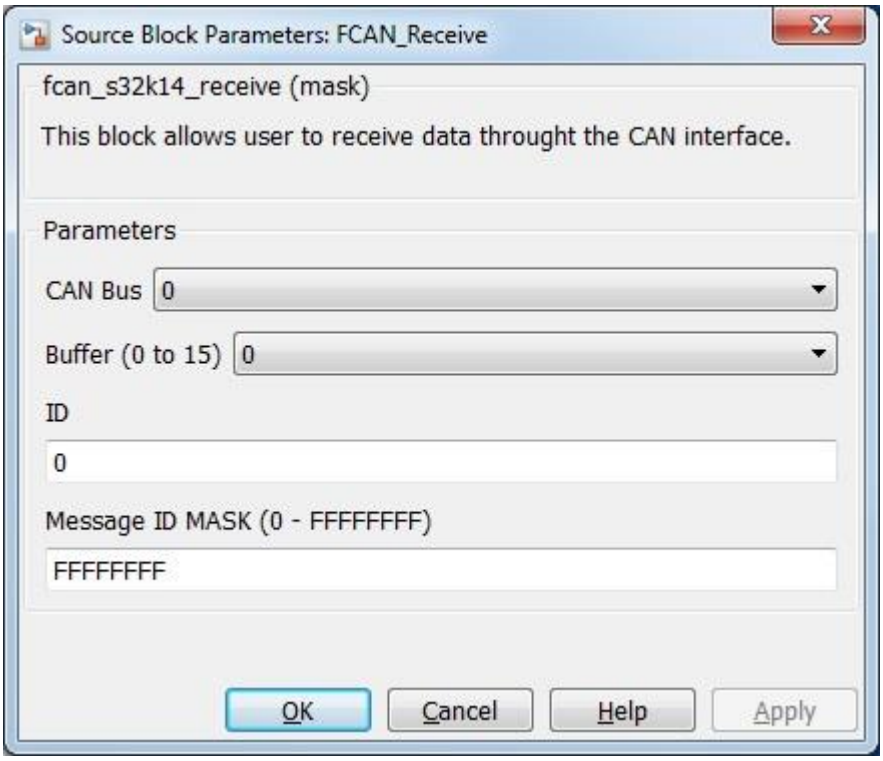
- None

5.3.2.5 Outputs:

- ID (uint8)
- ID Type (uint8)
- Message (uint8(8))
- Time stamp (unit16)

5.3.2.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
CAN Bus	List-Box	0 - 2	CAN Module
Buffer	List-Box	0 – 15	Buffer Number
ID	Text-box		ID of the message to receive
Message ID Mask	Text-box	0 - FFFFFFFF	Message maske to use for the Buffer.



5.3.2.7 Block Dependency

Please do the following:

1. Configure FCAN

5.3.2.8 Block Miscellaneous Details:

Please refer "CAN Configiration block" to get information about pin assignment.

5.3.3 FCAN Receive Data Trigger Block

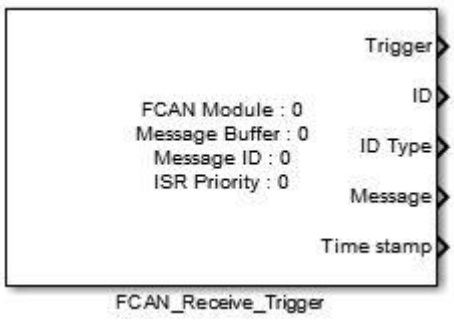
5.3.3.1 Block Name

FCAN Receive Data Trigger Block

5.3.3.2 Block Description

The main functionality of the block is to call user function when FCAN message will come.

5.3.3.3 Block Image



5.3.3.4 Inputs:

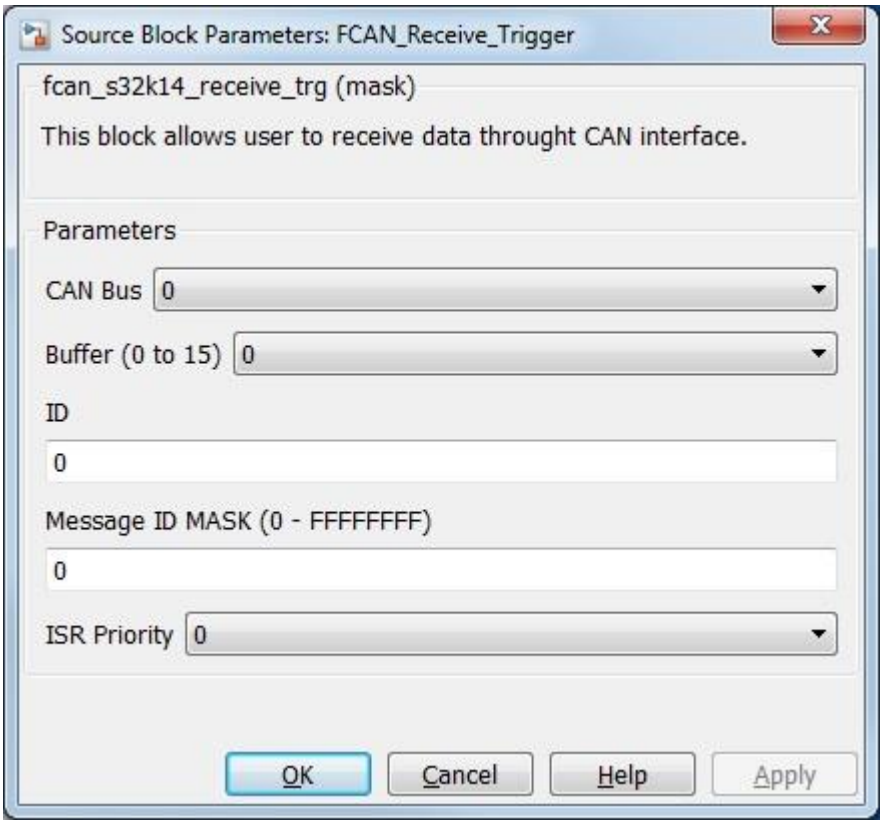
- None

5.3.3.5 Outputs:

- Function-Call
- ID (uint8)
- ID Type (uint8)
- Message (uint8(8))
- Time stamp (unit16)

5.3.3.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
CAN Bus	List-Box	0 - 2	CAN Module
Buffer	List-Box	0 – 15	Buffer Number
ID	Text-box		ID of the message to receive
Message ID Mask	Text-box	0 - FFFFFFFF	Message mask to use for the Buffer.
ISR Priority	List-Box	1 – 15	Global ISR Priority



5.3.3.7 Block Dependency

Please do the following:

1. Configure FCAN

5.3.3.8 Block Miscellaneous Details:

Please refer "CAN Configiration block" to get information about pin assignment.

5.3.4 FCAN Transmit Block

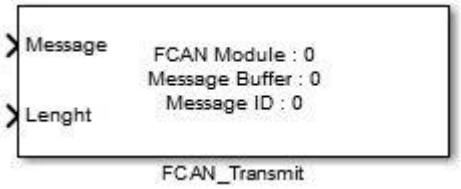
5.3.4.1 Block Name

FCAN Transmit Data Block

5.3.4.2 Block Description

The main functionality of the block is transmitting data through the FCAN interface.

5.3.4.3 Block Image



5.3.4.4 Inputs:

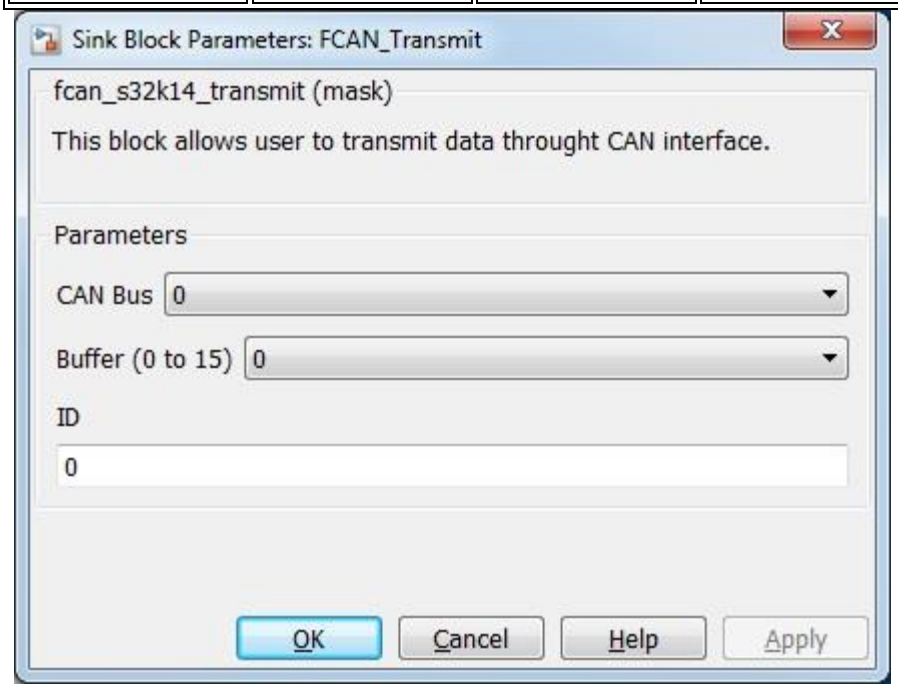
- Message (uint8(8))
- Length (uint8)

5.3.4.5 Outputs:

- None

5.3.4.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
CAN Bus	List-Box	0 - 2	CAN Module
Buffer	List-Box	0 – 15	Buffer Number
ID	Text-box		ID of the message to receive



5.3.4.7 Block Dependency

Please do the following:

1. Configure FCAN

5.3.4.8 Block Miscellaneous Details:

Please refer "CAN Configuration block" to get information about pin assignment.

5.3.5 FCAN ISR Block

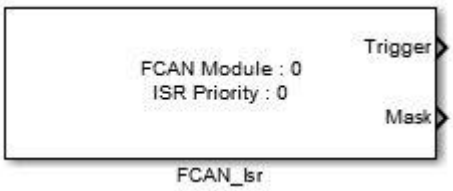
5.3.5.1 Block Name

FCAN ISR Block

5.3.5.2 Block Description

The main functionality of the block is to process FCAN ISR's.

5.3.5.3 Block Image



5.3.5.4 Inputs:

- None

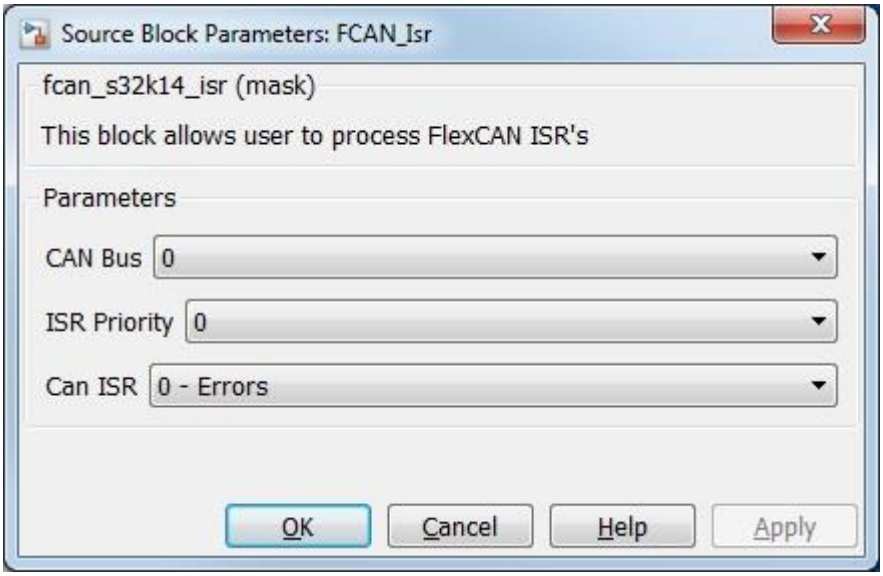
5.3.5.5 Outputs:

- Function-call
- Mask (uint32) - contains ESR register value when interrupt occurs.*

5.3.5.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
CAN Bus	List-Box	0 – 2	CAN Module
ISR Priority	List-Box	1 – 15	Global ISR Priority
CAN ISR	List-Box	0 - Errors 1 - Warnings	Interrupt source

* To get more information refer to Hardware Manual documentation.



5.3.5.7 Block Dependency

Please do the following:

1. Configure FlexCAN

5.3.5.8 Block Miscellaneous Details:

None

5.3.6 FCAN ISR Enable/Disable

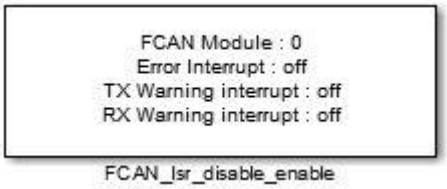
5.3.6.1 Block Name

FCAN Interrupt Enable/Disable Block

5.3.6.2 Block Description

The main functionality of the block is to enable/disable FCAN interrupts

5.3.6.3 Block Image



5.3.6.4 Inputs:

- None

5.3.6.5 Outputs:

- None

5.3.6.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
CAN Bus	Pop-up	0 - 2	CAN Module
Error interrupt	Check-box	Enable/Disable	This bit provides a mask for the Error Interrupt ERRINT in the CAN_ESR1 register.
Tx Warning interrupt	Check-box	Enable/Disable	This bit provides a mask for the Tx Warning Interrupt associated with the TWRNINT flag in the Error and Status Register 1 (ESR1). This bit is read as zero when CAN_MCR[WRNEN] bit is negated. This bit can be written only if CAN_MCR[WRNEN] bit is asserted.
Rx Warning interrupt	Check-box	Enable/Disable	This bit provides a mask for the Rx Warning Interrupt associated with the RWRNINT flag in the Error and Status Register 1 (ESR1). This bit is read as zero when CAN_MCR[WRNEN] bit is negated. This bit can be written only if CAN_MCR[WRNEN] bit is asserted.

5.3.6.7 Block Dependency

Please do the following:

1. Configure respective FCAN and its interrupts

5.3.6.8 Block Miscellaneous Details:

None

5.3.7 LPI2C Configuration Block

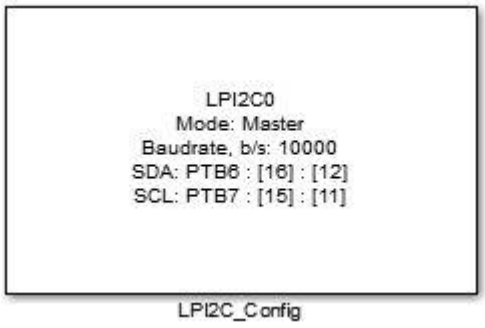
5.3.7.1 Block Name

I2C Configuration Block

5.3.7.2 Block Description

This block is used to configure the I2C module.

5.3.7.3 Block Image



5.3.7.4 Inputs:

- None

5.3.7.5 Outputs:

- None

5.3.7.6 Block Dialog and Parameters:

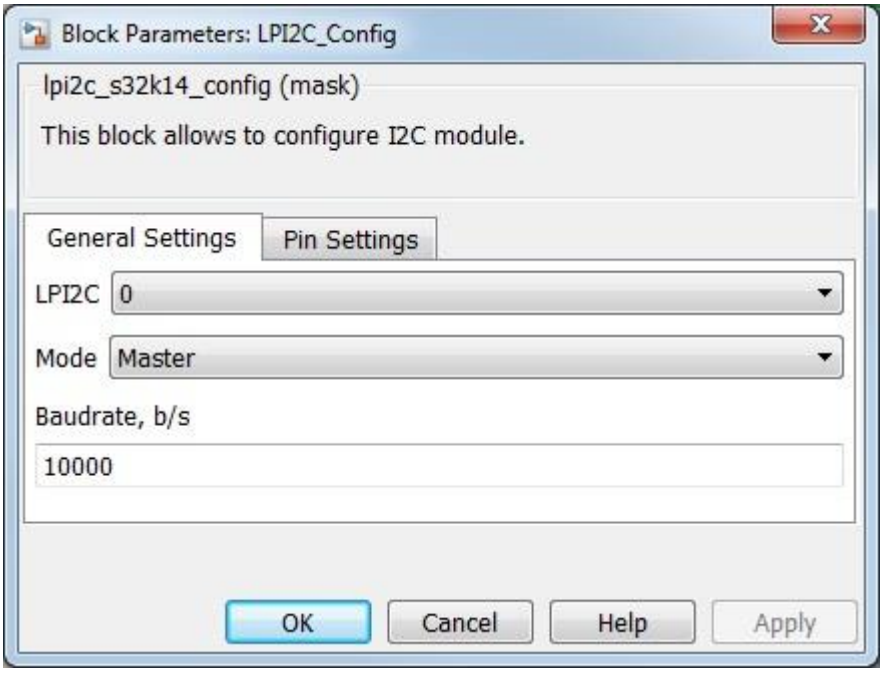
The block dialog consists of the following tabs:

- General Settings
- Address Parameters
- Pin Settings

- The General Settings tab contains the following parameters:

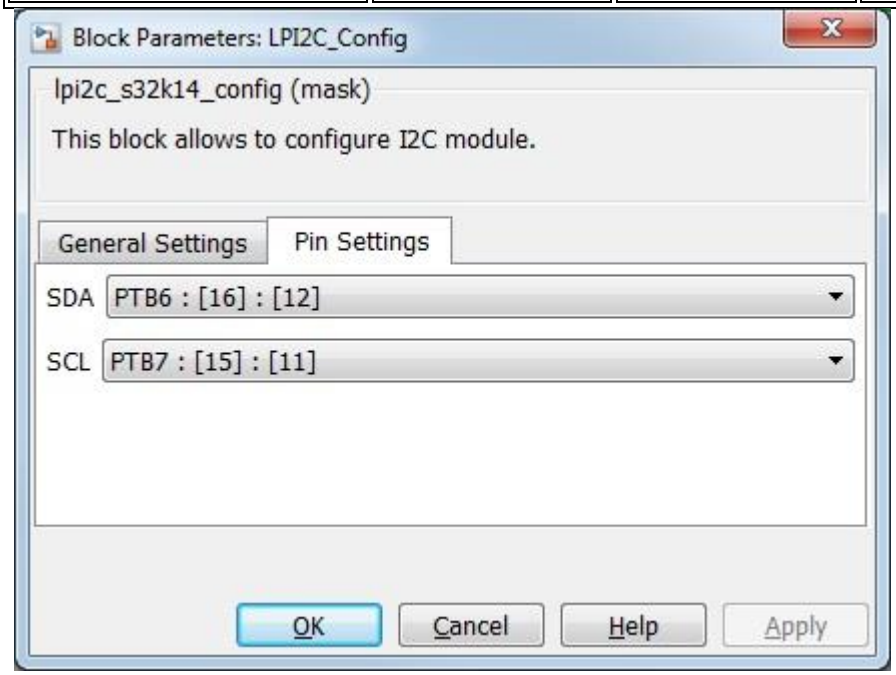
Names	Selection Types	Range	Description
I2C	List-box	0	Select I2C module.
Mode	List-box	Master Slave	Mode of operation * When Slave mode is selected all unnecessary settings disabled.
Baud Rate (BPS)	Text-box	0 to bus_clock/20/1000	The real baud rate is the closest possible value to specified baud rate. 32-bit integer value with resolution of 1 Baud.

* Read Hardware Manual documentation to get more information.



- The Pin Settings tab contains the following parameters:

Names	Selection Types	Range	Description
SDA	List-box	Pin Selections	Pin for I2C Data
SCL	List-box	Pin Selections	Pin for I2C Clock



5.3.7.7 Block Dependency

None

5.3.7.8 Block Miscellaneous Details:

None

5.3.8 LPI2C Transmit Block

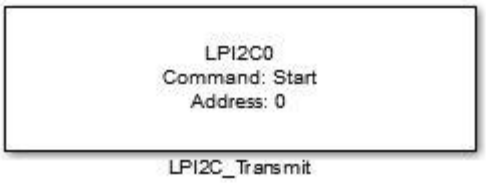
5.3.8.1 Block Name

I2C Transmit Block

5.3.8.2 Block Description

This block transmits data through a I2C module using basic operations of the i2c protocol. User will need to implement i2c state machine themselves.

5.3.8.3 Block Image



5.3.8.4 Inputs:

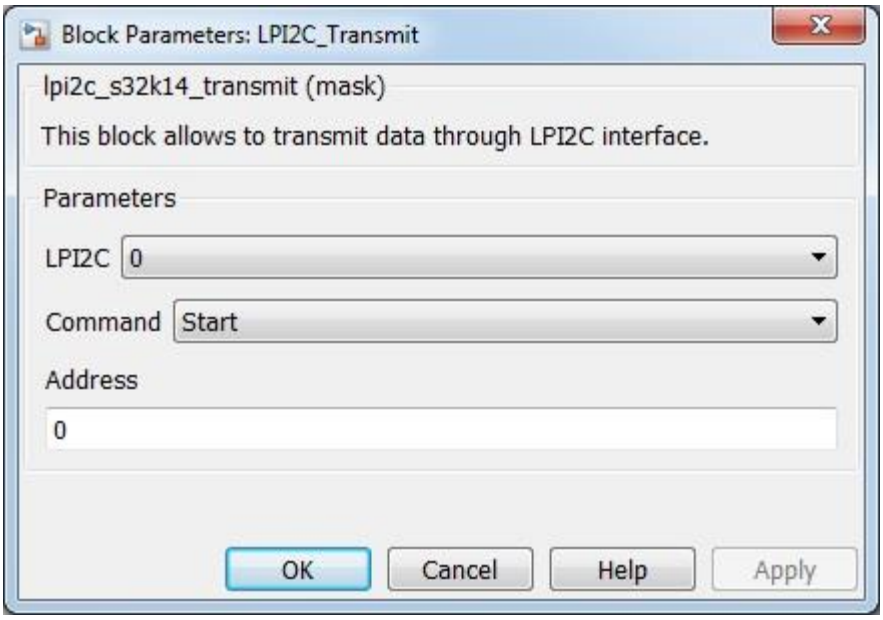
- Data to be transmitted (when Command is set to Receive) (uint8)

5.3.8.5 Outputs:

- None

5.3.8.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
I2C	List-box	0	Select I2C module.
Command	List-box	Start Receive Stop	Select which command to use.
Address	Text-box	0 - 1023	I2C slave address definition. Only available when Command is set to Start.



5.3.8.7 Block Dependency

Please do the following:

1. Configure I2C.

5.3.8.8 Block Miscellaneous Details:

None

5.3.9 LPI2C Receive Block

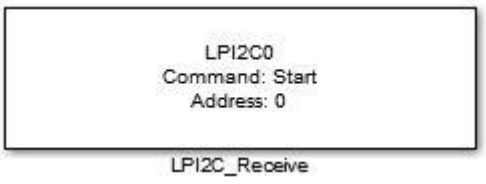
5.3.9.1 Block Name

I2C Receive Block

5.3.9.2 Block Description

This block receives data through an I2C module using basic operations of the i2c protocol. User will need to implement i2c state machine themselves.

5.3.9.3 Block Image



5.3.9.4 Inputs:

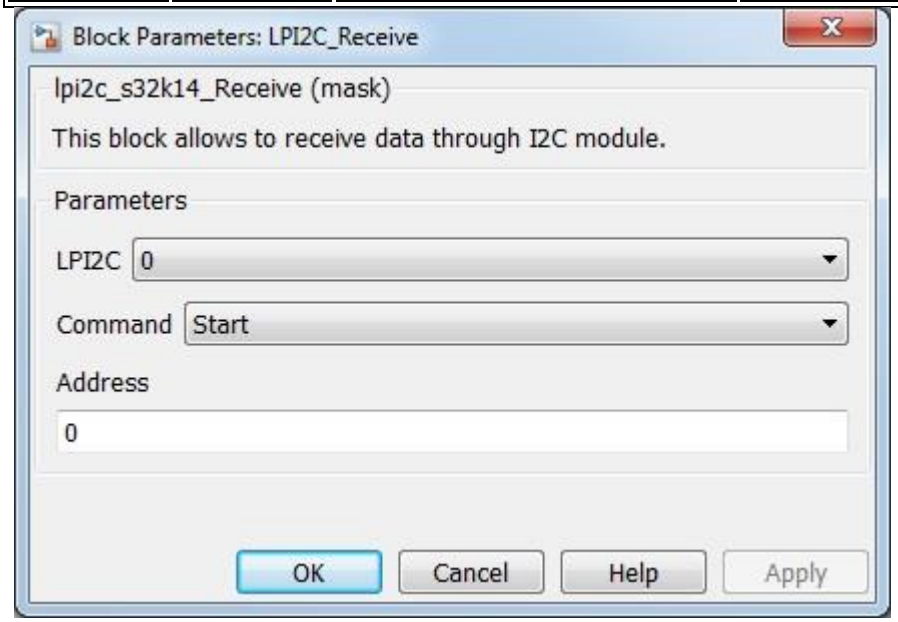
- None

5.3.9.5 Outputs:

- Data to be received (when Command is set to Receive) (uint8)

5.3.9.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
LPI2C	List-box	0	Select I2C module.
Command	List-box	Start Receive Stop	Select which command to use.
Address	Text-box	0 - 1023	I2C slave address definition. Only available when Command is set to Start.



5.3.9.7 Block Dependency

Please do the following:

1. Configure I2C.

5.3.9.8 Block Miscellaneous Details:

None

5.3.10 LPI2C ISR Block

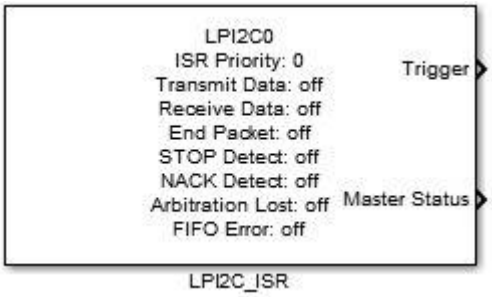
5.3.10.1 Block Name

I2C ISR Block

5.3.10.2 Block Description

The main functionality of the block is to process I2C ISRs.

5.3.10.3 Block Image



5.3.10.4 Inputs:

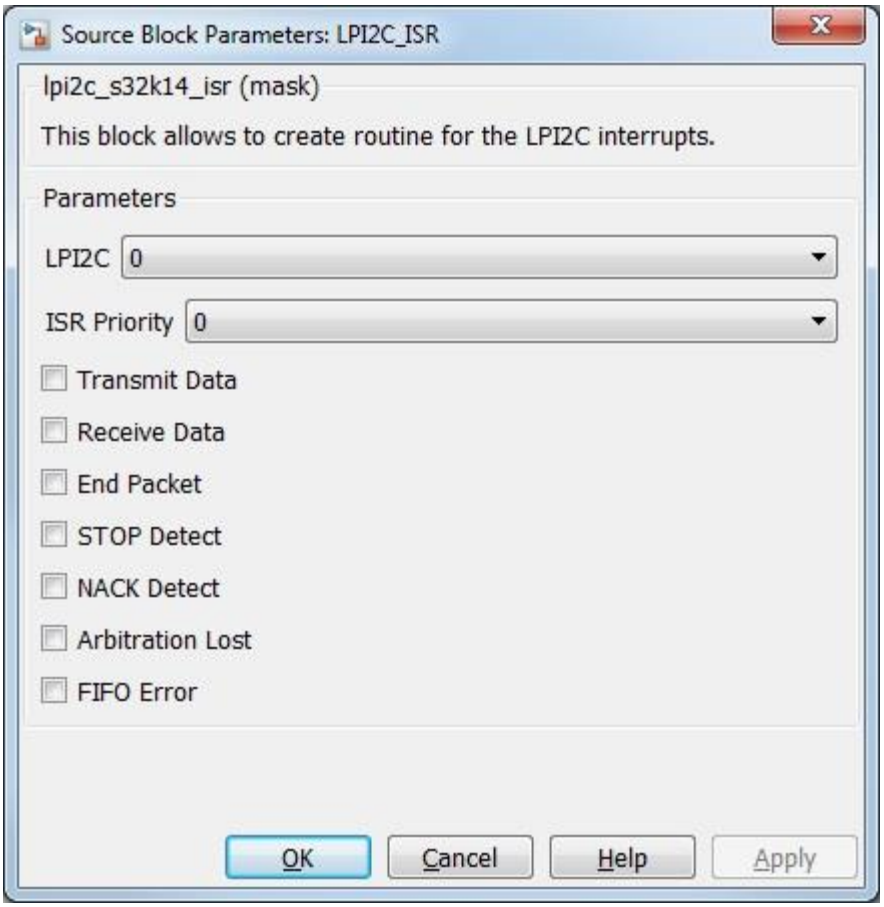
- None

5.3.10.5 Outputs:

- Function-Call
- Status Register (I2C_S) value (uint8)

5.3.10.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
LPI2C	List-box	0	Select I2C module.
ISR Level	List-box	0 – 15	Interrupt priority level
Transmit Data (TDIE)	Check-box	Enable/Disable	
Receive Data (RDIE)	Check-box	Enable/Disable	
End Packet (EPIE)	Check-box	Enable/Disable	
STOP Detect (SDIE)	Check-box	Enable/Disable	
NACK Detect (NDIE)	Check-box	Enable/Disable	
Arbitration Lost (ALIE)	Check-box	Enable/Disable	
FIFO Error (FEIE)	Check-box	Enable/Disable	



5.3.10.7 Block Dependency

Please do the following:

1. Configure I2C.

5.3.10.8 Block Miscellaneous Details:

I2C SMBus Control and Status register bit field description:

Field	Description
31–15 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
14 DMIE	Data Match Interrupt Enable 0 Interrupt disabled. 1 Interrupt enabled.
13 PLTIE	Pin Low Timeout Interrupt Enable 0 Interrupt disabled. 1 Interrupt enabled.
12 FEIE	FIFO Error Interrupt Enable 0 Interrupt enabled. 1 Interrupt disabled.
11 ALIE	Arbitration Lost Interrupt Enable 0 Interrupt disabled. 1 Interrupt enabled.
10 NDIE	NACK Detect Interrupt Enable 0 Interrupt disabled. 1 Interrupt enabled.
9 SDIE	STOP Detect Interrupt Enable 0 Interrupt disabled. 1 Interrupt enabled.
8 EPIE	End Packet Interrupt Enable 0 Interrupt disabled. 1 Interrupt enabled.
7–2 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
1 RDIE	Receive Data Interrupt Enable 0 Interrupt disabled. 1 Interrupt enabled.
0 TDIE	Transmit Data Interrupt Enable 0 Interrupt disabled. 1 Interrupt enabled

5.3.11 LPI2C ISR Enable/Disable Block

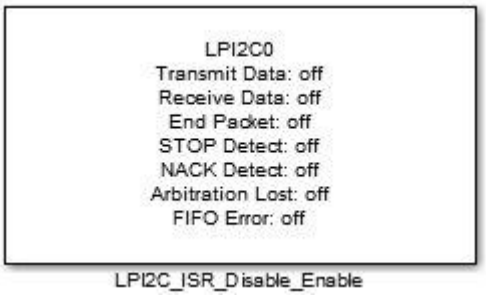
5.3.11.1 Block Name

I2C Interrupt Enable/Disable Block

5.3.11.2 Block Description

The main functionality of the block is to enable/disable I2C interrupts

5.3.11.3 Block Image



5.3.11.4 Inputs:

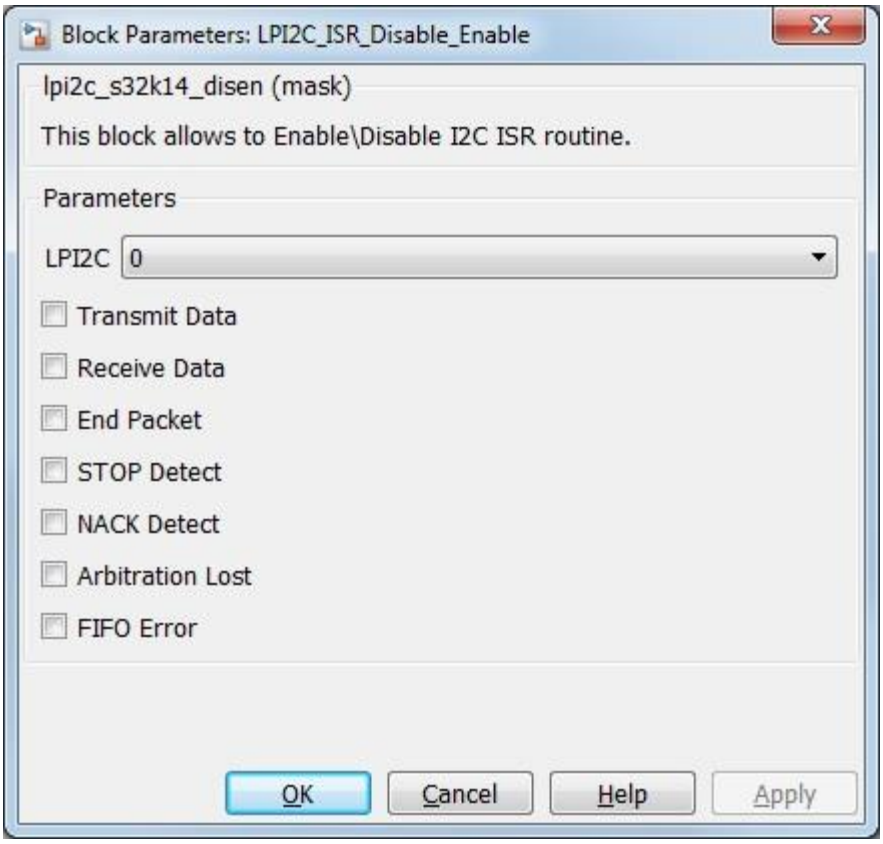
- None

5.3.11.5 Outputs:

- None

5.3.11.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
LPI2C	List-box	0	Select I2C module.
Transmit Data (TDIE)	Check-box	Enable/Disable	
Receive Data (RDIE)	Check-box	Enable/Disable	
End Packet (EPIE)	Check-box	Enable/Disable	
STOP Detect (SDIE)	Check-box	Enable/Disable	
NACK Detect (NDIE)	Check-box	Enable/Disable	
Arbitration Lost (ALIE)	Check-box	Enable/Disable	
FIFO Error (FEIE)	Check-box	Enable/Disable	



5.3.11.7 Block Dependency

Please do the following:

1. Configure respective I2C and its interrupts

5.3.11.8 Block Miscellaneous Details:

None

5.3.12 LPSPI Configuration Block

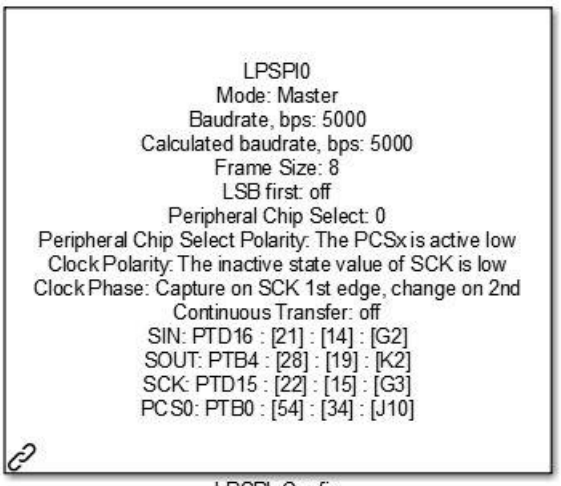
5.3.12.1 Block Name

LPSPI Configuration Block

5.3.12.2 Block Description

This block is used to configure the LPSPI module.

5.3.12.3 Block Image



LPSPI_Config

5.3.12.4 Inputs:

- None

5.3.12.5 Outputs:

- None

5.3.12.6 Block Dialog and Parameters:

The block dialog consists of the following tabs:

- General
- Pins

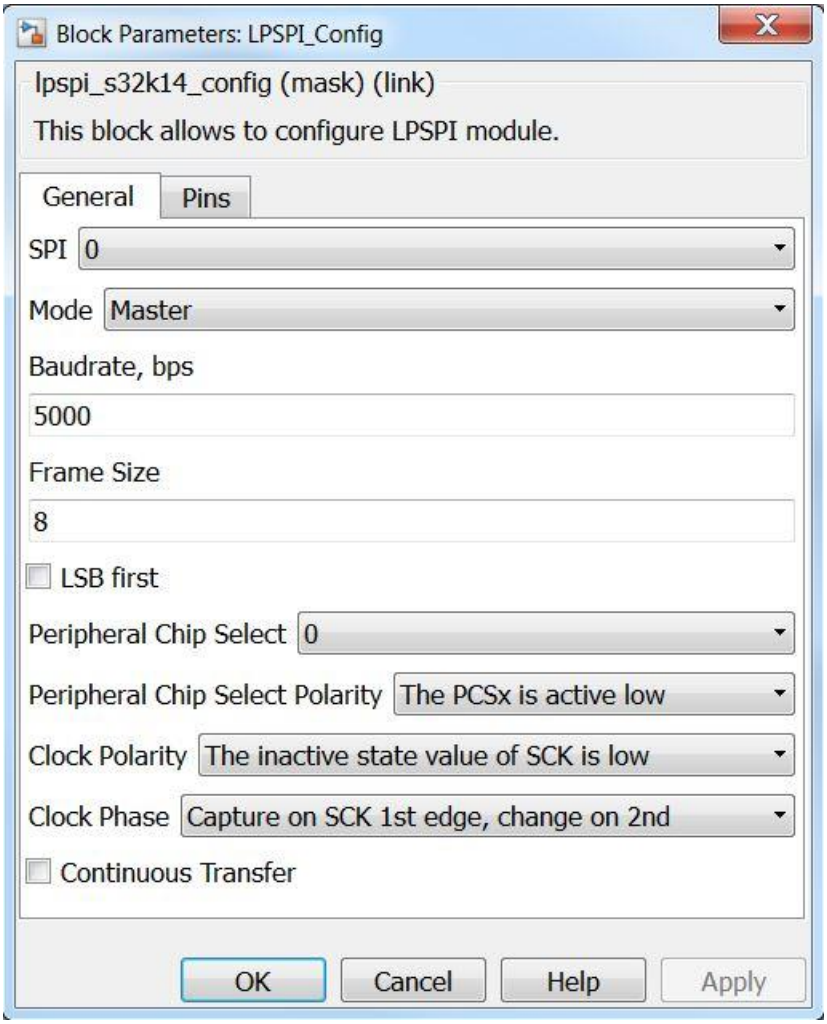
- The General tab contains the following parameters:

Names	Selection Types	Range	Description
SPI Module	List-box	0-2	Select which SPI module to use.
Mode	Pop-up	Slave Master	Mode of operation * Configures the LPSPI in master or slave mode. This bit directly controls the direction of the LPSPI_SCK and LPCPI_PCS pins.
Baudrate, bps	Text-box		Baudrate supported by the slave device, typically up to a few Mbps
Frame Size	Text-box		Configures the frame size in number of bits. The minimum frame size is 8 bits.

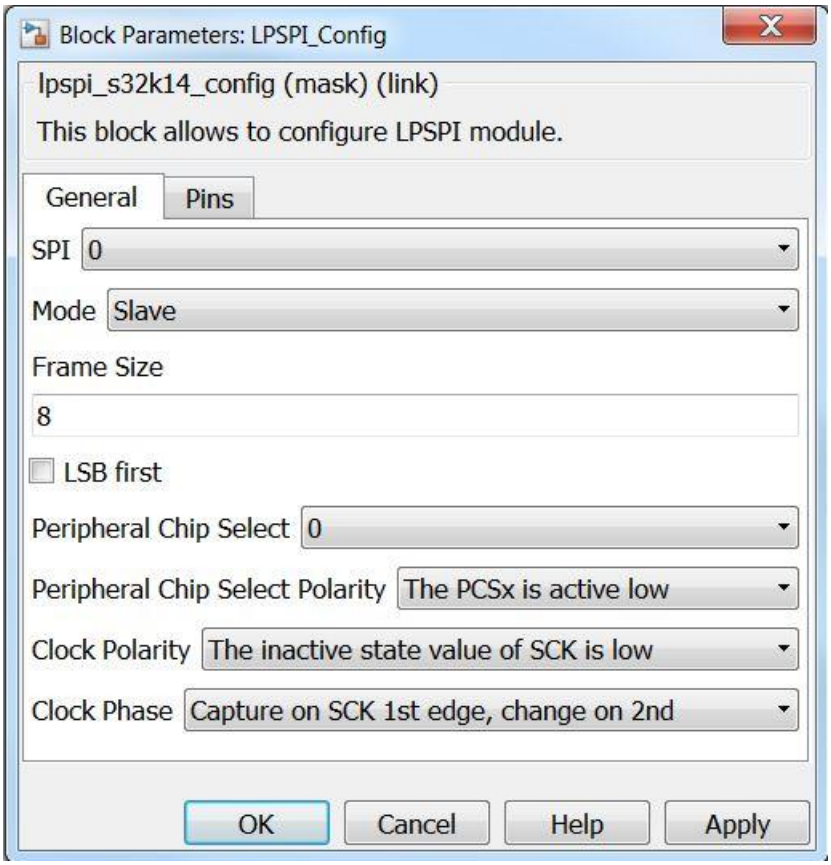
			If the frame size is larger than 32 bits, then the frame is divided into multiple words of 32-bits
LSB First	Check-box	On/Off	Selects LSB or MSB of the frame transferred first.
Peripheral Chip Select	List-box	0-3	Select which Peripheral Chip Select to use.
Peripheral Chip Select Polarity	List-box	The PCSx is active low The PCSx is active hight	This field is only updated between frames.
Clock Polarity	Pop-up	The inactive state of SCK is low. The inactive state of SCK is high.	This field is only updated between frames.
Clock Phase	Pop-up	Capture on SCK 1st edge, change on 2nd Change on SCK 1st edge, capture on 2nd	This field is only updated between frames.
Continuous Transfer	Check-box	disabled/enabled	In master mode, continuous transfer will keep the PCS asserted at the end of the frame size, until a command word is received that starts a new frame. In slave mode, when continuous transfer is enabled the LPSPI will only transmit the first FRAMESZ bits, after which it will transmit received data assuming a 32-bit shift register.

* Read Miscellaneous Details below or Hardware Manual documentation to get more information.

Master View



Slave View

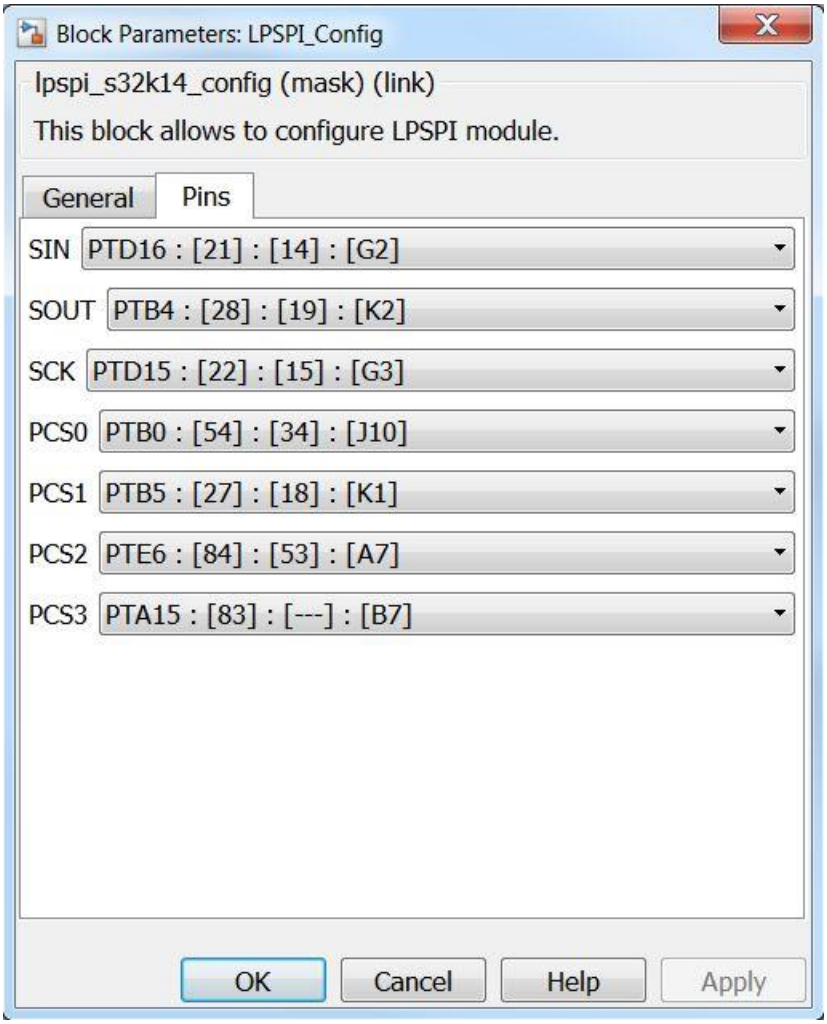


- The Pins tab contains the following parameters:

Names	Selection Types	Range	Description
SIN	Pop-up	The list of available pins depends on the selected SPI Module.	Serial Data Input pin selection. For usability the Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
SOUT	Pop-up	The list of available pins depends on the selected SPI Module.	Serial Data Output pin selection. For usability the Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
SCK	Pop-up	The list of available pins depends on the selected SPI Module.	Serial Clock pin selection, input in slave mode, output in master mode. For usability the Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
PCS0	Pop-up	The list of available pins depends on the selected SPI	Peripheral Chip Select pin selection, input in slave mode, output in master mode.

		Module.	For usability the Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
PCS1	Pop-up	The list of available pins depends on the selected SPI Module.	Peripheral Chip Select 1 pin selection, input in slave mode, output in master mode. For usability the Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
PCS2	Pop-up	The list of available pins depends on the selected SPI Module.	Peripheral Chip Select 2 pin selection, input in slave mode, output in master mode. For usability the Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
PCS3	Pop-up	The list of available pins depends on the selected SPI Module.	Peripheral Chip Select 3 pin selection, input in slave mode, output in master mode. For usability the Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format

* Read Hardware Manual documentation to get more information.



5.3.12.7 Block Dependency

None

5.3.12.8 Block Miscellaneous Details:

None

5.3.13 LPSPI Transmit Block

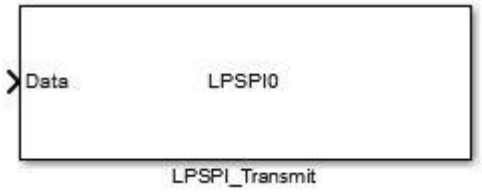
5.3.13.1 Block Name

SPI Transmit Block

5.3.13.2 Block Description

This block transmits data through a SPI module.

5.3.13.3 Block Image



5.3.13.4 Inputs:

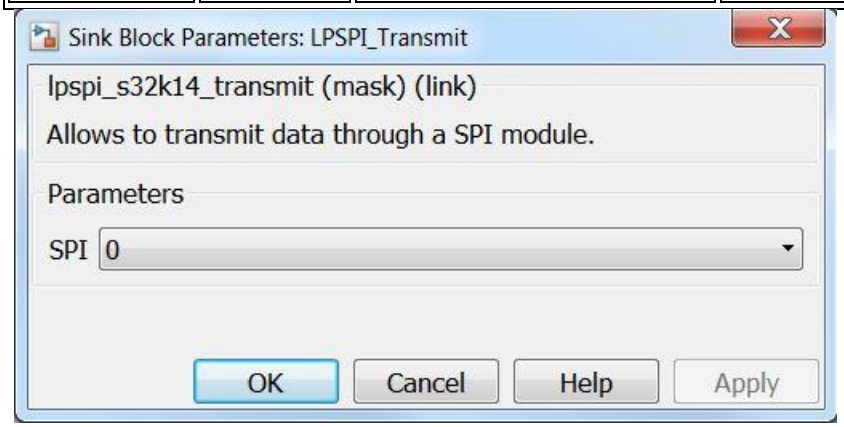
- Data to be transmitted (uint32)

5.3.13.5 Outputs:

- None

5.3.13.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
SPI Module	List-box	0-2	Select which SPI module to use.



5.3.13.7 Block Dependency

Use LPSPI_Config Block to configure LPSPI

5.3.13.8 Block Miscellaneous Details:

None

5.3.14 LPSPI Receive Block

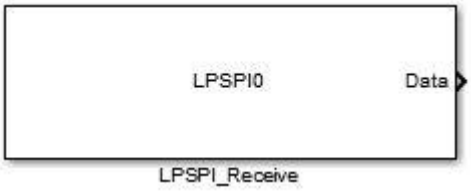
5.3.14.1 Block Name

SPI Receive Block

5.3.14.2 Block Description

The main functionality of the block is reading data from a SPI module.

5.3.14.3 Block Image



5.3.14.4 Inputs:

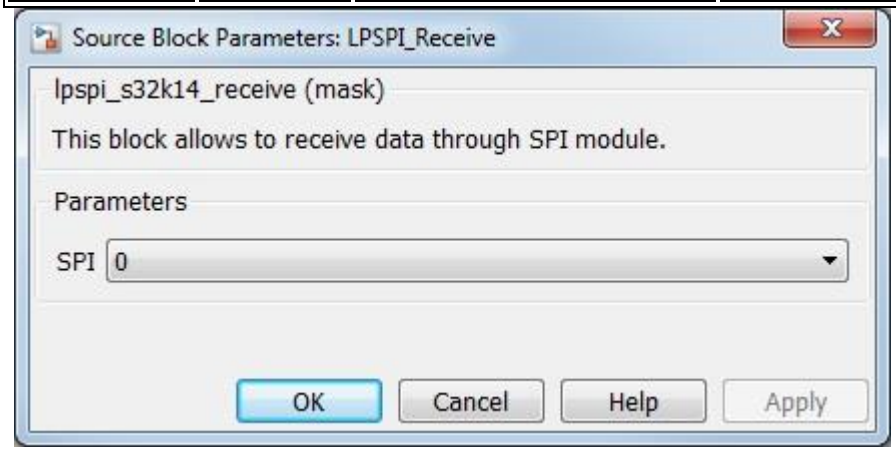
- None

5.3.14.5 Outputs:

- Data (uint32)

5.3.14.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
SPI Module	List-box	0-2	Select which SPI module to use.



5.3.14.7 Block Dependency

Use LPSPI_Config Block to configure LPSPI

5.3.14.8 Block Miscellaneous Details:

None

5.3.14.9

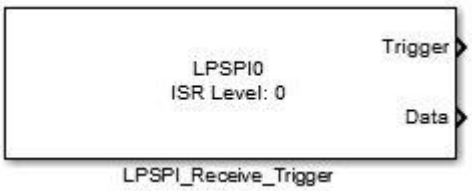
5.3.14.10 Block Name

SPI Receive Trigger Block

5.3.14.11 Block Description

The main functionality of the block is to read data when it is available in the SPI module.

5.3.14.12 Block Image



5.3.14.13 Inputs:

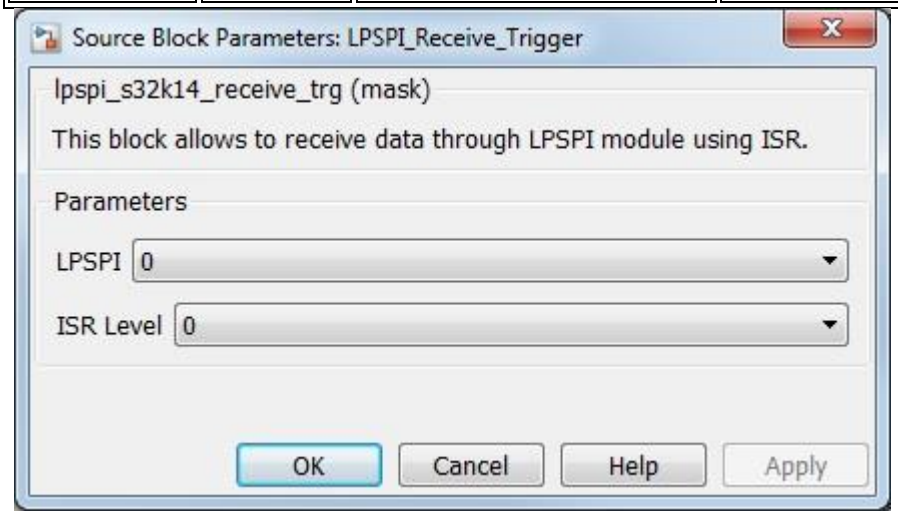
- None

5.3.14.14 Outputs:

- Function-call
- Data (uint32)

5.3.14.15 Block Dialog and Parameters:

Names	Selection Types	Range	Description
SPI Module	List-box	0-2	Select which SPI module to use.
ISR Priority	List-box	0 – 15	ISR priority



5.3.14.16 Block Dependency

Use LPSPI_Config Block to configure LPSPI

5.3.14.17 Block Miscellaneous Details:

None

5.3.15 LPSPI ISR Block

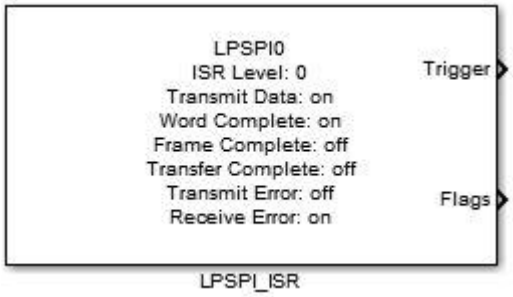
5.3.15.1 Block Name

LPSPI ISR Block

5.3.15.2 Block Description

The main functionality of the block is to process LPSPI ISRs.

5.3.15.3 Block Image



5.3.15.4 Inputs:

- None

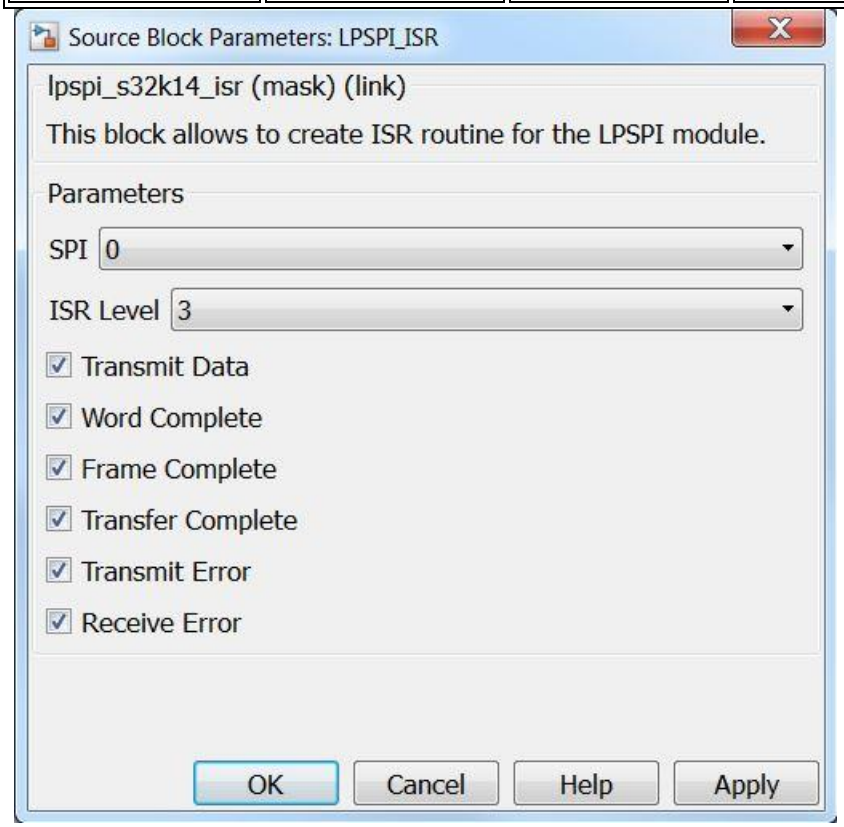
5.3.15.5 Outputs:

- Function-Call
- Status Register (LPSPIx_SR) value (uint32)

5.3.15.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
LPSPI	List-box	0 – 2	Select LPSPI module.
ISR Level	List-box	0 – 15	Interrupt priority level
Transmit Data	Check-box	Enable/Disable	The Transmit Data Flag is set whenever the number of words in the transmit FIFO is equal or less than TXWATER.
Word Complete	Check-box	Enable/Disable	This flag will set when the last bit of a received

			word is sampled.
Frame Complete	Check-box	Enable/Disable	This flag will set at the end of each frame transfer, when the PCS negates.
Transfer Complete	Check-box	Enable/Disable	This flag will set in master mode when the LPSPI returns to idle state with the transmit FIFO empty.
Transmit Error	Check-box	Enable/Disable	This flag will set when the Transmit FIFO underruns.
Receive Error	Check-box	Enable/Disable	This flag will set when the Receiver FIFO overflows.



5.3.15.7 Block Dependency

Use LPSPI_Config Block to configure LPSPI

5.3.15.8 Block Miscellaneous Details:

LPSPI Status Register (SR) bit field description:

Field	Function
—	
24 MBF	Module Busy Flag 0b - LPSPI is idle. 1b - LPSPI is busy.
23-14 —	Reserved
13 DMF	Data Match Flag Indicates that the received data has matched the MATCH0 and/or MATCH1 fields as configured by MATCFG. 0b - Have not received matching data. 1b - Have received matching data.
12 REF	Receive Error Flag This flag will set when the Receiver FIFO overflows. When this flag is set, it is recommended to first end the transfer, empty the Receive FIFO, clear this flag and then restart the transfer from the beginning. 0b - Receive FIFO has not overflowed. 1b - Receive FIFO has overflowed.
11 TEF	Transmit Error Flag This flag will set when the Transmit FIFO underruns. When this flag is set, it is recommended to first end the transfer, clear this flag and then restart the transfer from the beginning. 0b - Transmit FIFO underrun has not occurred. 1b - Transmit FIFO underrun has occurred
10 TCF	Transfer Complete Flag This flag will set in master mode when the LPSPI returns to idle state with the transmit FIFO empty. 0b - All transfers have not completed. 1b - All transfers have completed.
9 FCF	Frame Complete Flag This flag will set at the end of each frame transfer, when the PCS negates. 0b - Frame transfer has not completed. 1b - Frame transfer has completed.
8 WCF	Word Complete Flag This flag will set when the last bit of a received word is sampled. 0b - Transfer word not completed. 1b - Transfer word completed.
7-2 —	Reserved
1 RDF	Receive Data Flag The Receive Data Flag is set whenever the number of words in the receive FIFO is greater than RXWATER. 0b - Receive Data is not ready. 1b - Receive data is ready.
0 TDF	Transmit Data Flag The Transmit Data Flag is set whenever the number of words in the transmit FIFO is equal or less than TXWATER. 0b - Transmit data not requested. 1b - Transmit data is requested.

5.3.16 LPSPI Receive Trigger Block

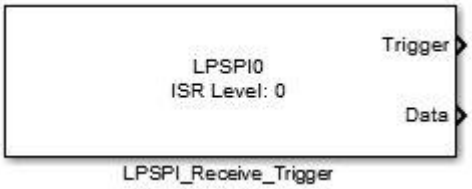
5.3.16.1 Block Name

SPI Receive Trigger Block

5.3.16.2 Block Description

The main functionality of the block is to read data when it is available in the SPI module.

5.3.16.3 Block Image



5.3.16.4 Inputs:

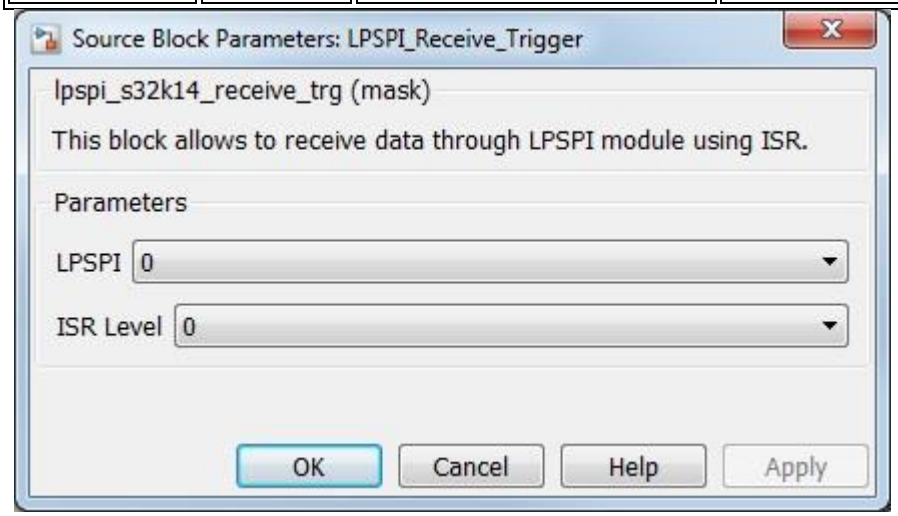
- None

5.3.16.5 Outputs:

- Function-call
- Data (uint32)

5.3.16.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
SPI Module	List-box	0-2	Select which SPI module to use.
ISR Priority	List-box	0 – 15	ISR priority



5.3.16.7 Block Dependency

Use LPSPI_Config Block to configure LPSPI

5.3.16.8 Block Miscellaneous Details:

None

5.3.17 LPSPI ISR Enable/Disable Block

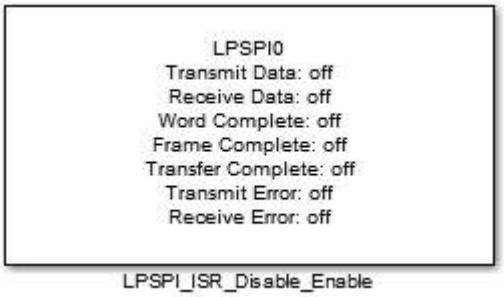
5.3.17.1 Block Name

LPSPI Interrupt Enable/Disable Block

5.3.17.2 Block Description

The main functionality of the block is to enable/disable LPSPI interrupts

5.3.17.3 Block Image



5.3.17.4 Inputs:

- None

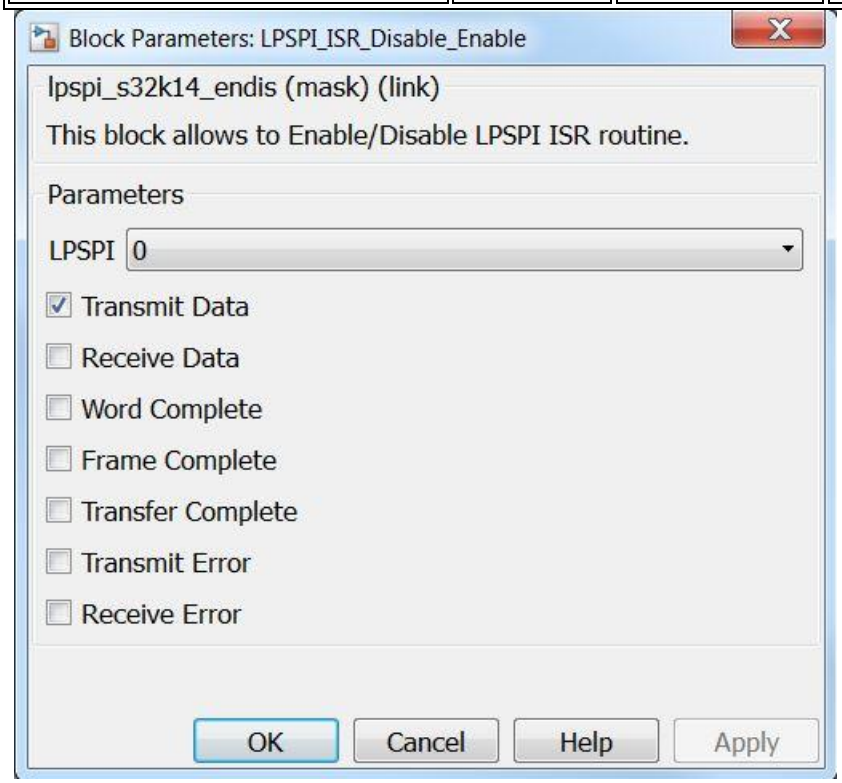
5.3.17.5 Outputs:

- None

5.3.17.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
LPSPI	List-box	0 – 2	Select LPSPI module.
Transmit Data	Check-box	Enable/Disable	The Transmit Data Flag is set whenever the number of words in the transmit FIFO is equal or less than TXWATER.
Receive Data	Check-box	Enable/Disable	The Receive Data Flag is set

			whenever the number of words in the receive FIFO is greater than RXWATER.
Word Complete	Check-box	Enable/Disable	This flag will set when the last bit of a received word is sampled.
Frame Complete	Check-box	Enable/Disable	This flag will set at the end of each frame transfer, when the PCS negates.
Transfer Complete	Check-box	Enable/Disable	This flag will set in master mode when the LPSPI returns to idle state with the transmit FIFO empty.
Transmit Error	Check-box	Enable/Disable	This flag will set when the Transmit FIFO underruns.
Receive Error	Check-box	Enable/Disable	This flag will set when the Receiver FIFO overflows.



5.3.17.7 Block Dependency

Please do the following:

1. Use LPSPI_Config Block to configure LPSPI
2. Use LPSPI_ISR Block to configure LPSPI ISR

5.3.17.8 Block Miscellaneous Details:

None

5.3.18 LPUART Configuration Block

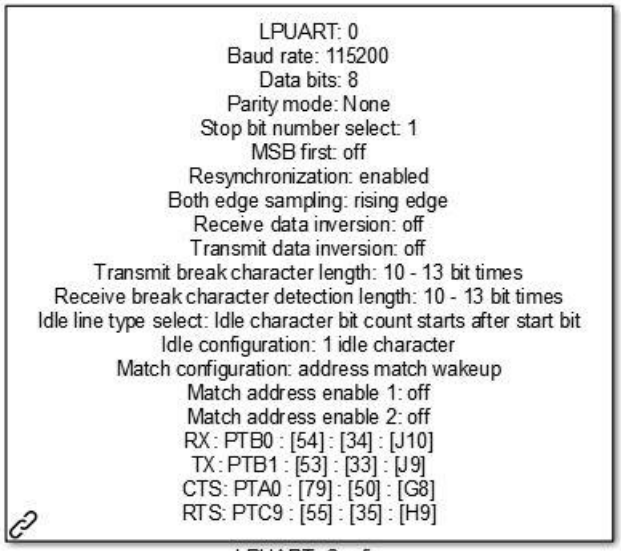
5.3.18.1 Block Name

Low Power Universal Asynchronous Receiver/Transmitter Configuration Block

5.3.18.2 Block Description

The main functionality of the block is to configure LPUART module.

5.3.18.3 Block Image



LPUART_Config

5.3.18.4 Inputs:

- None

5.3.18.5 Outputs:

- None

5.3.18.6 Block Dialog and Parameters:

The block dialog consists of the following tabs:

- General Settings
- Break and Idle Configuration
- Match Configuration

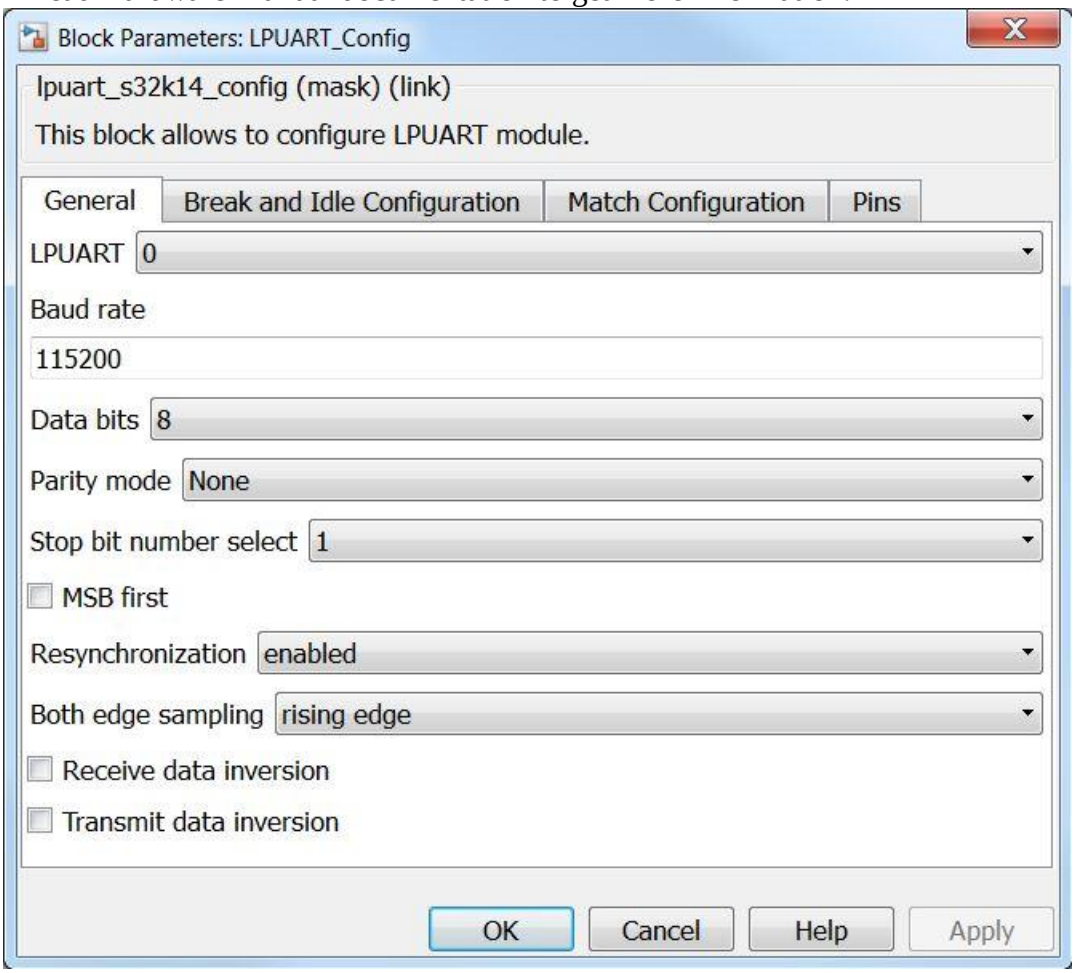
- Pins

  - The General Settings tab contains the following parameters:

Names	Selection Types	Range	Description
LPUART Module	List-box	0-2	Select which LPUART module to use.
Baud rate	Text-box		
Data bits	Pop-up	8 9 10	Select the number of data bits to use
Parity mode	Pop-up	None Even Odd	Odd parity means the total number of 1s in the data character, including the parity bit, is odd. Even parity means the total number of 1s in the data character, including the parity bit, is even.
Stop bit number select	Pop-up	1 2	SBNS determines whether data characters are one or two stop bits.
MSB first	Check-box	Enable/Disable	Setting this bit reverses the order of the bits that are transmitted and received on the wire. This bit does not affect the polarity of the bits, the location of the parity bit or the location of the start or stop bits.
Resynchronization	Pop-up	enabled disabled	When set, disables the resynchronization of the received data word when a data one followed by data zero transition is detected. enabled - Resynchronization during received data word is supported disabled - Resynchronization during received data word is disabled
Both edge sampling	Pop-up	rising edge rising and falling edges	Enables sampling of the received data on both edges of the baud rate clock, effectively doubling the number of times the receiver samples the input data for a given oversampling ratio. rising edge - Receiver samples input data using the rising edge of the

			baud rate clock rising and falling edges - Receiver samples input data using the rising and falling edge of the baud rate clock
Receive data inversion	Check-box	Enable/Disable	Setting this bit reverses the polarity of the received data input.
Transmit data inversion	Check-box	Enable/Disable	Setting this bit reverses the polarity of the transmitted data output.

* Read Hardware Manual documentation to get more information.

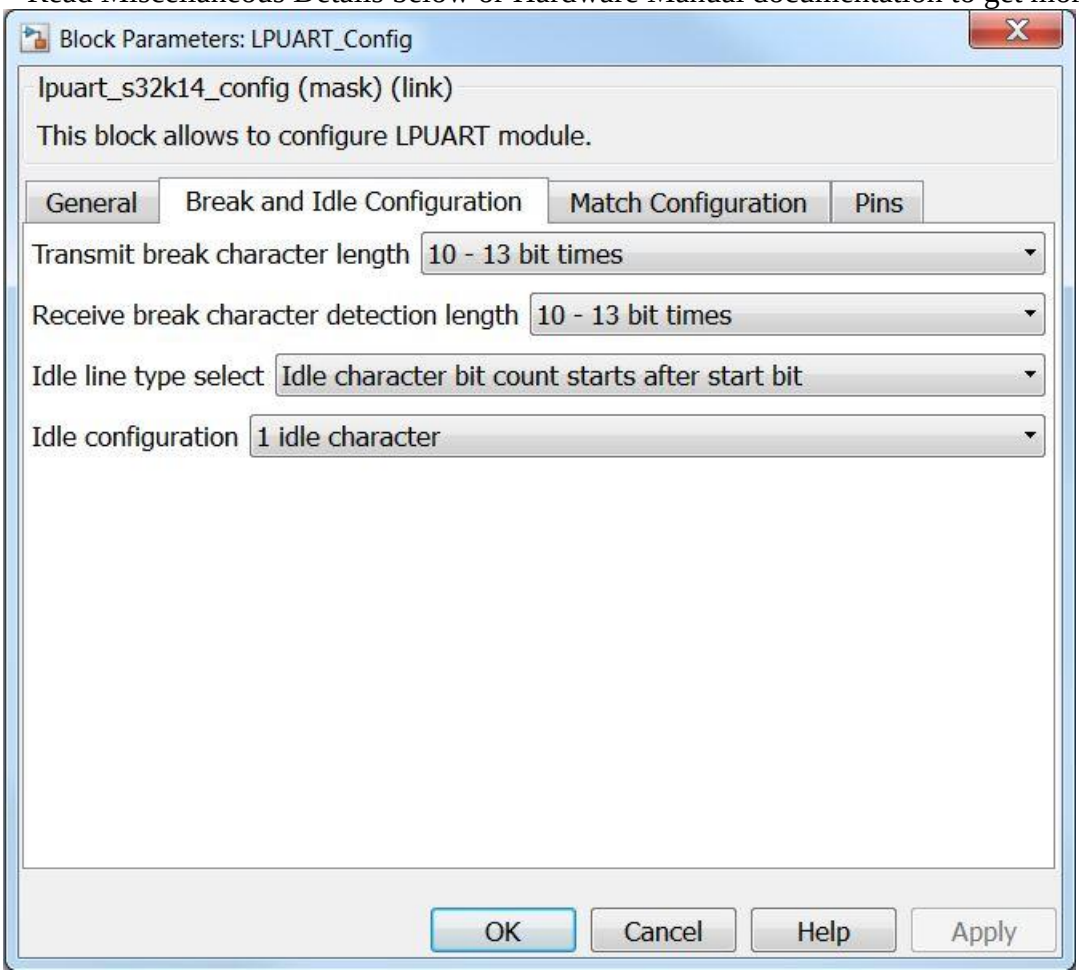


- The Break and Idle Configuration tab contains the following parameters :

Names	Selection Types	Range	Description
Transmit break character length	Pop-up	10 - 13 bit times 13 - 16 bit times	Selects a longer transmitted break

			character length. Detection of a framing error is not affected by the state of this selection. 1. Break character is transmitted with length of 10 to 13 bit times. 2. Break character is transmitted with length of 13 to 16 bit times.
Receive break character detection length	Pop-up	10 - 13 bit times 13 - 16 bit times	Selects a longer break character detection length. While 13-16 bit times option is set, receive data is not stored in the receive data buffer.*
Idle line type select	Pop-up	Idle character bit count starts after start bit Idle character bit count starts after stop bit	Determines when the receiver starts counting logic 1s as idle character bits. The count begins either after a valid start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit can cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions.
Idle configuration	Pop-up	1 idle character 2 idle characters 4 idle characters 8 idle characters 16 idle characters 32 idle characters 64 idle characters 128 idle characters	Configures the number of idle characters that must be received before the IDLE flag is set.

* Read Miscellaneous Details below or Hardware Manual documentation to get more information.

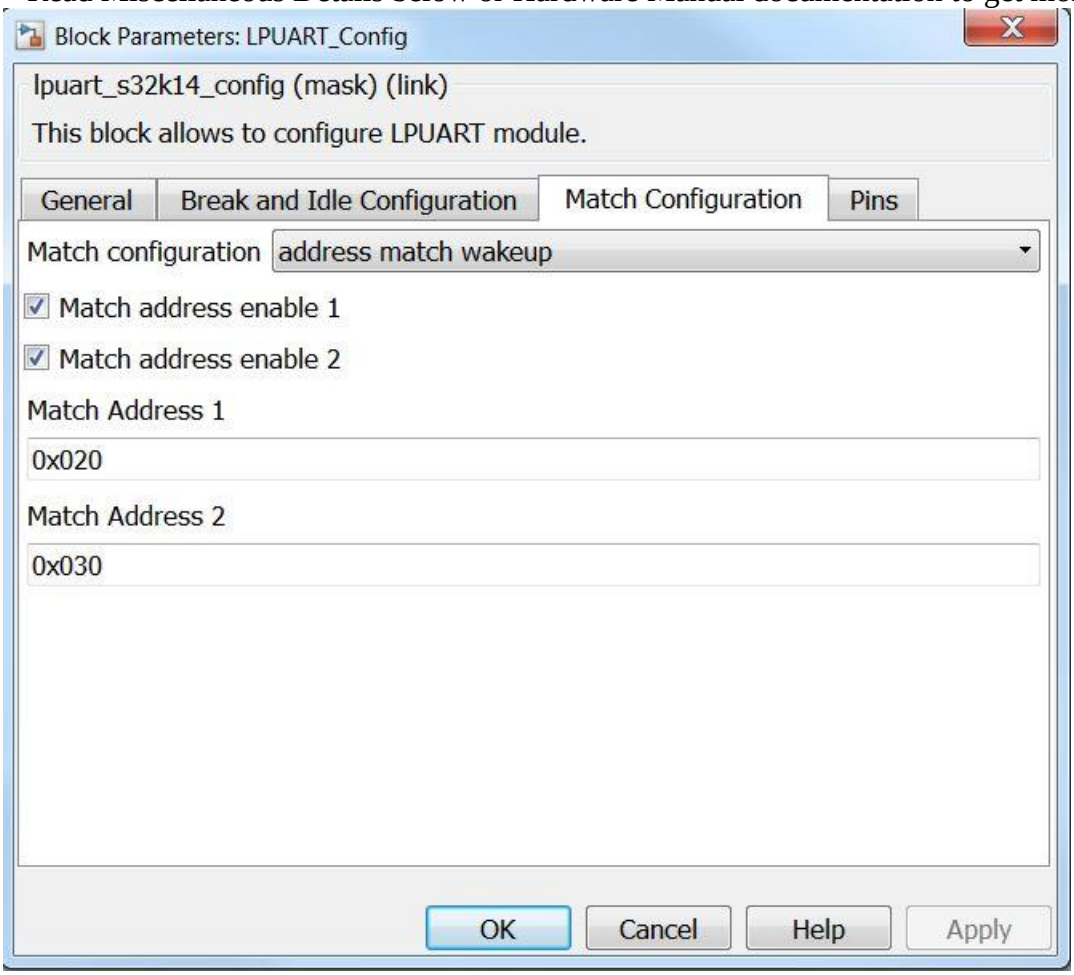


- The Match Configuration tab contains the following parameters:

Names	Selection Types	Range	Description
Match configuration	Pop-up	0-3	Configures the match addressing mode used. 0 - address match wakeup 1 - idle match wakeup 2 - match on and match off 3 - enables RWU on data match on/off for transmitter CTS input
Match address enable 1	Check-box	Enable/Disable	Disabled - Normal operation Enabled - Enables automatic address matching or data matching mode for MATCH[MA1]
Match address enable 2	Check-box	Enable/Disable	Disabled - Normal operation

			Enabled - Enables automatic address matching or data matching mode for MATCH[MA2]
Match address 1	Text-box	0-255	If a match occurs, the following data is transferred to the data register. If a match fails, the following data is discarded.
Match address 2	Text-box	0-255	If a match occurs, the following data is transferred to the data register. If a match fails, the following data is discarded. de adaugat si data selection

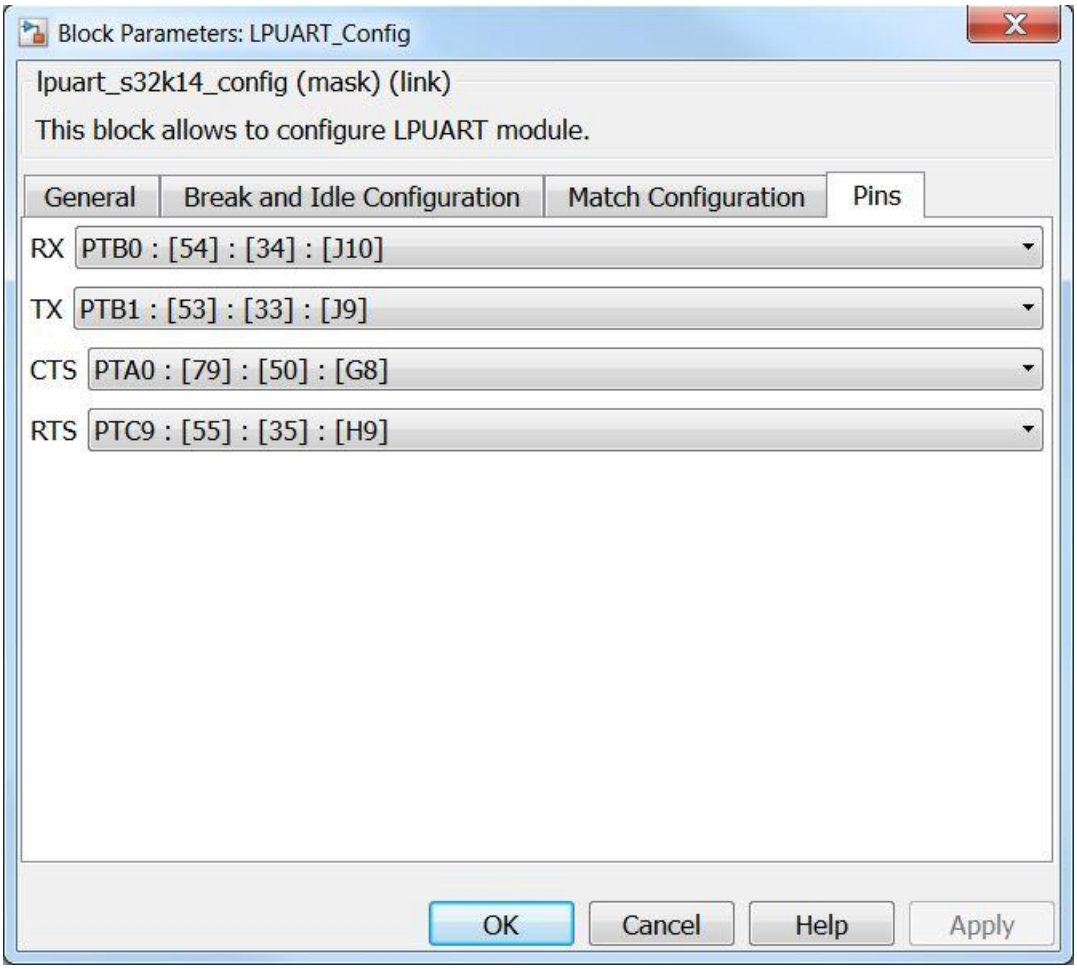
* Read Miscellaneous Details below or Hardware Manual documentation to get more information.



- The Pins tab contains the following parameters:

Names	Selection Types	Range	Description
RX	Pop-up	The list of available pins depends on the	RX pin selection.

		selected LPUART Module.	For usability the Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
TX	Pop-up	The list of available pins depends on the selected LPUART Module.	TX pin selection. For usability the Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
CTS	Pop-up	The list of available pins depends on the selected LPUART Module.	CTS pin selection. For usability the Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
RTS	Pop-up	The list of available pins depends on the selected LPUART Module.	RTS pin selection. For usability the Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format



5.3.18.7 Block Dependency

None

5.3.18.8 Block Miscellaneous Details:

None

5.3.19 LPUART Transmit Block

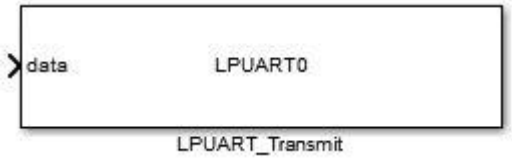
5.3.19.1 Block Name

LPUART Transmit Block

5.3.19.2 Block Description

The main functionality of the block is transmitting data through a LPUART module.

5.3.19.3 Block Image



5.3.19.4 Inputs:

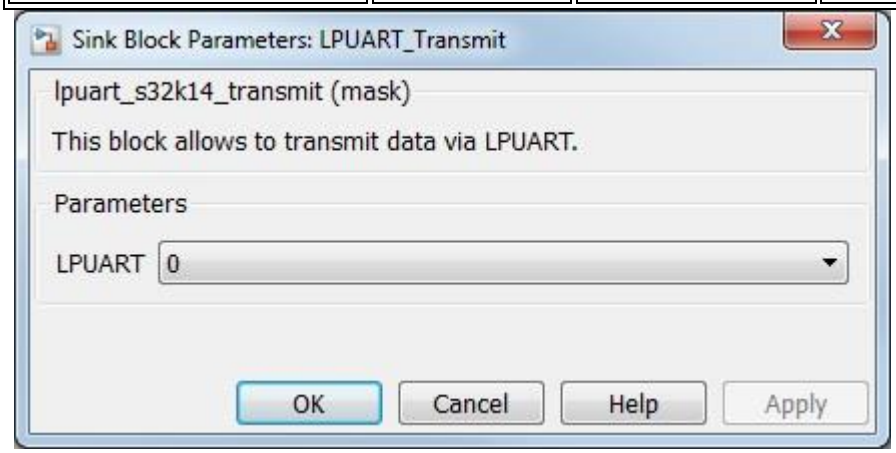
- None

5.3.19.5 Outputs:

- Data (uint16)

5.3.19.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
LPUART Module	List-box	0-2	Select which LPUART module to use.



5.3.19.7 Block Dependency

Use LPUART_Config Block to configure LPUART

5.3.19.8 Block Miscellaneous Details:

None

5.3.20 LPUART Receive Block

5.3.20.1 Block Name

LPUART Receive Block

5.3.20.2 Block Description

The main functionality of the block is reading data from a LPUART module.

5.3.20.3 Block Image

5.3.20.4 Inputs:

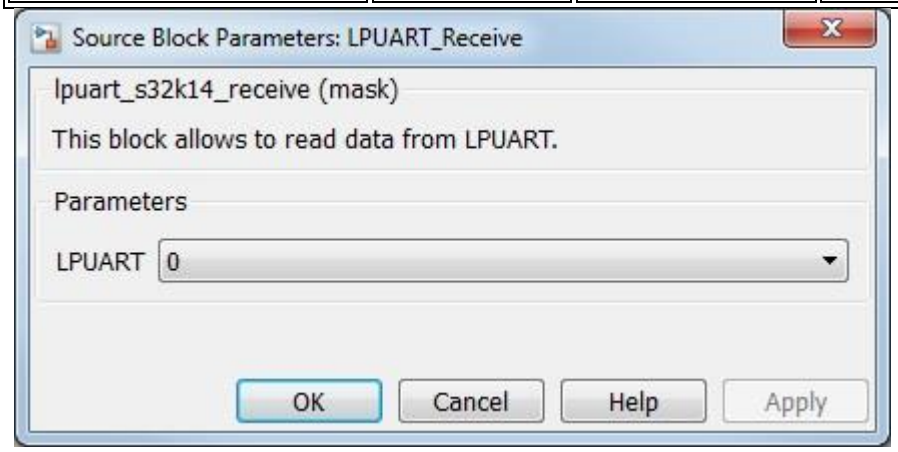
- None

5.3.20.5 Outputs:

- Data (uint16)

5.3.20.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
LPUART Module	List-box	0-2	Select which LPUART module to use.



5.3.20.7 Block Dependency

Use LPUART_Config Block to configure LPUART

5.3.20.8 Block Miscellaneous Details:

None

5.3.21 LPUART Receive/Transmit ISR Block

5.3.21.1 Block Name

LPUART Receive/Transmit Interrupt Enable/Disable Block

5.3.21.2 Block Description

The main functionality of the block is to enable/disable LPUART Receive/Transmit interrupts

5.3.21.3 Block Image

5.3.21.4 Inputs:

- None

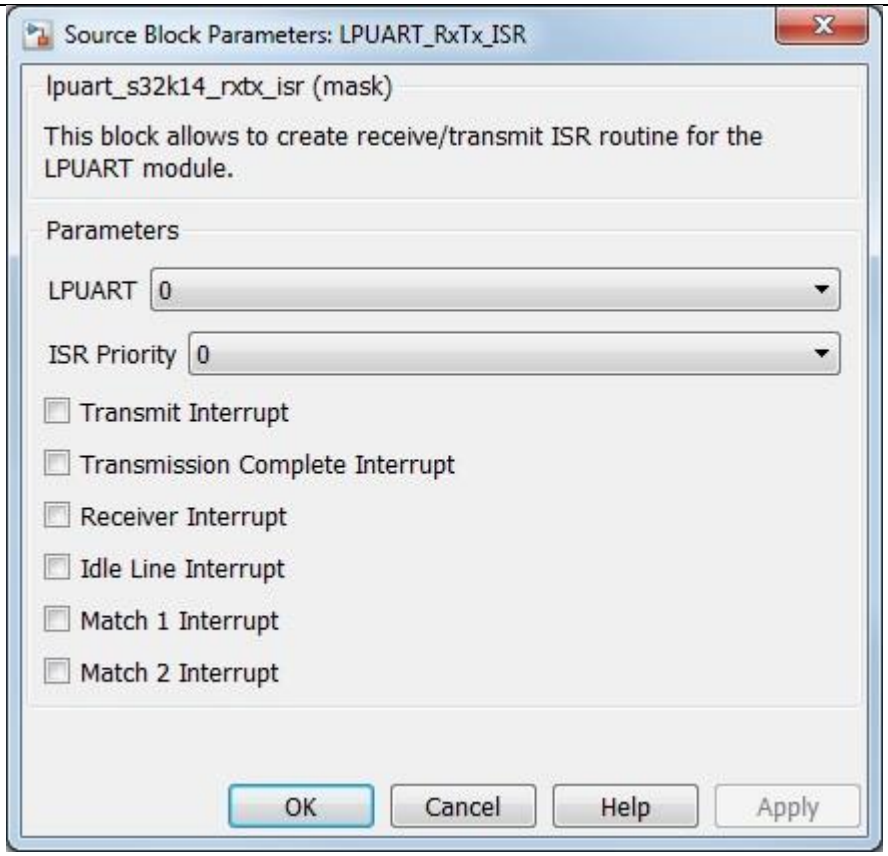
5.3.21.5 Outputs:

- Function-Call
- Status Register (LPUARTx_STAT) value (uint32)

5.3.21.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
LPUART Module	List-box	0-2	Select which LPUART module to use.
ISR Level	List-box	0 – 15	Interrupt priority level
Transmit Interrupt	Check-box	Enable/Disable	TDRE will set when the transmit data register (LPUART_DATA) is empty.
Transmission Complete Interrupt	Check-box	Enable/Disable	TC is cleared when there is a transmission in progress or when a preamble or break character is loaded. TC is set when the transmit buffer is empty and no data, preamble, or break character is being transmitted. When TC is set, the transmit data output signal becomes idle (logic 1).
Receiver Interrupt	Check-box	Enable/Disable	RAF is set when the receiver detects the beginning of a valid start bit, and RAF is cleared automatically when the receiver detects an idle line.
Idle Line Interrupt	Check-box	Enable/Disable	IDLE is set when the LPUART receive line becomes

			idle for a full character time after a period of activity. When ILT is cleared, the receiver starts counting idle bit times after the start bit. If the receive character is all 1s, these bit times and the stop bits time count toward the full character time of logic high, 10 to 13 bit times, needed for the receiver to detect an idle line. When ILT is set, the receiver doesn't start counting idle bit times until after the stop bits. The stop bits and any logic high bit times at the end of the previous character do not count toward the full character time of logic high needed for the receiver to detect an idle line.
Match 1 Interrupt	Check-box	Enable/Disable	MA1F is set whenever the next character to be read from LPUART_DATA matches MA1.
Match 2 Interrupt	Check-box	Enable/Disable	MA2F is set whenever the next character to be read from LPUART_DATA matches MA2.



5.3.21.7 Block Dependency

Use LPUART_Config Block to configure LPUART

5.3.21.8 Block Miscellaneous Details:

None

5.3.22 LPUART Error ISR Block

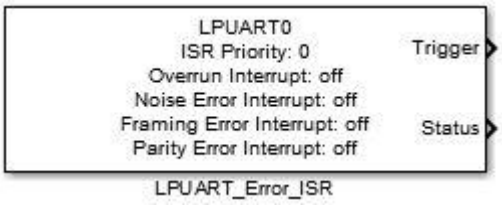
5.3.22.1 Block Name

LPUART Error Interrupt Enable/Disable Block

5.3.22.2 Block Description

The main functionality of the block is to enable/disable LPUART error interrupts

5.3.22.3 Block Image



5.3.22.4 Inputs:

- None

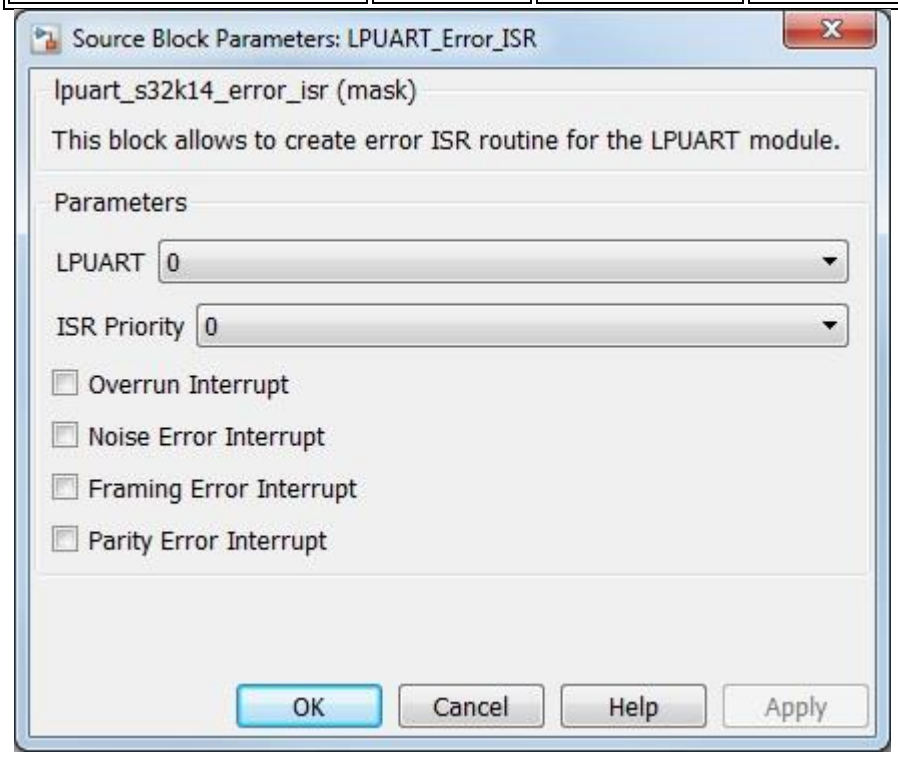
5.3.22.5 Outputs:

- Function-Call
- Status Register (LPUARTx_STAT) value (uint32)

5.3.22.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
LPUART Module	List-box	0-2	Select which LPUART module to use.
ISR Level	List-box	0 – 15	Interrupt priority level
Overrun Interrupt	Check-box	Enable/Disable	OR is set when software fails to prevent the receive data register from overflowing with data. The OR bit is set immediately after the stop bit has been completely received for the dataword that overflows the buffer and all the other error flags (FE, NF, and PF) are prevented from setting. The data in the shift register is lost, but the data already in the LPUART data registers is not affected. If LBKDE is enabled and a LIN Break is detected, the OR field asserts if LBKDIF is not cleared before the next

			data character is received.
Noise Error Interrupt	Check-box	Enable/Disable	The advanced sampling technique used in the receiver takes three samples in each of the received bits. If any of these samples disagrees with the rest of the samples within any bit time in the frame then noise is detected for that character. NF is set whenever the next character to be read from LPUART_DATA was received with noise detected within the character.
Framing Error Interrupt	Check-box	Enable/Disable	FE is set whenever the next character to be read from LPUART_DATA was received with logic 0 detected where a stop bit was expected.
Parity Error Interrupt	Check-box	Enable/Disable	PF is set whenever the next character to be read from LPUART_DATA was received when parity is enabled (PE = 1) and the parity bit in the received character does not agree with the expected parity value.



5.3.22.7 Block Dependency

Use LPUART_Config Block to configure LPUART

5.3.22.8 Block Miscellaneous Details:

None

5.3.23 LPUART ISR Enable/Disable Block

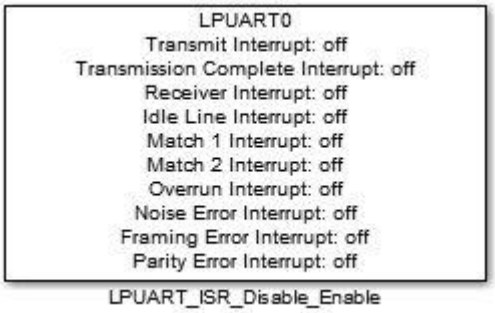
5.3.23.1 Block Name

LPUART Interrupt Enable/Disable Block

5.3.23.2 Block Description

The main functionality of the block is to enable/disable LPUART interrupts

5.3.23.3 Block Image



5.3.23.4 Inputs:

- None

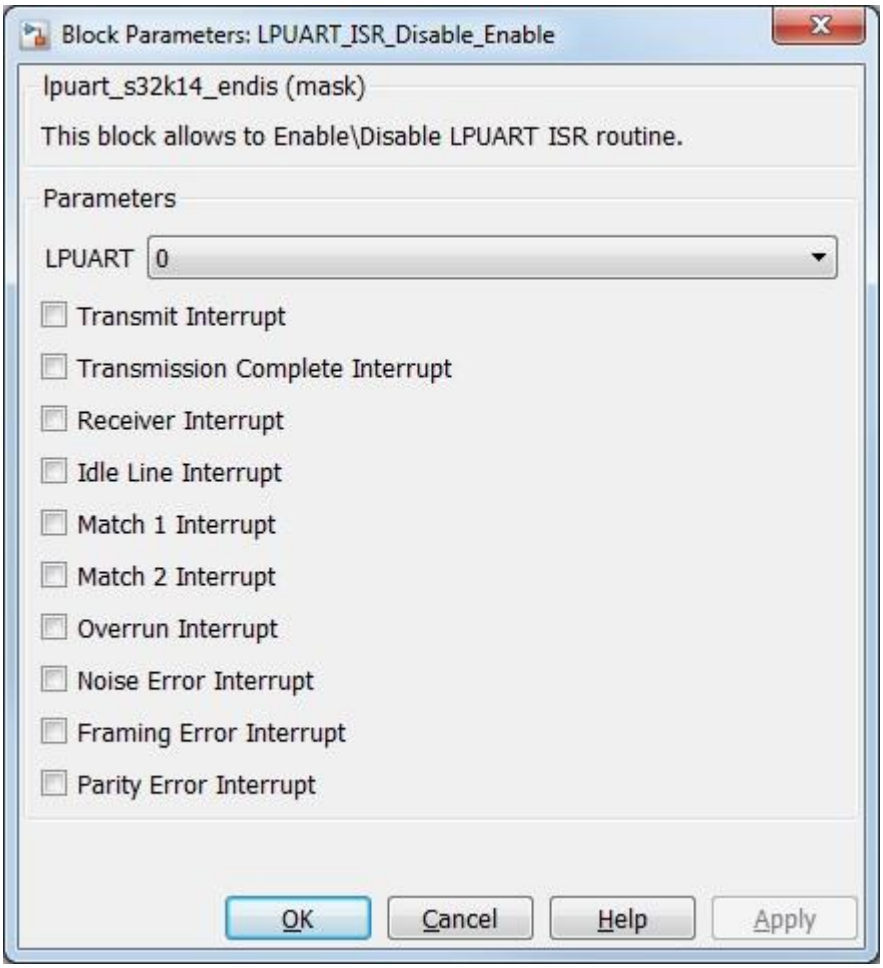
5.3.23.5 Outputs:

- None

5.3.23.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
LPUART Module	List-box	0-2	Select which LPUART module to use.
Transmit Interrupt	Check-box	Enable/Disable	TDRE will set when the transmit data register (LPUART_DATA) is empty.
Transmission Complete Interrupt	Check-box	Enable/Disable	TC is cleared when there is a transmission in progress or when a preamble or break character is loaded. TC is set when the transmit buffer is empty and no data, preamble, or break character is being transmitted. When TC is set, the transmit data output signal becomes idle (logic 1).
Receiver Interrupt	Check-	Enable/Disable	RAF is set when the receiver detects the beginning of

	box		a valid start bit, and RAF is cleared automatically when the receiver detects an idle line.
Idle Line Interrupt	Check-box	Enable/Disable	IDLE is set when the LPUART receive line becomes idle for a full character time after a period of activity. When ILT is cleared, the receiver starts counting idle bit times after the start bit. If the receive character is all 1s, these bit times and the stop bits time count toward the full character time of logic high, 10 to 13 bit times, needed for the receiver to detect an idle line. When ILT is set, the receiver doesn't start counting idle bit times until after the stop bits. The stop bits and any logic high bit times at the end of the previous character do not count toward the full character time of logic high needed for the receiver to detect an idle line.
Match 1 Interrupt	Check-box	Enable/Disable	MA1F is set whenever the next character to be read from LPUART_DATA matches MA1.
Match 2 Interrupt	Check-box	Enable/Disable	MA2F is set whenever the next character to be read from LPUART_DATA matches MA2.
Overrun Interrupt	Check-box	Enable/Disable	OR is set when software fails to prevent the receive data register from overflowing with data. The OR bit is set immediately after the stop bit has been completely received for the dataword that overflows the buffer and all the other error flags (FE, NF, and PF) are prevented from setting. The data in the shift register is lost, but the data already in the LPUART data registers is not affected. If LBKDE is enabled and a LIN Break is detected, the OR field asserts if LBKDIF is not cleared before the next data character is received.
Noise Error Interrupt	Check-box	Enable/Disable	The advanced sampling technique used in the receiver takes three samples in each of the received bits. If any of these samples disagrees with the rest of the samples within any bit time in the frame then noise is detected for that character. NF is set whenever the next character to be read from LPUART_DATA was received with noise detected within the character.
Framing Error Interrupt	Check-box	Enable/Disable	FE is set whenever the next character to be read from LPUART_DATA was received with logic 0 detected where a stop bit was expected.
Parity Error Interrupt	Check-box	Enable/Disable	PF is set whenever the next character to be read from LPUART_DATA was received when parity is enabled (PE = 1) and the parity bit in the received character does not agree with the expected parity value.



5.3.23.7 Block Dependency

Use LPUART_Config Block to configure LPUART

5.3.23.8 Block Miscellaneous Details:

None

5.4 Peripheral Interface Blocks

5.4.1 GPIO Digital Input Block

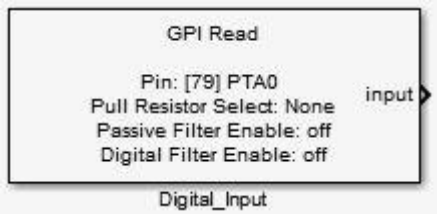
5.4.1.1 Block Name

Digital Input Block

5.4.1.2 Block Description

The main functionality of the block is to configure a single pin as a General Purpose Input.

5.4.1.3 Block Image



5.4.1.4 Inputs:

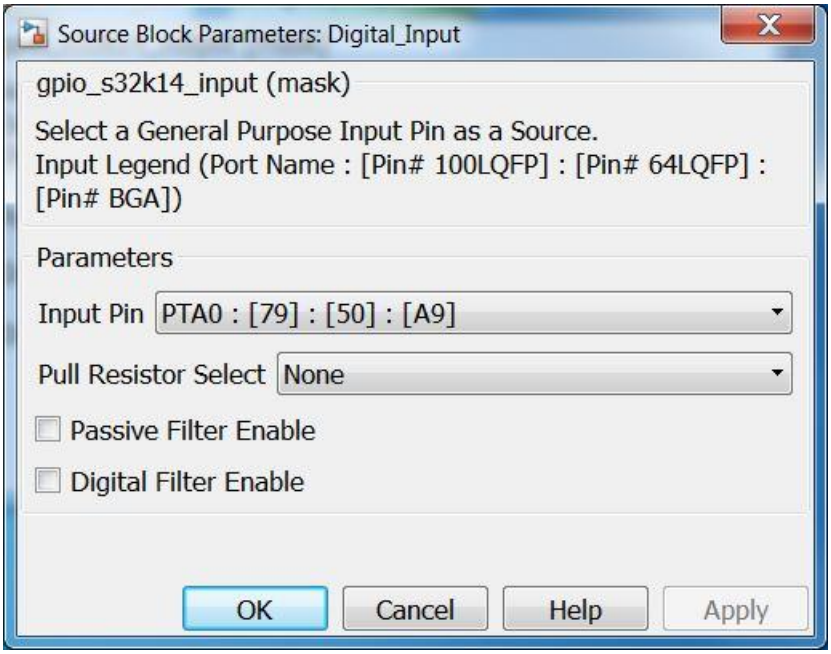
- None

5.4.1.5 Outputs:

- Input signal level (boolean)

5.4.1.6 Block Dialog Parameters:

Names	Selection Types	Range	Description
Input Pin	List-box	Various GPIO pins	Input Pin Selection. For usability the Input Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
Pull Resistor Select	List-box	None Pulldown Pullup	Internal pullup or pulldown resistor is enabled on the Selected pin.
Passive Filter Enable	Check-box	Enable/Disable	Passive input filter is enabled on the corresponding pin. Refer to the device data sheet for filter characteristics.
Digital Filter Enable	Check-box	Enable/Disable	Digital input filter is enabled on the corresponding pin. Refer to the device data sheet for filter characteristics.



5.4.1.7 Block Dependency

None

5.4.1.8 Block Miscellaneous Details:

None

5.4.2 GPIO Digital Output Block

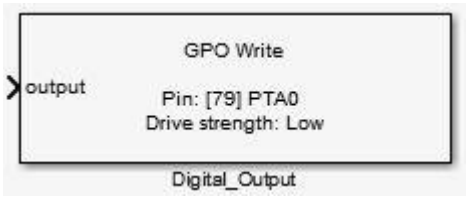
5.4.2.1 Block Name

Digital Output Block

5.4.2.2 Block Description

The main functionality of the block is to configure a single pin as a General Purpose output.

5.4.2.3 Block Image



5.4.2.4 Inputs:

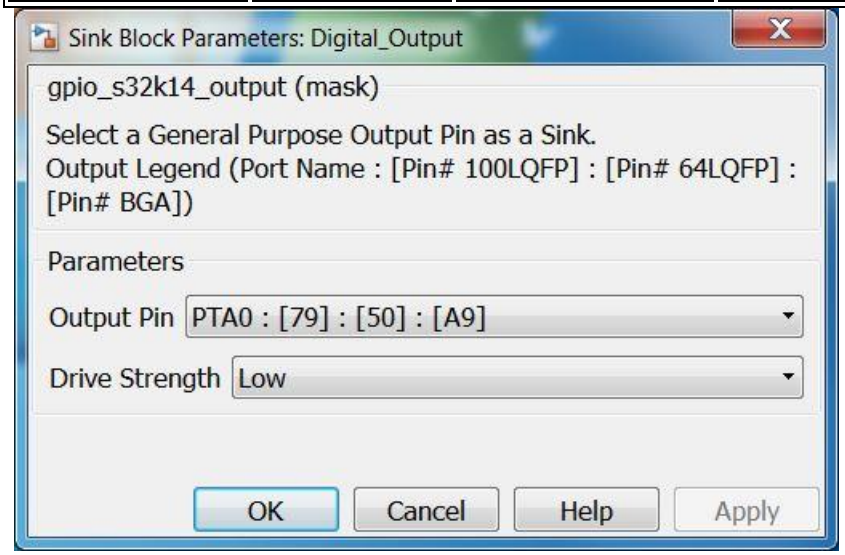
- Output signal level (boolean)

5.4.2.5 Outputs:

- None

5.4.2.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Output Pin	List-box	Various GPIO pins	Output Pin Selection. For usability the Output Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
Drive Strength	List-box	Low/High	Low/High drive strength is configured on the selected pin



5.4.2.7 Block Dependency

None

5.4.2.8 Block Miscellaneous Details:

None

5.4.3 GPIO Digital Input ISR Block

5.4.3.1 Block Name

Digital Input ISR Block

5.4.3.2 Block Description

The main functionality of the block is to process GPIO ISRs.

5.4.3.3 Block Image

5.4.3.4 Inputs:

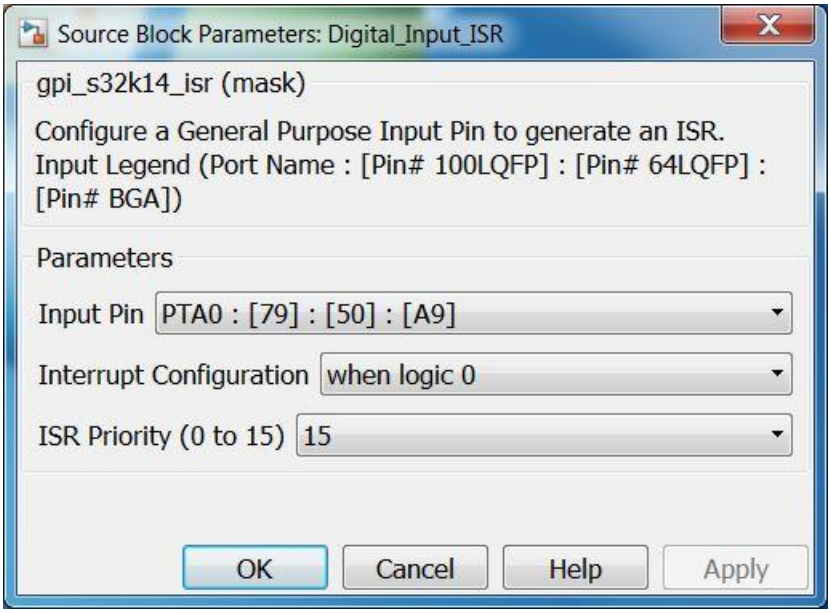
- None

5.4.3.5 Outputs:

- Function-Call

5.4.3.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Input Pin	List-box	Various Pins	Select which Pin to trigger ISR. For usability the Output Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
Interrupt Configuration	List-box	when logic 0 on rising-edge on falling-edge on either-edge when logic 1	Sets up the GPIO interrupt requests.
ISR Level	List-box	0 – 15	Interrupt priority level



5.4.3.7 Block Dependency

None

5.4.3.8 Block Miscellaneous Details:

None

5.4.4 GPIO Digital Input ISR Enable/Disable Block

5.4.4.1 Block Name

GPIO Interrupt Enable/Disable Block

5.4.4.2 Block Description

The main functionality of the block is to enable/disable PORT pin interrupts

5.4.4.3 Block Image

5.4.4.4 Inputs:

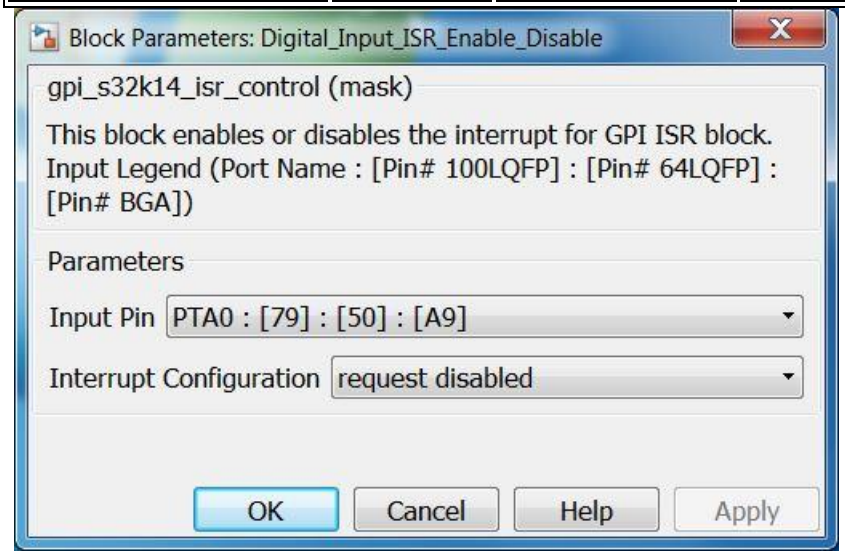
- None

5.4.4.5 Outputs:

- None

5.4.4.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Input Pin	List-box	Various Pins	Select Input Pin to use. For usability the Output Pin selection is displayed as: (Port Name : [Pin# 100LQFP] : [Pin# 64LQFP] : [Pin# 100BGA]) format
Interrupt Configuration	List-box	request disabled when logic 0 on rising-edge on falling-edge on either-edge when logic 1	Configure the PORT interrupt type



5.4.4.7 Block Dependency

None

5.4.4.8 Block Miscellaneous Details:

None

5.4.5 GPIO Glitch Filter Block

5.4.5.1 Block Name

Glitch Filter Block

5.4.5.2 Block Description

The main functionality of the block is to configure the Digital Filter Clock Settings for a PORT:A-E.

5.4.5.3 Block Image

5.4.5.4 Inputs:

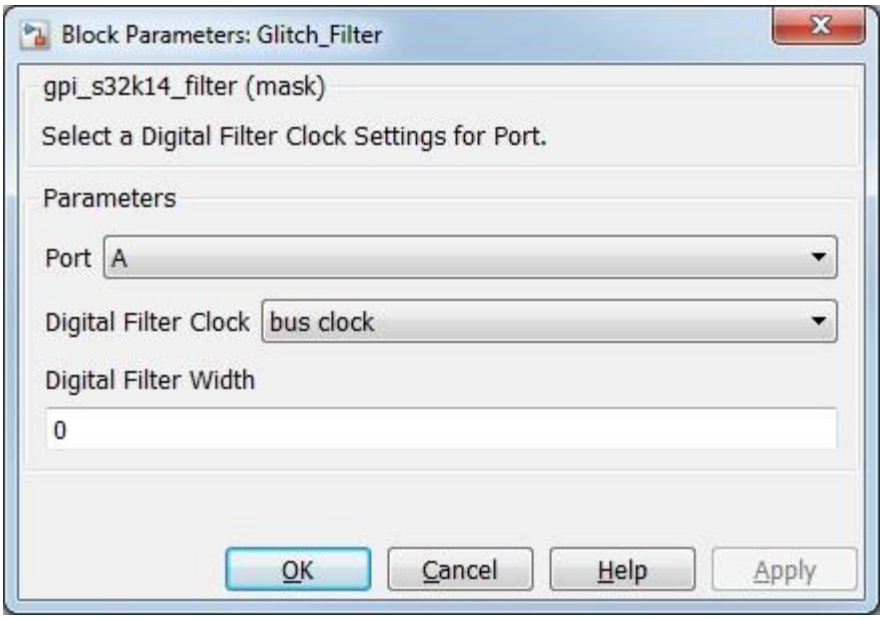
- None

5.4.5.5 Outputs:

- None

5.4.5.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
PORT	List-box	A B C D E	PORT Selection for Digital Filter
Digital Filter Clock	List-box	Bus Clock LPO Clock	Clock Selection for Digital Filter
Digital Filter Length	Text-box	0 - 31	Configures the maximum size of the glitches, in clock cycles, that the digital filter absorbs for the enabled digital filters. Glitches that are longer than this register setting will pass through the digital filter, and glitches that are equal to or less than this register setting are filtered.



5.4.5.7 Block Dependency

None

5.4.5.8 Block Miscellaneous Details:

The digital filter configuration is valid in all digital pin muxing modes. The digital filter is enabled on the corresponding pin, if the pin is configured as a digital input. Use Digital_Input block to enable/disable the digital filter

5.4.6 Programmable Delay Configuration Block

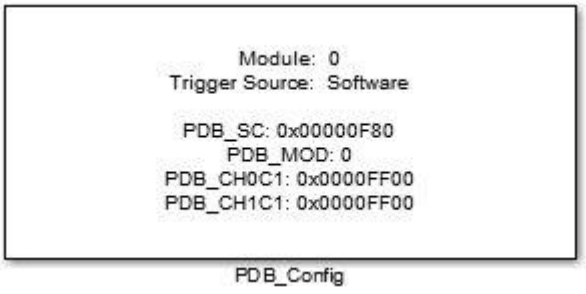
5.4.6.1 Block Name

Programmable Delay Block

5.4.6.2 Block Description

This block is used to setup the programmable delay module (PDB). The PDB provides controllable delays from an external trigger, or a programmable interval tick, to the hardware trigger inputs of ADCs. The PDB can optionally provide pulse outputs (Pulse-Out's) that are used as the sample window in the CMP block.

5.4.6.3 Block Image



5.4.6.4 Inputs:

- None

5.4.6.5 Outputs:

- None

5.4.6.6 Block Dialog and Parameters:

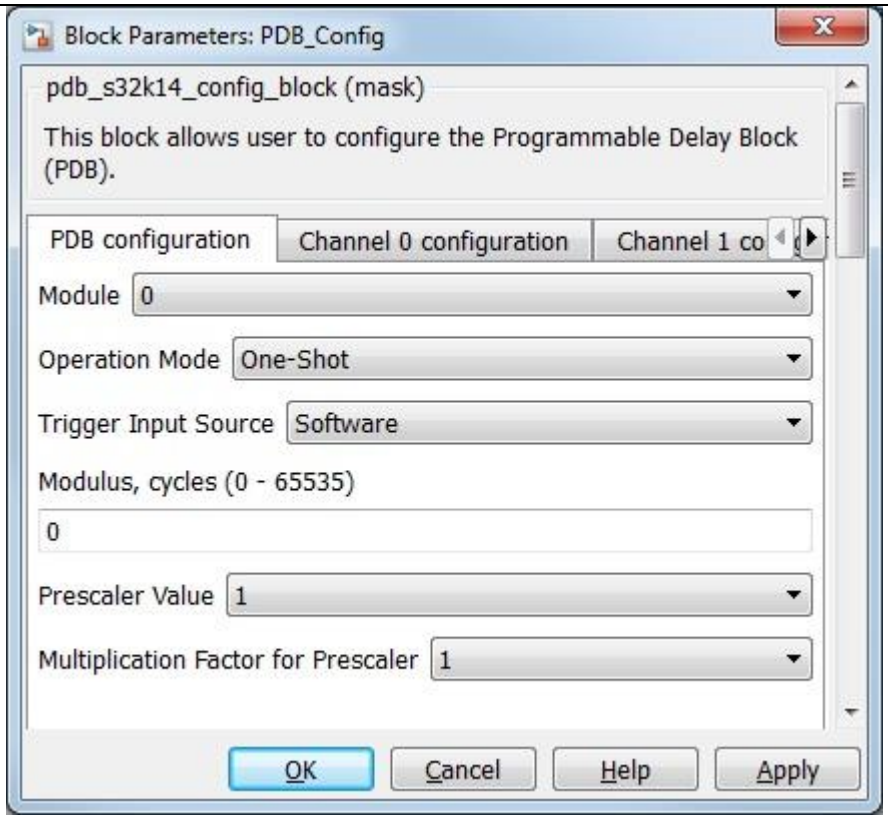
The block dialog consists of the following tabs:

- General
- Channel 0 Configuration
- Channel 1 Configuration
- Pulse-Out Configuration

- The General tab contains the following parameters:

Names	Selection Types	Range	Description
PDB Module	List-box	0-1	Select which PDB module to use.
Operation Mode (CONT)	List-box	One-Shot Continuous	In One-Shot mode the counter is enabled and restarted at count zero upon receiving a positive edge on the selected trigger input source or software trigger. In Continuous mode the counter is enabled and restarted at count zero. The counter is rolled over to zero again when the count reaches the value specified in the modulus register, and the counting is restarted. This enables a continuous stream of pretriggers/trigger outputs as a result of a single trigger input event.
Trigger Input Source (TRGSEL)	List-box	External (TRGMUX_PDB_TRIG) Software	Selects the trigger input source for the PDB. PDB trigger source selection is implemented through the TRGMUX module. For each PDB unit, there is only one trigger input from TRGMUX, but it supports different trigger sources
Input signal for External trigger (TRGMUX_PDB_TRIG Only)	List-box	List of Pins	Available external trigger input pins.

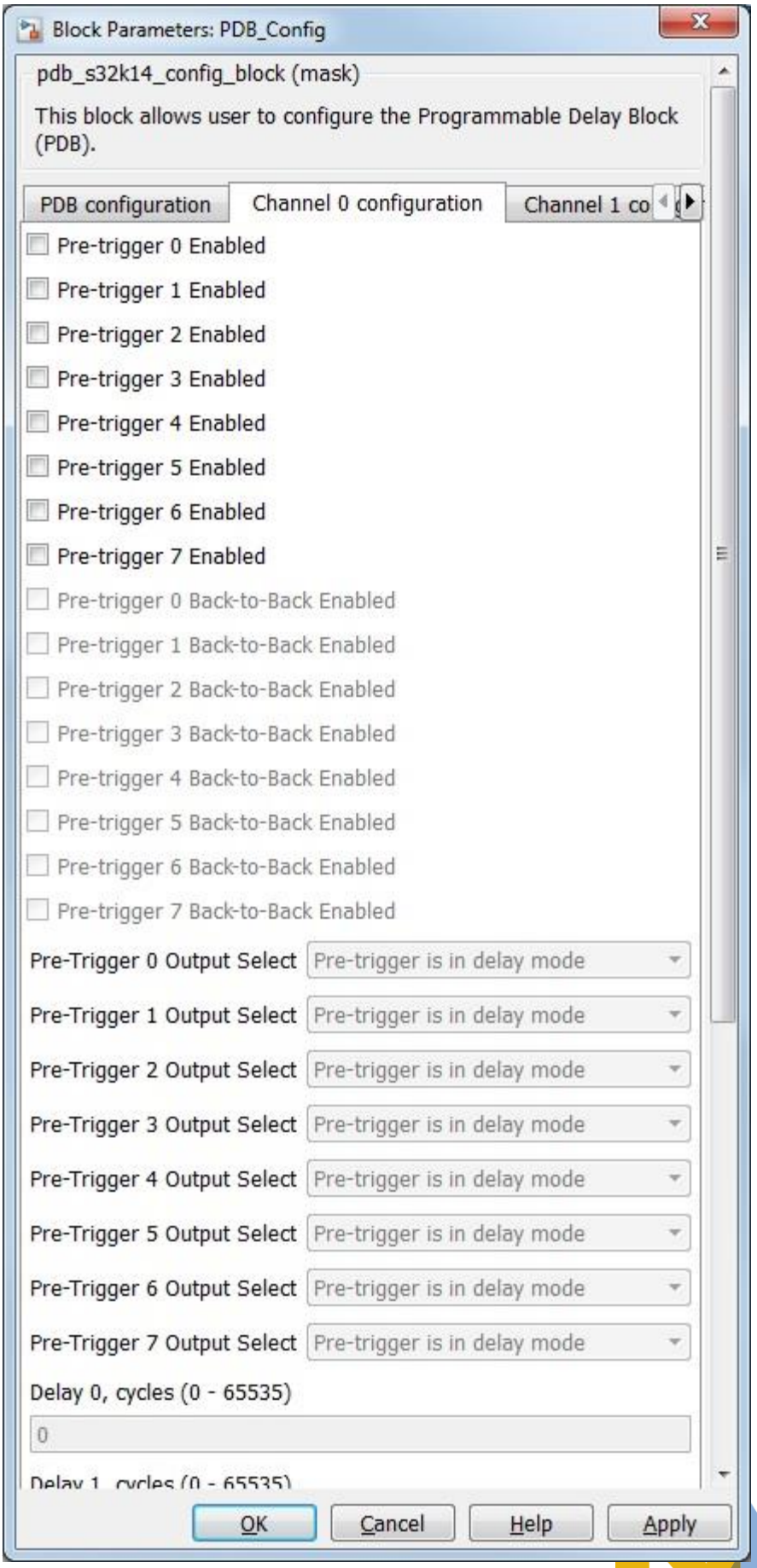
PDB Modulus (MOD)	Text-box	0 – 65535	Specifies the period of the counter. When the counter reaches this value, it will be reset back to zero. If the PDB is in Continuous mode, the count begins anew.
Prescaler Value (PRESCALER)	List-box	1, 2, 4, 8, 16, 32, 64, 128	Counting uses the peripheral clock divided by x times multiplication factor selected by MULT.
Multiplication Factor for Prescaler Value (MULT)	List-box	1, 10, 20, 40	Selects the multiplication factor of the prescaler divider for the counter clock.



- The Channel 0 Configuration tab contains the following parameters:

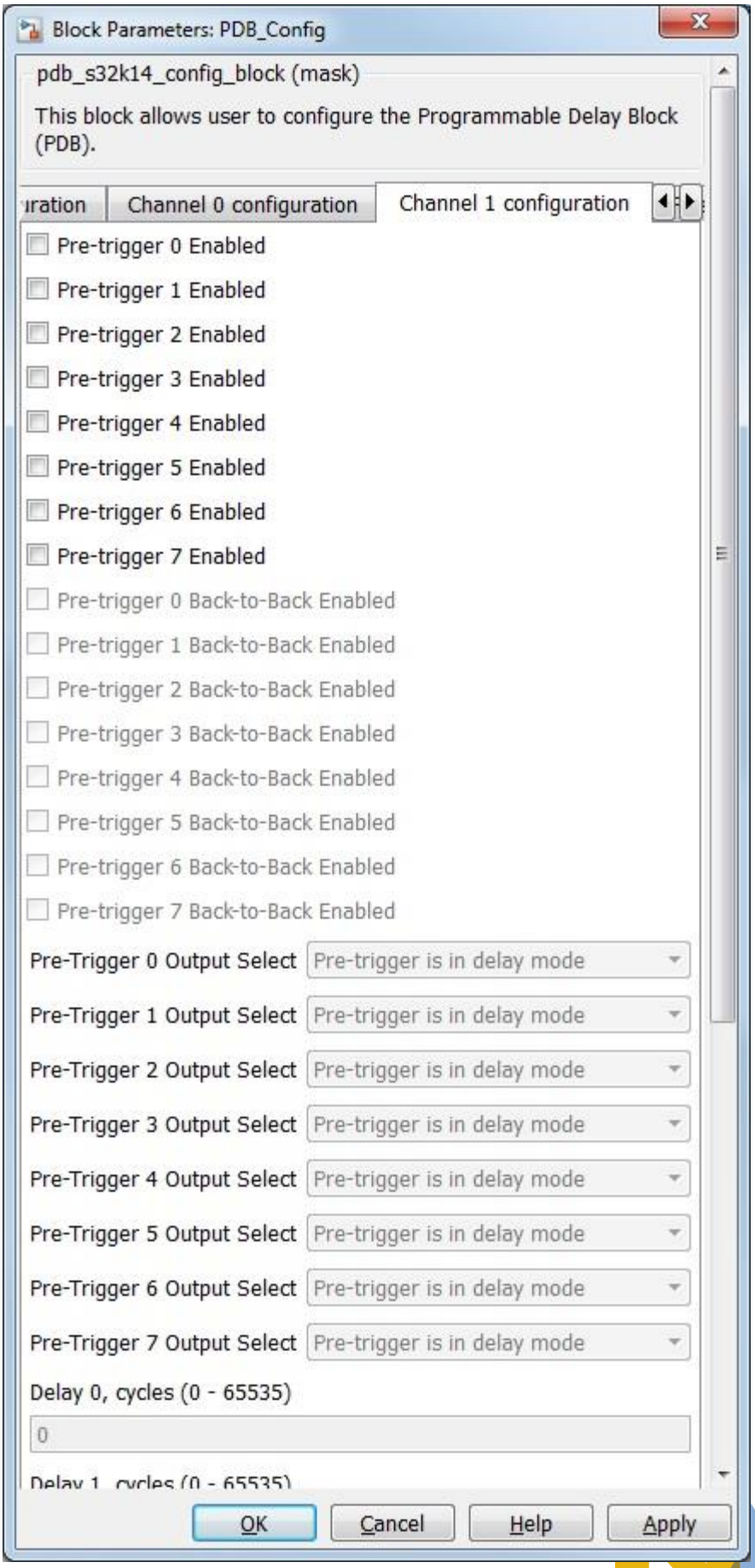
Names	Selection Types	Range	Description
Pre-Trigger x Enabled	Check-box	Enable/Disable	Enable the PDB ADC pre-trigger.
Pre-Trigger x Back-To-Back Enabled	Check-box	Enable/Disable	Back-to-back operation enables the ADC conversions complete to trigger the next PDB channel pre-trigger and

			trigger output, so that the ADC conversions can be triggered on next set of configuration and results registers. Application code must only enable the back-to-back operation of the PDB pre-triggers at the leading of the back-to-back connection chain.
Pre-Trigger x Output Select (TOS)	List-box	Pre-triggers bypassed mode; Pre-triggers delay mode	Selects the PDB ADC pre-trigger mode.
Delay x (DLY)	Text-box	0-65535	Specifies the delay value for the channel's corresponding pre-trigger. The pre-trigger asserts when the counter is equal to DLY.



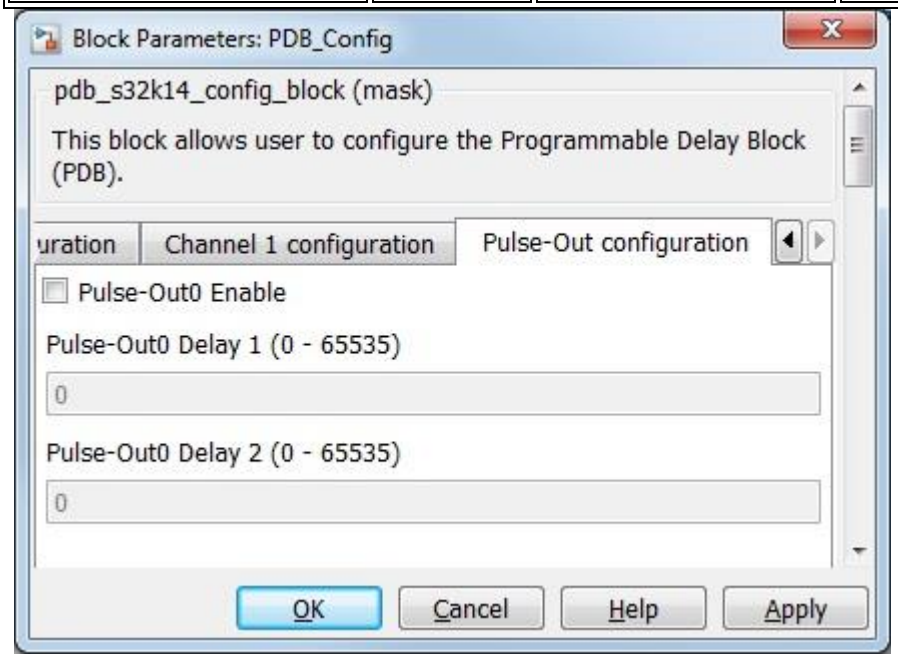
- The Channel 1 Configuration tab contains the following parameters:

Names	Selection Types	Range	Description
Pre-Trigger x Enabled	Check-box	Enable/Disable	Enable the PDB ADC pre-trigger.
Pre-Trigger x Back-To-Back Enabled	Check-box	Enable/Disable	Back-to-back operation enables the ADC conversions complete to trigger the next PDB channel pre-trigger and trigger output, so that the ADC conversions can be triggered on next set of configuration and results registers. Application code must only enable the back-to-back operation of the PDB pre-triggers at the leading of the back-to-back connection chain.
Pre-Trigger x Output Select (TOS)	List-box	Pre-triggers bypassed mode; Pre-triggers delay mode	Selects the PDB ADC pre-trigger mode.
Delay x (DLY)	Text-box	0-65535	Specifies the delay value for the channel's corresponding pre-trigger. The pre-trigger asserts when the counter is equal to DLY.



- The Pulse-Out Configuration tab contains the following parameters:

Names	Selection Types	Range	Description
Pulse-Outx Enable	Check-box	Enable/Disable	Enable Pulse out.
Pulse-Outx Delay 1	Text-box	0-65535	Specifies the delay 1 value for the PDB Pulse-Out. Pulse-Out goes high when the PDB counter is equal to the DLY1.
Pulse-Outx Delay 2	Text-box	0-65535	Specifies the delay 2 value for the PDB Pulse-Out. Pulse-Out goes low when the PDB counter is equal to the DLY2.



5.4.6.7 Block Dependency

None

5.4.6.8 Block Miscellaneous Details:

None

5.4.7 PDB Interrupt Block

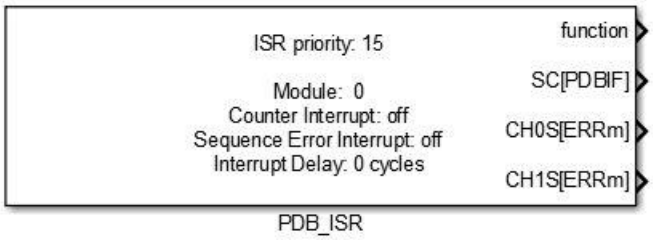
5.4.7.1 Block Name

Programmable Delay ISR Block

5.4.7.2 Block Description

This block is used to call user function on PDB Interrupt (when the counter value is equal to the IDLY register) or on PDB Sequence Error Interrupt.

5.4.7.3 Block Image



5.4.7.4 Inputs:

- None

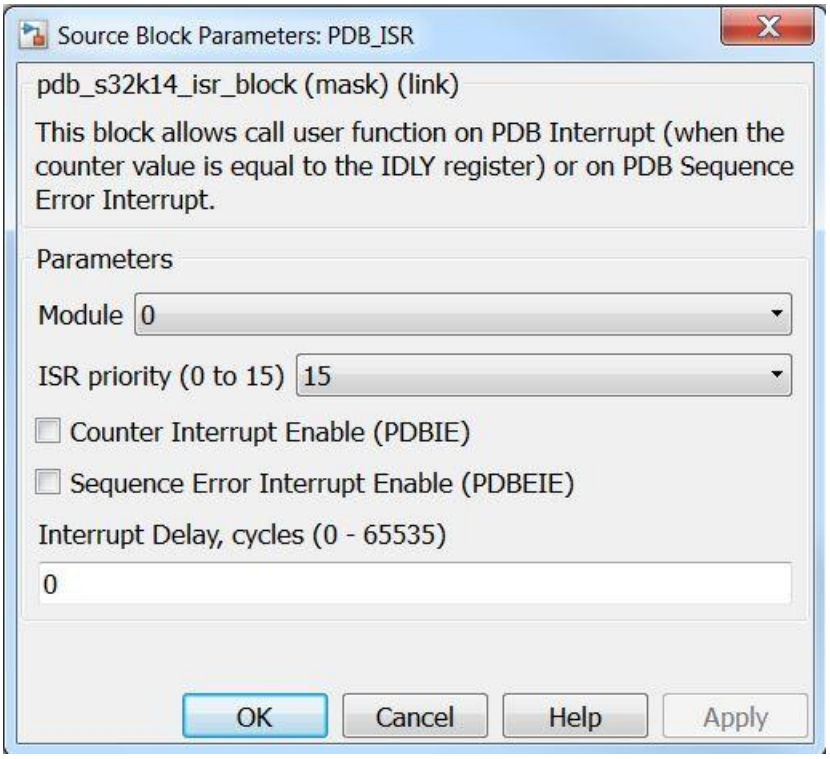
5.4.7.5 Outputs:

- Function-call
- Timer Interrupt flags (uint32)
- Channel 0 ADC Pre Trigger Sequence Error flags (uint32)
- Channel 1 ADC Pre Trigger Sequence Error flags (uint32)

5.4.7.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
PDB Module	List-box	0-1	Select which PDB module to use.
ISR Priority	List-box	0 – 15	ISR priority
Counter Interrupt Enable (PDBIE)	Check-box	Enable/Disable	
Sequence Error Interrupt Enable (PDBEIE)	Check-box	Enable/Disable	Sequence error detected on PDB channel's corresponding pre-trigger.*
Interrupt Delay (IDLY)	Text-box	0 – 65535	Specifies the delay value for the channel's corresponding pre-trigger. The pre-trigger asserts when the counter is equal to DLY.

*Read Hardware Manual documentation to get more information.



5.4.7.7 Block Dependency

Use PDB_Config Block to configure PDB

5.4.7.8 Block Miscellaneous Details:

None

5.4.8 PDB Interrupt Enable/Disable Block

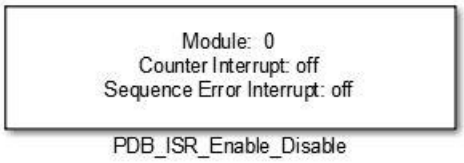
5.4.8.1 Block Name

PDB ISR Enable Disable Block

5.4.8.2 Block Description

The main functionality of the block is to allow the user to Enable/Disable PDB ISRs.

5.4.8.3 Block Image



5.4.8.4 Inputs:

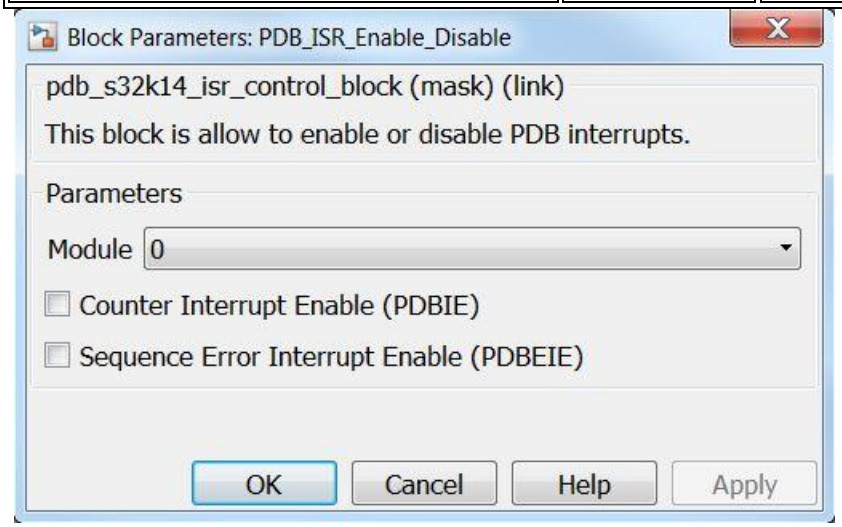
- None

5.4.8.5 Outputs:

- None

5.4.8.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
PDB Module	List-box	0-1	Select which PDB module to use.
Counter Interrupt Enable (PDBIE)	Check-box	Enable/Disable	Enables the PDB interrupt. When PDBIE is set and DMAEN is cleared, PDBIF generates a PDB interrupt.
Sequence Error Interrupt Enable (PDBEIE)	Check-box	Enable/Disable	Enables the PDB sequence error interrupt. When PDBEIE is set, any of the PDB channel sequence error flags generates a PDB sequence error interrupt.



5.4.8.7 Block Dependency

Use PDB_Config Block to configure PDB

5.4.8.8 Block Miscellaneous Details:

None

5.4.9 PDB Start Soft Trigger Block

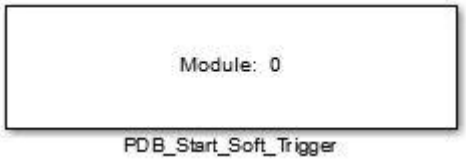
5.4.9.1 Block Name

PDB Start Soft Trigger Block

5.4.9.2 Block Description

When PDB is enabled and the software trigger is selected as the trigger input source, this block allows resets and restarts of the PDB counter.

5.4.9.3 Block Image



5.4.9.4 Inputs:

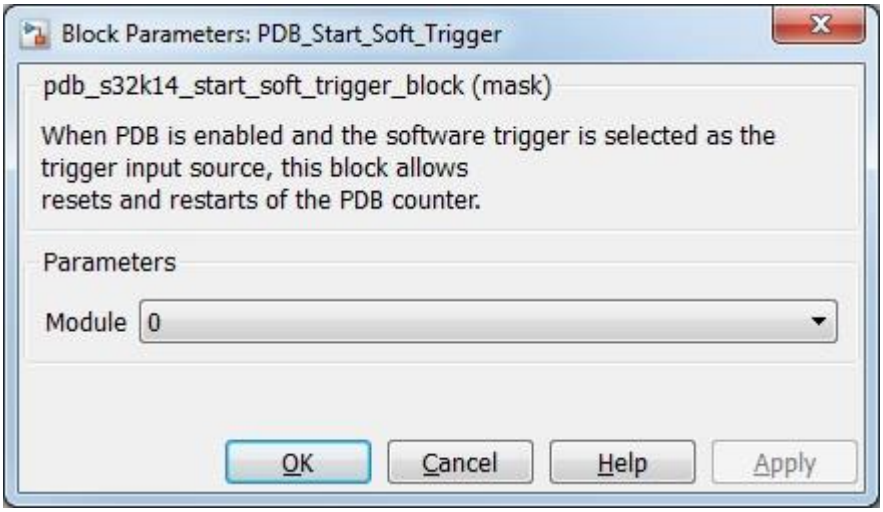
- None

5.4.9.5 Outputs:

- None

5.4.9.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
PDB Module	List-box	0-1	Select which PDB module to use.



5.4.9.7 Block Dependency

Use PDB_Config Block to configure PDB

5.4.9.8 Block Miscellaneous Details:

None

5.4.10 PDB Update Block

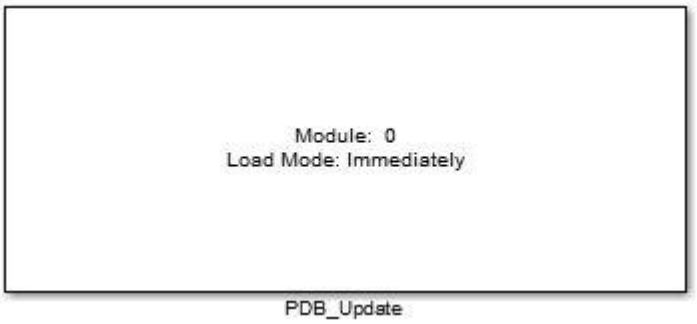
5.4.10.1 Block Name

Programmable Delay Update Block

5.4.10.2 Block Description

This block is used to update the MOD, IDLY, CHnDLYm registers, after 1 is written to LDOK.

5.4.10.3 Block Image



5.4.10.4 Inputs (if selected):

- Modulus (uint16)
- Interrupt Delay (uint16)
- Ch0 Delay 0 (uint16)

- Ch0 Delay 1 (uint16)
- Pulse-Out 0 Delay
- Pulse-Out 1 Delay
- DAC 0 Interval

5.4.10.5 Outputs:

- None

5.4.10.6 Block Dialog and Parameters:

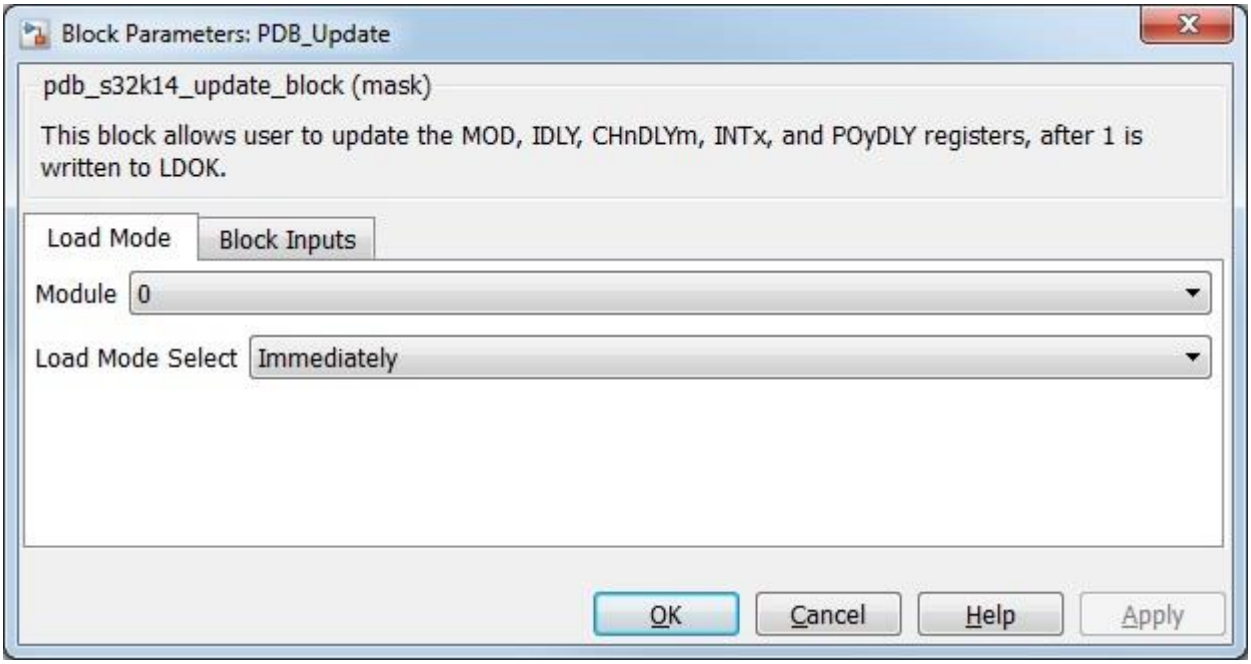
The block dialog consists of the following tabs:

- Load Mode
- Block Inputs

- The Load Mode tab contains the following parameters:

Names	Selection Types	Range	Description
PDB Module	List-box	0-1	Select which PDB module to use.
Load Mode Select	List-box	Immediately; PDB Counter reaches MOD reg value; Trigger input event is detected; PDB Counter reaches the MOD register value or a trigger input event is detected	Selects the mode to load the MOD, IDLY, CHnDLYm, INTx, and POyDLY registers.

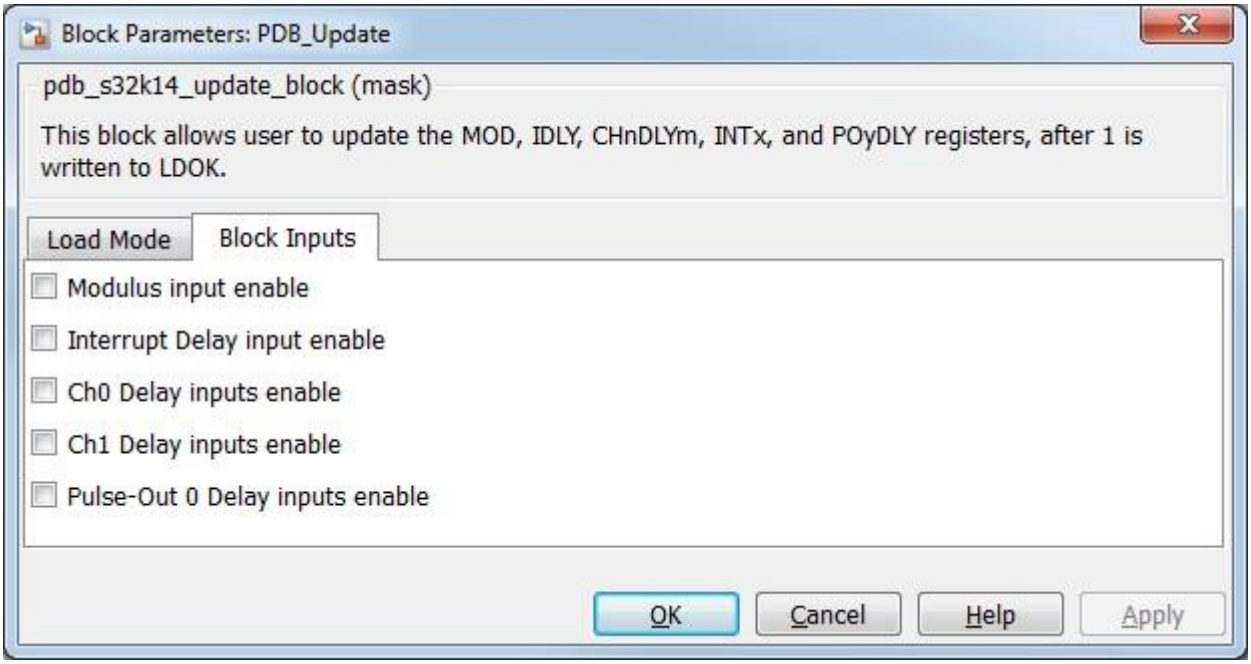
*Read Hardware Manual documentation to get more information.



- The Block Inputs tab contains the following parameters:

Names	Selection Types	Range	Description
Modulus Input Enable	Check-box	Enable/Disable	When enabled input will show up on block.
Interrupt Delay Input Enable	Check-box	Enable/Disable	When enabled input will show up on block.
Ch0 Delay Inputs Enable	Check-box	Enable/Disable	When enabled input will show up on block.
Ch1 Delay Inputs Enable	Check-box	Enable/Disable	When enabled input will show up on block.
Pulse-Out 0 Delay Inputs Enable	Check-box	Enable/Disable	When enabled input will show up on block.

*Read Hardware Manual documentation to get more information.



5.4.10.7 Block Dependency

Use PDB_Config Block to configure PDB

5.4.10.8 Block Miscellaneous Details:

None

5.5 Utility Blocks

The Model Based Design Toolbox provides utility blocks for use with your targeted application. The utility blocks allow the user to leverage certain processor capabilities for software engineering and configuration optimization tasks. The user can use the profiling block to determine the execution time of a specific function in code.

5.5.1 Periodic Interrupt Timer Block

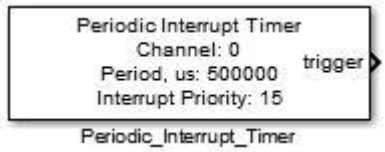
5.5.1.1 Block Name

Periodic Interrupt Timer (PIT) Block

5.5.1.2 Block Description

This block is used to trigger an interrupt routine periodically.

5.5.1.3 Block Image



5.5.1.4 Inputs:

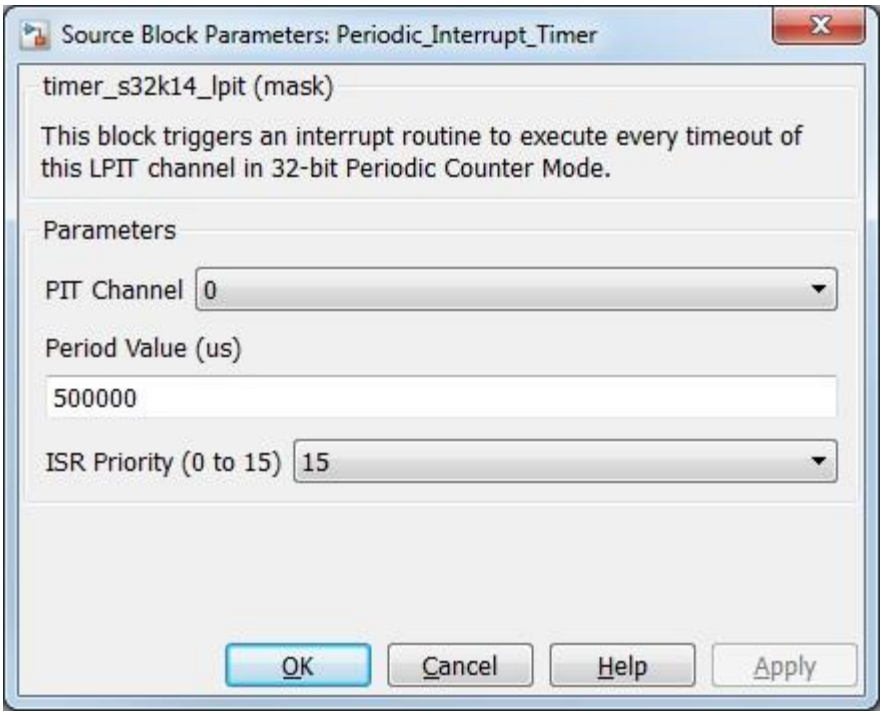
- None

5.5.1.5 Outputs:

- Function-call

5.5.1.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
PIT Channel	List-Box	0 – 3	
PIT Timeout Value (us)	Text-box	Based on system clock rate selected.	Timeout period for PIT interrupts.
Interrupt Priority	List-Box	0 – 15	Interrupt priority level



5.5.1.7 Block Dependency

None

5.5.1.8 Block Miscellaneous Details:

PIT channel 3 is also used by the profiler block if it is present in the model.

5.5.2 PIT ISR Enable/Disable Block

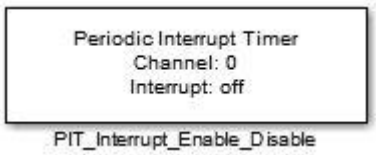
5.5.2.1 Block Name

PIT Interrupt Enable/Disable Block

5.5.2.2 Block Description

This block is used to enable/disable PIT interrupts

5.5.2.3 Block Image



5.5.2.4 Inputs:

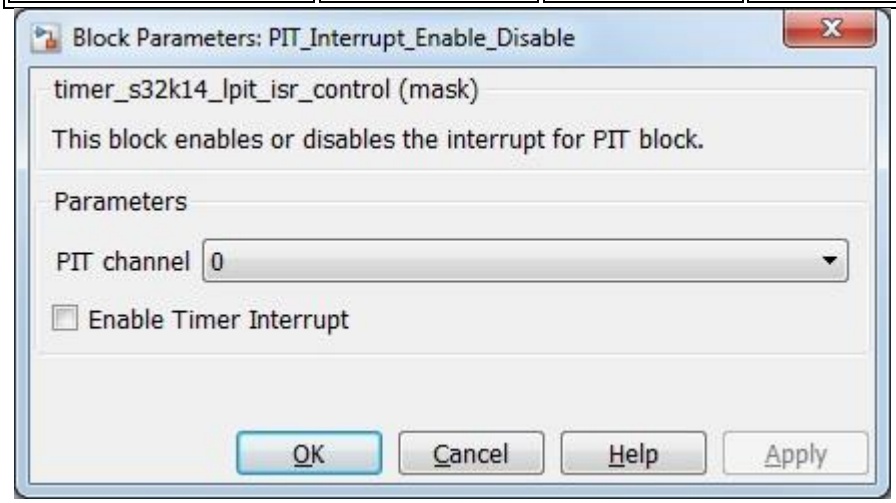
- None

5.5.2.5 Outputs:

- None

5.5.2.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
PIT Channel	List-Box	0 – 3	
Enable Timer Interrupt	Check-box	On/Off	Enable/Disable Timer Interrupt



5.5.2.7 Block Dependency

Please do the following:

1. Configure related PIT channel via PIT Configuration Block

5.5.2.8 Block Miscellaneous Details:

PIT channel 3 is also used by the profiler block it is present in the model.

5.5.3 Memory Read Block

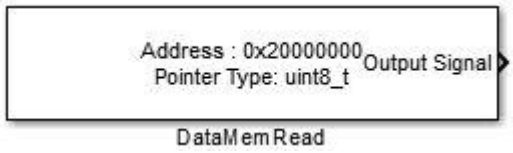
5.5.3.1 Block Name

Memory Read Block

5.5.3.2 Block Description

The main functionality of the block is to read data at memory location specified by the base address and the offset value. That is reading data at memory location (Base Address + Offest.)

5.5.3.3 Block Image



5.5.3.4 Inputs:

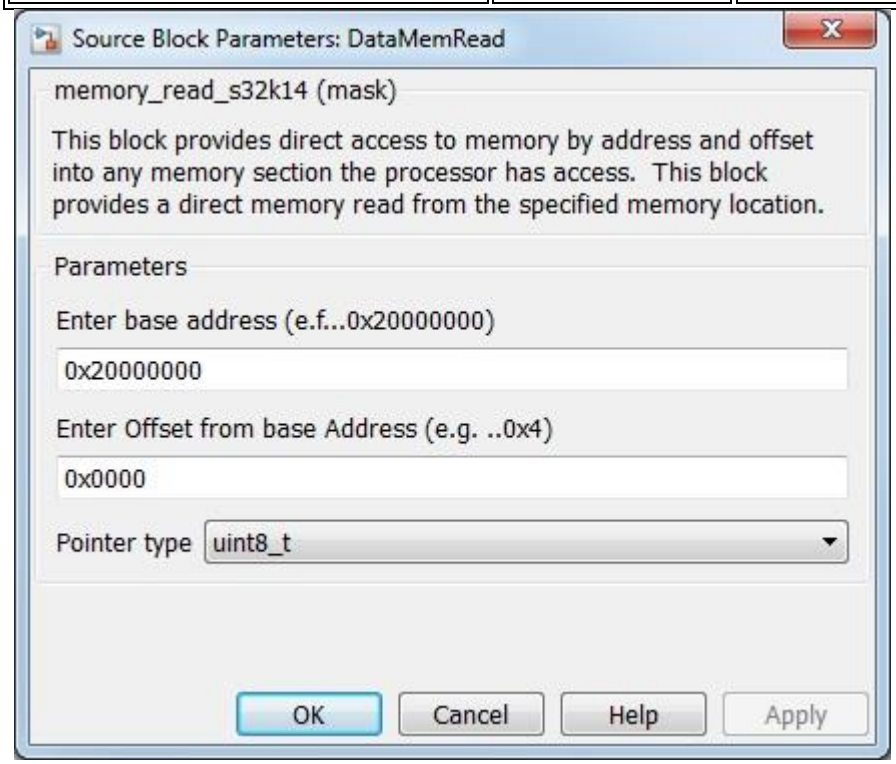
- None

5.5.3.5 Outputs:

- 8/16/32bit Data at the specified memory location.

5.5.3.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Enter base Address	Text-box	Hex value	
Enter Offset from the base address	Text-box	Hex value	
Pointer type	List-box	uint8_t uint16_t uint32_t	Data size type to use.



5.5.3.7 Block Dependency

None

5.5.3.8 Block Miscellaneous Details:

None

5.5.4 Memory Write Block

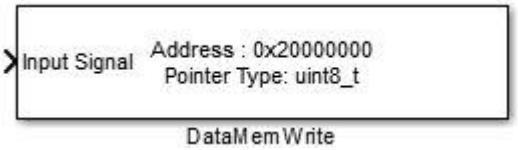
5.5.4.1 Block Name

Memory Write Block

5.5.4.2 Block Description

The main functionality of the block is to write data at memory location specified by the base address and the offset value. That is reading data at memory location (Base Address + Offest.)

5.5.4.3 Block Image



5.5.4.4 Inputs:

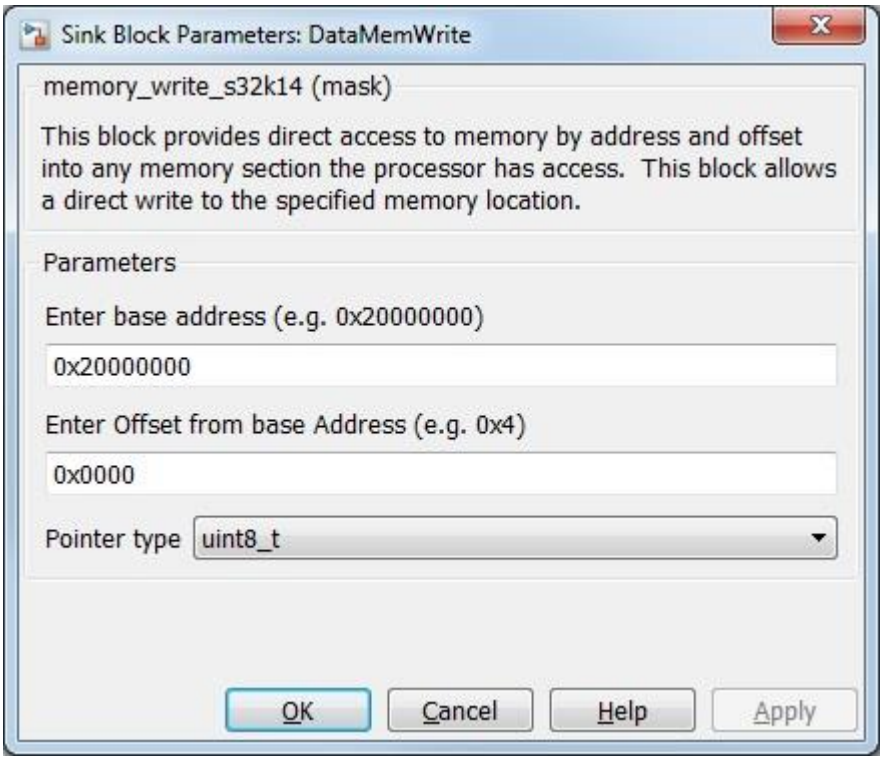
- 8/16/32bit Data at the specified memory location to write to.

5.5.4.5 Outputs:

- None

5.5.4.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Enter base Address	Text-box	Hex value	
Enter Offset from the base address	Text-box	Hex value	
Pointer type	List-box	uint8_t uint16_t uint32_t	Data size type to use.



5.5.4.7 Block Dependency

None

5.5.4.8 Block Miscellaneous Details:

The block requires that the memory address (base address + offset).

5.5.5 Profiler Function Block

The profiling block works with atomic subsystems that have been deemed to generate function code. The profiling function instruments the generated code by placing a call just inside the top of the function and just before exiting the function at the bottom. The profiling function takes a snap shot of the timing register at the top and bottom of the function. Then at the end of the function finds the difference between these two values, because the timer runs at the system clock rate by using this as a timing device the number of clock cycles used during execution is captured faithfully. This will account for things like interrupts and such while the function is executing. There is overhead in capturing the clock cycles of a function. This value is NOT removed from the raw numbers of the profile for the function. The use of the profile send function at the end of profiling for sending data over the serial interface add significantly more cycles in overhead to the process. The overhead is incurred after the measurement is taken but will show up when profile function blocks are embedded with hierarchical subsystems being measured, the parent subsystems will inherit the overhead.

The profiling block is supported for PIL simulation and on Target execution only, not supported in SIL simulation or normal simulation.

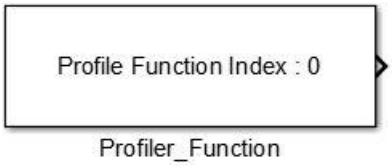
5.5.5.1 Block Name

Profiler Function Block

5.5.5.2 Block Description

This block profiles the execution time of a function. It places profiling code at the beginning and the end of the function this block is placed in. Up to 100 functions can be profiled at once so a profile index must be selected for each block.

5.5.5.3 Block Image



5.5.5.4 Inputs:

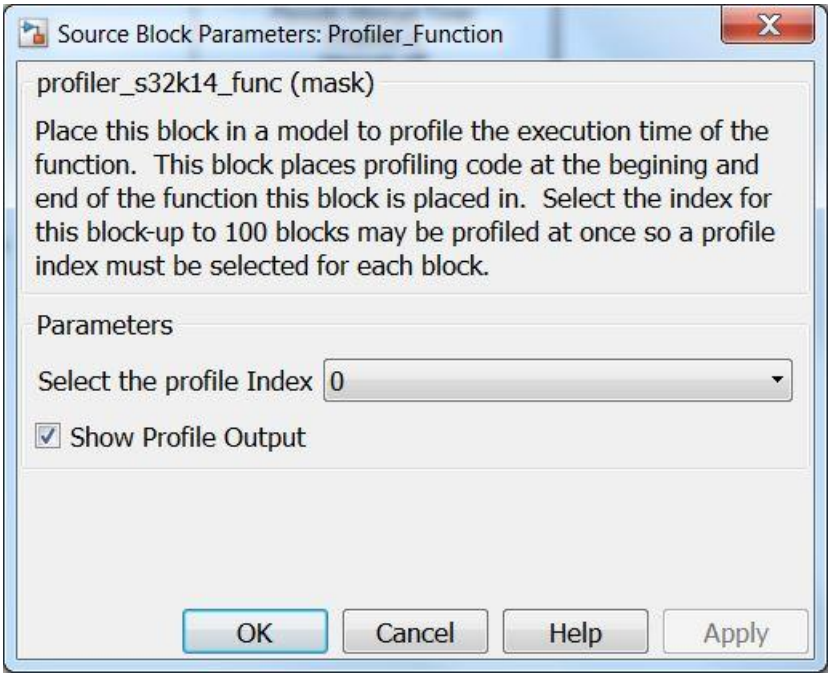
- None

5.5.5.5 Outputs:

- Execution time length in bus clock ticks (UINT32) (if "Show Profile Output" is set).

5.5.5.6 Block Dialog and Parameters:

Names	Selection Types	Range	Description
Profile index	List-box	0 – 99	Index of Profile buffer
Show Profile Output	Check-box	On/Off	Enables Profile Output



5.5.5.7 Block Dependency

Profiler function may be used when the PIT channel 3 is not being used in the model.

5.5.5.8 Block Miscellaneous Details:

None

5.5.6 FreeMASTER Data Recorder Block

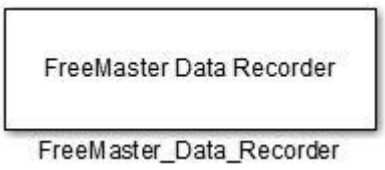
5.5.6.1 Block Name

FreeMaster Data Recorder Block

5.5.6.2 Block Description

This block allows the user to store variables in internal memory and download them through FreeMaster tool.

5.5.6.3 Block Image



5.5.6.4 Inputs:

- None

5.5.6.5 Outputs:

- None

5.5.6.6 Block Dialog and Parameters:

5.5.6.7 Block Dependency

FreeMaster should be enabled in the FreeMASTER Configuration Menu.

5.5.6.7.1 Block Miscellaneous Details:

None

5.5.6.8 Initialization Call Insertion Block

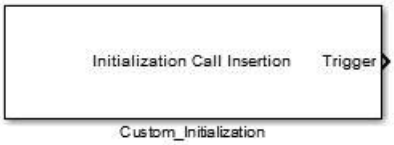
5.5.6.9 Block Name

Initialization Call Insertion Block

5.5.6.10 Block Description

The main scope of this type of block is to insert a function call, **init_call_trigger**, between the System Initialization and first System Task. Using this function the user will be able to write any register or make any desired modification before the model first step.

5.5.6.11 Block Image



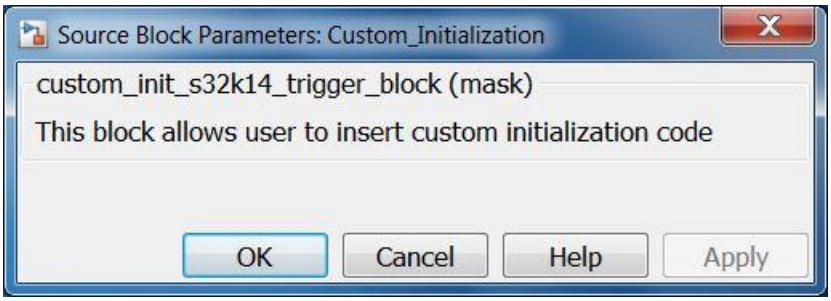
5.5.6.12 Inputs:

- None

5.5.6.13 Outputs:

- Function-Call

5.5.6.14 Block Dialog and Parameters:



5.5.6.15 Block Dependency

None

5.5.6.16 Block Miscellaneous Details:

None

6 Embedded Targets

The embedded target provides a Flash memory configuration. The MBD Toolbox target is derived from EC Embedded Real-Time Target (ERT) target so all code generation options for the MBD Toolbox target are available just as the ERT from MathWorks. All code generation options from ERT are available to the MBD Toolbox target. There is also support for including user-specific files into the build.

6.1 User-Specific Files Needed for Build

There may be instances where variables are used from code that is not part of the model but are instead hand coded. In these instances, user specific files will need to be included in the build directory created by toolbox. The user can specify which files to include in the build directory by creating/modifying a file called mbd_s32k14_user_copy_required_files.m and locate it somewhere in one of the MATLAB paths. There is an example of this file located in the ‘mscripts’ directory that demonstrates how to include user specific files.

6.2 Using Interrupt Service Routine (ISR) Blocks

Simulink does not inherently support ISR function calls (asynchronous code generation functionality calls). We have provided support for this in the MBD Toolbox. The ISR code generation is possible under select circumstances. However, the Simulink Environment does not have the appropriate checks/warning messages developed to prevent users from implementing this functionality in subsystems where they may not work. The following are suggestions for the user when building models with ISR blocks:

- Interrupts should not be placed in model reference blocks, non-inlined or re-usable subsystem
- Interrupts can work if placed in inlined or non-reusable subsystems

7 FreeMASTER Interface

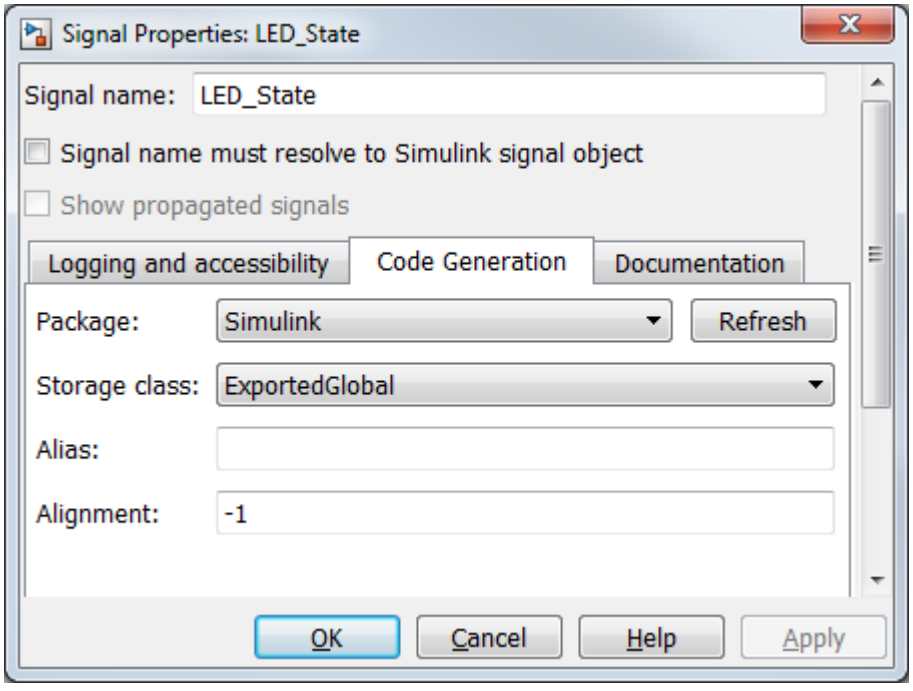
The FreeMASTER is a real-time monitor pc-based application that connects to your embedded target through various communication links.

The FreeMASTER Interface works with systems that have been deemed to generate function code. It incorporates FreeMASTER serial communication protocol files targeted for MCU platform. The FreeMASTER function provides communication interfaces between the Target and the host PC using FreeMASTER protocol.

Either UART(SCI) or CAN communication links can be used with FreeMASTER. Currently, both the Bootloader and the PIL mode use the UART(SCI) communication link. Due to the limitations of the UART(SCI) link, FreeMASTER cannot be used on the same UART(SCI) as either Bootloader or when running PIL. Additionally, many applications use the CAN link for node to node communications, making the CAN link more generally supported throughout the development cycle. Multiple interfaces can use the CAN link concurrently. For these reasons, the CAN communication link is the recommended connection for FreeMASTER.

To configure your Model Based Design Toolbox enhanced Simulink model for FreeMASTER, complete the following steps:

1. Identify the signals to monitor with FreeMASTER and provide them with a unique name.
2. In Signal Properties, Real-Time Workshop tab:
    a. Package: ‘Simulink’
    b. Storage class: ‘ExportedGlobal’



3. In MBD_S32K14x_Config_Information block, FreemasterSetup tab
    a. Freemaster Interface: ‘Serial’
    b. Freemaster Interface Rate: <select your preferred rate from the list>
    c. Remaining Serial interface settings are not user-selectable

Or

d. Freemaster Interface: ‘CAN’
e. Remaining CAN interface settings are not user-selectable

For more information on FreeMASTER, see *pcm_um.pdf*.

8 Bootloader

The RAppID Boot Loader works with several Freescale MCUs. The Boot Loader supports the operational modes of the different part family silicon instantiations. The Boot Loader provides a streamlined method for programming code into FLASH or RAM on either target EVBs or custom boards. Once programming is complete the application code automatically starts. For more information, refer to the Boot Loader User Manual *RAppidBL_UserManual.pdf*

9 PIL/SIL Operational Mode

Model Based Design Toolbox provides support for both Processor-In-the-Loop (PIL) and Software-In-the-Loop (SIL) simulations. PIL simulation allows execution of the production source code on the target. SIL simulation provides the same benefit of verifying the production source code, but without the hardware.

9.1 PIL & SIL Automatic Configuration

Model Based Design Toolbox provides via the Tools pull-down menu for easy transition between simulation modes as well as generation of PIL & SIL blocks.

There is support for the following simulation mode transitions:

1) To PIL Mode on S32K14
2) To SIL Mode
3) To Normal Mode
4) To Accelerator Mode

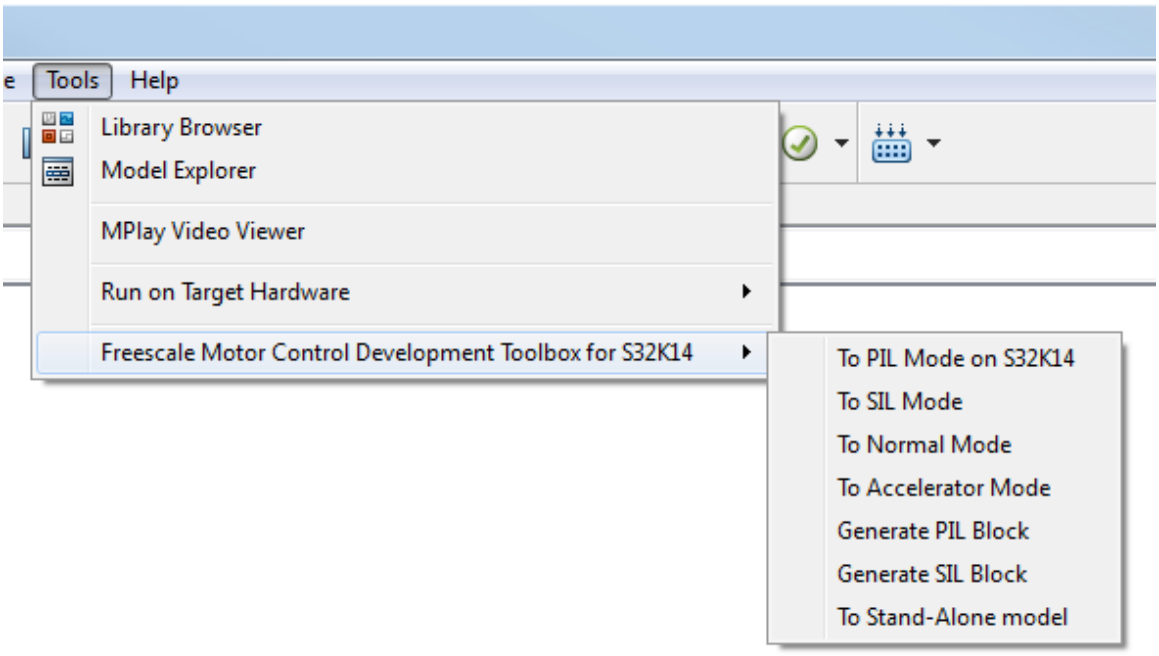
Note: These four options only support the Model Block PIL mode and can only be executed from the model containing the model reference block.

There is support for the following Build Model actions:

1) Generate PIL Block
2) Generate SIL Block
3) To Stand-Alone model

Note: These menu items are only supported for Block PIL and this needs to be used from the model that contains the logic to be used in PIL mode.

'To Stand-Alone Model' puts the target model into ordinary mode: set target to mbd_s32k14, switch CreateSILPILBlock off, switch pil_download_enable off, set hardware settings to Freescale. In contrast to 'To Normal Mode' it can be applied to the target model, for example after 'Generate SIL block' while 'To Normal Mode' is applicable to the top level model.



Note: In addition to executing the script, it is necessary to set the Processor-In-Loop option in the MBD_S32K14x_Config_Information block settings when transitioning to PIL Mode.

9.2 PIL & SIL Manual Configuration

Alternatively, it is possible to change the settings manually. The following table identifies the additional settings required to transition to PIL & SIL modes (these settings are ignored in Normal and Accelerator Modes). These settings apply regardless of whether you are using PIL/SIL block or Model block (using model-reference) PIL/SIL method:

	PIL	**SIL**
'Configuration Parameters'		
'Code Generation' - 'System target file'	'mbd_s32k14.tlc'	'ert.tlc'
'Code Generation' – 'Interface' – 'absolute time'	Off	Off
'Code Generation' – 'Symbols' – 'Maximum identifier length'	63	63
'Hardware Implementation' – 'Device Vendor'	'ARM Compatible'	'Generic'
'Hardware Implementation' – 'Device type'	'ARM Cortex'	'Custom'
'Hardware Implementation' – 'Byte ordering'	'LittleEndian'	'LittleEndian'
'Hardware Implementation' – 'Signed integer division rounds'	'Zero'	'Zero'
'PIL and Download Config' – 'Enable PIL Mode Download'	On	Off
Set 'ModelReferenceCompliant' in Command Window: set_param(<model_name>, 'ModelReferenceCompliant', 'on');	On	On

Next, perform the following steps depending on which method you have chosen:

- PIL/SIL block

1. Set from Tools pulldown menu Code Generation -> Options -> SIL and PIL Verification section -> Create block to either SIL or PIL.
2. Build Model

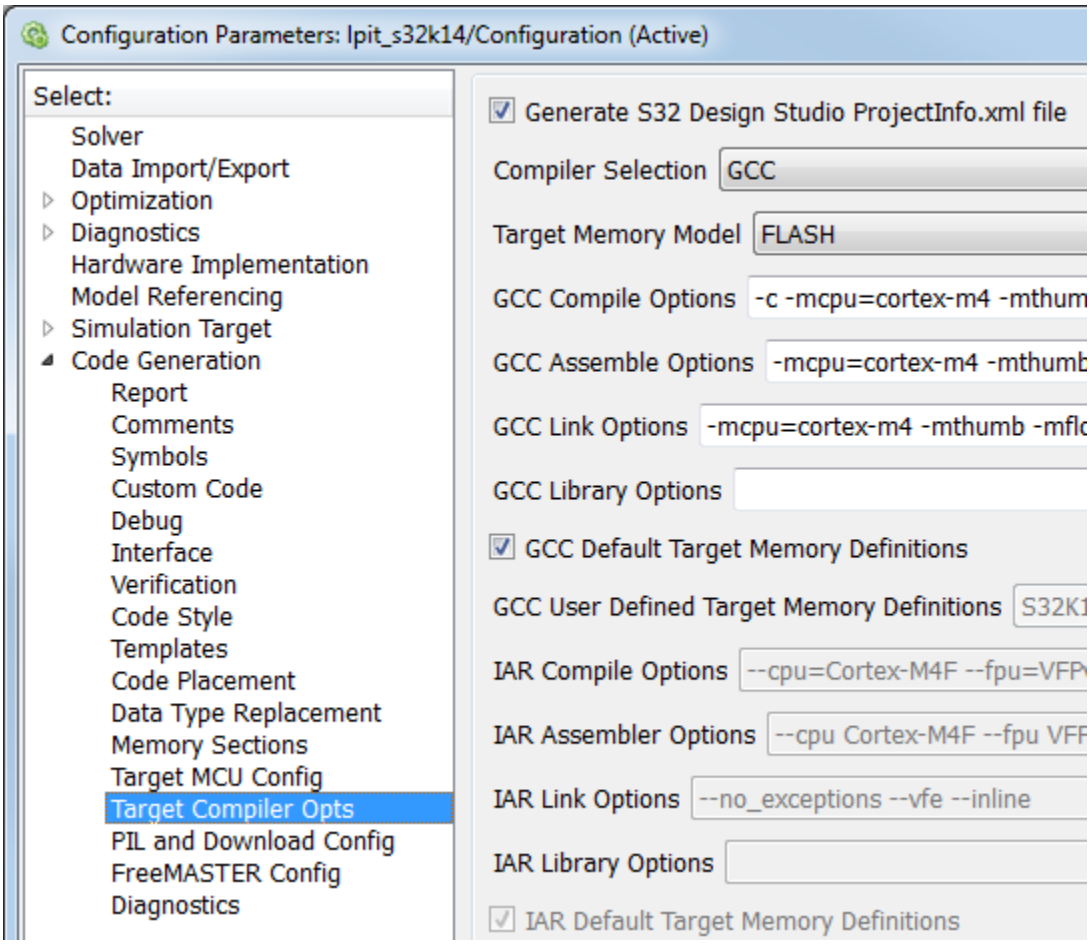
- Model block PIL/SIL
    1. Change the Simulation Mode in ModelReference Parameters menu to PIL or SIL.

Now you are ready to simulate your PIL/SIL model.

Note: PIL block & SIL block are supported in all versions of MATLAB currently supported by Model Based Design Toolbox.

10 S32DS for ARM Project File Generation

There is an option in the Target Compiler Opts to generate a project file for S32 Design Studio. Check the box as shown below, with GCC selected as the compiler. Then when you build the model and generate code, there will also be a ProjectInfo.xml file generated. Please follow the documentation within the S32 Design Studio for details on how to import the project file.



The project file import within S32DS for ARM is supported in v1.3 (with latest update package) or later.