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LPC1114 SSP TX FIFO clear

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Wed, 2014-10-22 01:41

romko
Offline

Joined: 2013-04-13
Posts: 2

Hi,

I have iplemanted SPI slave device on my LPC1114 processor. My system put data to the SSP TX FIFO on the TXMIS (TX FIFO is at least half empty) interrupt. So it is always "pumping" data to the TX FIFO.
For providing packet integrity I need somehow reset data that already exists in the TX FIFO in case when some error occured. For now I haven't find better solution than reseting complete SSP peripheral by

```
LPC_SYSCON->PRESETCTRL &= ~(0x01 << 0);
LPC_SYSCON->PRESETCTRL |= (0x01 << 0);
```

Is the better way to clear SSP TX FIFO ?

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Wed, 2014-10-22 09:35   #1

NXP_Paul
Offline

NXP Support

Joined: 2011-10-04
Posts: 123

Using the PRESETCTRL register is the best way that I am aware of to reset the SSP periperal.

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