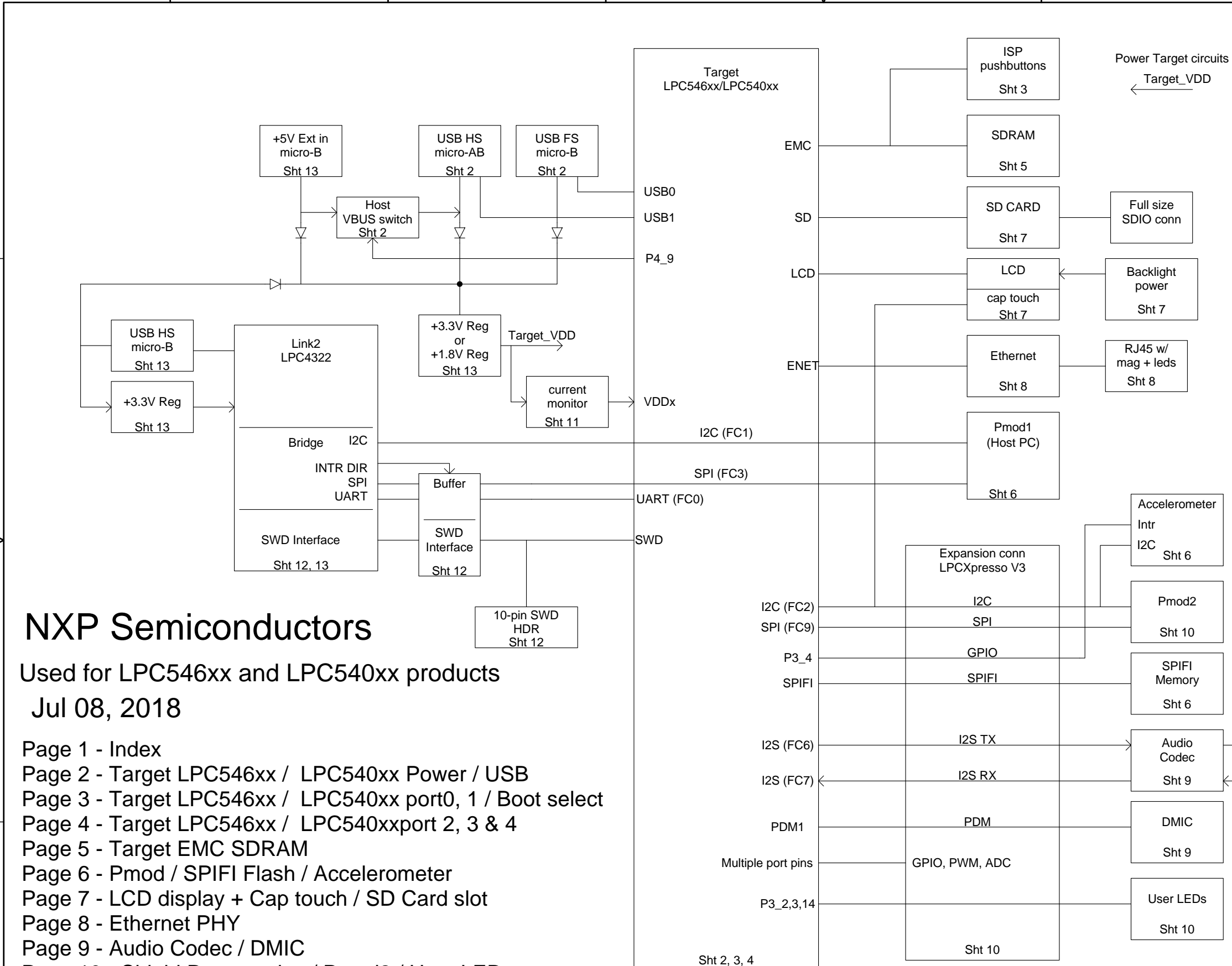


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1	PCB Rev 1 release; refdes renumbered	10/05/2015	
1a	U27 changed to MX25L12835FM2I-10G for 1.8V assy; sht 6.	10/14/2015	
1b	C13, C14 changed to 220pF; sht 9.	10/19/2015	
A	PCB Rev A release to production	04/19/2016	
B	Add USB0 FS Host; JP9 - JP13, U29, R119 Sht 2, 3, 4, 9	08/10/2016	
C	Add FC0 Uart to P4; Add R120; replace JP8 with JS33 - JS36. Sht 3, 4, 11	10/31/2016	
D	Correct I2C FC1 SCL, SDA at J14, JS15, JS16. Sht 6, 13 Change D5 to PESD3V3L5UY; Sht 12	06/14/2017	
E	1) Add P0_20 and P0_21 to expansion conn J10; with 0ohm solder jumpers; Sht 5,10 2) JP5 changed to TH; Sht 12	11/08/2017	
F	Change SWD ISPEN to ISPO; Sht 12 Add alternates for U28, U26A1, U27; Sht 5,6	07/08/2018	

Notes:
 1) "DNI" = Do Not Install by default
 2) "JSx" solder jumpers use 0ohm resistor for default strapping.
 3) This board design is used for LPC546xx and LPC540xx products.



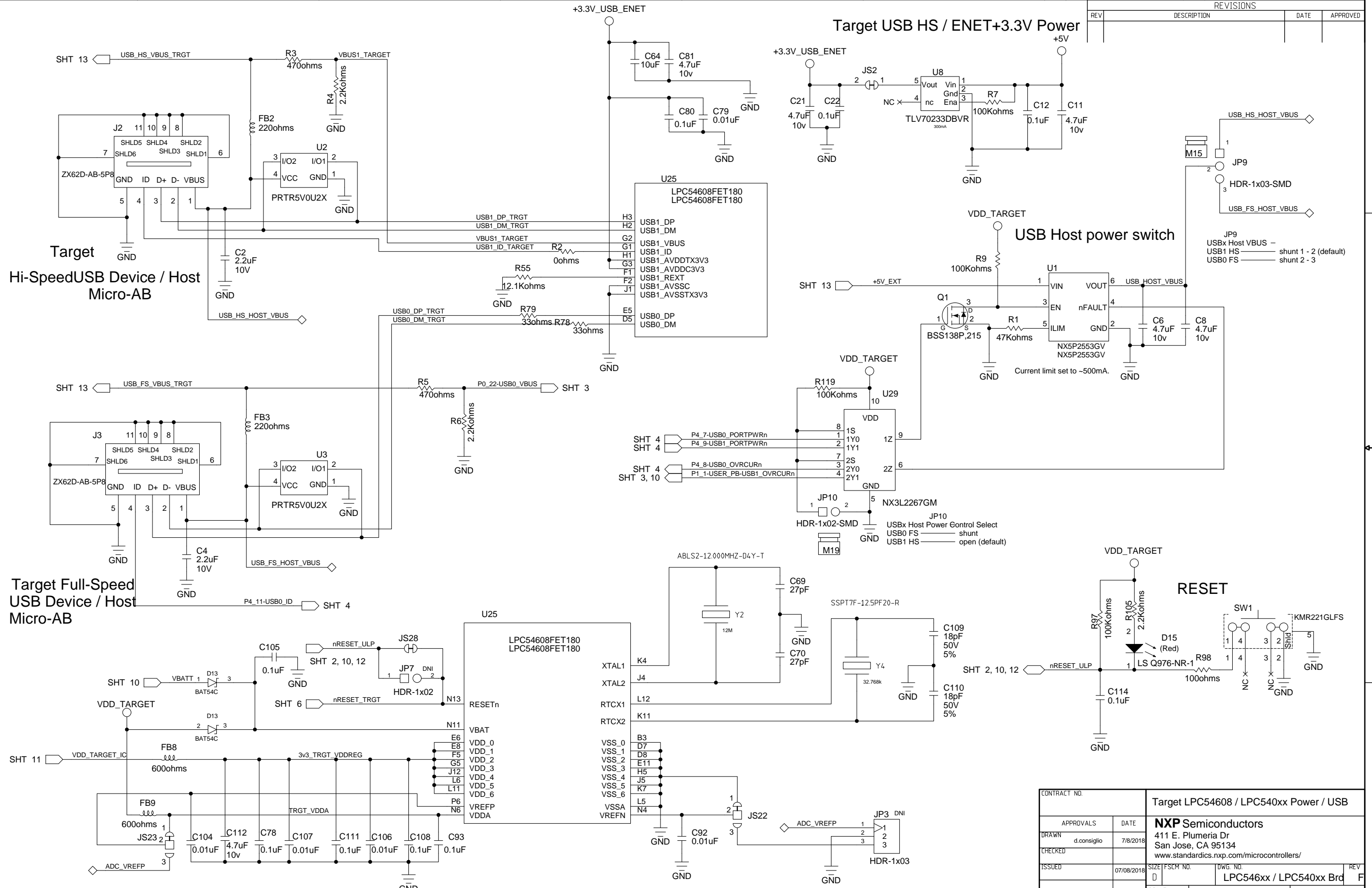
NXP Semiconductors

Used for LPC546xx and LPC540xx products
 Jul 08, 2018

- Page 1 - Index
- Page 2 - Target LPC546xx / LPC540xx Power / USB
- Page 3 - Target LPC546xx / LPC540xx port0, 1 / Boot select
- Page 4 - Target LPC546xx / LPC540xxport 2, 3 & 4
- Page 5 - Target EMC SDRAM
- Page 6 - Pmod / SPIFI Flash / Accelerometer
- Page 7 - LCD display + Cap touch / SD Card slot
- Page 8 - Ethernet PHY
- Page 9 - Audio Codec / DMIC
- Page 10 - Shield Receptacles / Pmod2 / User LEDs
- Page 11 - LPC546xx/LPC540xx current monitor; LINK2 Bridge buffer
- Page 12 - Debug LINK2 LPC4322 Peripherals / debug buffer
- Page 13 - Debug LINK2 LPC4322 / LINK2 USB / Board Power

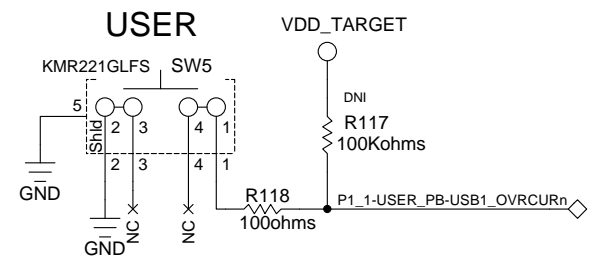
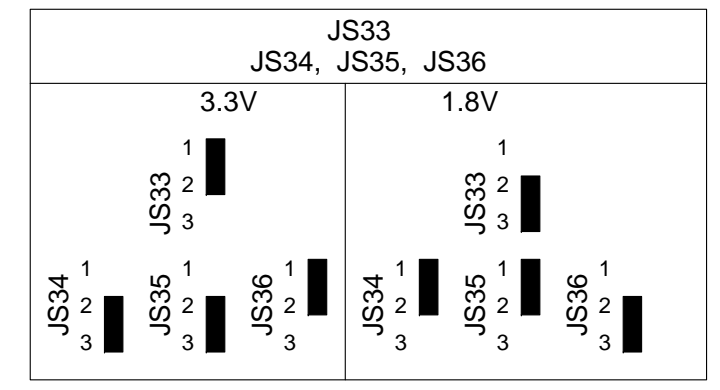
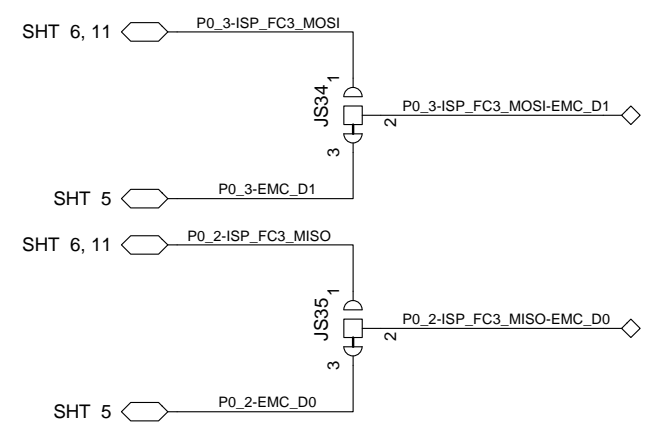
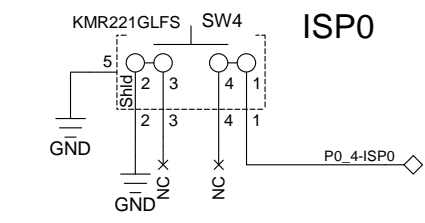
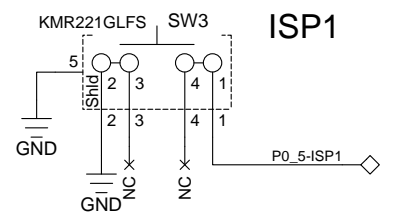
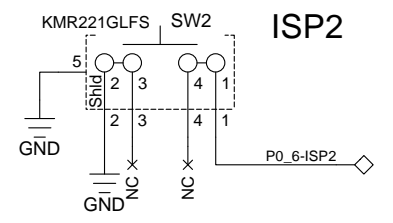
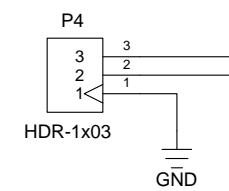
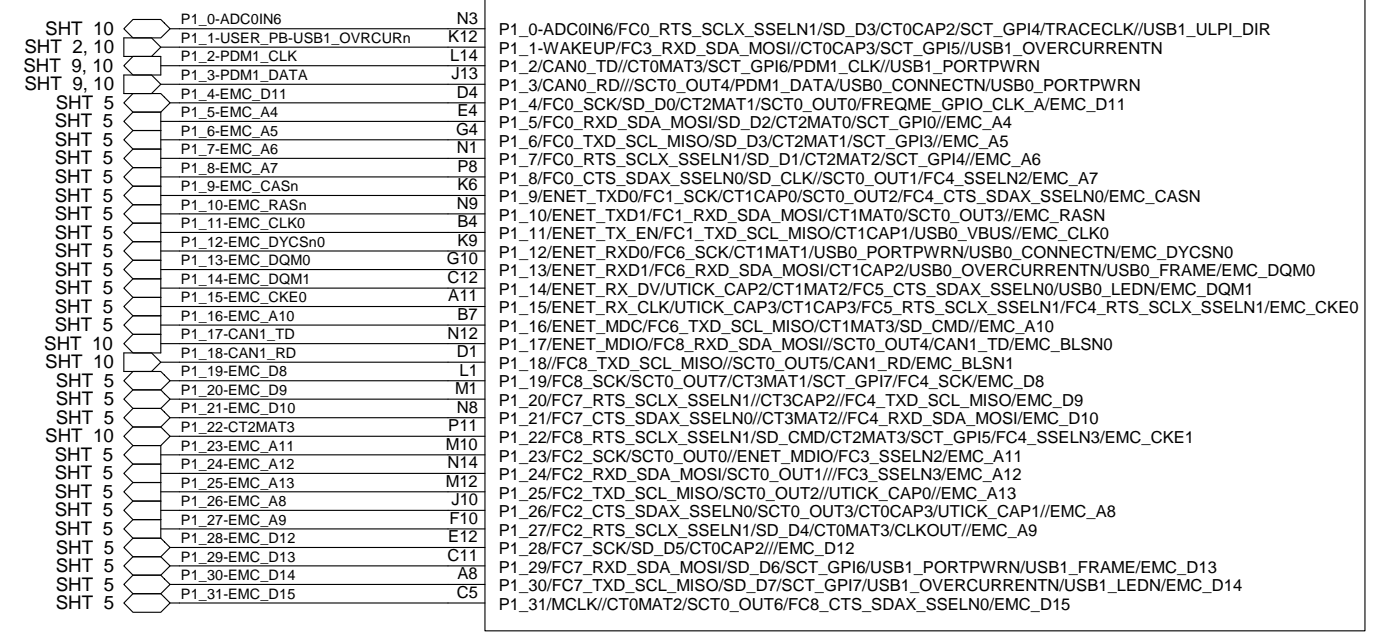
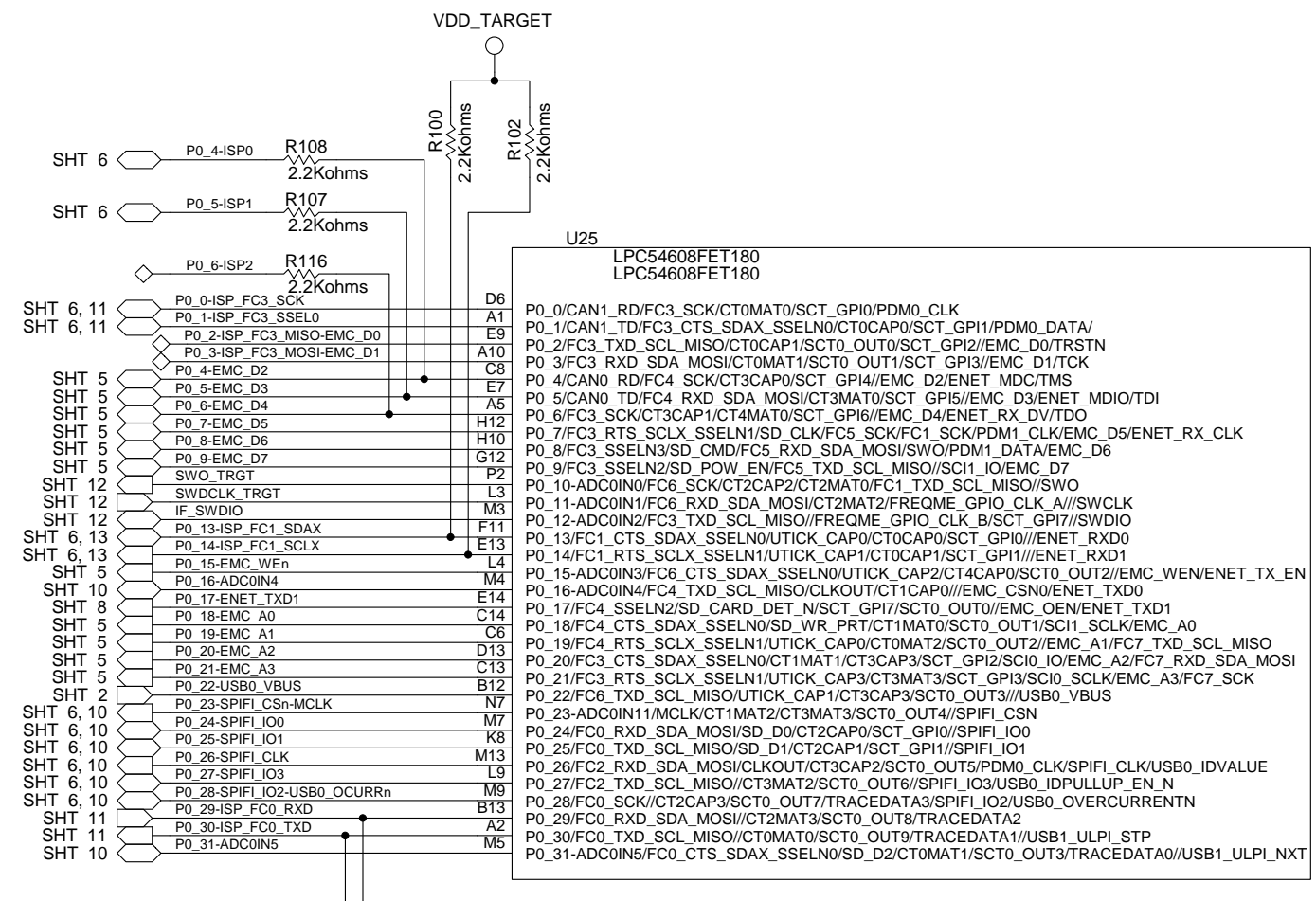
CONTRACT NO.		LPC546xx / LPC540xx	
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	7/8/2018		
CHECKED			
ISSUED	07/08/2018		
SIZE	D	DWG. NO.	LPC546xx / LPC540xx Brd
SCALE		SHEET	1 OF 13

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



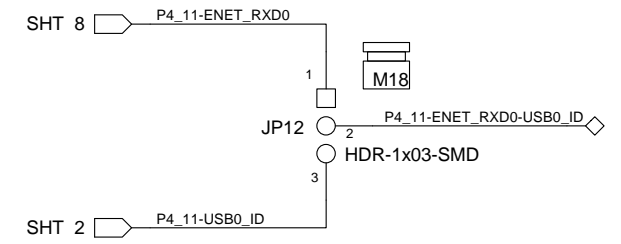
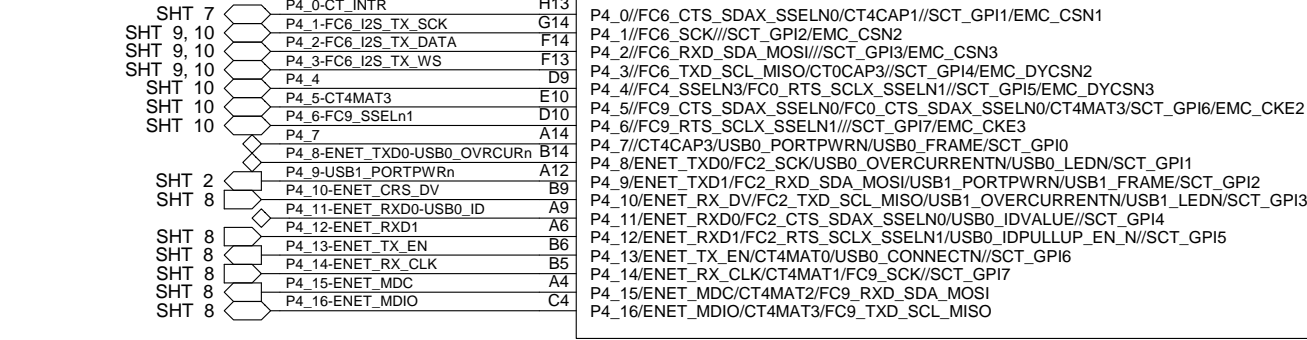
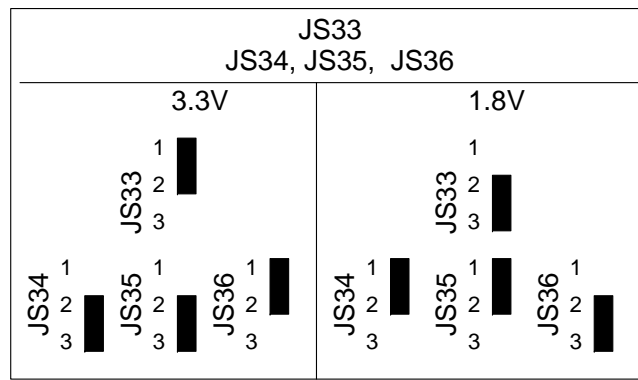
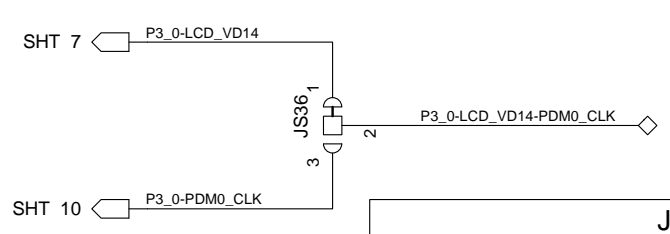
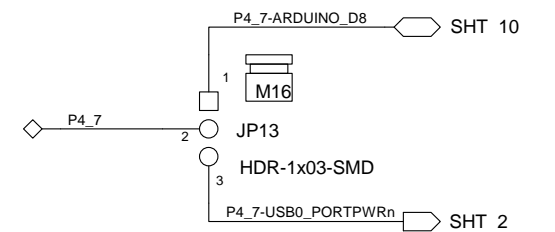
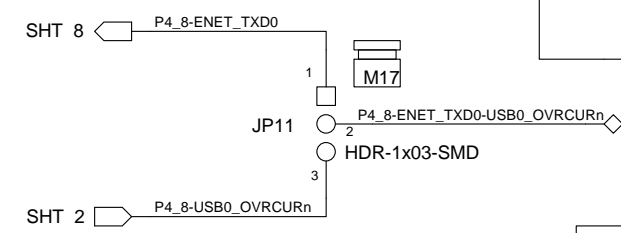
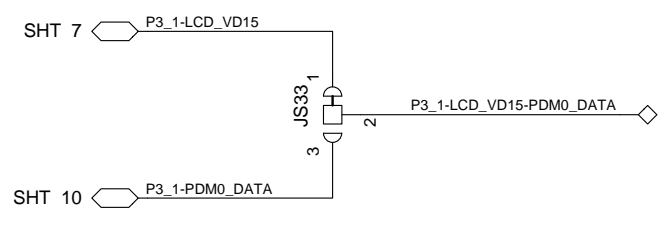
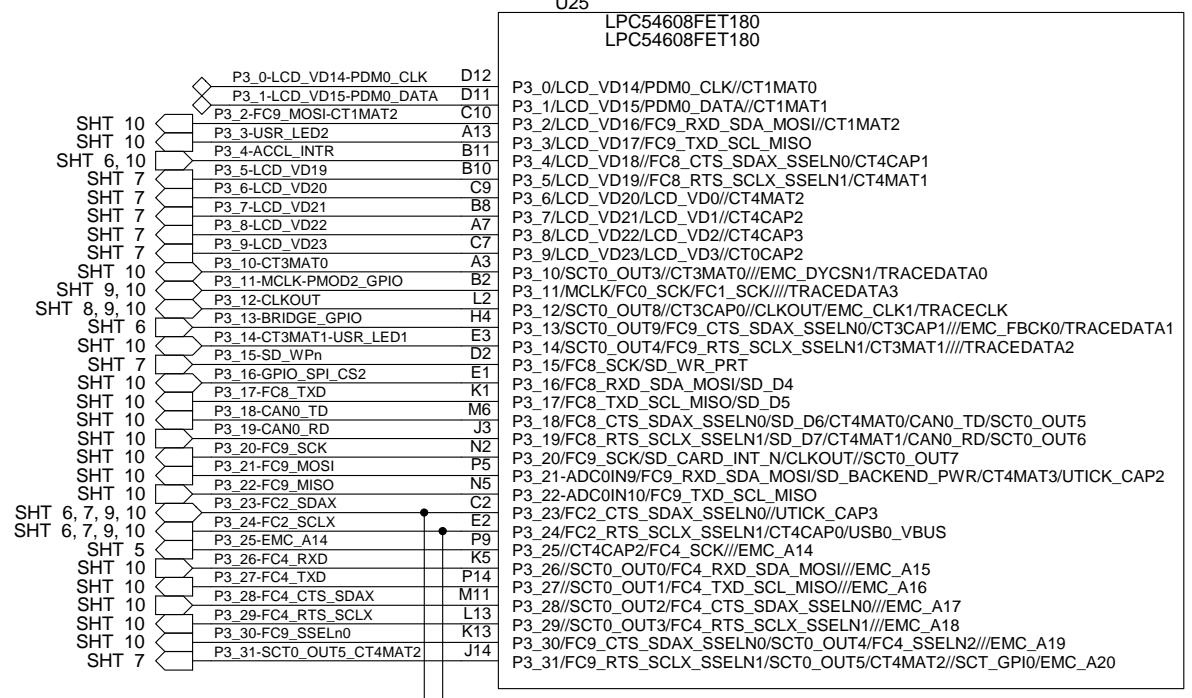
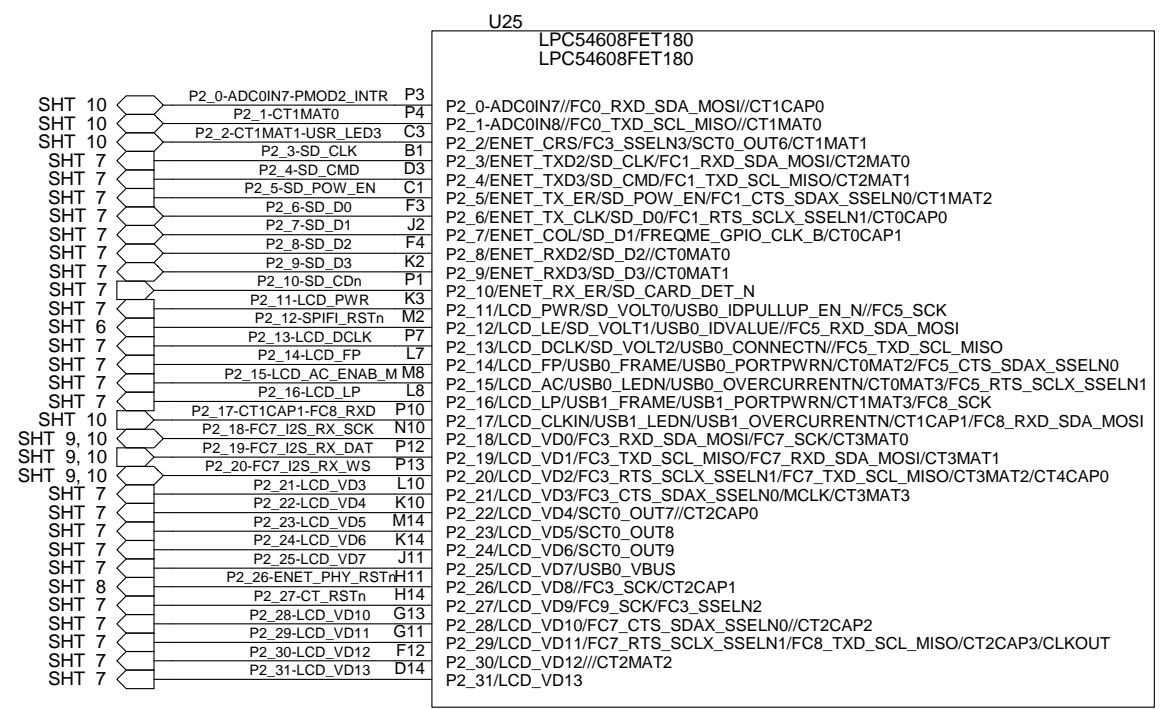
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APPROVALS	DATE	NXP Semiconductors	
DRAWN	d.consiglio	411 E. Plumeria Dr	
CHECKED	7/8/2018	San Jose, CA 95134	
ISSUED	07/08/2018	www.standardics.nxp.com/microcontrollers/	
SIZE	FSCM NO.	DWG. NO.	REV
D		LPC546xx / LPC540xx Brd	F
SCALE		SHEET 2 OF 13	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



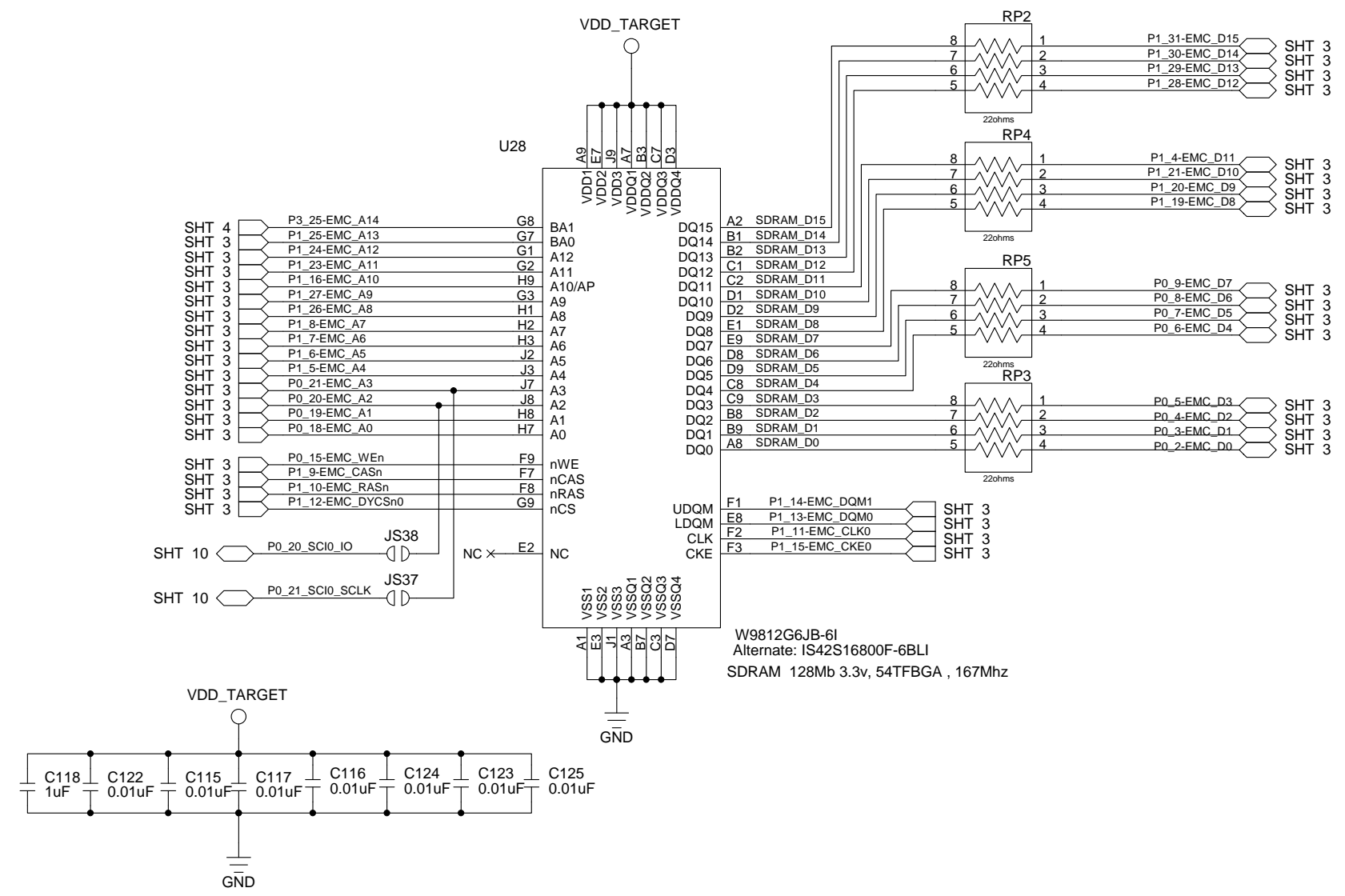
CONTRACT NO.		Target LPC546xx / LPC540xx port0, 1 / Boot select	
APPROVALS	DATE	NXP Semiconductors	
DRAWN d.consiglio	7/8/2018	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED		SIZE D	DWG. NO. LPC546xx / LPC540xx Brd
ISSUED	07/08/2018	SCALE	REV F
		SHEET 3 OF 13	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		Target LPC546xx / LPC540xx port 2, 3 & 4	
APPROVALS	DATE	NXP Semiconductors	
DRAWN d.consiglio	7/8/2018	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED		SIZE	D
ISSUED	07/08/2018	DWG. NO.	LPC546xx / LPC540xx Brd
		REV	F
SCALE		SHEET	4 OF 13

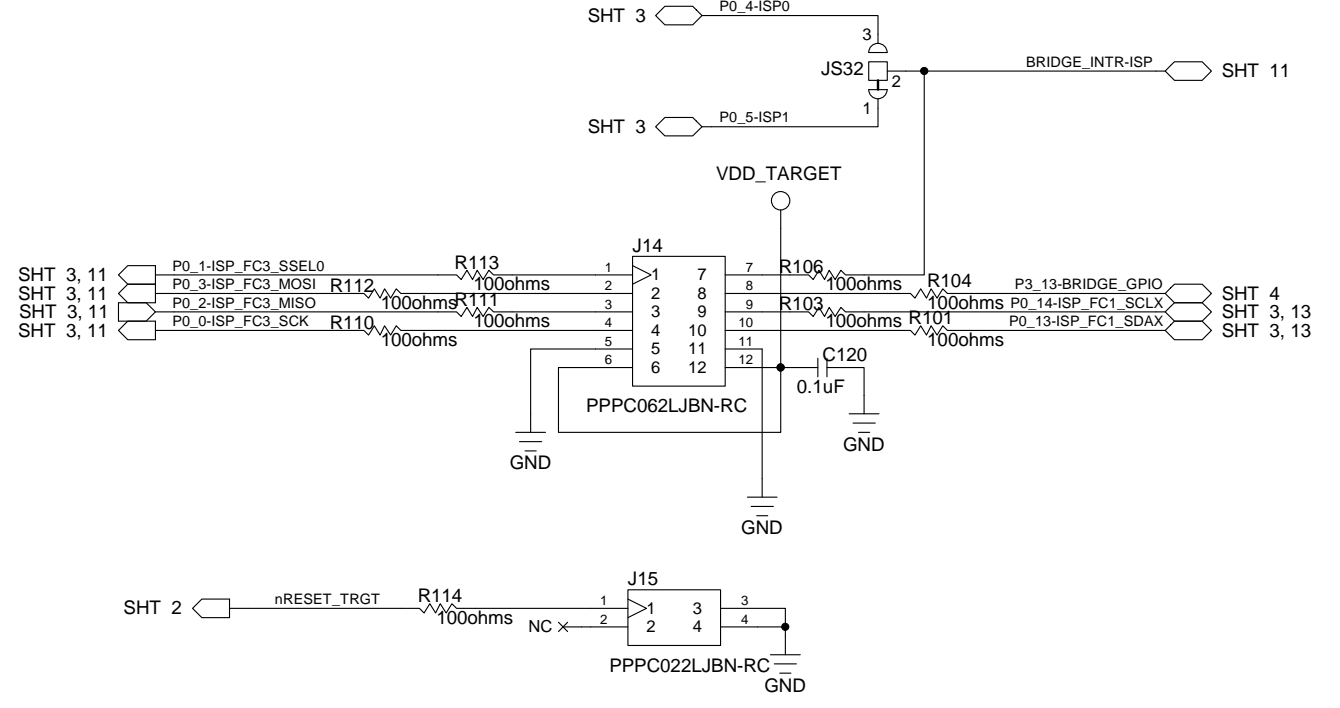
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		Target EMC SDRAM		
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/		
DRAWN	d.consiglio			7/8/2018
CHECKED				
ISSUED	07/08/2018	SIZE	D	
		FSCM NO.		
		DWG. NO.	LPC546xx / LPC540xx Brd	
		REV	F	
		SCALE	SHEET 5 OF 13	

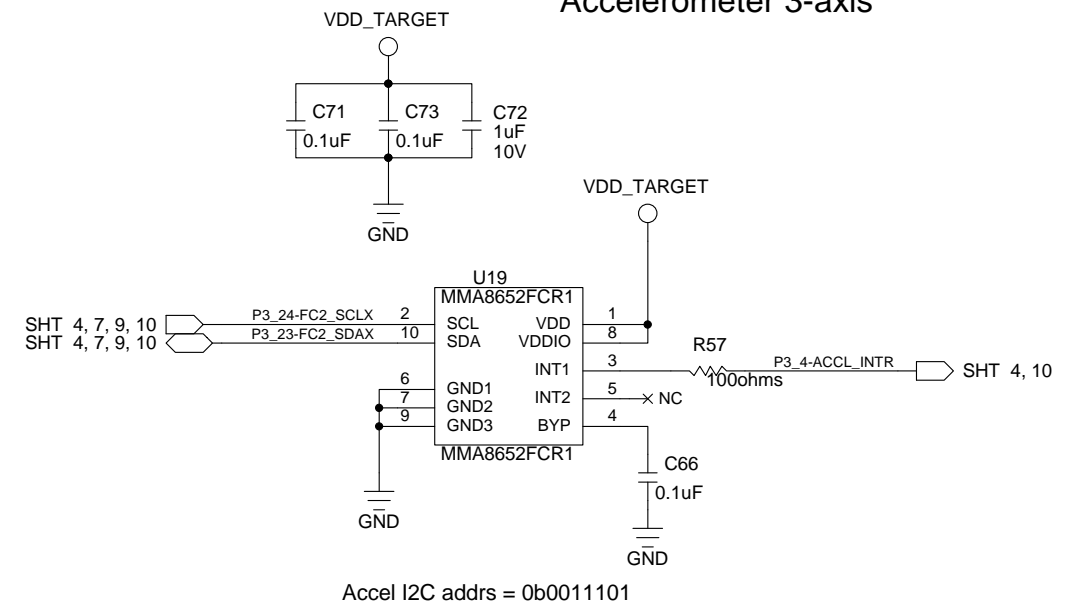
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

SPI / I2C header (PMOD compatible) Host interface



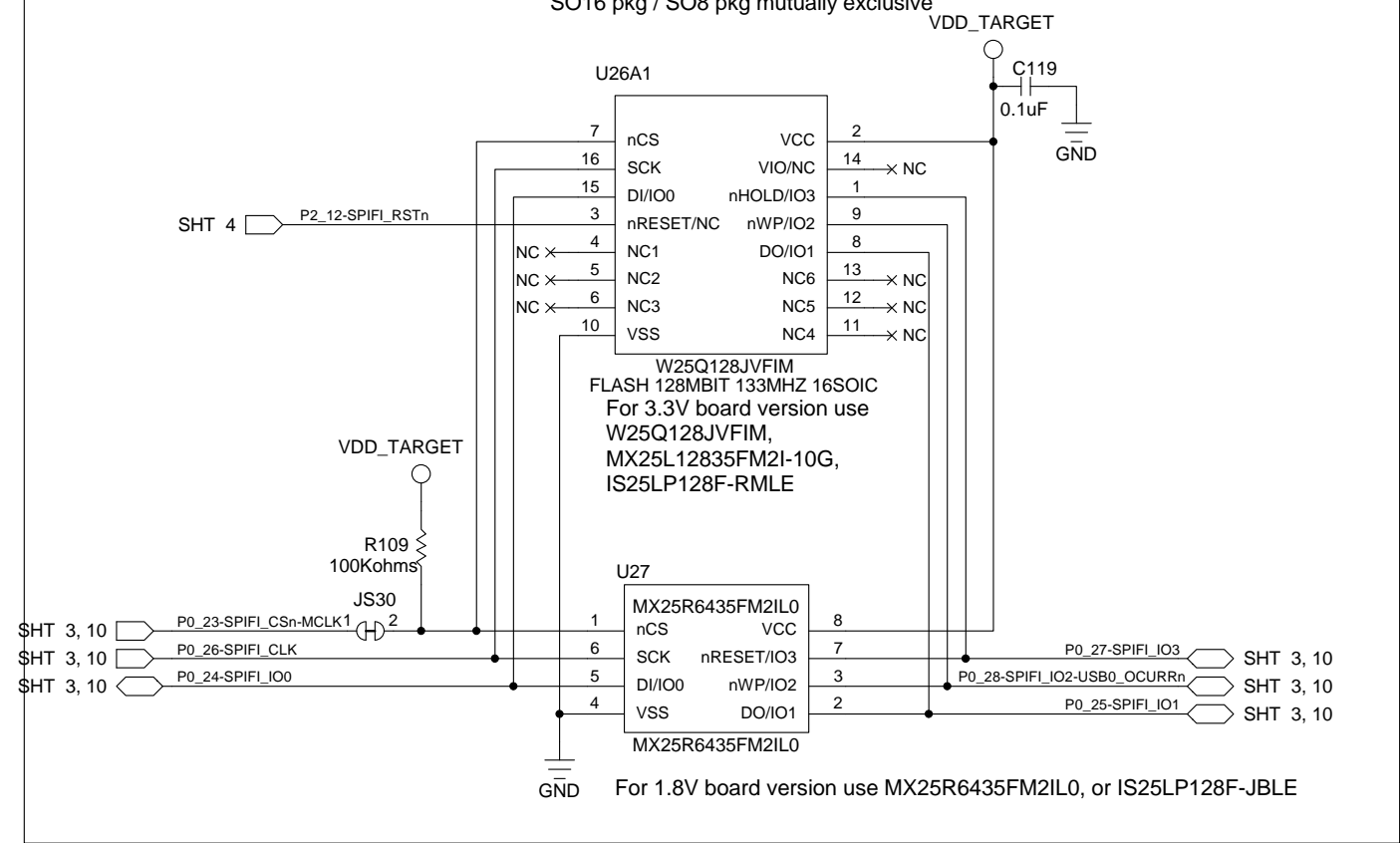
PMOD pin function	LPC546xx/540xx supported function
Pin 1: GPIO/SPI-SSEL(out)/UART-CTS(in)	GPIO/SPI-SSEL(in/out)
Pin 2: GPIO/SPI-MOSI(out)/UART-TXD(out)	GPIO/SPI-MOSI(in/out)
Pin 3: GPIO/SPI-MISO(in)/UART-RXD(in)	GPIO/SPI-MISO(out/in)
Pin 4: GPIO/SPI-SCK(out)/UART-RTS(out)	GPIO/SPI-SCK(in/out)
Pin 5: GND	GND
Pin 6: VCC(3.3V)	VCC(3.3V)
Pin 7: GPIO/INT(in)	GPIO/INT(out/in)
Pin 8: GPIO/RESET(out)	GPIO/RESET(out)
Pin 9: GPIO/SCL	SCL
Pin 10:GPIO/SDA	SDA
Pin 11:GND	GND
Pin 12:VCC(3.3V)	VCC(3.3V)

Accelerometer 3-axis



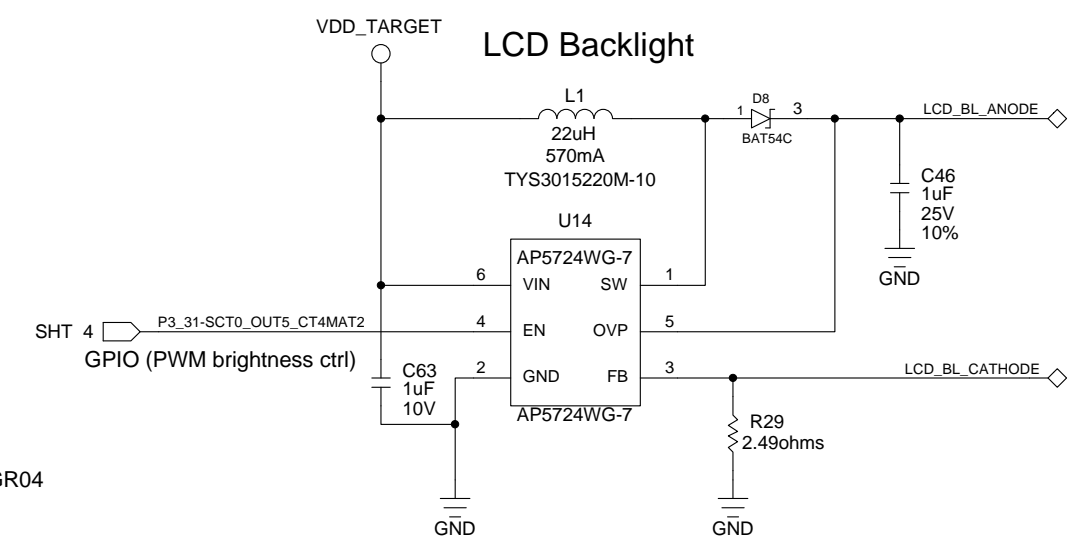
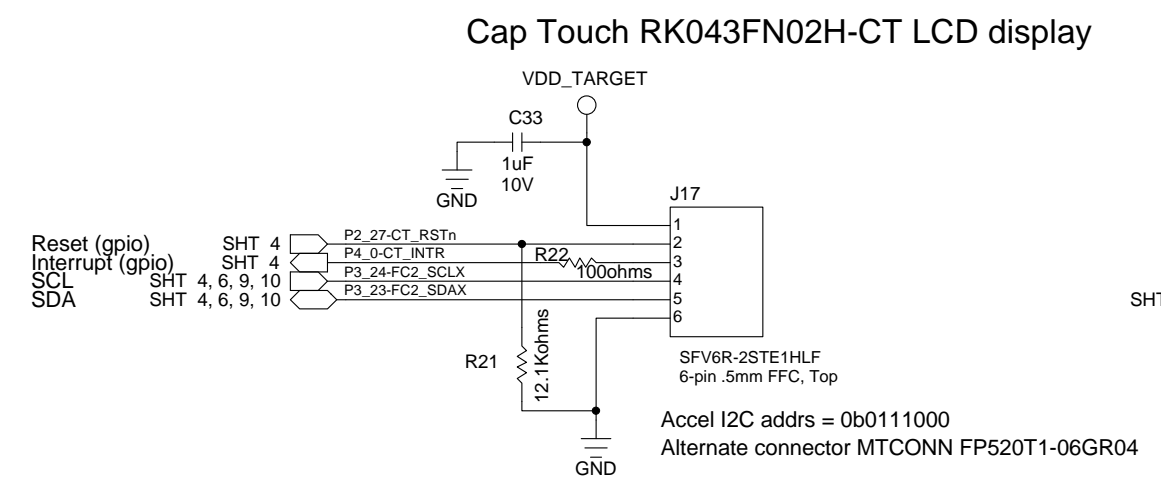
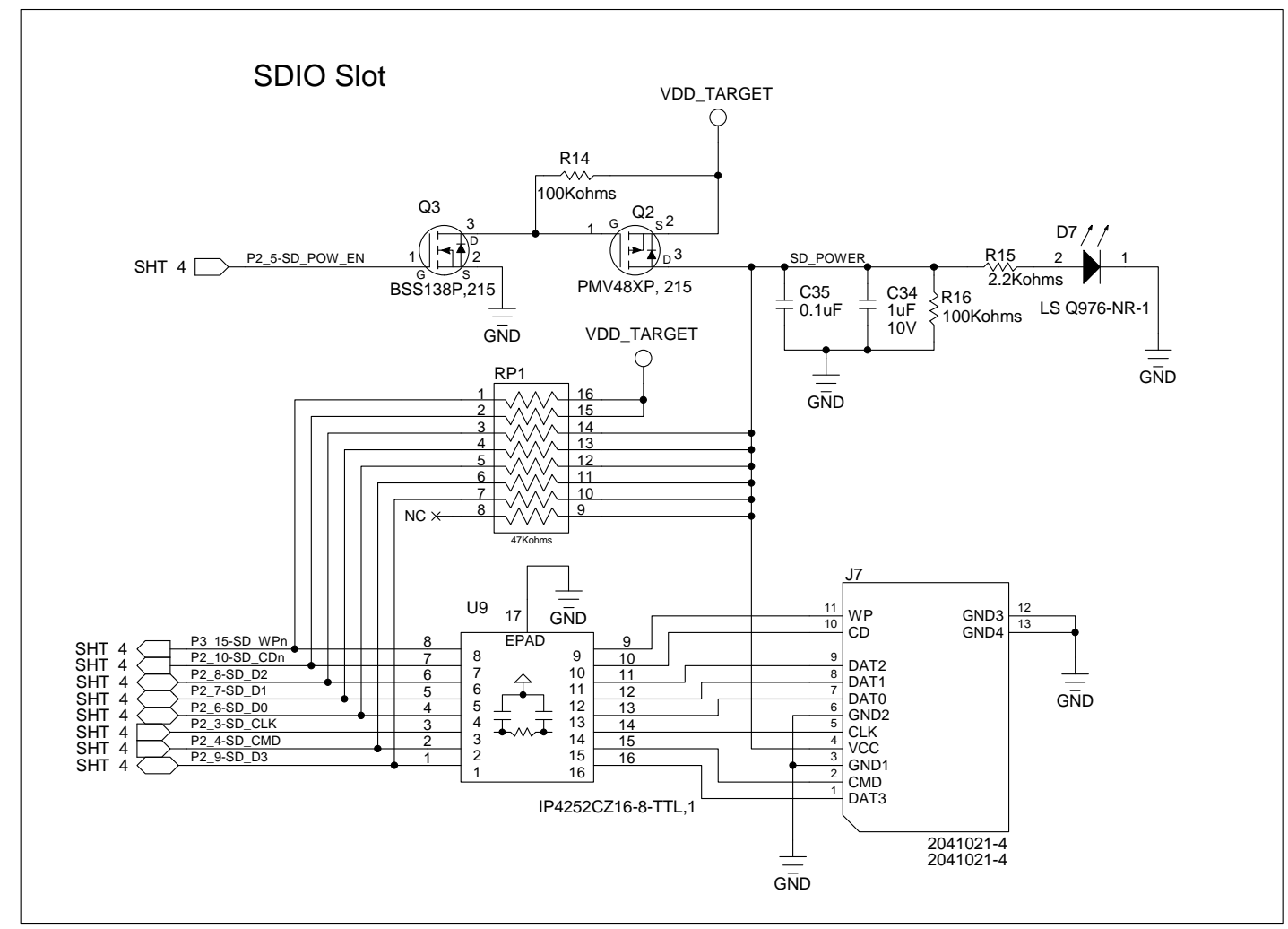
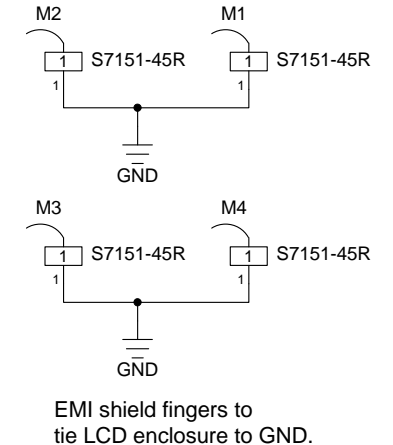
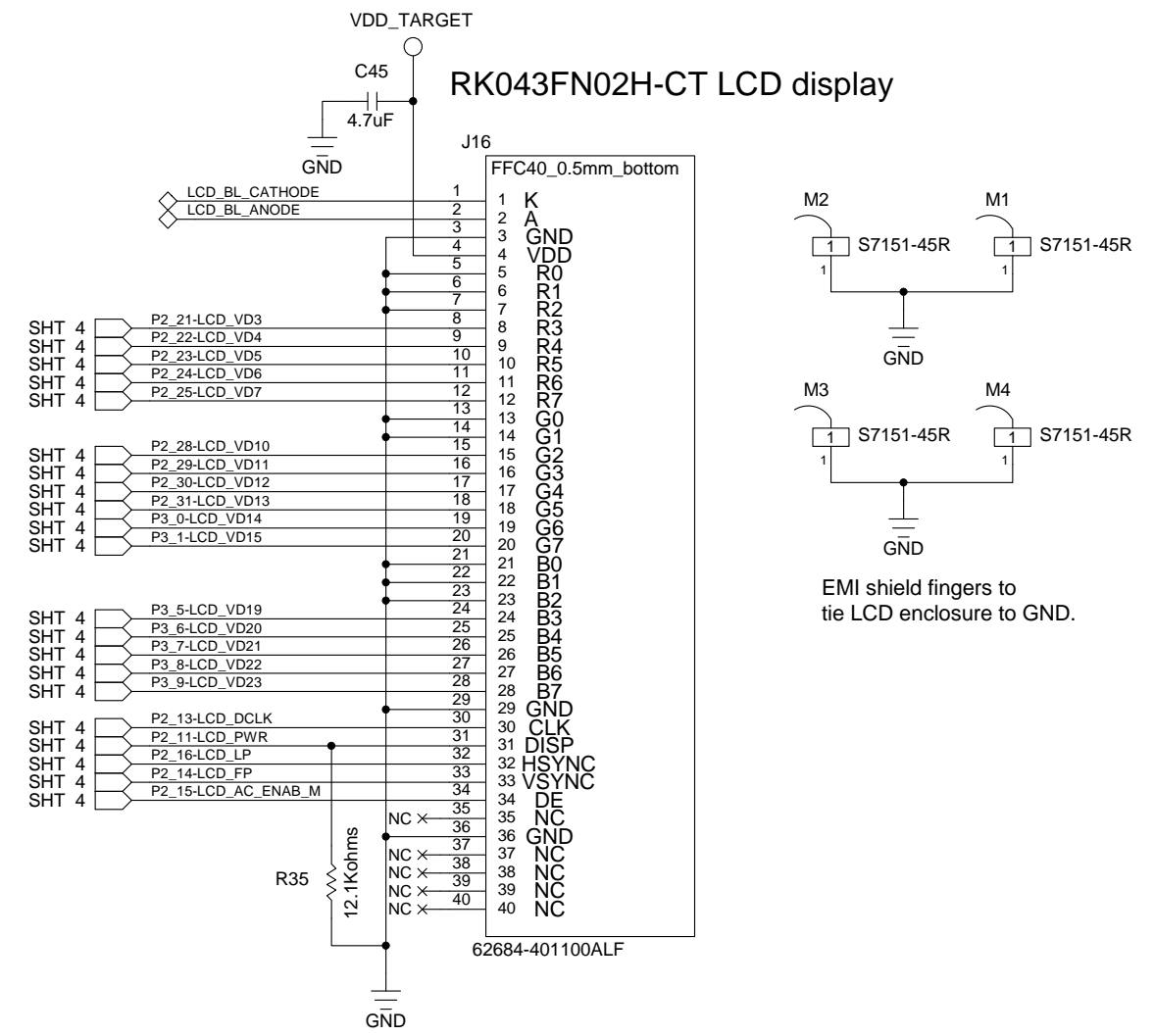
QSPI (SPIFI) NOR Flash

SO16 pkg / SO8 pkg mutually exclusive



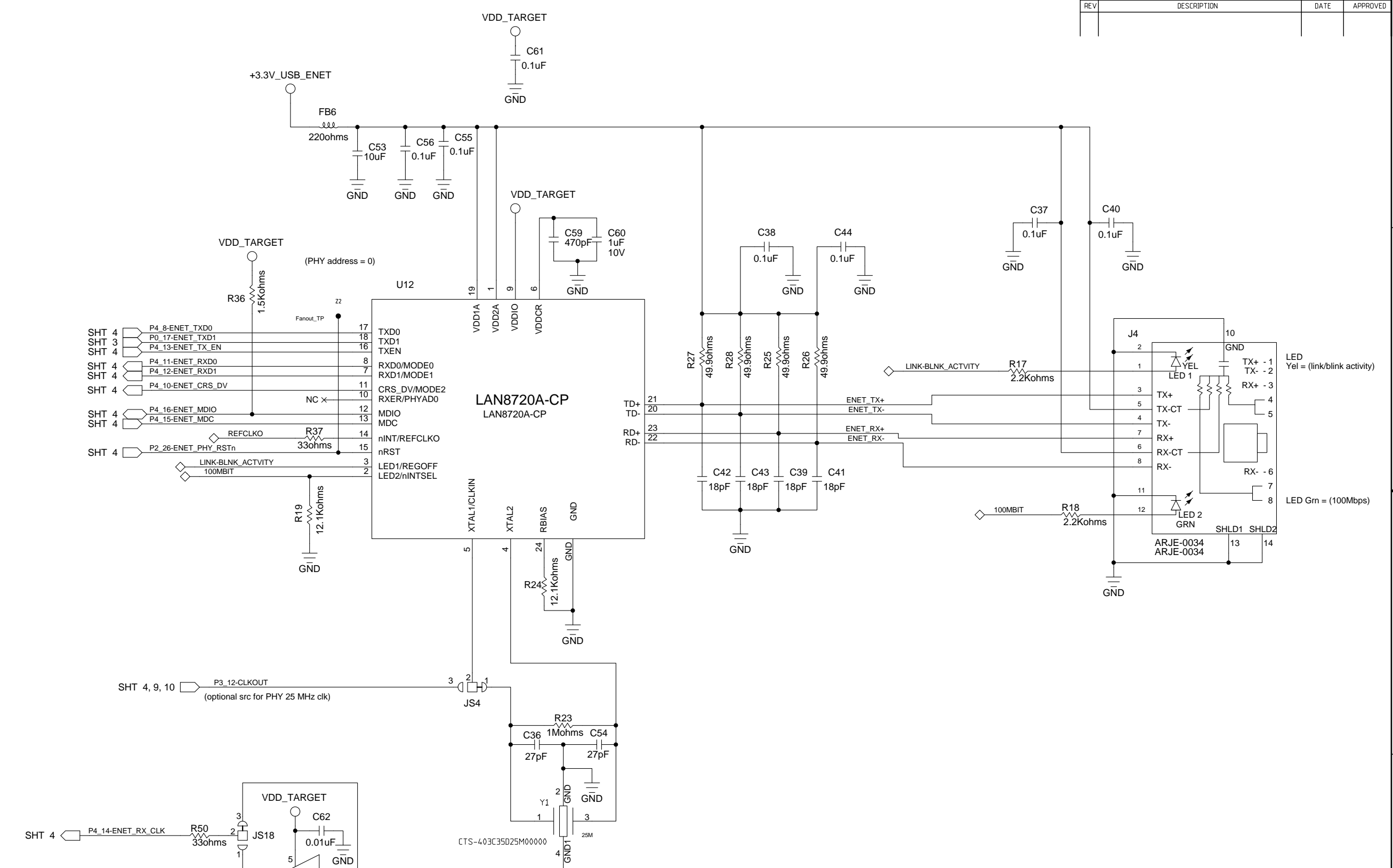
CONTRACT NO.		Pmod / SPIFI Flash / Accelerometer	
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN	d.consiglio		
CHECKED			
ISSUED	07/08/2018		
SCALE		SIZE / FSCM NO.	DWG. NO.
			LPC546xx / LPC540xx Brd
			REV F
		SHEET	6 OF 13

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



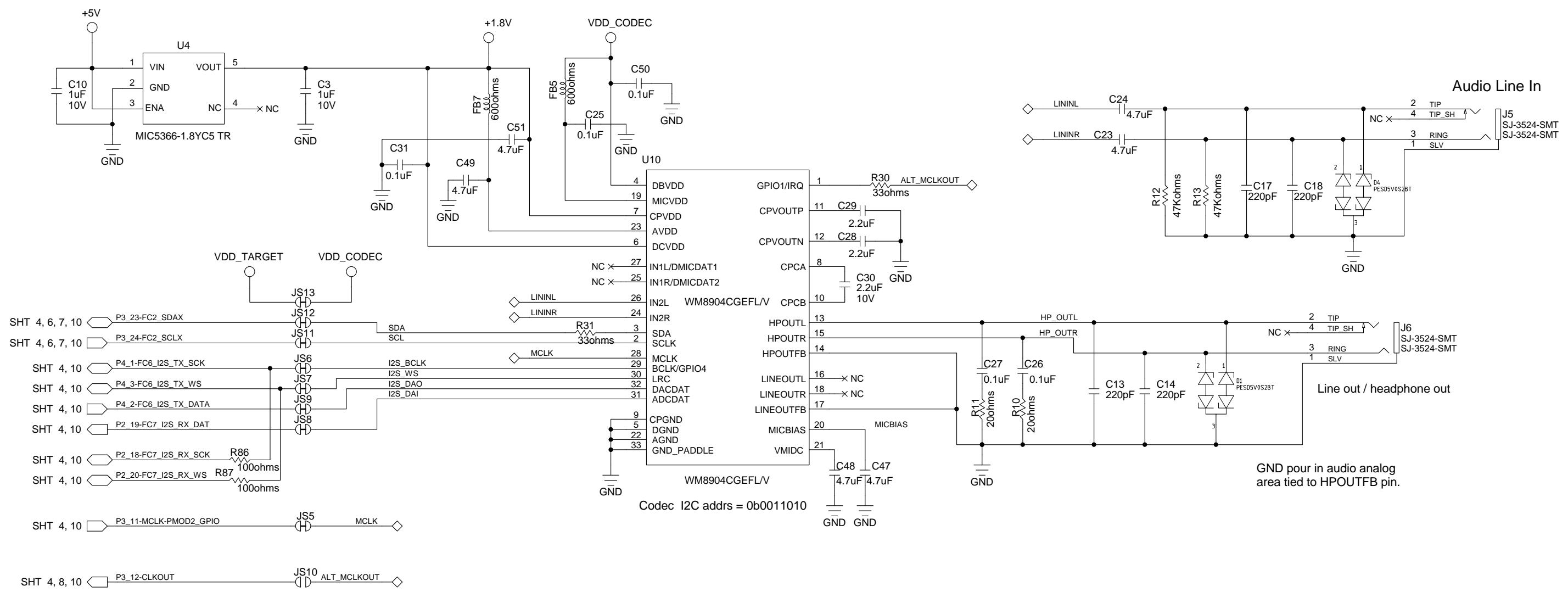
CONTRACT NO.		LCD display + Cap touch / SD Card slot	
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN	7/8/2018		
CHECKED			
ISSUED	07/08/2018	SIZE	D
		DWG. NO.	LPC546xx / LPC540xx Brd
		REV	F
		SCALE	SHEET 7 OF 13

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

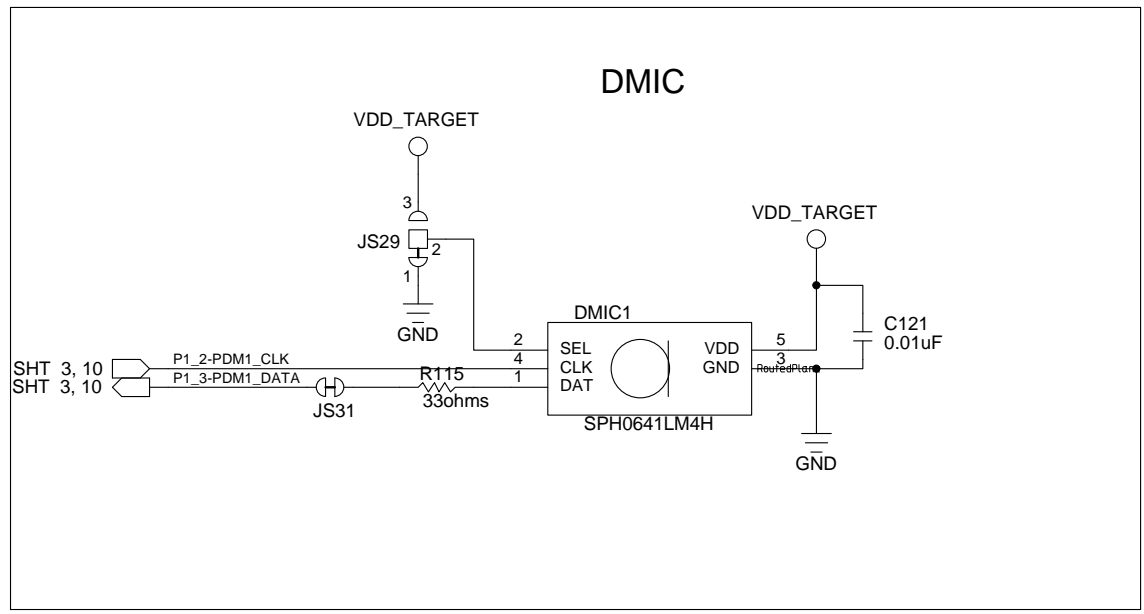


CONTRACT NO.		Ethernet PHY	
APPROVALS	DATE	NXP Semiconductors	
DRAWN	7/8/2018	411 E. Plumeria Dr	
CHECKED		San Jose, CA 95134	
ISSUED	07/08/2018	www.standardics.nxp.com/microcontrollers/	
SIZE	FSCM NO.	DWG. NO.	REV
D		LPC546xx / LPC540xx Brd	F
SCALE		SHEET 8 OF 13	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

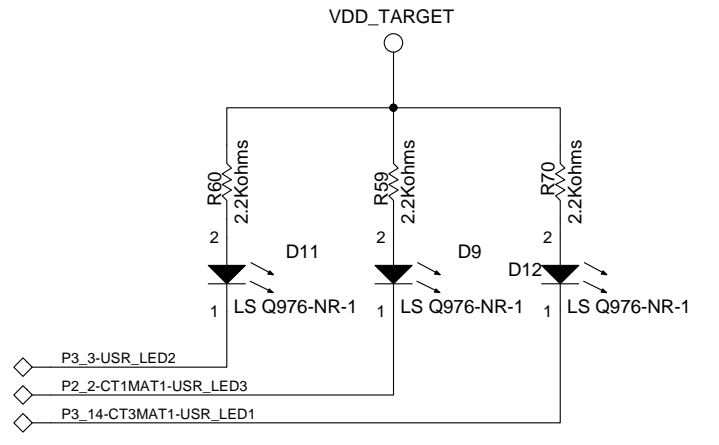
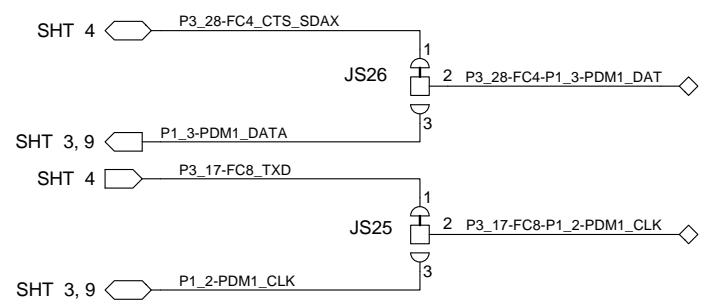
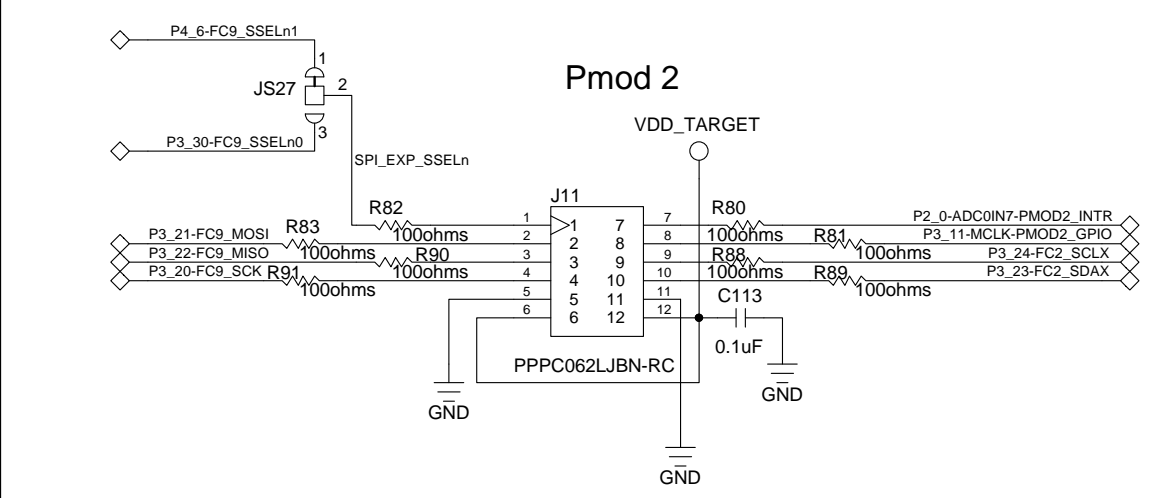
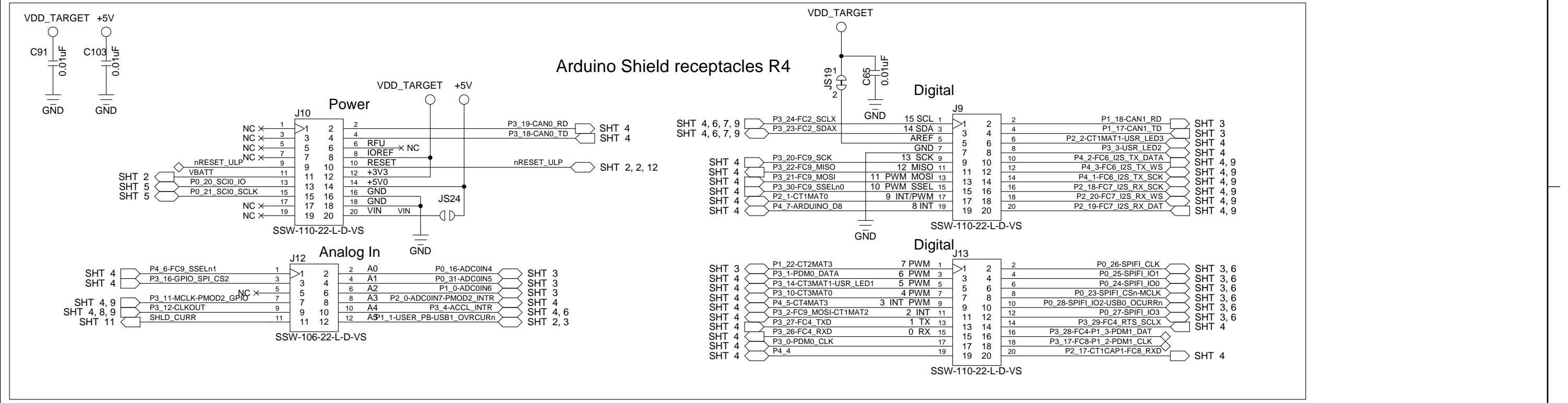


DMIC

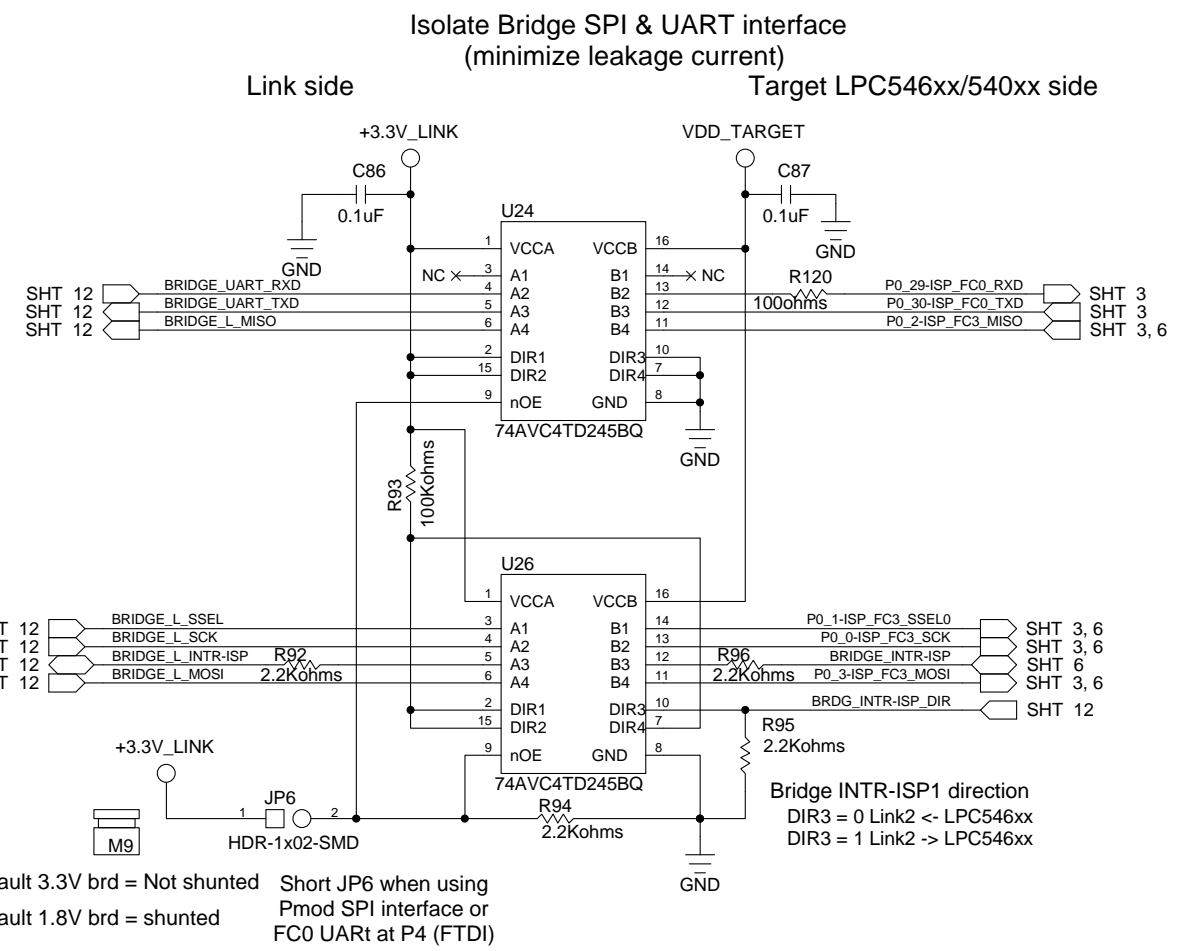


CONTRACT NO.		Audio Codec / DMIC		
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/		
DRAWN	d.consiglio			7/8/2018
CHECKED				
ISSUED	07/08/2018	SIZE / FSCM NO.	DWG. NO.	
			LPC546xx / LPC540xx Brd	
		SCALE	SHEET 9 OF 13	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

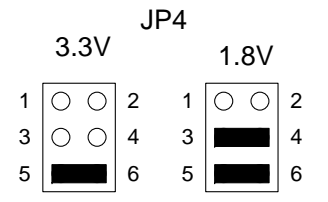


CONTRACT NO.		Shield Receptacles / Pmod2 / User LEDs	
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN	d.consiglio		
CHECKED	7/8/2018		
ISSUED	07/08/2018	SIZE	D
SCALE		DWG. NO.	LPC546xx / LPC540xx Brd
		REV	F
		SHEET 10 OF 13	



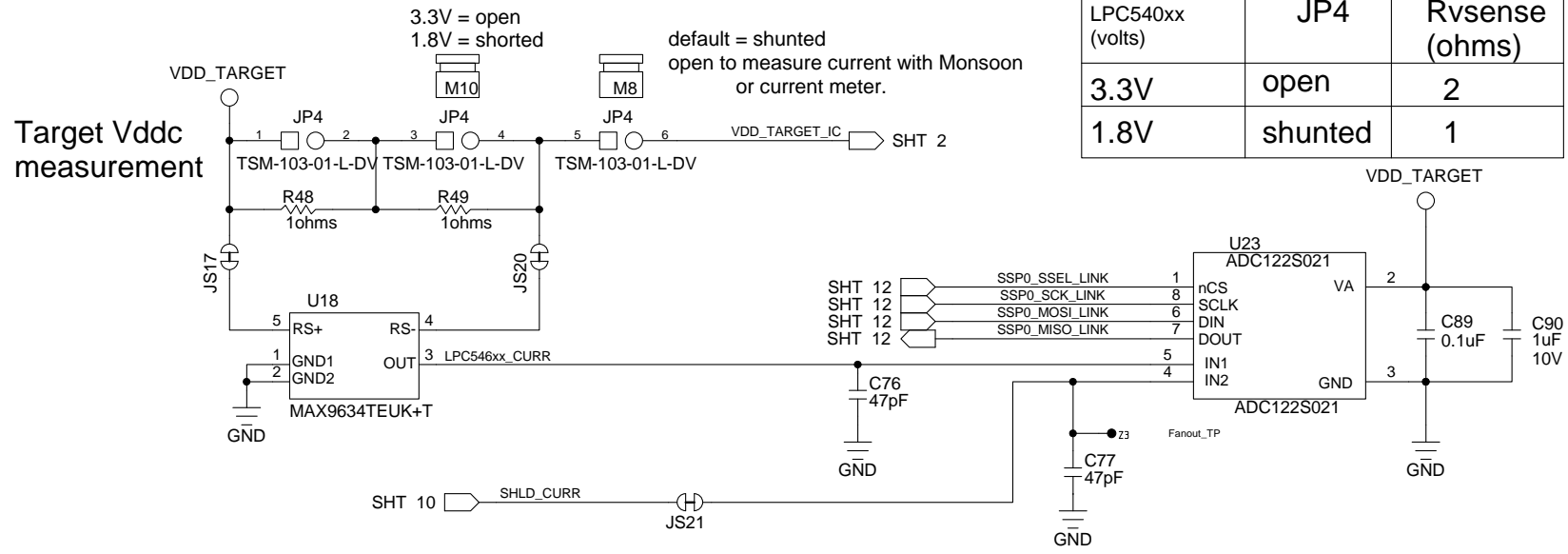
LPC546xx/540xx				
LPC546xx/540xx				ADC111S021 12bit ADC
Vsense (1) voltage 1-lsb	JP4.3/4 open LPC546xx LPC540xx	JP4.3/4 shunted LPC546xx LPC540xx	maximum current	ADC input 1-lsb 800uV
32uV	16uA	32uA	65mA	

(1) Vsense voltage is between U18 RS+ to RS-. Total Rvsense = R48 + (R49 || JP4.5/6).



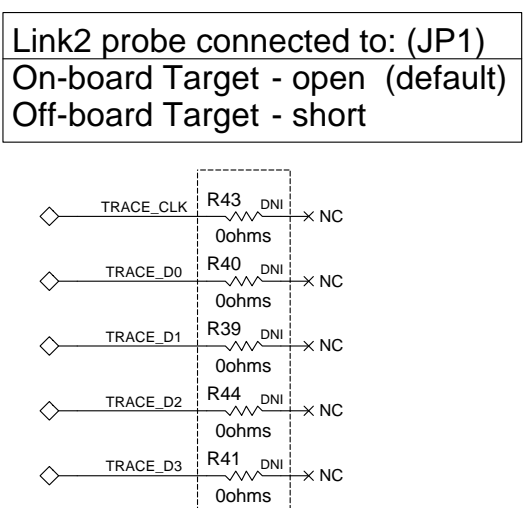
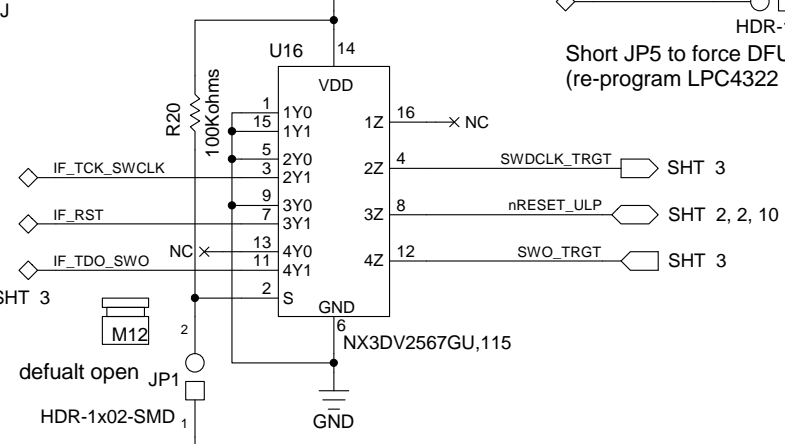
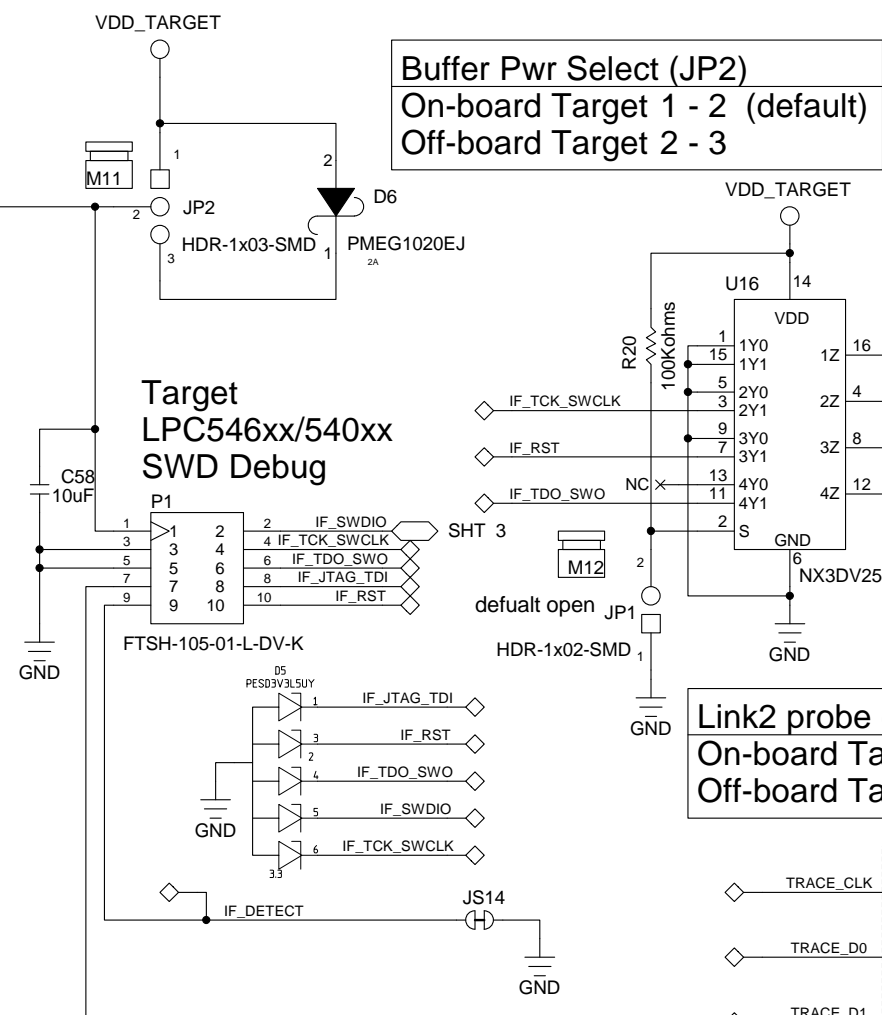
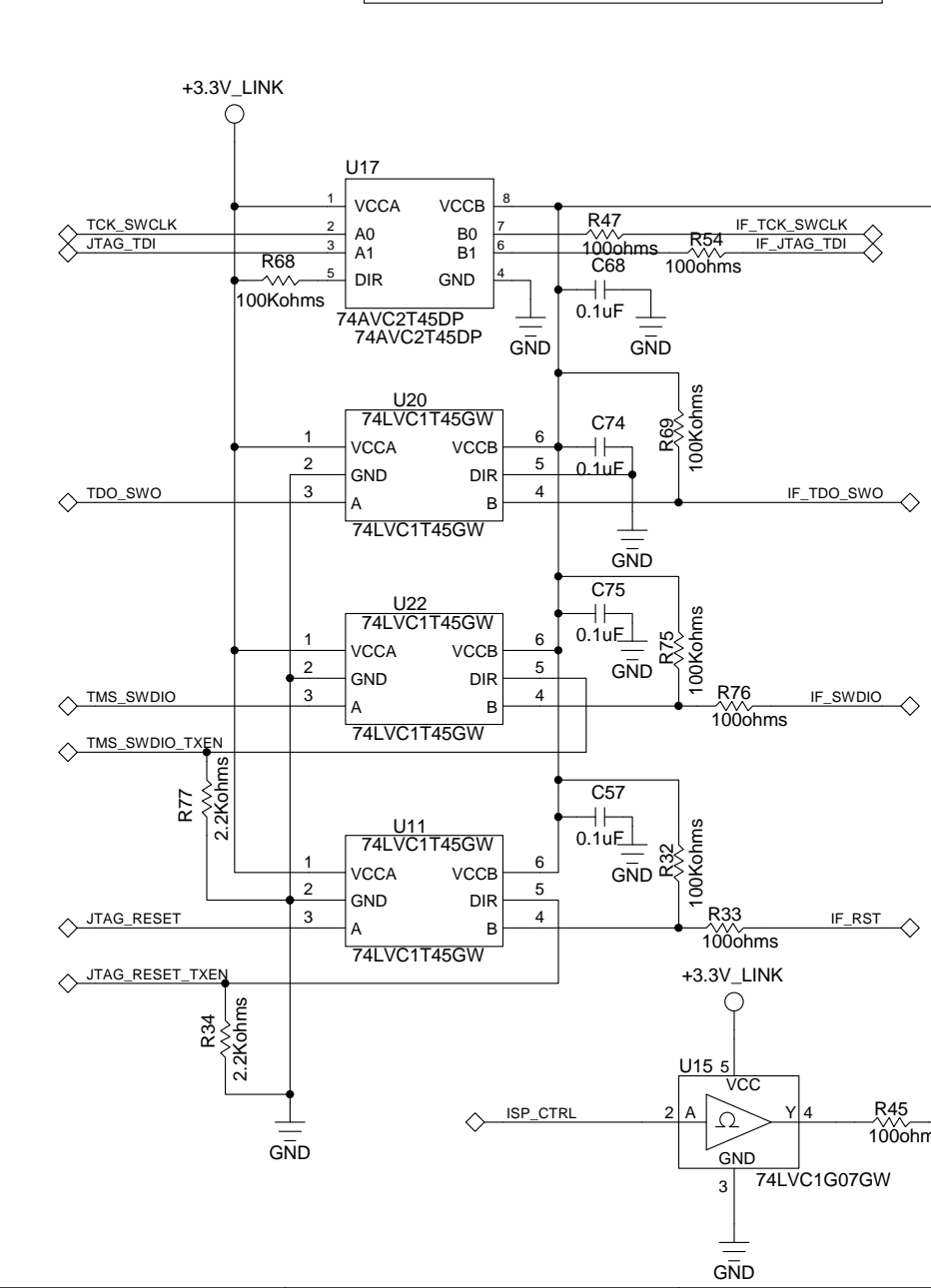
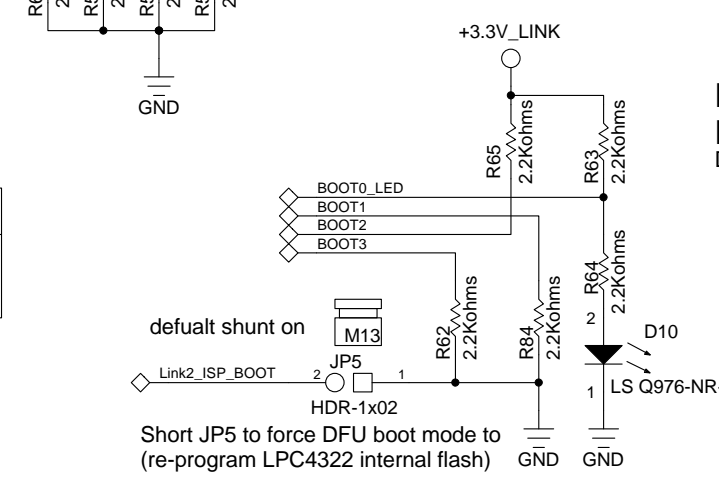
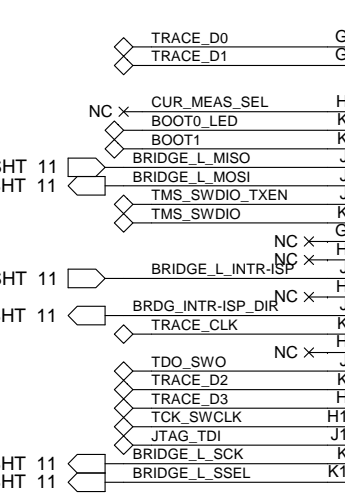
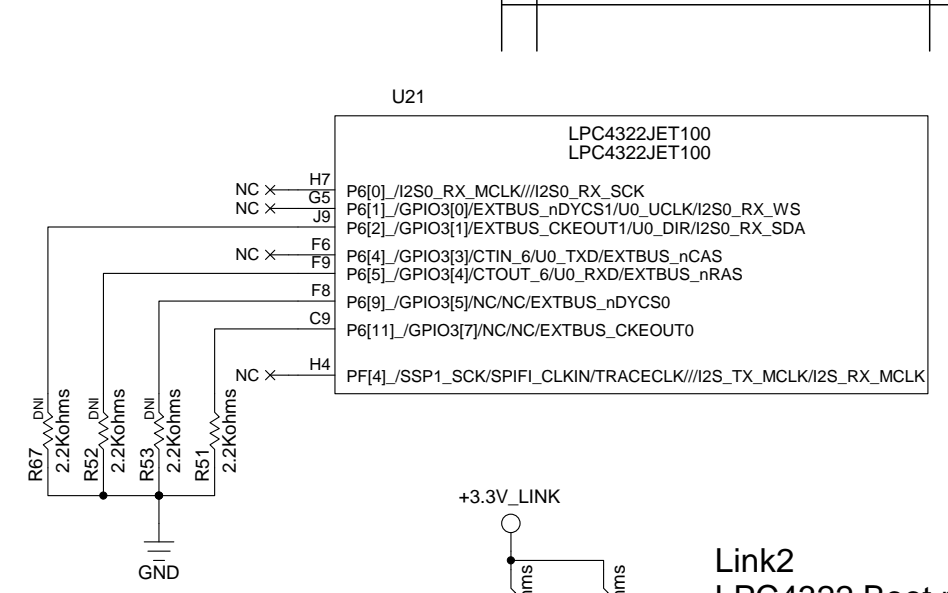
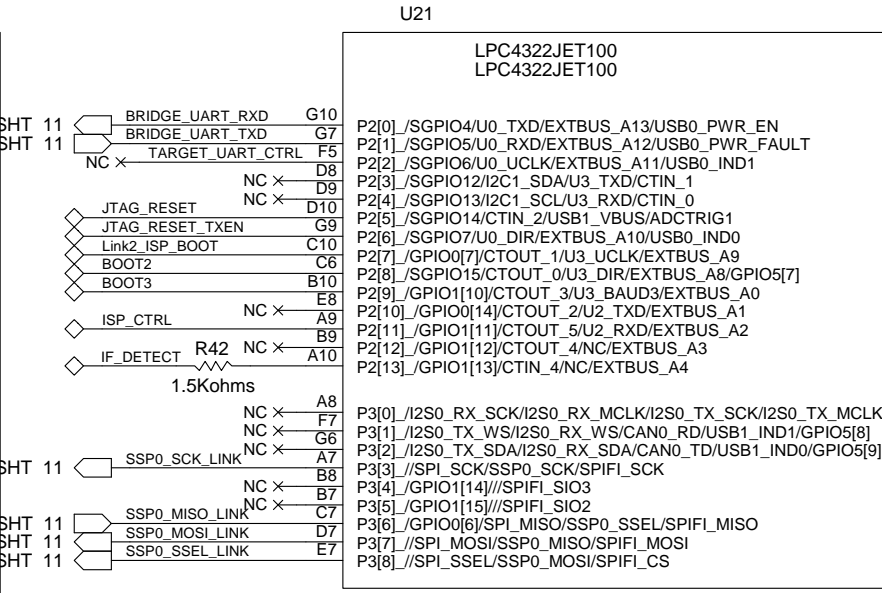
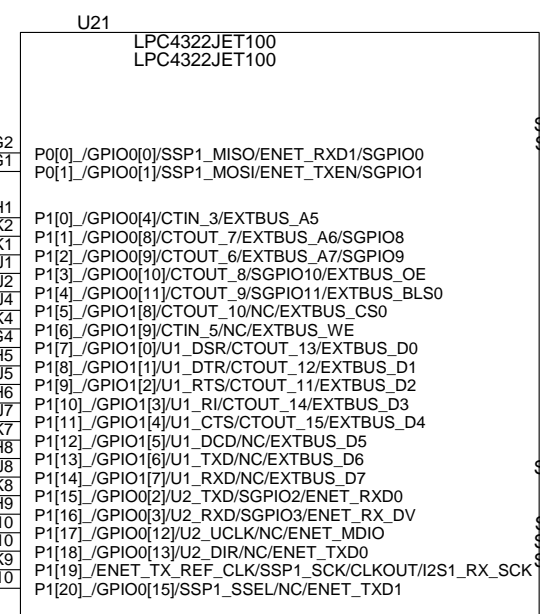
JP4 Setting

VDD LPC546xx LPC540xx (volts)	JP4	Total Rvsense (ohms)
3.3V	open	2
1.8V	shunted	1



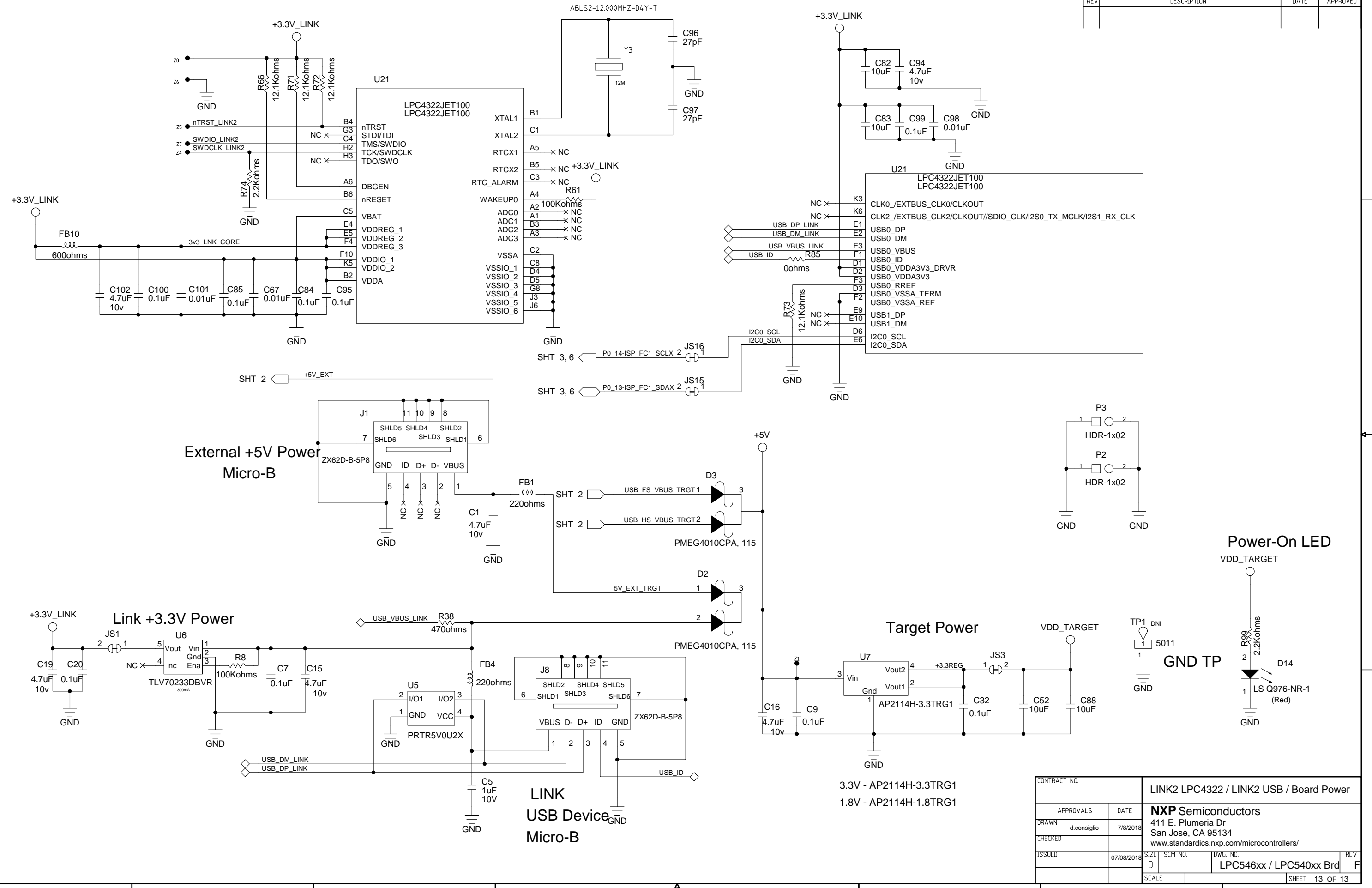
CONTRACT NO.		LPC546xx / LPC540xx current monitor LINK2 Bridge buffer	
APPROVALS	DATE	NXP Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN	d.consiglio	7/8/2018	REV
CHECKED			
ISSUED	07/08/2018	SIZE	D
		DWG. NO.	LPC546xx / LPC540xx Brd
		SCALE	SHEET 11 OF 13

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		LINK2 LPC4322 Peripherals / debug buffer	
APPROVALS	DATE	NXP Semiconductors	
DRAWN d.consiglio	7/8/2018	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED		SIZE	DWG. NO.
ISSUED	07/08/2018	D	LPC546xx / LPC540xx Brd
		SCALE	SHEET 12 OF 13

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



**External +5V Power
Micro-B**

Link +3.3V Power

Target Power

Power-On LED

**LINK
USB Device
Micro-B**

CONTRACT NO.		LINK2 LPC4322 / LINK2 USB / Board Power	
APPROVALS	DATE	NXP Semiconductors	
DRAWN d.consiglio	7/8/2018	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
CHECKED		SIZE	D
ISSUED	07/08/2018	DWG. NO.	LPC546xx / LPC540xx Brd
		REV	F
		SHEET	13 OF 13