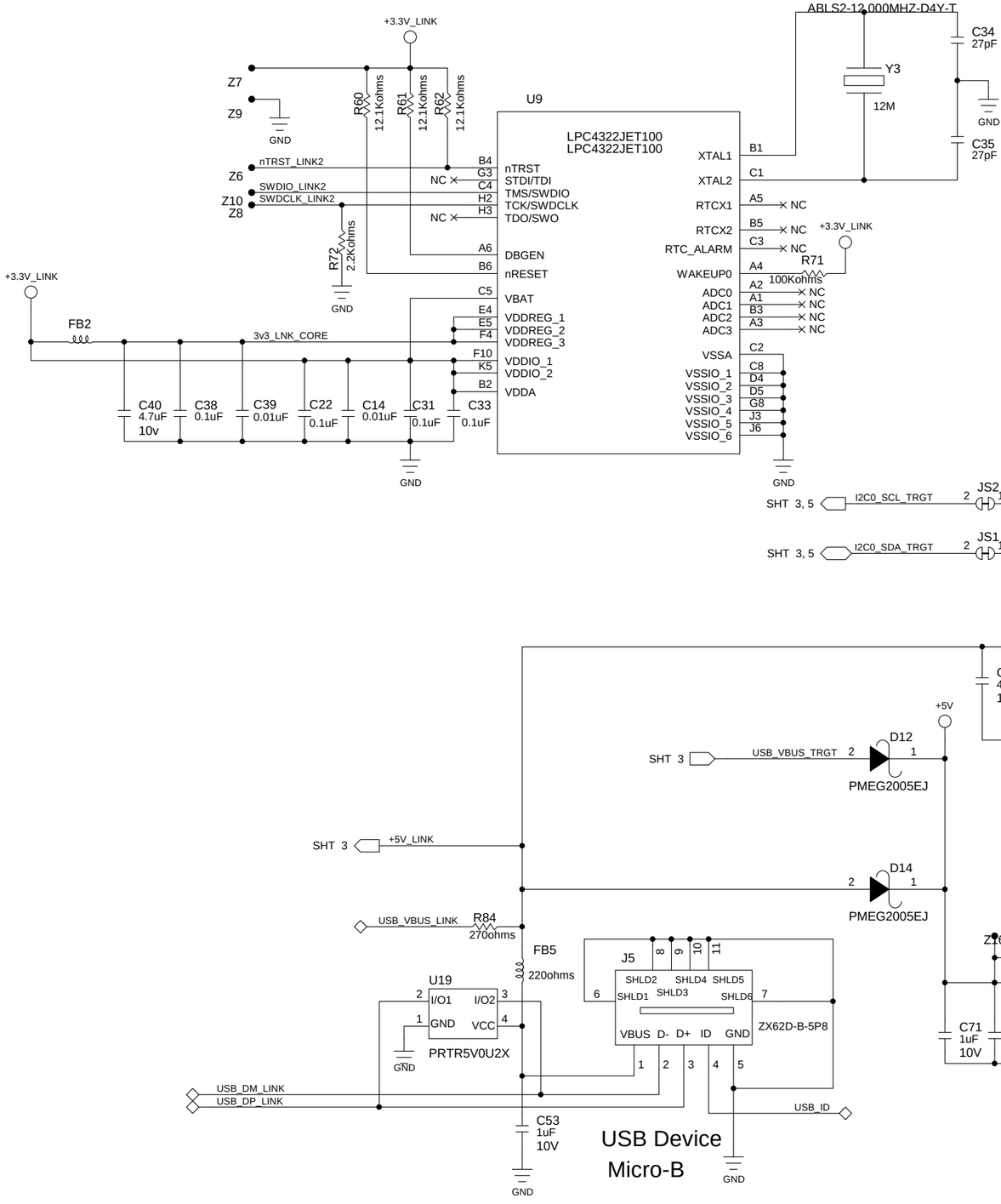
DWG. NO.	SH	REV
LPCXpresso43/18xx v3	1	B

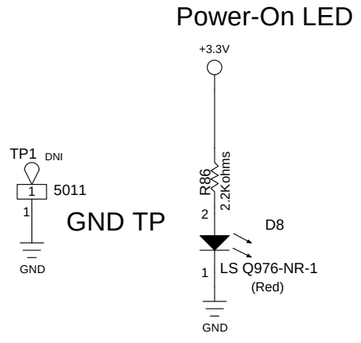
REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	- U4 (A71x) chip SPI_CLK pd to gnd; - add 3-pos JS20 to RESETn; sht 5	12/23/2014	
A1	- change JS16 default to 2-3; sht 6	02/02/2015	
A2	- change JS20 default to 2-3; sht 5	02/03/2015	
A3	- corrected refdes in notes; sht multiple	02/19/2015	
B	- Add hdr JP9 to do Uart ISP Boot; sht 4 - Add hdr JP8 to selcect Uart 0 port; sht 4 - Add VDDR/VDDIO current monitor crkt; sht 8	04/28/2015	

Notes:

1) "DNI" = Do Not Install by default
2) "JSx" solder jumpers use 0ohm resistor for default strapping.





CONTRACT NO.		LINK2 LPC4322 / USB / Power	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	5/1/2015		
CHECKED			
ISSUED	05/01/2015	SIZE D / FSCM NO. / DWG. NO. LPCXpresso43/18xx v3 / REV B	
		SCALE	SHEET 1 OF 08

H=8ND; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

U9
LPC4322JET100
LPC4322JET100

TRACE_D0 G2
TRACE_D1 G1
P0[0]_/GPIO0[0]/SSP1_MISO/ENET_RXD1/SGPIO0
P0[1]_/GPIO0[1]/SSP1_MOSI/ENET_TXEN/SGPIO1

SHT 8 CUR_MEAS_SEL H1
BOOT0_LED K2
BOOT1 K1
SHT 4, 5 P1_1-BOOT0_LED-SSP0_MISO J1
SHT 4, 5 P1_2-BOOT1_TRGT-SSP0_MOSI J2
TMS_SWDIO_TXEN J4
TMS_SWDIO K4
G4
NC H5
NC J5
SHT 4, 5 P6_2-GPIO3_1 H6
NC J7
NC K7
TRACE_CLK H8
NC J8
TDO_SWO K8
TRACE_D2 H9
TRACE_D3 J10
TCK_SWCLK J10
JTAG_TDI K9
SHT 4, 5 P3_0-SSP0_SCK K10
SHT 4, 5 P1_0-SSP0_SSEL
P1[0]_/GPIO0[4]/CTIN_3/EXTBUS_A5
P1[1]_/GPIO0[8]/CTOUT_7/EXTBUS_A6/SGPIO8
P1[2]_/GPIO0[9]/CTOUT_6/EXTBUS_A7/SGPIO9
P1[3]_/GPIO0[10]/CTOUT_8/SGPIO10/EXTBUS_OE
P1[4]_/GPIO0[11]/CTOUT_9/SGPIO11/EXTBUS_BLS0
P1[5]_/GPIO1[8]/CTOUT_10/NC/EXTBUS_CS0
P1[6]_/GPIO1[9]/CTIN_5/NC/EXTBUS_WE
P1[7]_/GPIO1[0]/U1_DSR/CTOUT_13/EXTBUS_D0
P1[8]_/GPIO1[1]/U1_DTR/CTOUT_12/EXTBUS_D1
P1[9]_/GPIO1[2]/U1_RTS/CTOUT_11/EXTBUS_D2
P1[10]_/GPIO1[3]/U1_RI/CTOUT_14/EXTBUS_D3
P1[11]_/GPIO1[4]/U1_CTS/CTOUT_15/EXTBUS_D4
P1[12]_/GPIO1[5]/U1_DCD/NC/EXTBUS_D5
P1[13]_/GPIO1[6]/U1_TXD/NC/EXTBUS_D6
P1[14]_/GPIO1[7]/U1_RXD/NC/EXTBUS_D7
P1[15]_/GPIO0[2]/U2_TXD/SGPIO2/ENET_RXD0
P1[16]_/GPIO0[3]/U2_RXD/SGPIO3/ENET_RX_DV
P1[17]_/GPIO0[12]/U2_UCLK/NC/ENET_MDIO
P1[18]_/GPIO0[13]/U2_DIR/NC/ENET_TXD0
P1[19]_/ENET_TX_REF_CLK/SSP1_SCK/CLKOUT/I2S1_RX_SCK
P1[20]_/GPIO0[15]/SSP1_SSEL/NC/ENET_TXD1

U9
LPC4322JET100
LPC4322JET100

TARGET_UART_RXD G10
TARGET_UART_TXD G7
TARGET_UART_CTRL F5
D8
NC D9
NC D10
JTAG_RESET G9
JTAG_RESET_TXEN C10
Link2_ISP_BOOT C6
BOOT2 B10
BOOT3 E8
NC A9
ISP_CTRL B9
NC A10
IF_DETECT R33 1.5Kohms
A8
NC F7
NC G6
SHT 8 SSP0_SCK_LINK NC A7
B8
NC B7
SHT 8 SSP0_MISO_LINK NC C7
SHT 8 SSP0_MOSI_LINK D7
SHT 8 SSP0_SSEL_LINK E7
P2[0]_/SGPIO4/U0_TXD/EXTBUS_A13/USB0_PWR_EN
P2[1]_/SGPIO5/U0_RXD/EXTBUS_A12/USB0_PWR_FAULT
P2[2]_/SGPIO6/U0_UCLK/EXTBUS_A11/USB0_IND1
P2[3]_/SGPIO12/I2C1_SDA/U3_TXD/CTIN_1
P2[4]_/SGPIO13/I2C1_SCL/U3_RXD/CTIN_0
P2[5]_/SGPIO14/CTIN_2/USB1_VBUS/ADCTRIG1
P2[6]_/SGPIO7/U0_DIR/EXTBUS_A10/USB0_IND0
P2[7]_/GPIO0[7]/CTOUT_1/U3_UCLK/EXTBUS_A9
P2[8]_/SGPIO15/CTOUT_0/U3_DIR/EXTBUS_A8/GPIO5[7]
P2[9]_/GPIO1[10]/CTOUT_3/U3_BAUD3/EXTBUS_A0
P2[10]_/GPIO0[14]/CTOUT_2/U2_TXD/EXTBUS_A1
P2[11]_/GPIO1[11]/CTOUT_5/U2_RXD/EXTBUS_A2
P2[12]_/GPIO1[12]/CTOUT_4/NC/EXTBUS_A3
P2[13]_/GPIO1[13]/CTIN_4/NC/EXTBUS_A4
P3[0]_/I2S0_RX_SCK/I2S0_RX_MCLK/I2S0_TX_SCK/I2S0_TX_MCLK
P3[1]_/I2S0_TX_WS/I2S0_RX_WS/CAN0_RD/USB1_IND1/GPIO5[8]
P3[2]_/I2S0_TX_SDA/I2S0_RX_SDA/CAN0_TD/USB1_IND0/GPIO5[9]
P3[3]_//SPI_SCK/SSP0_SCK/SPIFI_SCK
P3[4]_/GPIO1[14]///SPIFI_SIO3
P3[5]_/GPIO1[15]///SPIFI_SIO2
P3[6]_/GPIO0[6]/SPI_MISO/SSP0_SSEL/SPIFI_MISO
P3[7]_//SPI_MOSI/SSP0_MISO/SPIFI_MOSI
P3[8]_//SPI_SSEL/SSP0_MOSI/SPIFI_CS

U9
LPC4322JET100
LPC4322JET100

NC H7
NC G5
J9
F6
NC F9
F8
C9
H4
P6[0]_/I2S0_RX_MCLK///I2S0_RX_SCK
P6[1]_/GPIO3[0]/EXTBUS_nDYCS1/U0_UCLK/I2S0_RX_WS
P6[2]_/GPIO3[1]/EXTBUS_CKEOUT1/U0_DIR/I2S0_RX_SDA
P6[4]_/GPIO3[3]/CTIN_6/U0_TXD/EXTBUS_nCAS
P6[5]_/GPIO3[4]/CTOUT_6/U0_RXD/EXTBUS_nRAS
P6[9]_/GPIO3[5]/NC/NC/EXTBUS_nDYCS0
P6[11]_/GPIO3[7]/NC/NC/EXTBUS_CKEOUT0
NC
PF[4]_/SSP1_SCK/SPIFI_CLKIN/TRACECLK///I2S_TX_MCLK/I2S_RX_MCLK

R51 2.2Kohms DNI
R49 2.2Kohms DNI
R50 2.2Kohms DNI
R48 2.2Kohms
GND

+3.3V_LINK
R59 2.2Kohms
R46 2.2Kohms
BOOT0_LED
BOOT1
BOOT2
BOOT3
R57 2.2Kohms
R78 2.2Kohms
R47 2.2Kohms
defualt shunt on
M3
Link2_ISP_BOOT
JP6
HDR-1x02
D5
LS Q976-NR-1
GND
GND

Short JP6 to force DFU boot mode to
(re-program LPC4322 internal flash)

Link2
LPC4322 Boot mode
DFU USB0 = B3:0 = 0101

+3.3V_LINK
U6
TCK_SWCLK
JTAG_TDI
VCCA VCCB
A0 B0
A1 B1
DIR GND
SN74AVC2T45DCTR
SN74AVC2T45DCTR
R53 100Kohms
R36 100ohms
R52 100ohms
C10 0.1uF
IF_TCK_SWCLK
IF_JTAG_TDI
IF_JTAG_TDI
SHT 3
GND
GND

+3.3V
M1
JP1
HDR-1x03
D3
PMEG1020EJ
2A

Buffer Pwr Select (JP1)
On-board Target 1 - 2 (default)
Off-board Target 2 - 3

U10
74LVC1T45GW
C15 0.1uF
R65 100Kohms
TDO_SWO
IF_TDO_SWO
GND
GND

U11
74LVC1T45GW
C23 0.1uF
R66 100Kohms
TMS_SWDIO
TMS_SWDIO_TXEN
R67 100ohms
IF_TMS_SWDIO
R73 2.2Kohms

U1
74LVC1T45GW
C1 0.1uF
R4 100Kohms
JTAG_RESET
JTAG_RESET_TXEN
R5 100ohms
IF_RST
R18 2.2Kohms
GND

+3.3V_LINK
U2
VCC
ISP_CTRL
A Y
GND
74LVC1G07GW
R17 100ohms
IF_ISPEN
GND

Target (LPC433x)
SWD Debug

C5 10uF
P1
IF_TMS_SWDIO
IF_TCK_SWCLK
IF_TDO_SWO
IF_JTAG_TDI
IF_RST
SHT 3
FTSH-105-01-L-DV-K
GND

D2
PESD3V3L5UK
IF_JTAG_TDI
IF_RST
IF_TDO_SWO
IF_TMS_SWDIO
IF_TCK_SWCLK
3.3
GND

IF_DETECT
JS6
GND

+3.3V
U3
VDD
R29 100Kohms
IF_TCK_SWCLK
IF_RST
IF_TDO_SWO
1Y0 1Z NC
1Y1
2Y0 2Z TCK-SWDCLK_TRGT SHT 3
2Y1
3Y0 3Z nRESET_TRGT SHT 3, 5, 6, 7
3Y1
NC 4Y0 4Z TDO-SWO_TRGT SHT 3
4Y1
S GND
NX3DV2567GU,115
M2
defualt open JP2
HDR-1x02
GND

Link2 probe connected to: (JP2)
On-board Target - open (default)
Off-board Target - short

+3.3V
U14
VDD
SEL
TARGET_UART_CTRL
SHT 7 P2_1-ISP_U0_RX_FTDI Y0 Z P2_1-ISP_U0_RX SHT 4
TARGET_UART_RXD Y1
GND
R74 2.2Kohms
74LVC1G3157GW
GND

TRACE_CLK R34 DNI 0ohms NC
TRACE_D0 R31 DNI 0ohms NC
TRACE_D1 R30 DNI 0ohms NC
TRACE_D2 R35 DNI 0ohms NC
TRACE_D3 R32 DNI 0ohms NC

LPC433xJET100 Target
does not have parallel trace.

TARGET_UART_TXD R63 100ohms U0_TX SHT 4, 7
IF_ISPEN R19 0ohms P2_7-ISP_EN-T3_MAT3-GREEN SHT 3, 4

CONTRACT NO.		LINK2 LPC4322 Peripherals / debug buffer	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	5/1/2015		
CHECKED			
ISSUED	05/01/2015	SIZE D / FSCM NO. / DWG. NO. LPCXpresso43/18xx v3 / REV B	
		SCALE	SHEET 2 OF 08

H:8N0; V:4LA

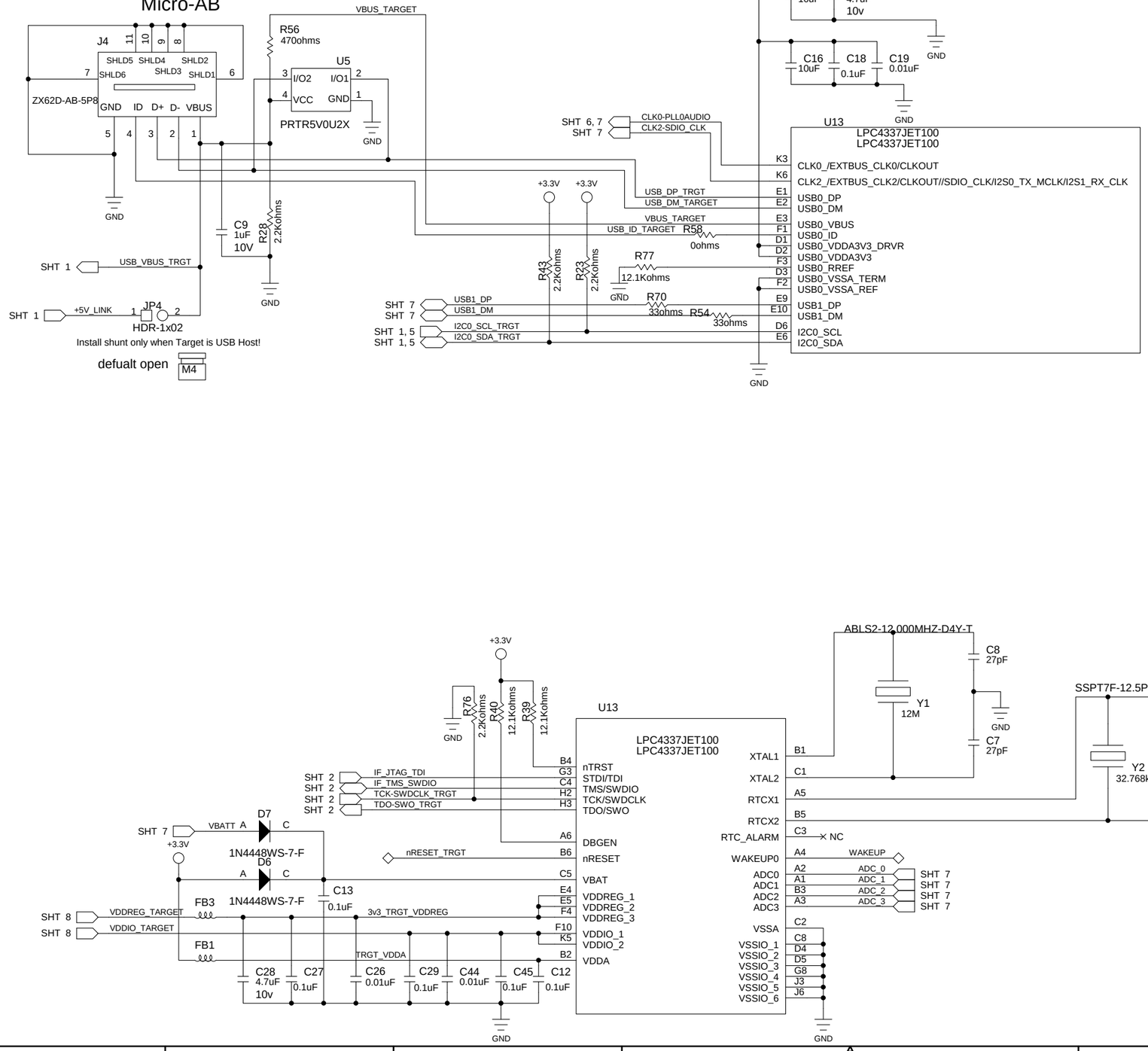
DWG. NO.	SH.	REV.
LPCXpresso43/18xx v3	3	B

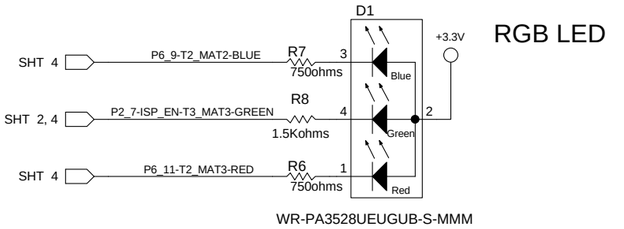
REVISIONS

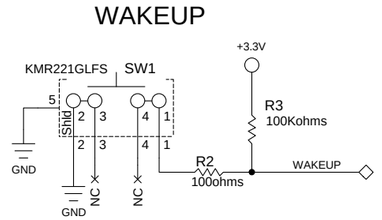
REV	DESCRIPTION	DATE	APPROVED

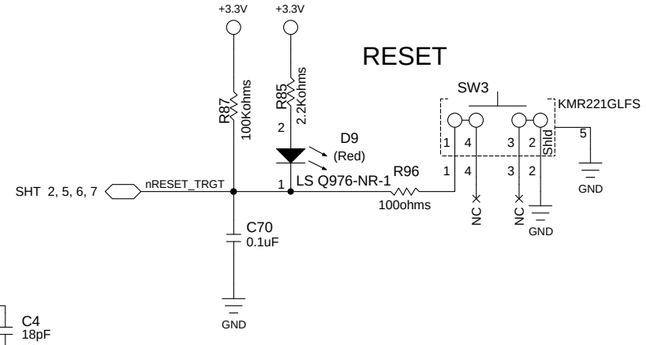
Target

Hi-SpeedUSB Device / Host Micro-AB









CONTRACT NO.		Target LPC433x / Power / USB
APPROVALS	DATE	**NXP** Semiconductors
DRAWN d.consiglio	5/1/2015	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/
CHECKED		
ISSUED	05/01/2015	

SIZE	FSCM NO.	DWG. NO.	REV
D		LPCXpresso43/18xx v3	B

SCALE | SHEET 3 OF 08

H=8ND, V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

U13
LPC4337JET100
LPC4337JET100

SHT 6	P0_0-ENET_RXD1	G2	P0[0]_/GPIO0[0]/SSP1_MISO/ENET_RXD1/SGPIO0
SHT 6	P0_1-ENET_TXEN	G1	P0[1]_/GPIO0[1]/SSP1_MOSI/ENET_TXEN/SGPIO1
SHT 2, 5	P1_0-SSP0_SSEL	H1	P1[0]_/GPIO0[4]/CTIN_3/EXTBUS_A5
SHT 2, 5	P1_1-BOOT0_LED-SSP0_MISO	K2	P1[1]_/GPIO0[8]/CTOUT_7/EXTBUS_A6/SGPIO8
SHT 2, 5	P1_2-BOOT1_TRGT-SSP0_MOSI	K1	P1[2]_/GPIO0[9]/CTOUT_6/EXTBUS_A7/SGPIO9
SHT 7	P1_3-CTOUT8-MISO1	J1	P1[3]_/GPIO0[10]/CTOUT_8/SGPIO10/EXTBUS_OE
SHT 7	P1_4-CTOUT9-MOSI1	J2	P1[4]_/GPIO0[11]/CTOUT_9/SGPIO11/EXTBUS_BLS0
SHT 7	P1_5-CTOUT10-SSEL1	J4	P1[5]_/GPIO1[8]/CTOUT_10/NC/EXTBUS_CS0
SHT 7	P1_6-SD_CMD	K4	P1[6]_/GPIO1[9]/CTIN_5/NC/EXTBUS_WE
SHT 7	P1_7-CTOUT13	G4	P1[7]_/GPIO1[0]/U1_DSR/CTOUT_13/EXTBUS_D0
SHT 7	P1_8-CTOUT12	H5	P1[8]_/GPIO1[1]/U1_DTR/CTOUT_12/EXTBUS_D1
SHT 7	P1_9-SD_DAT0	J5	P1[9]_/GPIO1[2]/U1_RTS/CTOUT_11/EXTBUS_D2
SHT 7	P1_10-SD_DAT1	H6	P1[10]_/GPIO1[3]/U1_RI/CTOUT_14/EXTBUS_D3
SHT 7	P1_11-SD_DAT2	J7	P1[11]_/GPIO1[4]/U1_CTS/CTOUT_15/EXTBUS_D4
SHT 7	P1_12-SD_DAT3	K7	P1[12]_/GPIO1[5]/U1_DCD/NC/EXTBUS_D5
SHT 7	P1_13-U1_TX-SD_CD	H8	P1[13]_/GPIO1[6]/U1_TXD/NC/EXTBUS_D6
SHT 7	P1_14-U1_RX	J8	P1[14]_/GPIO1[7]/U1_RXD/NC/EXTBUS_D7
SHT 6	P1_15-ENET_RXD0	K8	P1[15]_/GPIO0[2]/U2_TXD/SGPIO2/ENET_RXD0
SHT 6	P1_16-ENET_CRS_DV	H9	P1[16]_/GPIO0[3]/U2_RXD/SGPIO3/ENET_RX_DV
SHT 6	P1_17-ENET_MDIO	H10	P1[17]_/GPIO0[12]/U2_UCLK/NC/ENET_MDIO
SHT 6	P1_18-ENET_TXD0	J10	P1[18]_/GPIO0[13]/U2_DIR/NC/ENET_TXD0
SHT 6	P1_19-ENET_REF_CLK	K9	P1[19]_/ENET_TX_REF_CLK/SSP1_SCK/CLKOUT/I2S1_RX_SCK
SHT 6	P1_20-ENET_TXD1	K10	P1[20]_/GPIO0[15]/SSP1_SSEL/NC/ENET_TXD1

+3.3V +3.3V
R13 2.2Kohms
R14 2.2Kohms

U13
LPC4337JET100
LPC4337JET100

SHT 6	P2_0-ISP_U0_TX-ENET_MDC	G10	P2[0]_/SGPIO4/U0_TXD/EXTBUS_A13/USB0_PWR_EN
SHT 2	P2_1-ISP_U0_RX	G7	P2[1]_/SGPIO5/U0_RXD/EXTBUS_A12/USB0_PWR_FAULT
SHT 7	P2_2	F5	P2[2]_/SGPIO6/U0_UCLK/EXTBUS_A11/USB0_IND1
SHT 5, 7	P2_3-I2C1_SDA	D8	P2[3]_/SGPIO12/I2C1_SDA/U3_TXD/CTIN_1
SHT 5, 7	P2_4-I2C1_SCL	D9	P2[4]_/SGPIO13/I2C1_SCL/U3_RXD/CTIN_0
SHT 7	P2_5-USB1_VBUS	D10	P2[5]_/SGPIO14/CTIN_2/USB1_VBUS/ADCTRIG1
SHT 7	P2_6	G9	P2[6]_/SGPIO7/U0_DIR/EXTBUS_A10/USB0_IND0
SHT 2, 3	P2_7-ISP_EN-T3_MAT3-GREEN	C10	P2[7]_/GPIO0[7]/CTOUT_1/U3_UCLK/EXTBUS_A9
	P2_8-BOOT2_TRGT	C6	P2[8]_/SGPIO15/CTOUT_0/U3_DIR/EXTBUS_A8/GPIO5[7]
SHT 7	P2_9-BOOT3_TRGT-CTOUT3	B10	P2[9]_/GPIO1[10]/CTOUT_3/U3_BAUD3/EXTBUS_A0
SHT 7	P2_10-U2_TX	E8	P2[10]_/GPIO0[14]/CTOUT_2/U2_TXD/EXTBUS_A1
SHT 7	P2_11-U2_RX	A9	P2[11]_/GPIO1[11]/CTOUT_5/U2_RXD/EXTBUS_A2
SHT 7	P2_12-CTOUT4	B9	P2[12]_/GPIO1[12]/CTOUT_4/NC/EXTBUS_A3
SHT 7	P2_13	A10	P2[13]_/GPIO1[13]/CTIN_4/NC/EXTBUS_A4
SHT 2, 5	P3_0-SSP0_SCK	A8	P3[0]_/I2S0_RX_SCK/I2S0_RX_MCLK/I2S0_TX_SCK/I2S0_TX_MCLK
SHT 5, 7, 7	P3_2-I2S0_RX_SDA-CAN-TD	F7	P3[1]_/I2S0_TX_WS/I2S0_RX_WS/CAN0_RD/USB1_IND1/GPIO5[8]
	P3_3-SSP0_SCK-SPIFI_SCK	G6	P3[2]_/I2S0_TX_SDA/I2S0_RX_SDA/CAN0_TD/USB1_IND0/GPIO5[9]
	P3_4-SPIFI_SIO3-U1_TX	A7	P3[3]_//SPI_SCK/SSP0_SCK/SPIFI_SCK
SHT 7	P3_5-SPIFI_SIO2-I2S0_TX_SDA	B8	P3[4]_/GPIO1[14]///SPIFI_SIO3
	P3_6-SSP0_MISO-SPIFI_MISO	B7	P3[5]_/GPIO1[15]///SPIFI_SIO2
	P3_7-SSP0_MOSI-SPIFI_MOSI	C7	P3[6]_/GPIO0[6]/SPI_MISO/SSP0_SSEL/SPIFI_MISO
	P3_8-SPIFI_CS	D7	P3[7]_//SPI_MOSI/SSP0_MISO/SPIFI_MOSI
		E7	P3[8]_//SPI_SSEL/SSP0_MOSI/SPIFI_CS

P3_4-SPIFI_SIO3-SJ 1 2 3 P3_4-U1_TX-SJ SHT 7
JS9
P3_1-I2S0_TX_WS-CAN0_RD
JS13 P3_1-SSEL1_MUX_CTL SHT 7
JS12 P3_1-I2S0_TX_WS SHT 7
JS14 P3_1-CAN0_RD SHT 7

Only one SJ should be shoted at a time

U13
LPC4337JET100
LPC4337JET100

SHT 7	P6_0-I2S0_RX_SCK	H7	P6[0]_/I2S0_RX_MCLK///I2S0_RX_SCK
SHT 7	P6_1-I2S0_RX_WS	G5	P6[1]_/GPIO3[0]/EXTBUS_nDYCS1/U0_UCLK/I2S0_RX_WS
SHT 2, 5	P6_2-GPIO3_1	J9	P6[2]_/GPIO3[1]/EXTBUS_CKEOUT1/U0_DIR/I2S0_RX_SDA
	P6_4-U0_TX	F6	P6[4]_/GPIO3[3]/CTIN_6/U0_TXD/EXTBUS_nCAS
SHT 7	P6_5-CTOUT6	F9	P6[5]_/GPIO3[4]/CTOUT_6/U0_RXD/EXTBUS_nRAS
SHT 3	P6_9-T2_MAT2-BLUE	F8	P6[9]_/GPIO3[5]/NC/NC/EXTBUS_nDYCS0
SHT 3	P6_11-T2_MAT3-RED	C9	P6[11]_/GPIO3[7]/NC/NC/EXTBUS_CKEOUT0
SHT 7	PF_4-SCK1	H4	PF[4]_/SSP1_SCK/SPIFI_CLKIN/TRACECLK///I2S_TX_MCLK/I2S_RX_MCLK

P2_0-ISP_U0_TX-ENET_MDC
1 M5
JP11 2 U0_TX SHT 2, 7
3 HDR-1x03
P6_4-U0_TX

KMR221GLFS SW2
5 Shld 2 3 4 1
2 3 4 1
GND NC NC GND
R1 100ohms P2_7-ISP_EN-T3_MAT3-GREEN

ISP Bootload Enable

Target LPC43xx Boot Modes					
Mode	P2_7	P2_9	P2_8	P1_2	P1_1
No ISP Flash boot	high	X	X	X	X
ISP USB	low	low	high	low	high
ISP SPIFI	low	low	low	low	high
ISP USART0	low	low	low	low	low

+3.3V
R83 100Kohms
JS23 1 2
P3_8-SPIFI_CS
P3_3-SSP0_SCK-SPIFI_SCK
P3_7-SSP0_MOSI-SPIFI_MOSI
U16
MX25L8035EM2I-10G
nCS 1 | VCC 8
SCK 6 | nHOLD/IO3 7
DI/IO0 5 | nWP/IO2 3
VSS 4 | DO/IO1 2
MX25L8035EM2I-10G
P3_4-SPIFI_SIO3-SJ
P3_5-SPIFI_SIO2-I2S0_TX_SDA
P3_6-SSP0_MISO-SPIFI_MISO
GND
Z15 Z2 Z1 Z11
Fanout_TP Fanout_TP Fanout_TP Fanout_TP

+3.3V
C46 0.1uF
GND
Z4 Z3 Z14 Z12
Fanout_TP Fanout_TP Fanout_TP Fanout_TP

+3.3V
R11 2.2Kohms
P1_1-BOOT0_LED-SSP0_MISO
P1_2-BOOT1_TRGT-SSP0_MOSI
P2_8-BOOT2_TRGT
P2_9-BOOT3_TRGT-CTOUT3
R9 2.2Kohms
R10 2.2Kohms
M6 M7
R41 2.2Kohms
R12 2.2Kohms DNI
JP5 1 2 HDR-1x02
R75 2.2Kohms
JP3 1 2 HDR-1x02
D4 LS Q976-NR-1
GND

If the boot process fails, LED blinks at a 1 Hz rate for 60 seconds.

CONTRACT NO.		LPC433x Target Peripherals / Boot select	
APPROVALS	DATE	**NXP** Semiconductors	
DRAWN d.consiglio	5/1/2015	411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
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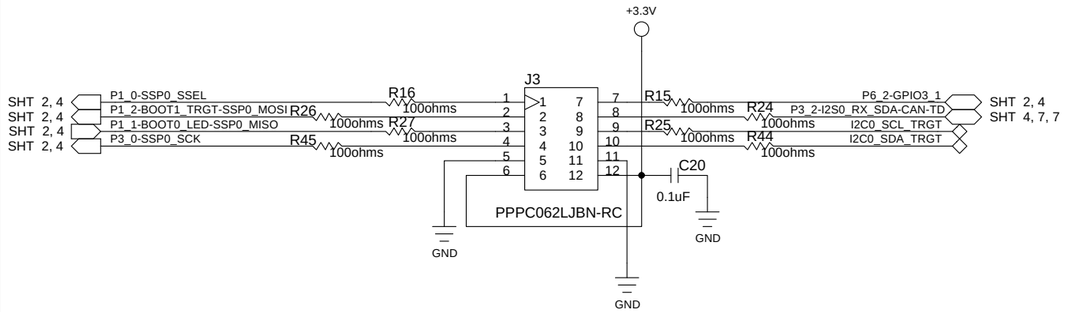
ISSUED	05/01/2015	SIZE D / FSCM NO. / DWG. NO. LPCXpresso43/18xx v3 / REV B	
		SCALE / SHEET 4 OF 08	

H:8N0; V:4LA

REVISIONS

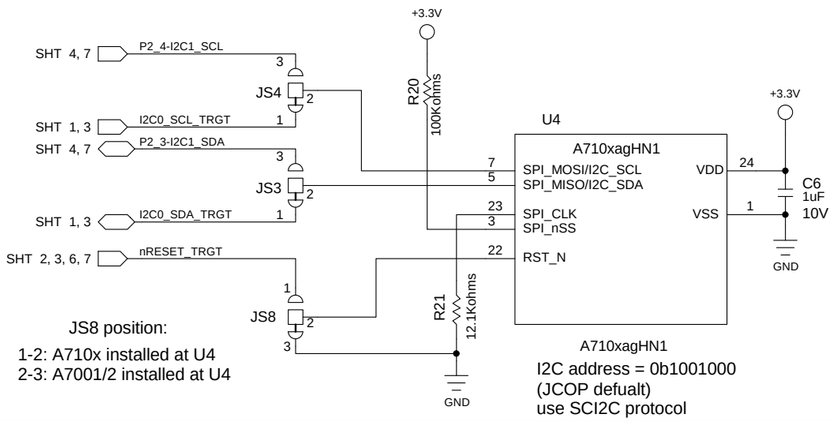
REV	DESCRIPTION	DATE	APPROVED

SPI / I2C header (PMOD compatible)



PMOD pin function	LPC43xx supported function
Pin 1: GPIO/SPI-SSEL(out)/UART-CTS(in)	GPIO/SPI-SSEL(in/out)
Pin 2: GPIO/SPI-MOSI(out)/UART-TXD(out)	GPIO/SPI-MOSI(in/out)
Pin 3: GPIO/SPI-MISO(in)/UART-RXD(in)	GPIO/SPI-MISO(out/in)
Pin 4: GPIO/SPI-SCK(out)/UART-RTS(out)	GPIO/SPI-SCK(in/out)
Pin 5: GND	GND
Pin 6: VCC(3.3V)	VCC(3.3V)
Pin 7: GPIO/INT(in)	GPIO/INT(out/in)
Pin 8: GPIO/RESET(out)	GPIO/RESET(out)
Pin 9: GPIO/SCL	SCL
Pin 10:GPIO/SDA	SDA
Pin 11:GND	GND
Pin 12:VCC(3.3V)	VCC(3.3V)

NXP A70xx / A71 secure MCU



JS8 position:

1-2: A710x installed at U4
2-3: A7001/2 installed at U4

A710xagHN1

I2C address = 0b1001000
(JCOP defualt)
use SCI2C protocol

CONTRACT NO.		NXP A7xxx security / Pmod interfaces	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
DRAWN d.consiglio	5/1/2015		
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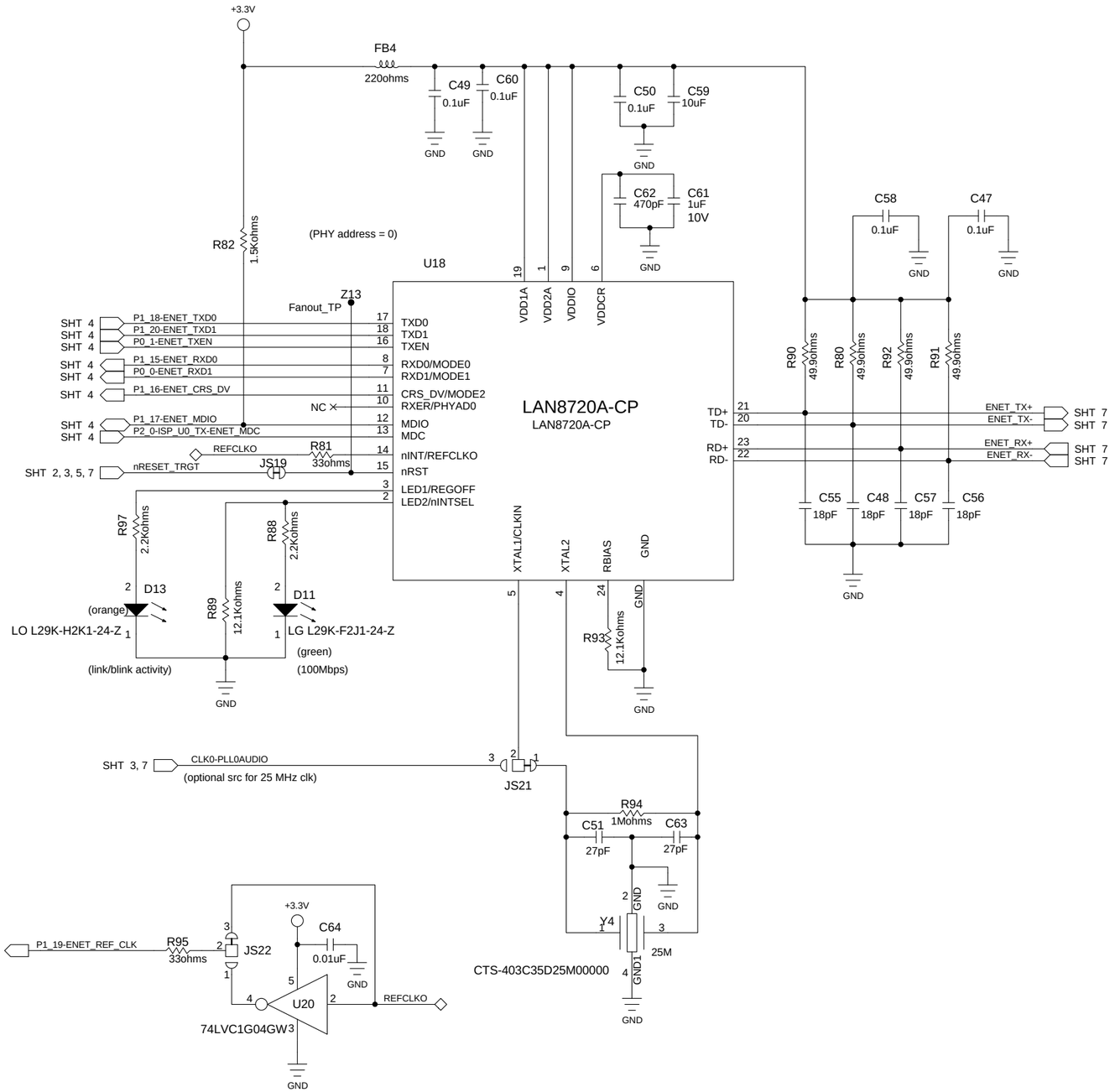
ISSUED	05/01/2015	SIZE D / FSCM NO. / DWG. NO. LPCXpresso43/18xx v3 / REV B	
		SCALE / SHEET 5 OF 08	

REVISIONS

REV	DESCRIPTION	DATE	APPROVED



CONTRACT NO.		Ethernet PHY	
APPROVALS	DATE	**NXP** Semiconductors 411 E. Plumeria Dr San Jose, CA 95134 www.standardics.nxp.com/microcontrollers/	
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		SCALE / SHEET 6 OF 08	

H=8ND; V=4LA

REVISIONS

REV	DESCRIPTION	DATE	APPROVED

Arduino Shield receptacles R4

+3.3V +5V

C72 0.01uF GND
C73 0.01uF GND

Power

J6

SHT 6	ENET_RX-	1	2		
SHT 6	ENET_RX+	3	4		
SHT 6	ENET_TX-	5	6	RFU	NC
SHT 6	ENET_TX+	7	8	IOREF	
	nRESET_TRGT	9	10	RESET	nRESET_TRGT SHT 2, 3, 5, 6
SHT 3	VBATT	11	12	+3V3	
NC		13	14	+5V0	
NC		15	16	GND	
SHT 3	USB1_DM	17	18	GND	
SHT 3	USB1_DP	19	20	VIN	VIN JS25

P3_1-CAN0_RD SHT 4
P3_2-I2S0_RX_SDA-CAN-TD SHT 4, 5, 7

PPPC102LFBN-RC

Analog In

J7

NC		1	2	A0	ADC_0 SHT 3
NC		3	4	A1	ADC_1 SHT 3
NC		5	6	A2	ADC_2 SHT 3
NC		7	8	A3	ADC_3 SHT 3
NC		9	10	A4	NC
NC		11	12	A5	P2_5-USB1_VBUS SHT 4
NC		13	14		NC
NC		15	16		NC
NC		17	18		NC
NC		19	20		NC

SPI_SSEL1 (secondary) P1_5-CTOUT10-SSEL1_ALT

PPPC102LFBN-RC

Digital

+3.3V
JS5
C2 0.01uF GND

J1

SHT 4, 5	P2_4-I2C1_SCL	15	SCL	1	2 NC
SHT 4, 5	P2_3-I2C1_SDA	14	SDA	3	4 NC
			AREF	5	6 NC
			GND	7	8 NC
SHT 4	PF_4-SCK1	13	SCK	9	10 P3_5-SPIFI_SIO2-I2S0_TX_SDA SHT 4
SHT 4	P1_3-CTOUT8-MISO1	12	MISO	11	12 P3_1-I2S0_TX_WS SHT 4
SHT 4	P1_4-CTOUT9-MOSI1	11	PWM MOSI	13	14 CLK0-PLL0AUDIO SHT 3, 6
	P1_5-CTOUT10-SSEL1_PRI	10	PWM SSEL	15	16 P6_0-I2S0_RX_SCK SHT 4
SHT 4	P6_5-CTOUT6	9	INT/PWM	17	18 P6_1-I2S0_RX_WS SHT 4
SHT 4	P2_6	8	INT	19	20 P3_2-I2S0_RX_SDA-CAN-TD SHT 4, 5, 7

PPPC102LFBN-RC

Digital

J2

SHT 4	P2_12-CTOUT4	7	PWM	1	2 CLK2-SDIO_CLK SHT 3
SHT 4	P2_9-BOOT3_TRGT-CTOUT3	6	PWM	3	4 P1_6-SD_CMD SHT 4
SHT 4	P1_7-CTOUT13	5	PWM	5	6 P1_9-SD_DAT0 SHT 4
SHT 4	P2_2	4	PWM	7	8 P1_12-SD_DAT3 SHT 4
SHT 4	P1_8-CTOUT12	3	INT PWM	9	10 P1_10-SD_DAT1 SHT 4
SHT 4	P2_13	2	INT	11	12 P1_11-SD_DAT2 SHT 4
SHT 4	P2_10-U2_TX	1	TX	13	14 NC
SHT 4	P2_11-U2_RX	0	RX	15	16 NC
SHT 4	P3_4-U1_TX-SJ			17	18 P1_13-U1_TX-SD_CD SHT 4
SHT 4	P1_14-U1_RX			19	20 NC

PPPC102LFBN-RC

+3.3V

+3.3V
U8
5 VDD
SEL 6
Y0 3
Y1 1
GND 2
74LVC1G3157GW
GND

R22 100Kohms
R55 100Kohms
R42 100Kohms

SHT 4 P1_5-CTOUT10-SSEL1 4 Z
P3_1-SSEL1_MUX_CTL SHT 4
P1_5-CTOUT10-SSEL1_ALT
P1_5-CTOUT10-SSEL1_PRI

SSP1 SSEL Mux

SEL = 1 = Arduino Dig10 (default)
SEL = 0 = Expansion J7.3
SW must set P3_1 low to use SSEL1 at Expansion J7.3

+5V

UARTto FTDI USB

TTL-232R-3V3 compatible

1 D10 2
PMEG2005EJ

C52 0.1uF

P4

	1	1	GND
NC	2	2	CTS
	3	3	VD
	4	4	
	5	5	
NC	6	6	RTS

HDR-1x06-RA

SHT 2 P2_1-ISP_U0_RX_FTDI
SHT 2, 4 U0_TX

GND

CONTRACT NO.		Shield Receptacles; FTDI	
APPROVALS	DATE	**NXP** Semiconductors	
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ISSUED	05/01/2015	SIZE D / FSCM NO. / DWG. NO. LPCXpresso43/18xx v3 / REV B	
		SCALE / SHEET 7 OF 08	

H=8ND; V=4LA

REVISIONS

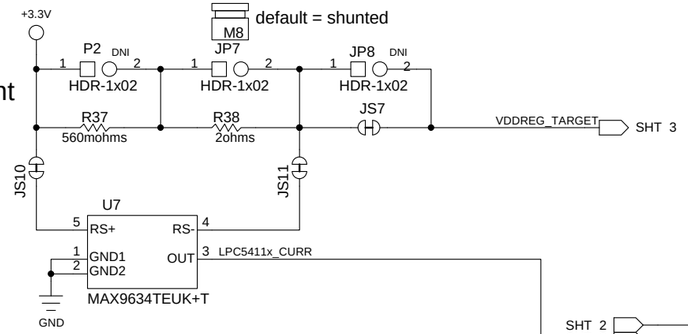
REV	DESCRIPTION	DATE	APPROVED

LPC43/18xx VDDREG Current measurement				
LPC43/18xx				ADC111S021 12bit ADC
Vsense (1) voltage 1-lsb	JP7 open LPC43/18xx Current 1-lsb	JP7 shunted LPC43/18xx Current 1-lsb	maximum current	ADC input 1- lsb 800uV
32uV	12.6uA	57.55uA	235mA	

(1) Vsense voltage is between U7 RS+ to RS-. Total Rvsense = R37 + (R38 || JP7).

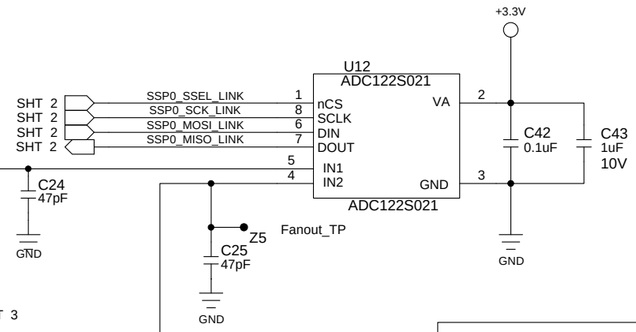
Tables need to be update once current range high / low are set.

Target Vddc measurement



JP7 Setting

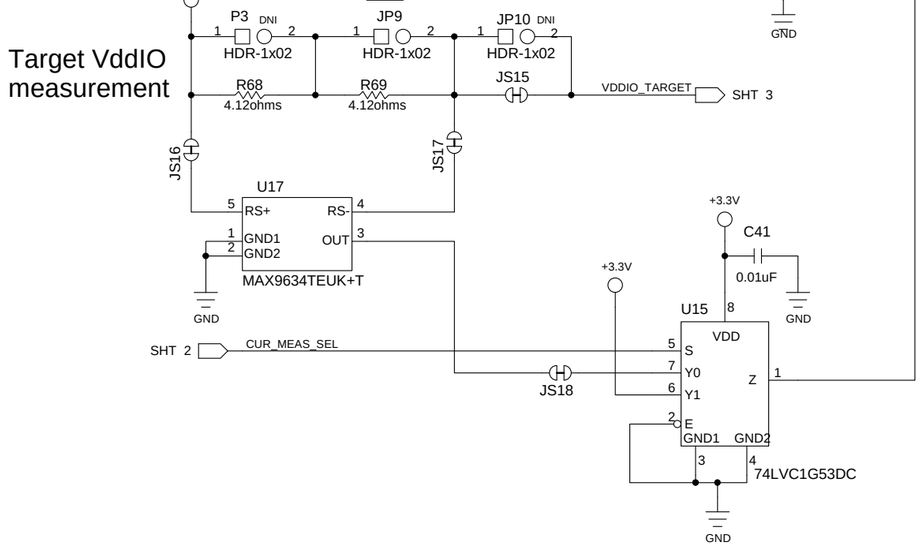
VDD LPC43/18xx (current range)	JP7	Total Rvsense (ohms)
12.6uA -52mA	open	2.56
58uA - 235mA	shunted	0.56



JP9 Setting

VDD LPC43/18xx (current range)	JP9	Total Rvsense (ohms)
4uA - 16mA	open	8.24
8uA - 32mA	shunted	4.12

Target VddIO measurement



LPC43/18xx VDDIO Current measurement				
LPC43/18xx				ADC111S021 12bit ADC
Vsense (1) voltage 1-lsb	JP9 open LPC43/18xx Current 1-lsb	JP9 shunted LPC43/18xx Current 1-lsb	maximum current	ADC input 1- lsb 800uV
32uV	3.9uA	7.8uA	32mA	

(1) Vsense voltage is between U17 RS+ to RS-. Total Rvsense = R68 + (R69 || JP9).

CONTRACT NO.	LPC43xx/18xx current monitor
APPROVALS / DATE	**NXP** Semiconductors
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SCALE / SHEET 8 OF 08	

H=8ND; V=4LA