SYSTEM CONTROL

LPC546XX TRAINING SERIES

EXTERNAL USE

SECURE CONNECTIONS
FOR A SMARTER WORLD

Agenda

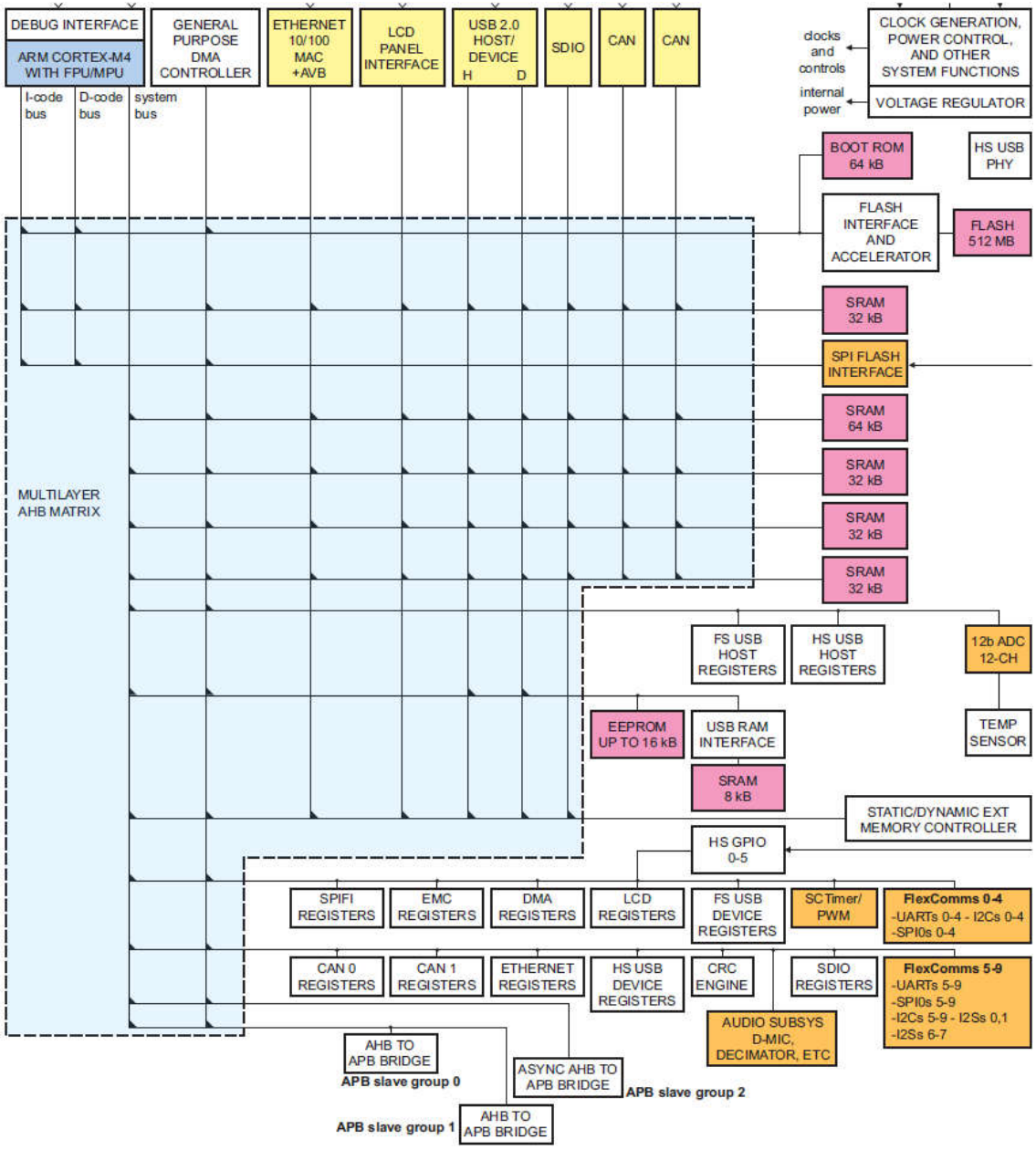
- Clocking
- Clock generators
- Other system control features

LPC546xx key highlights

- High performance
  - 180MHz Cortex-M4F.
  - Large AHB matrix with many masters and slaves
- Large memory
  - 512kB Flash, 200kB RAM, 16kB EEPROM
  - SPI Flash interface (SPIFI) for QSPI XIP flash
  - External Memory Controller (EMC), for SRAM, SDRAM, NOR Flash, etc.
- Broad connectivity
  - 10 flexcomms (UART/I2C/SPI, and two muxed with I2S)
  - 2 additional smartcard UARTs
  - ADC 12 bit at 5Msps/s
- Rich advanced peripherals
  - Ethernet100+1588+AVB,
  - USB-HS H/D w/ HS PHY, USB-FS H/D w/ FS PHY
  - SD/MMC/SDIO,
  - CANFD x2
  - Audio sub-system for DMIC based voice triggering
- Close consistency with LPC54xxx, LPC8xx
  - Similar system control
    - Especially, downward compatible with LPC5411x whenever applicable
  - Most basic peripherals are the same (Flexcomm, ADC, timers, GPIO, power control, etc)

LPC546xx blocks overview

- CPU, DMA and advanced modules are bus masters
  - Take advantage of bus matrix, better throughput
- RAM has several blocks but most are adjacent in address
  - SRAMX for CPU, USB RAM are exceptions
- Faster modules are on AHB bus
  - Flexcomms
  - Register files for some faster peripherals
- 3 APB buses, one has dedicated clock selector.



LPC546xx part numbers

Part Number	Basic Type	M4	Flash (KB)	RAM (KB)	Security Features	Voice Detection	Graphic LCD	Ethernet AVB	CAN FD	USB H/D	Package
LPC54608	LPC54608J512ET180	1	512	200	Optional	Yes	1	1	2	HS+FS	180 BGA
	LPC54608J512BD208	1	512	200	Optional	Yes	1	1	2	HS+FS	208 LQFP
LPC54607	LPC54607J512ET180	1	512	200	Optional	Yes	1	1	0	HS+FS	180 BGA
	LPC54607J512BD208	1	512	200	Optional	Yes	1	1	0	HS+FS	208 LQFP
LPC54606	LPC54606J512BD208	1	512	200	Optional	Yes	0	1	2	HS+FS	208 LQFP
	LPC54606J512ET180	1	512	200	Optional	Yes	0	1	2	HS+FS	180 BGA
LPC54605	LPC54605J512ET180	1	512	200	Optional	Yes	0	1	0	HS+FS	180 BGA
	LPC54605J256ET180	1	256	200	Optional	Yes	0	1	0	HS+FS	180 BGA
LPC54604	LPC54604J512BD100	1	512	200	Optional	Yes	0	1	2	FS	100 LQFP
	LPC54604J512BD64	1	512	200	Optional	Yes	0	1	2	FS	64 LQFP
	LPC54604J256BD100	1	256	200	Optional	Yes	0	1	2	FS	100 LQFP
LPC54603	LPC54603J512BD100	1	512	200	Optional	Yes	0	1	0	FS	100 LQFP
	LPC54603J256BD100	1	256	200	Optional	Yes	0	1	0	FS	100 LQFP
LPC54602	LPC54602J512BD100	1	512	200	Optional	Yes	0	0	2	FS	100 LQFP
	LPC54602J512BD64	1	512	200	Optional	Yes	0	0	2	FS	64 LQFP
	LPC54602J256BD64	1	256	200	Optional	Yes	0	1	2	FS	64 LQFP
LPC54601	LPC54601J512BD64	1	512	200	Optional	Yes	0	0	0	FS	64 LQFP
	LPC54601J256BD64	1	256	200	Optional	Yes	0	0	0	FS	64 LQFP

CLOCKING

Overview of clock tree

- Clock sources
  - **FRO** – improved internal RC with 2 outputs: 12M, and 48/96M.
  - **Watchdog Oscillator** (WDTOsc)
  - **1MHz-25MHz XTAL**
    - (no external clock waveform input)
  - **32kHz RTC XTAL**
  - **PLLs** – System PLL, Audio PLL, USB PLL
- **Main clock** domain
  - CPU, RAM, Flash, EEPROM, EMC
  - Most APB peripherals

- CPU and some peripherals has **clock dividers**.
  - All integer dividers can divide input clock by 1,2,3,…,255
  - A special fraction divider mainly for UART
- Some peripherals have fixed clock source
  - RTC: uses 32kHz input
  - WDT and uTick: uses WDTOsc.
- Some Peripherals such as flexcomm have **clock selectors,** making them immune to CPU clock change.
- Some peripherals such as PININT can **function w/o clock**, enable them to wake up MCU from low power modes.

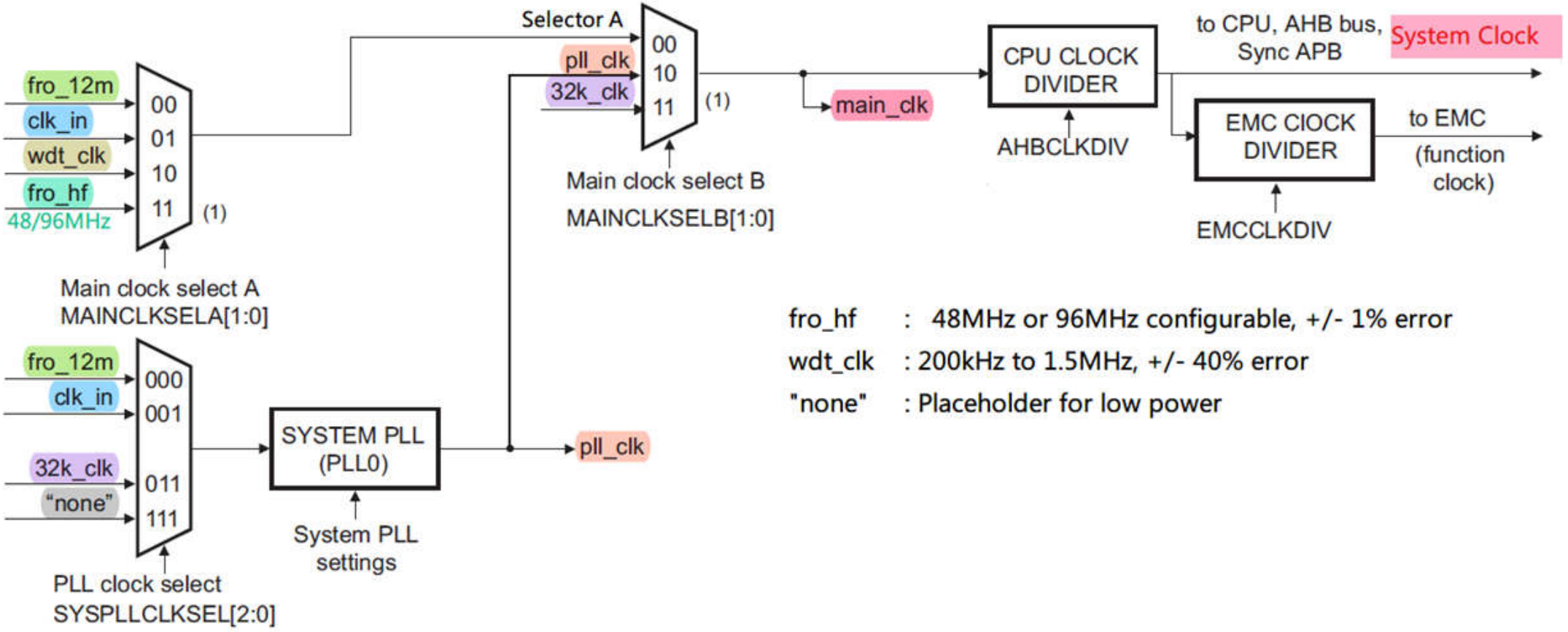
Clock Generation Unit – clock sources

Clock Sources	Characteristics
FRO	• System clock by default • Stable. Quick power up and power down • 12/48/96 MHz (±1% over specified temperature and voltage)
Crystal Oscillator	XTAL: 1 MHz – 20MHz or 15MHz – 25MHz,
32 KHz RTC Oscillator	32.768 KHz
Watchdog Oscillator	• Low power operation and Low frequency oscillator • 6 kHz – 1.5 MHz (+/- 40%) • Clock source to Watchdog Timer and Micro-tick Timer

Clock Generation Unit - PLLs

Clock Sources	Characteristics
SYS PLL	Multiplies the clock source (FRO, Main Osc, CLKIN) Input Frequency: 32.768 kHz to 25 MHz
USB PLL	Multiplies the clock source (Main Osc) Input Frequency: 1 MHz to 25 MHz
Audio PLL	Multiplies the clock source (FRO, Main Osc) Input Frequency: 1MHz to 25 MHz

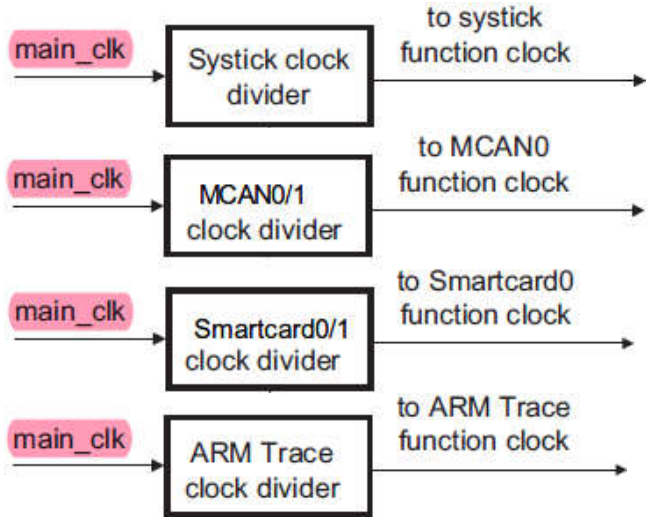
Main clock and system clock generation



Main clock domain

- After divider, supply system clock to a vast range of modules
  - CPU (Cortex-M4)
  - EMC w/ divider
  - AHB bus
    - AHB Peripheral registers: all USB ports, SPIFI, EMC, DMA, LCD, CANs, Ethernet, SDIO
    - AHB Peripheral function: ADC, EEPROM, GPIO, SCT, Flexcomms, CRC, DMIC
  - APB0 bus
    - SysCon, IOCon, PinINT, GroupINT, InMux, MRT, EEPROM registers, OTP, WDT & uTick registers,
  - APB1 bus
    - Timer2, PMU registers, RIT, Flash registers, Smartcards, RNG

- After divider, supply additional peripherals:
  - Systick
  - CAN0
  - CAN1
  - Smartcard0
  - Smartcard1
  - Core trace



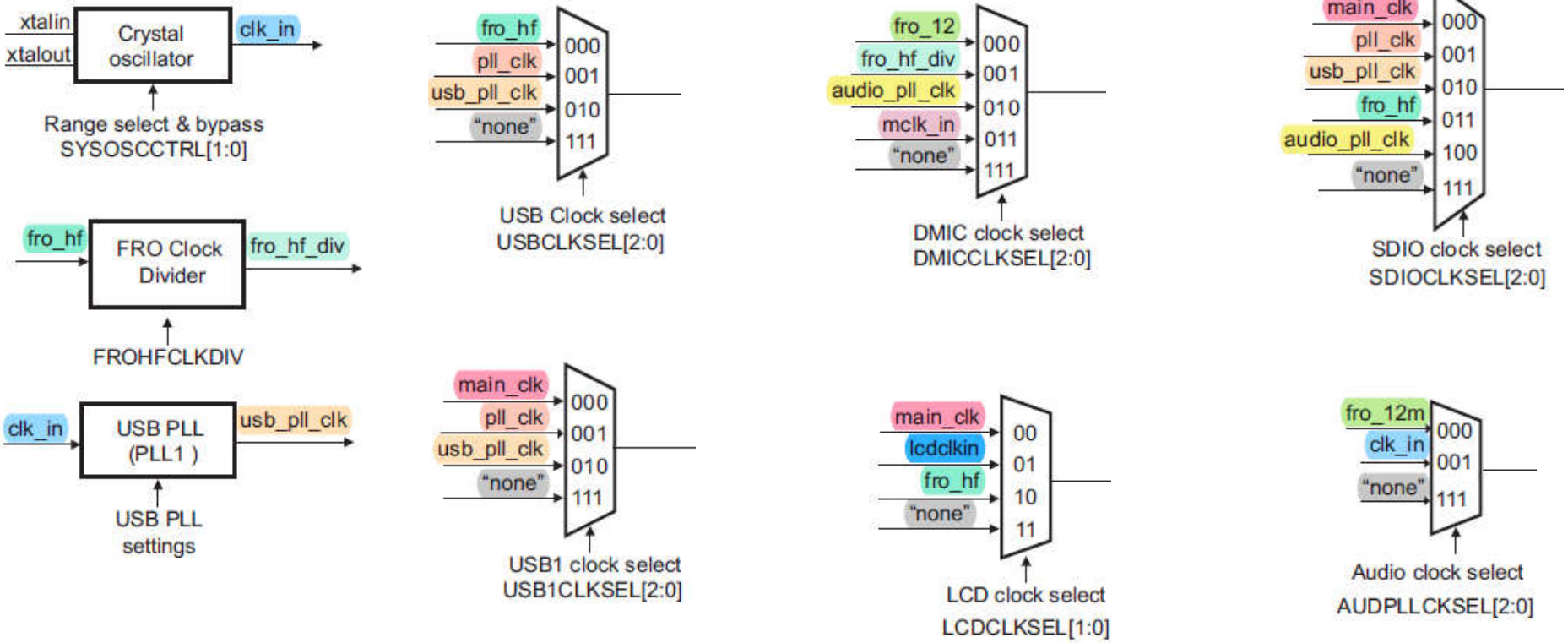
- Clock option of peripherals with clock selectors.

Peripherals with dedicated clock selector

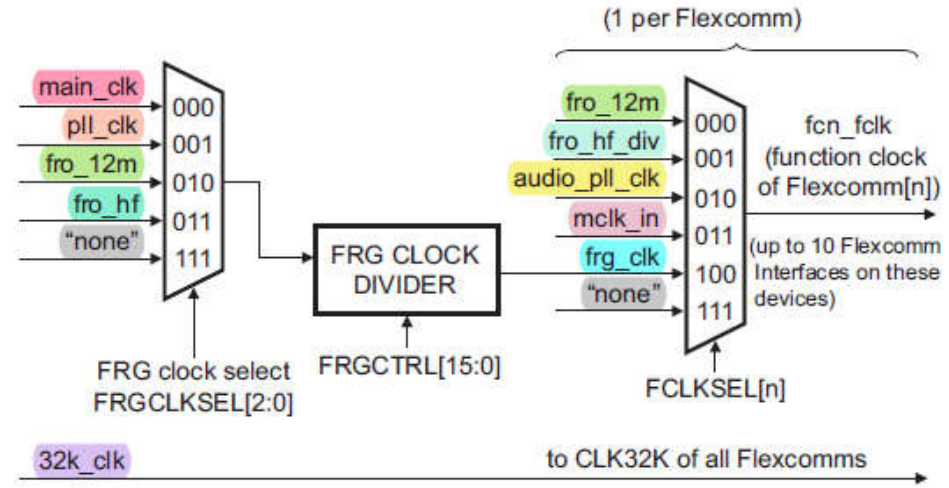
- Peripherals
  - ADC,
  - USB0, USB1PHY
  - DMIC
  - SDIO
  - Audio PLL
  - Fractional clock (mainly for USART)
  - Flexcomm - USART/I2C/SPI/I2S
  - SCT – State Configurable Timer
  - LCD
  - SPIFI – SPI Flash Interface
  - CLKOUT
  - Timer 3 and 4 (Async APB)
- Selectors except flexcomm have their output clock dividers
  - Flexcomm: use FRG clock divider

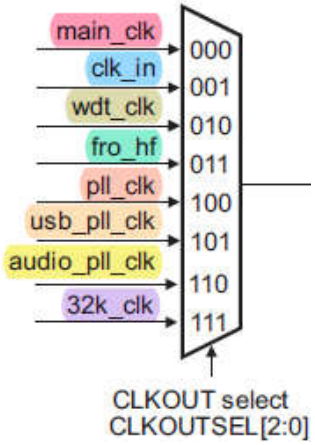
- Benefits
  - Changing CPU clock does not affect operation rate,
  - especially useful for connectivity peripherals such as USART.
  - Less constraint for CPU clock settings. E.g., for 44100Hz, available clock inputs are very limited.
  - Simplifies main clock selectors, no need to cover all clock sources. E.g., “lcdclkin” only presents on LCD clock selector.

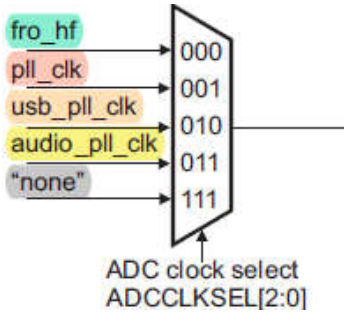
Clock selectors

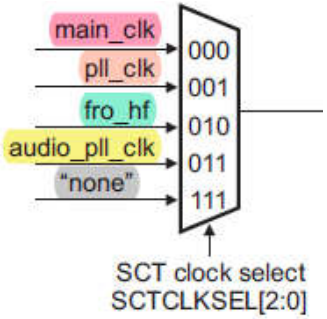


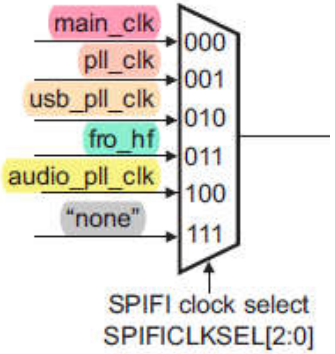
Clock selectors (continued)

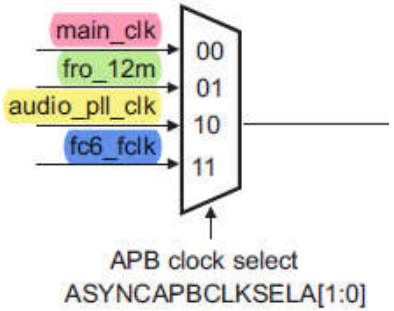


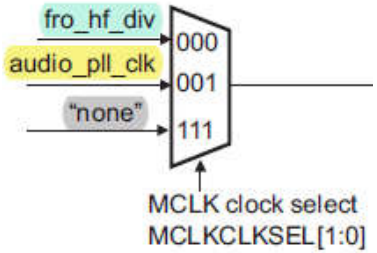






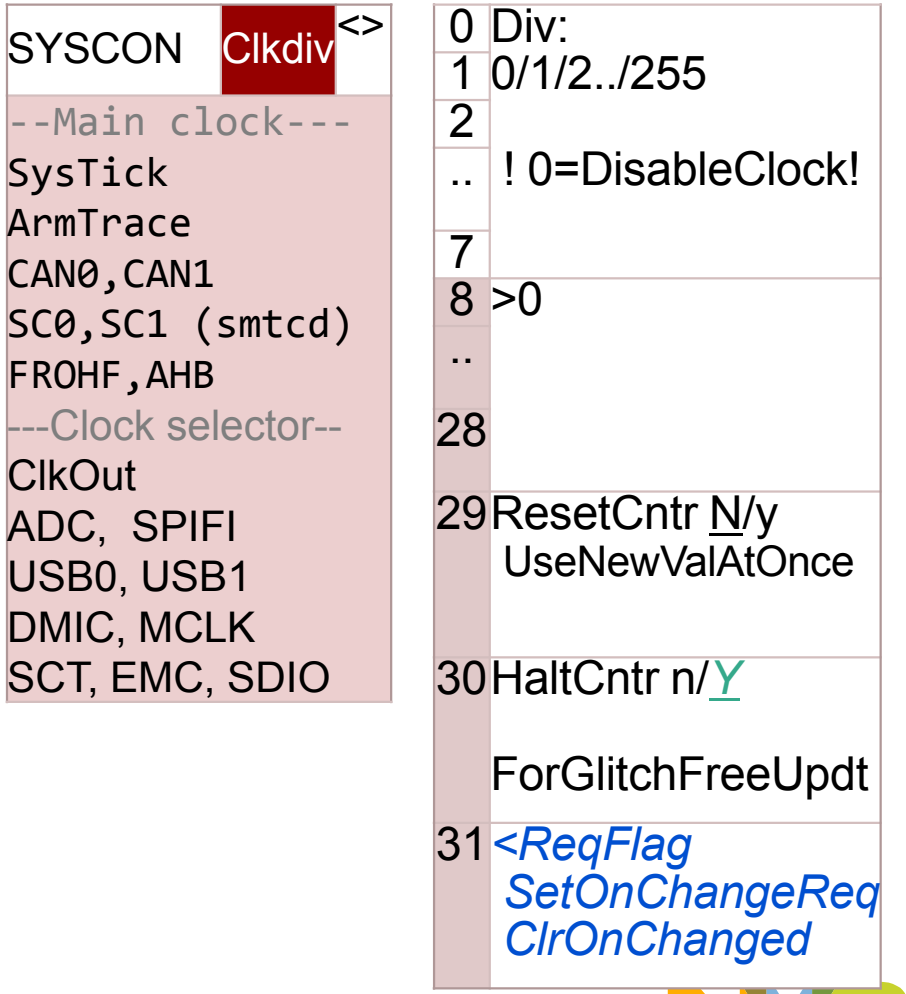






Clock dividers

- Integer dividers (except FRG)
  - All are the same
  - Divider range: 1,2,3,…,256 (0 means no clock)
  - Can manually halt and reset internal 8 bit prescaler.
    - For glitch free clock change: update divider with it halt and reset
- Fractional clock divider
  - Mainly for convenient USART baudrate settings
  - Fractional clock = FRGClkSel / (1 + Mult[7:0]/256)
  - Divisor range: 1+0/256, 1+1/256, 1+2/256, …, 1+255/256



CLOCK GENERATORS

Introduction to the Free Running Oscillator (FRO)

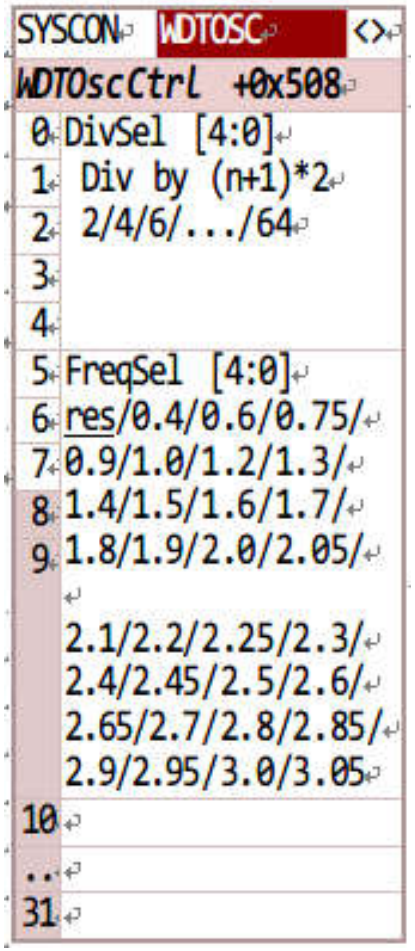
- Low power internal Free-Running Oscillator (~100 uA, replaces former “IRC”)
- Provides two selectable outputs:
  a) 48 MHz or 96 MHz (choose only one as the high frequency output)
  b) 12 MHz output.
- Factory Trimmed for 48 MHz and 96 MHz
- +/- 1% accuracy over the full spec
- Some peripherals allow asynchronous operation from FRO while CPU operates from main clock
- FRO can be used as Main clock or PLL clock source
- Reduces dependency on System PLL
  - Benefit: fast restart after halting the CPU by sleep modes
  - Benefit: low power!
- Main Clock selects the 12 MHz FRO as the clock source on power-up or after reset

FRO for crystal-less Full Speed USB Device

- LPC546xx has an on-chip USB full-speed device.
- 48 MHz input clock should be provided to the Full Speed USB device controller
  - 96MHz FRO with divider, or 48MHz FRO direct
- Automatic USB clock adjustment mode:
  - USB host sends “SOF” packets at 1ms interval, USB FS device automatically trim the FRO based on SOF timing base.
  - No need of external crystal or PLL
- Supports remote wake-up and wake-up from deep-sleep mode on USB activity

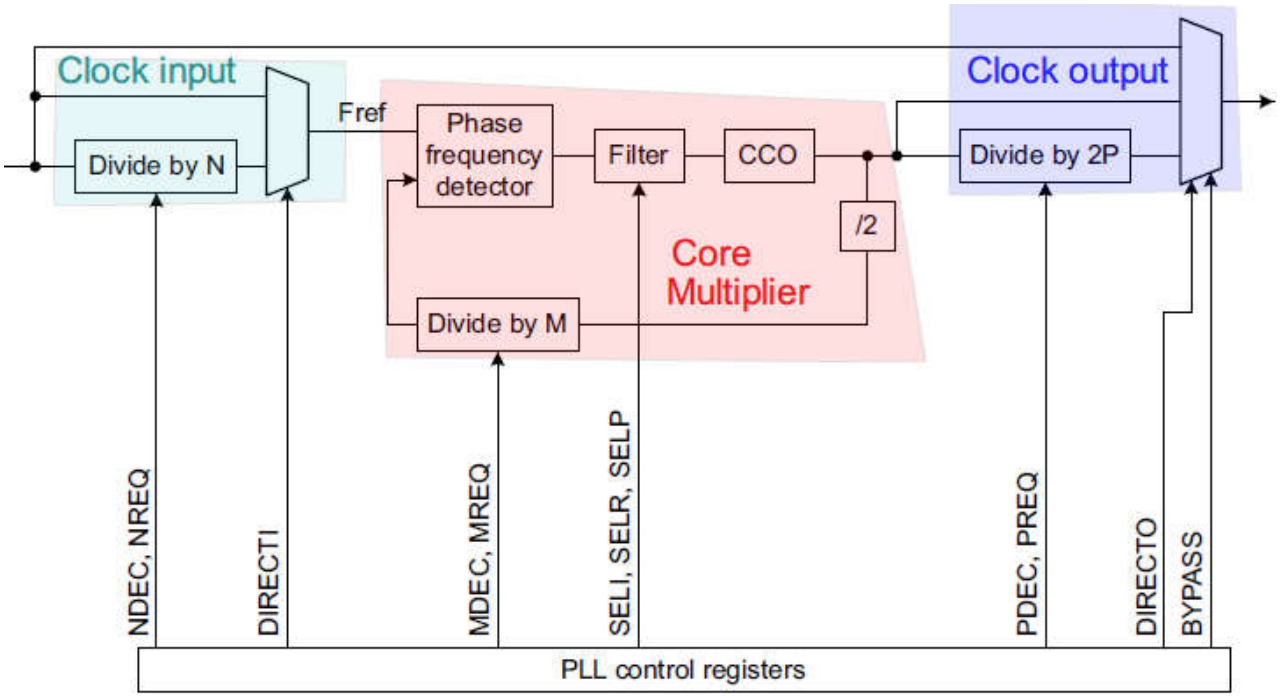
On-chip Watchdog oscillator

- Usage
  - Always supplies Watchdog timer (WDT) and micro tick timer (uTick)
  - Clock candidate of main clock.
- Features
  - Lower power than FRO and XTAL
  - Low accuracy: +/- 40% error
    - Use “frequency measurement” to calibrate
  - 32 programmable outputs ranging from 0.4MHz to 3.05MHz
  - Clock output divider by 2,4,6,…,64



System PLL

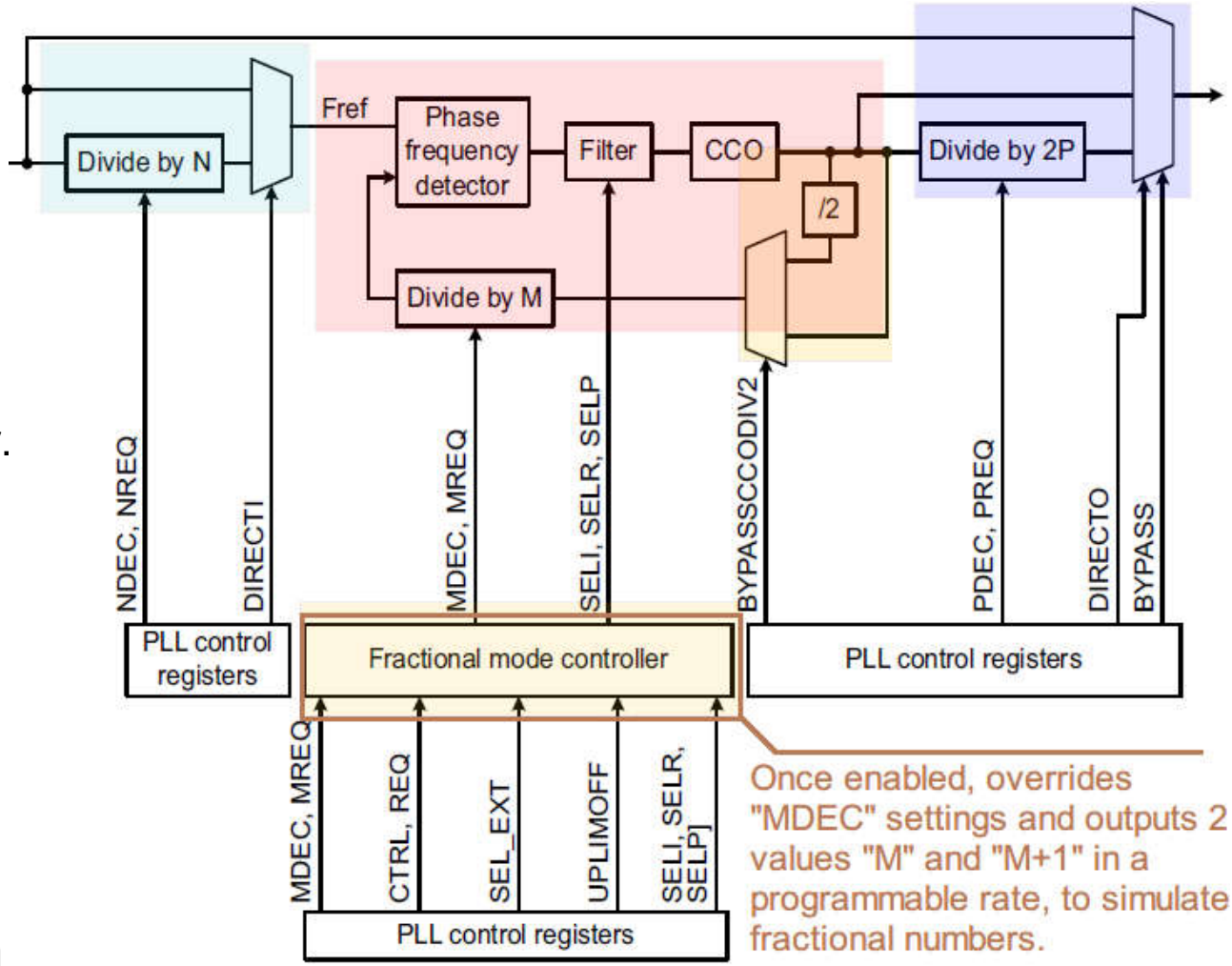
- Key principles
  - The core multiplier of PLL is a Current Controlled Oscillator (CCO), whose output frequency is controlled by input current.
  - The Phase Frequency Detector with a post filter controls CCO input.
- Key features
  - Input :RTCClk, FRO 12MHz, 4-25MHz XTAL
  - Can output a vast range from 4.3MHz to 550MHz (LPC546xx max freq. = 180MHz)
  - Power down mode and auto re-lock on exit.
- Key programmable parameters
  - Pre divider for input clock source of PLL
  - Filter and feedback divider for PLL core part
  - Post divider for output clock, does not affect PLL internal state.



- Remarks
  - **N, M, and P are not plain binary, but encoded**, makes PLL not straightforward to configure manually, recommended to use SDK API to determine them.
  - If Fref < 100kHz or Fref > 20MHz, lock indicator is not reliable
  - 4kHz <= Fref <= 20MHz

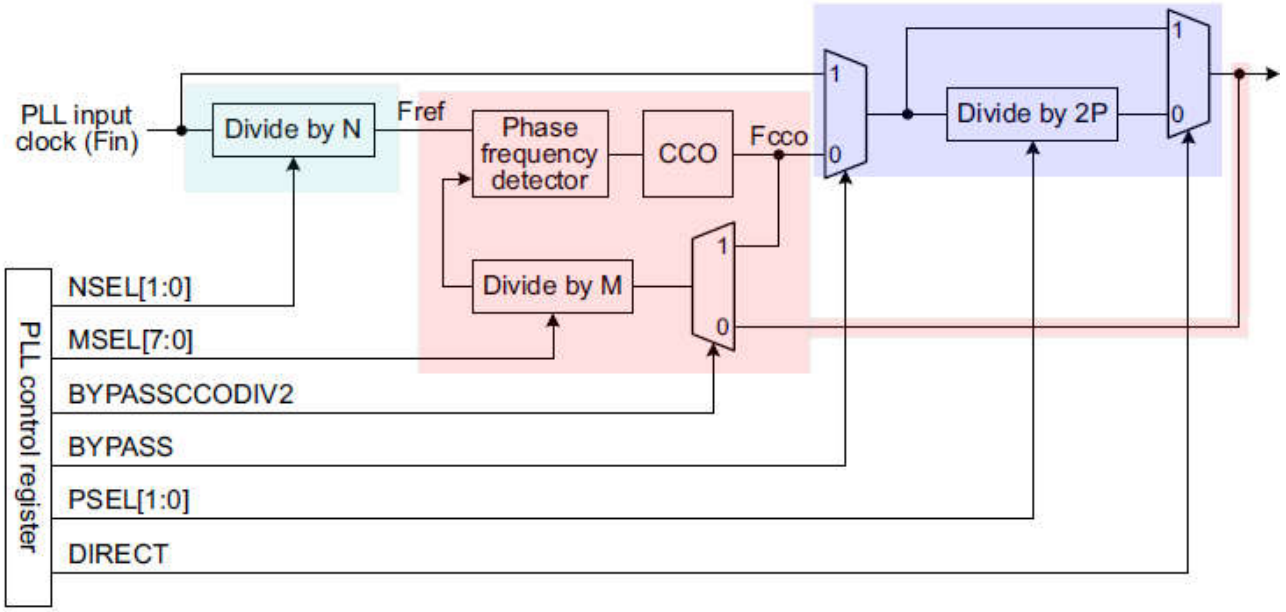
Audio PLL

- Based on system PLL but enhanced in
  - Optional fractional mode for popular audio sample rates (such as 44100).
  - Feedback clock can bypass “/2” divider.
- Optional fractional mode
  - An add-on facility, does not affect original PLL structure.
  - Adjust feedback divider parameter “M”, by using values of M and M+1 in a proper rate to simulate fraction.
    - E.g., “3,3,4,3,3,4” simulates 3.33
  - Once enabled, overrides the settings in feedback divider.



USB PLL

- Mainly for generating 48MHz clock to USB for both full speed and high speed
- Simpler than System PLL and Audio PLL, and no encoded parameters, use binary presentation.
  - Derived from the PLL used in LPC18xx/43xx
- Key features
  - Input range 1MHz – 25MHz
  - Output range 9.75MHz – 320MHz
  - dividers
    - Pre-divider from 1 to 256
    - Feedback divider from 1 to 32768
    - Post-divider 2,4,6,…,64
  - Feedback clock can choose final output
    - Save power if <=Fcco (internal output)



OTHER SYSTEM CONTROL FEATURES

Brown out detector

- Monitors VDD supply to MCU
- Can generate IRQ when VDD drops below a programmable threshold
  - 2.05V/2.45V/2.75V/3.1V
  - A dedicated enable bit
- Can reset MCU when VDD drops below another programmable threshold
  - 1.5V/1.85V/2.0V/2.3V
  - A dedicated enable bit
- Provide flag bits of BoD IRQ and reset
- Note:
  - Avoid Vdd drops to a level that can't restore MCU operation but above Power on reset trigger level.

SysCon		RW
BoDCtrl = 0		
0	BodRstLev	
1	BoD reset level (V) 1.5/1.85/2.0/2.3	
2	BoDRstEna	
	Enable BoD reset: N/y	
3	BodIntLev	
4	BoD interrupt level (V) 2.05/2.45/2.75/3.1	
5	BodIntEna	
	Enable BoD IRQ: N/y	
6	BodRstStat	
	BoD reset status, write 1 to clear	
7	BodIntStat w1c	
	BoD IRQ status, write 1 to clear	
..		
31		

Improved boot ROM support

- Flexible boot modes determined by 3 boot pins (Detailed in next slide)
  - On-chip Flash
  - Improved ISP from UART@Flexcomm0, I2C@Flexcomm1, SPI@Flexcomm3
    - First “PROBE” command determines which one to use. SPI pins have conflict with EMC
  - MSC or DFU on either USB0 or USB1
- More image types for robust firmware upgrade
  - Legacy (0 at 0x24)
  - Single-Enhanced for better protection (**0xEDDC9494** at 0x24)
  - Dual-enhanced for “OTA” style firmware upgrade and backup image scheme (**0x0FFEB6B6** at 0x24)
  - Note: Enhanced images use image headers to mark meta data
- Enhanced CRP and optional OTP bits to prevent cracking
  - Disable ISP, IAP, debug, and lock flash sectors
  - OTP: Store some global enhanced CRP constraints.

ISP Entry from bootloader (via Pins)

ISP Modes				
Boot Source	**ISP-2 PIO0_4**	**ISP-1 PIO0_5**	**ISP-0 PIO0_6**	**Description**
FLASH, no ISP	1	1	1	ISP is bypassed. The device boots from flash if valid user code is detected
UART/ I2C / SPI (Auto Detect)	1	1	0	The first valid probe message on USART, I2C, or SPI locks in that interface
USB 0 MSC	1	0	1	Allow programming flash as USB 0 MSC
Reserved	1	0	0	Reserved
USB 1 MSC	0	1	1	Allow programming flash as USB 1 MSC
USB 0 DFU	0	1	0	Allow programming flash as USB 0 DFU
USB 1 DFU	0	0	1	Allow programming flash as USB 1 DFU

Misc system configurations

- Vector table remap
  - Boot loader, RAM, Flash
- AHB Matrix Priority (4 levels)
  - CPU: Icode, Dcode, Sys
  - Masters: DMA, Eth, USB0, USB1, SDIO, CAN0, CAN1
- NMI source selection
  - Can select one IRQ as NMI
- Async APB enable/disable
- System reset flags
  - POR, Pin, WDT, BoD, System
- Bits to to control reset state of each peripheral, laid in some registers
  - PResetCtrl[3], reset status and r-m-w
  - PResetCtrlSet[3], write 1 only to set reset
  - PResetCtrlClr[3], write 1 only to clear reset
- Capture PIO state upon PoR and other reset

Frequency measurement

- Measure relative rate of one target clock to a reference clock
  - Watchdog Oscillator has +/- 40% error rate, use this to calibrate with
- Use “INMUX” (Input mux) to select:
  - Reference clock (FreqMeas_Ref)
  - Target clock to measure (FreqMeas_Tgt)
- Measures how many target clocks elapsed during 16384 reference clocks

Target clock should be **SLOWER** than ref clock

InMux	R/W
FreqMeas_Ref (Reference clock) **FreqMeas_Tgt** (Target clock)	
0 1 2 3 4	ClkIn [4:0] (Clock select) 0:XTAL 1:FRO_12 (12MHz) 2:FRO_HF (48MHz/96MHz) 3:Watchdog oscillator 4:RTC (32768Hz) 5:Main clock 6:FreqMe_Gpio_Clk_A pin at P1.4/P0.11 7:FreqMe_Gpio_Clk_B pin at P2.7/P0.12
5 .. 31	-

Flash controller settings: wait states and buffer (cache) usage

- **!ATTENTION!** Flash wait states
  - must be programmed properly to avoid occasional wired / hard-to-reproduce issues.
  - Insufficient wait states may still work OK in most conditions or in some batches of chips.

Max CPU MHz	Wait states (FLASHTIM)
12	0
24	1
36	2
60	3
96	4
120	5
144	6
168	7
180	8

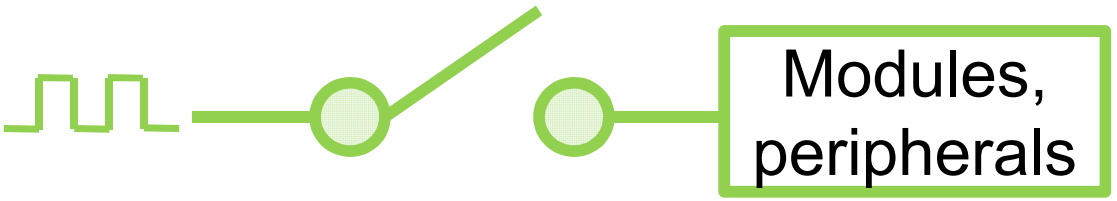
- Flash buffer usage settings :
  - Improve performance and lower power consumption by flash access
  - Configures buffer allocation for both code fetch and data access: None/one buffer/all buffer
  - code prefetch control: Allows auto read of next flash line following current execution address
  - Code prefetch priority: Allows code prefetch to preempt current ongoing fetch operations.
  - Balance between determinism and performance: can apply wait state setting regardless of buffer hit

System control for peripherals

- EMC system control
  - Address right shift for 16/32 bit bus
  - Prevent EMC from being reset except when POR, BOD happens
  - Disable burst to avoid unwanted access when accessing memory mapped I/O
- EMC feedback clock select
- EMC command delay and delay time calibration, mainly for SDRAM

- Ethernet
  - PHY interface select: MII or RMII
  - Sideband flow control
- SD/MMC
  - Phase shift controls for card driving clock and sampling clock
  - Micro-tune of delays of card driving clock and sampling clock

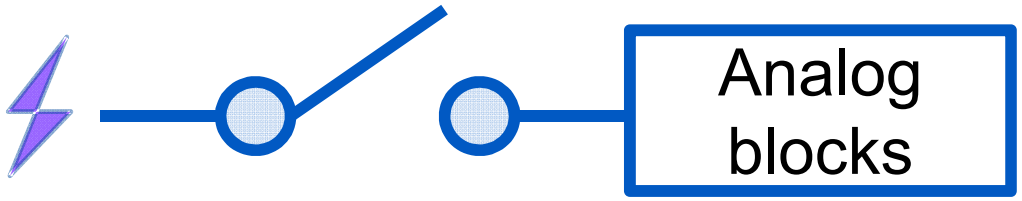
Clock gating for peripherals



- Clock to on-chip modules and peripherals clock can be stopped (gated) to fine tune power consumption
  - Memories (ROM, RAM, Flash, EEPROM)
  - Peripherals with bus masters (DMA, USB, Ethernet, SDIO, CAN)
  - AHB peripherals
  - APB peripherals
  - Async APB peripherals
- For digital part, stopping clock means power consumption is almost 0.

- One bit per target, bits are organized in control registers
  - Most modules and peripherals
    - AHBClkCtrl[3]
    - AHBClkCtrlSet[3]
    - AHBClkCtrlClr[3]
  - Async registers (Timer 3 and 4)
    - ASyncAPBClkCtrl
    - ASyncAPBClkCtrlSet
    - ASyncAPBClkCtrlClr

Power gating for analog blocks



- Power can be shut down for analog blocks
  - Clock generators: FRO, XTAL, WDT Osc, PLLs
  - VDDA, ADC, temperature sensor
  - Memories: SRAM blocks (4), EEPROM, Flash, ROM
  - USB PHY 0 and 1
  - RNG

- One bit per switch, bits are organized in control registers
  - PDRunCfg[2]
  - PDRunCfgSet[2]
  - PDRunCfgClr[2]

Wake up settings

- Controls what peripherals can wake up MCU from reduced power modes
  - **Sleep**: CPU clock stopped
  - **Deep sleep**: Sleep + clock source and flash shutdown, except WDT and RTC along with selected analog blocks can be programmed to on.
  - **Deep power down**: deep sleep + RAM shutdown, wakeup will reset the MCU.
- One bit per peripheral, bits are organized in control registers and their set/clear only companions
  - StarterP[2], StarterPSet[2], StarterPClr[2]
- Some peripherals need clock to wake in deep sleep and deep power down modes.

- Wake up sources :
  - Deep power down
    - RESET pin, RTC
  - Deep sleep
    - PinINT 0-7 and group INT 0-1
    - WDT and micro-tick timer (uTick)
    - BoD
    - All flexcomms: I2C/SPI slave mode, USART sync mode
    - RTC
    - USB need clock 0-1
    - (When clocked): DMA, timers, DMIC, USB 0-1
  - Sleep
    - All enabled interrupts

Hardware wake control for low power data batching by DMA

- Enables **low power data batching by DMA** from flexcomm or DMIC with CPU still in deep sleep mode, wakes up non-CPU part and go back to sleep after data transfer.
  1. Can prevent MCU except CPU core from entering deep sleep. (ForceWake)
  2. Can wake up MCU except the ARM core when a flexcomm has its FIFO reach threshold, then return to sleep when DMA consumes FIFO to below threshold.
  3. Like item2, but for DMIC
  4. (Use together with item 2 or 3) Even if FIFO is consumed to below threshold, return to deep sleep can be delayed until DMA completely exhausts the FIFO.

- Remarks:
  - To allow flexcomm or DMIC to work under deep sleep mode, must manually keep their clock source on when entering deep sleep.
    - Can use WDTOsc or RTC as their clock source.
  - HWWAKE is completely a normal wakeup, but CPU remains “SLEEPDEEP”.
  - Once the situation that triggered HWWAKE goes away, MCU goes back to deep sleep again, unless CPU also meets its wake up condition.
    - HWWAKE is independent from CPU wake

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