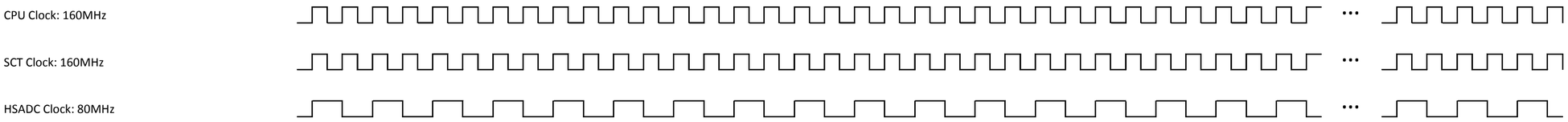
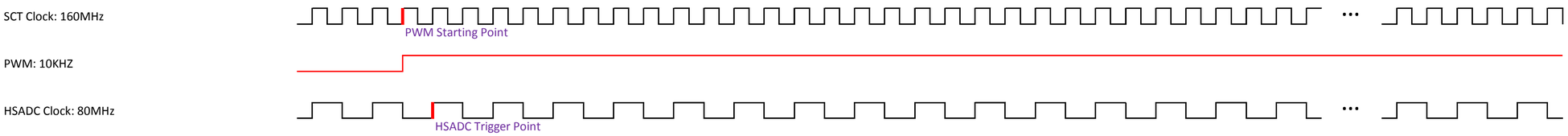
CPU Clock, SCT Clock, and HSADC Clock are all generated from Main PLL with 20MHz external crystal. The rising edges of these 3 clocks are all lined up.



SCT generates a 10KHz PWM, and this 10KHz PWM is wired to HSADC trigger (rising edge) via GIMA. PWM signal starts by software writing to the SCT control register, so PWM can either start as Scenario 1 or start as Scenario 2.

Issue: There is always a half HSADC clock cycle difference of T_PtoA between Scenario 1 and Scenario 2. For Banner TOF application, we want the T_PtoA to be fixed, i.e., we want all the T_PtoA are in Scenario 1. Or we want all the T_PtoA are in Scenario 2.

Scenario 1: **The dalay between PWM starting point and HSADC trigger point (T_PtoA): half HSADC Clock + An fixed HSADC trigger Latency**



Scenario 2: **The dalay between PWM starting point and HSADC trigger point (T_PtoA): one HSADC clock + An fixed HSADC trigger Latency**