THINKING ABOUT MIGRATING FROM 8-BIT? WAIT NO LONGER – LPC80X MCUs ARE YOUR 32-BIT ANSWER!

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OMAR CRUZ – PRODUCT MARKETER

MAY 31, 2018

SECURE CONNECTIONS FOR A SMARTER WORLD

Agenda

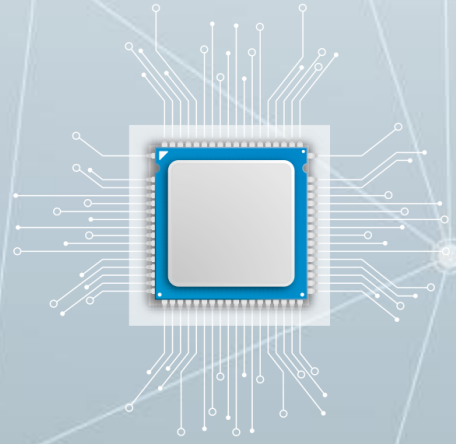
- Introduction
- LPC80x MCU Family Overview
- User case/application
- Arm® Cortex®-M0+
- Low Power Modes
- Memory (Flash + ROM)
- Clock Generation
- GPIO
- Dual Power Supply
- Analog
- Other Peripherals
- Enablement
- Summary

LPC MICROCONTROLLERS
Broad Market Leader

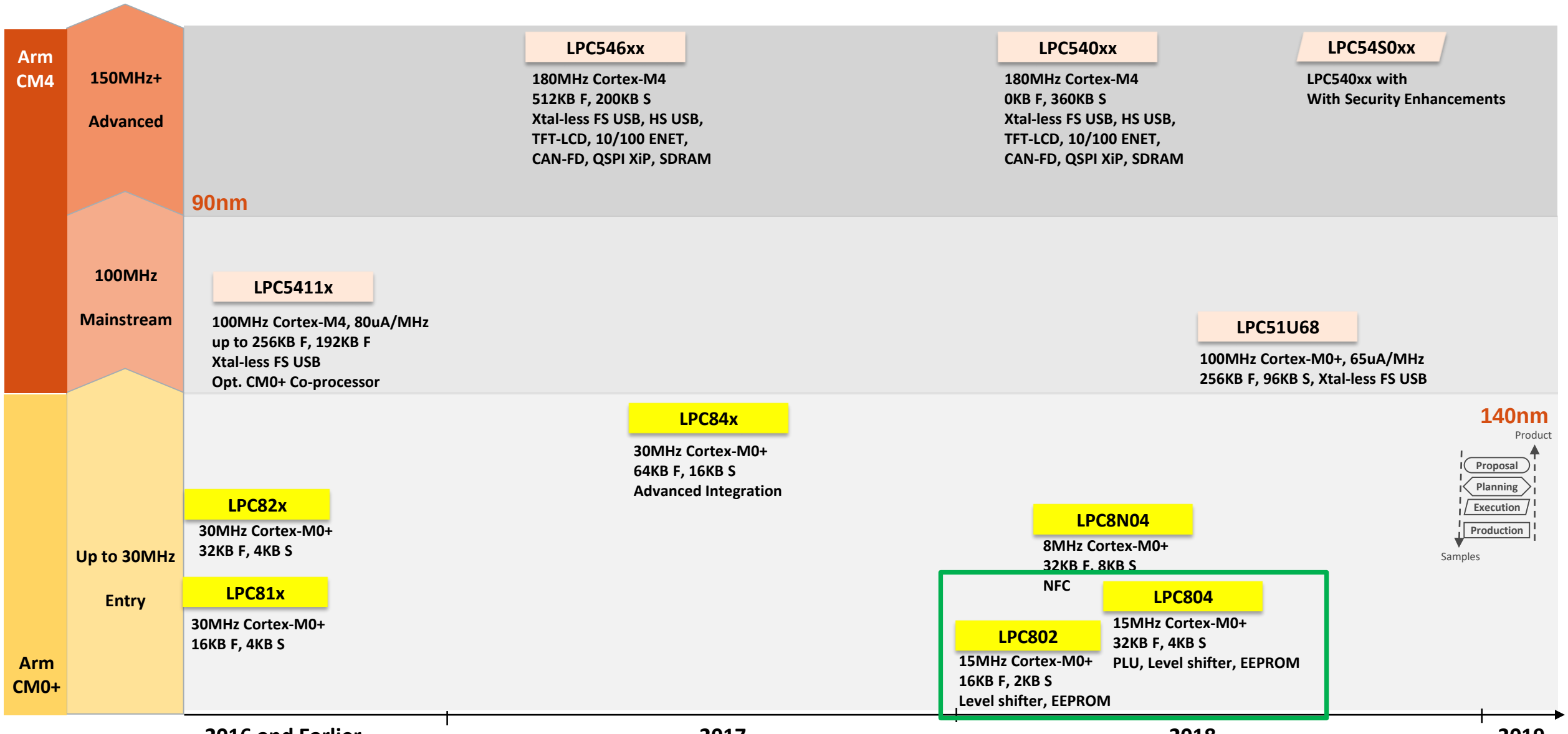
Architecting Scalable MCU Families with Flexible Integration
Enabling Fast Time To Market & Platform Re-use

1. **Innovative Arm®-based MCU Portfolio**
2. **Ecosystem & Partners**
3. **Supply, Longevity, & Quality**
4. **Local Support Network**
5. **Extensive Software & Tools**

- Accelerating the transition from 8-bit to 32-bit Arm® **Cortex-M based MCUs**
- **Low power, high performance MCUs** for energy conscious applications

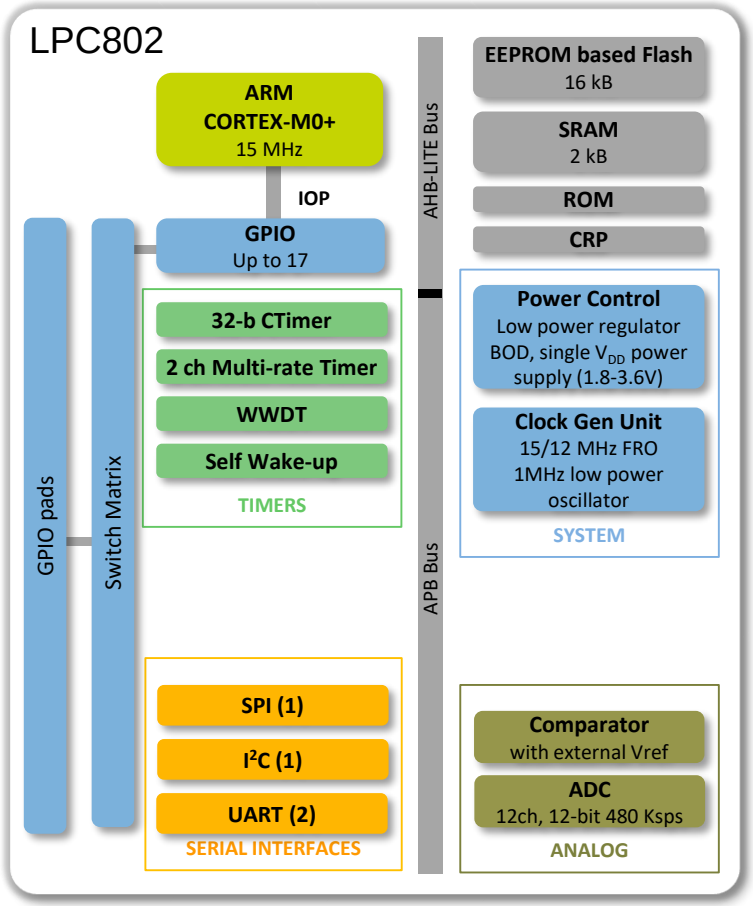


General Purpose MCU Roadmap | Power Efficient & Embedded Flash



LPC80x MCU FAMILY OVERVIEW

LPC802 MCUs: 15MHz Cortex-M0+ with 16KB Flash



Performance

- **15-MHz Cortex-M0+** ARM core
- **16 kB EEPROM-based Flash, with 64 B page size**
- 2 kB RAM

Serial connectivity and GPIOs

- 1 I2C (Fm), 1 SPI, 2 UART
- Up to 18 GPIOs with **pattern matching and level shifting**
- **Switch matrix** for flexible I/O pin assignment

Analog

- 12ch, 12-bit 480 Ksps ADC
- Analog Comparator: 4 input pins
- **Level shifter option**

Timers

- 1x 32-bit CTimer
- 2-ch Multi-Rate Timer (MRT)
- Wakeup Timer
- Watchdog Timer

Single **power supply**: **1.71 to 3.6V**

Temperature range: **-40 to +105 ° C** (ambient)

Packages: TSSOP16, TSSOP20, HVQFN33, WLCSP16 (Q3, 2018, engineering sample: Now)

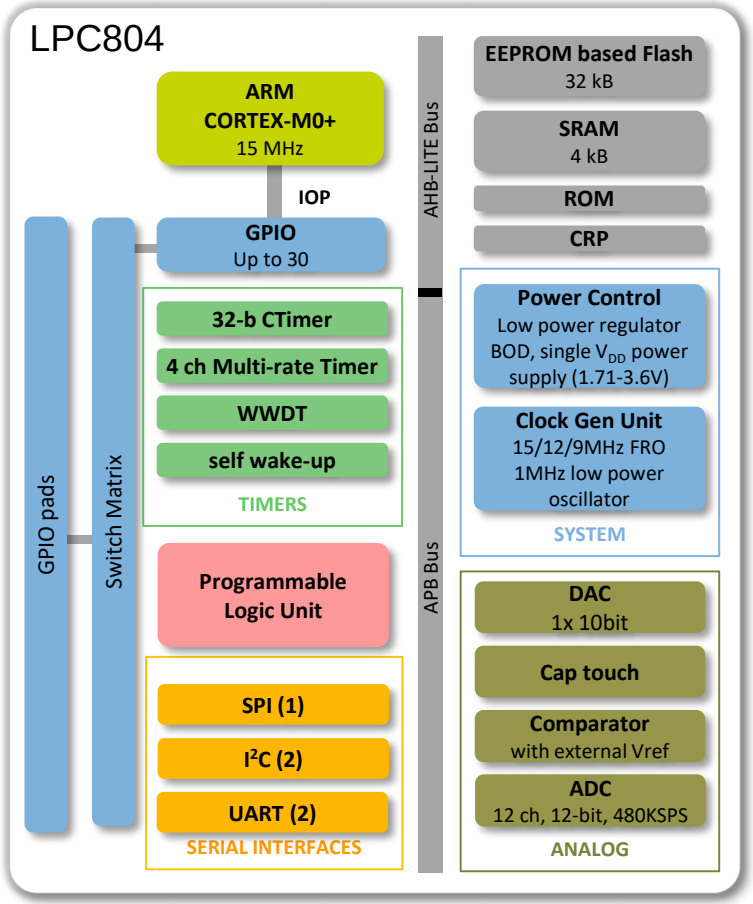
Key Differentiators

- Power optimized 15 MHz Arm Cortex-M0+ core
- 32-bit MCU alternative to 8-bit MCU
- Level shifting option thanks to separate power rails
- Switch matrix capability
- Small footprint in popular packages

Product Availability

In Mass Production Now

LPC804 MCUs: 15MHz Cortex-M0+ with 32KB Flash



System

- **15-MHz Cortex-M0+** ARM core
- Up to **32 kB EEPROM-based Flash, with 64 B page size**
- Up to 4 kB RAM

Serial connectivity and GPIOs

- 2 I2C (Fm), 1 SPI, 2 UART
- Up to 30 GPIOs with **pattern matching and level shifting**
- **Switch matrix** for flexible I/O pin assignment

Analog

- 12-bit, 480ksps ADC
- Analog Comparator: 4 input pins
- **1x 10-bit DAC**
- **Level shifter option**
- **Capacitive Touch**

Timers

- 1x 32-bit CTimer
- 4-ch Multi-Rate Timer (MRT)
- Wakeup Timer
- Watchdog Timer

Programmable Logic Unit (PLU)

- For customer defined sequential and combinational logic

Single **power supply**: **1.71 to 3.6V**

Temperature range: **-40 to +105 °C** (ambient)

Packages: TSSOP20, TSSOP24, HVQFN33, WLCSP20(Q4, 2018)

Product Longevity

Key Differentiators

- Power optimized 15 MHz Arm Cortex-M0+ core
- 32-bit MCU alternative to 8-bit MCU
- Level shifting option thanks to separate power rails
- Logic replacement with integrated MCU
- Advanced Analog Integration with DAC & Cap Touch
- Switch matrix capability
- Small footprint in popular packages

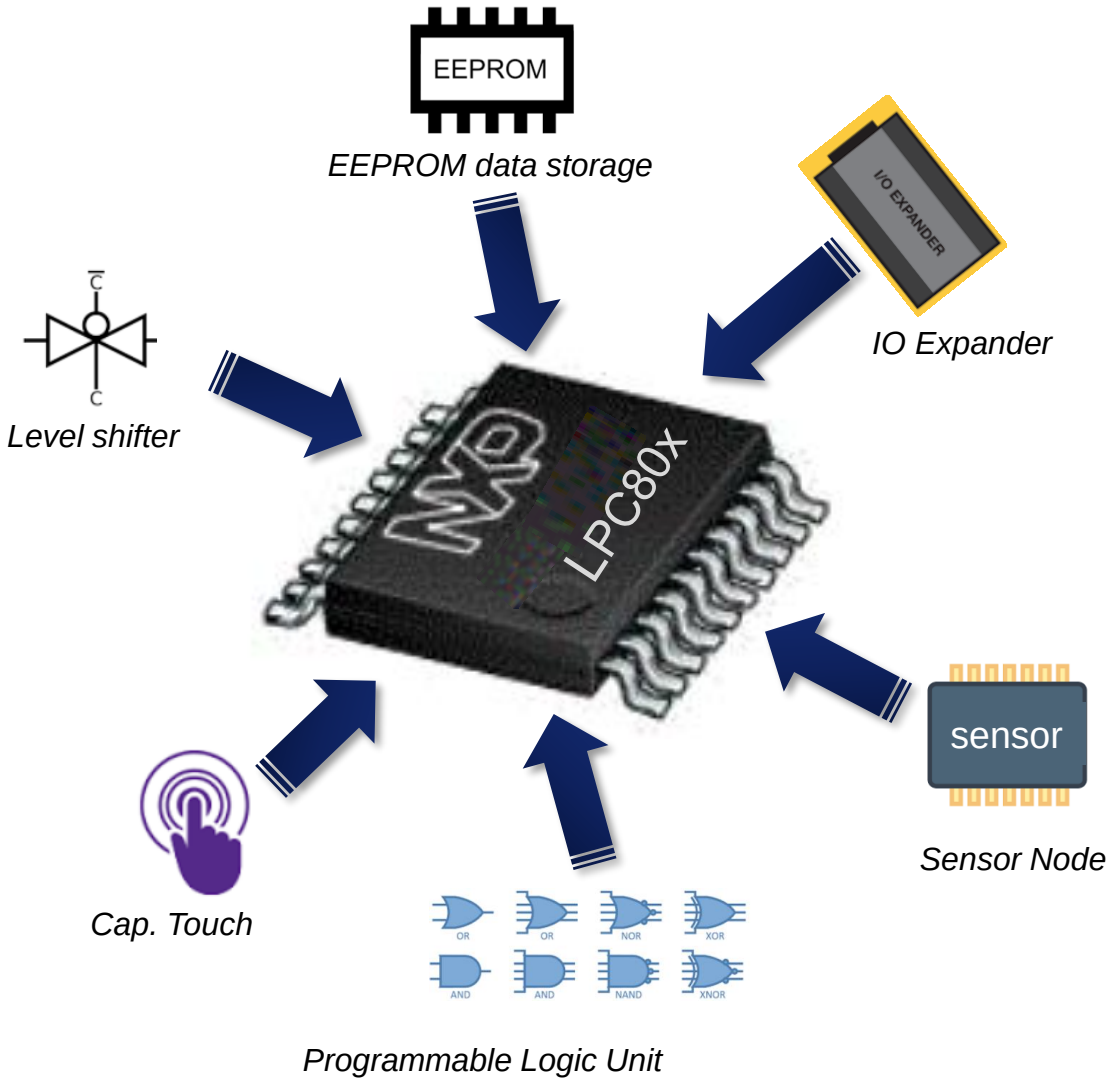
Product Availability

In Mass Production Now

Excellent Companion Processor

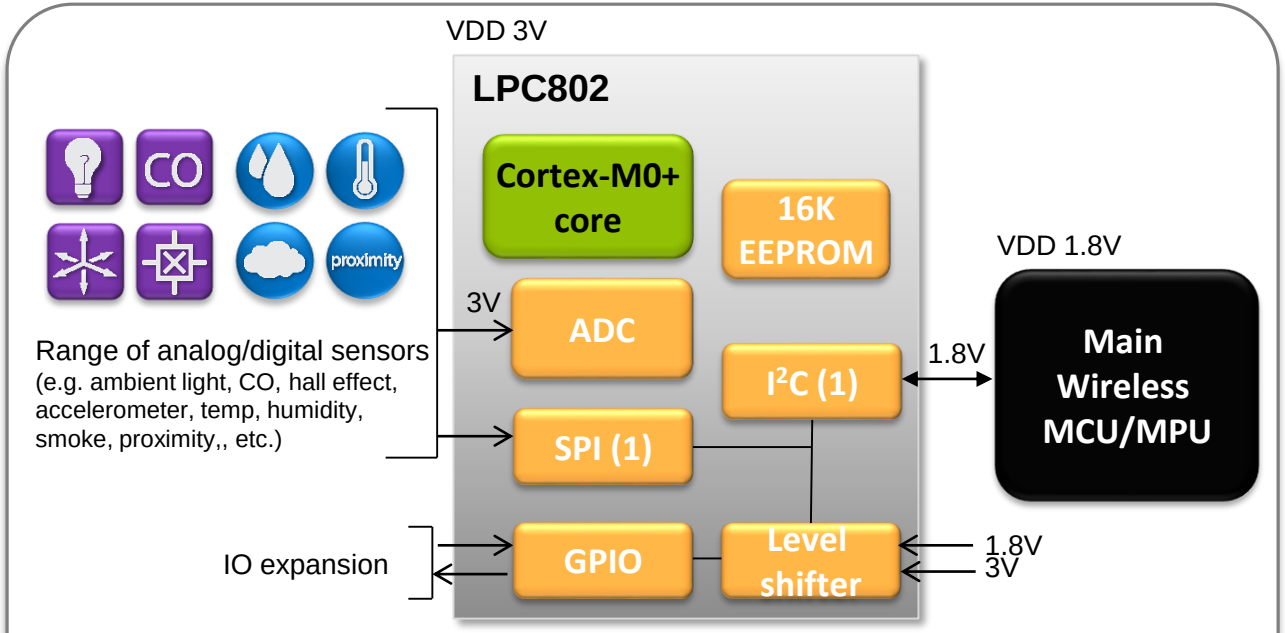
EEPROM (100K+ R/W cycles)

+ IO expander (I2C/SPI/UART I/F)
+ Level shifter (e.g. 3.3V->1.8V)
+ Small logic units (AND/OR/NAND/Flip-Flop, etc.)
+ Power efficient sensor node controller
+ PMU (Power Management Unit)
+ Cap. touch
+ GPIO control
+ Smaller footprint for all of above features



Low-Cost Companion MCU for Robotic Vacuum

Example Application for LPC802



NXP Recommended 'Attach' Products:

- **Digital Sensors:**
  - MMA8451Q (Accelerometer)
  - FXLS8471Q (Accelerometer)
  - MMA8652FC (Accelerometer)
  - FXAS21002C (Gyroscope)
  - FXOS8700CQ (Accel. + Mag.)
  - MAG3110 (Magnetometer)

- **LPC802 for broad range of main MCU/MPU resource extension**
  - Analog sensor interface (light, motion, CO, etc.)
  - Digital sensor interface (temp, humidity, smoke, etc.)
  - Companion MCU for wireless MCU/MPU-based applications
- **LPC802 provides**
  - EEPROM storage for MCU/MPU
  - I2C to ADC interface to main MCU/MPU
  - 12-bit ADC for multiple analog sensors
  - SPI, I²Cs for connectivity and digital sensor interfaces
  - Wake-up IO to wake up main MCU/MPU
  - Tiny WLCSP (1.86x1.86 mm) package

LPC800 Series MCU Target Applications

- **Power- and size-sensitive control and connectivity tasks such as:**
  - Sensor gateways – connect to & concentrate data from analog and/or digital sensors
  - End-node connectivity, e.g. NFC, BLE, Zigbee ,etc.
  - Capacitive touch for HMI
  - Simple motor control
  - 8/16-bit applications
- **In wide range of entry-level products in Consumer, Industrial, IoT, Wearable, and Gaming markets, such as:**
  - Thermostats and home environment monitoring devices
  - Gaming controllers
  - Home & building automation
  - Industrial controls
  - Lighting
  - Server/rack monitoring
  - Portable/Wearable fitness products
  - And many more…



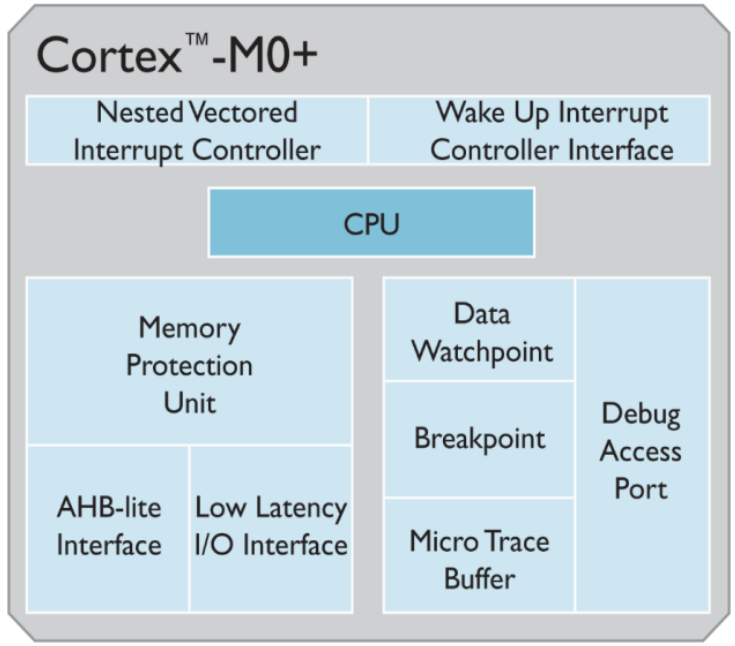




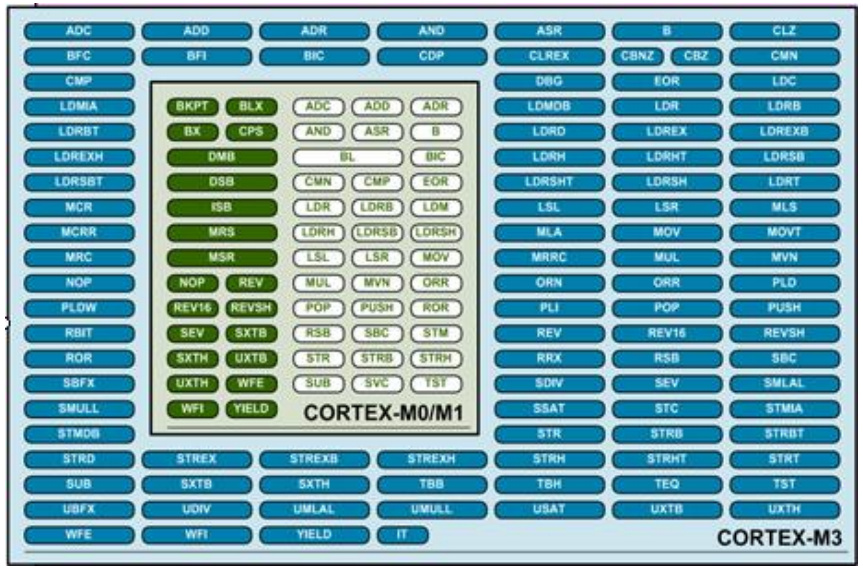
ARM CORTEX-M0+ CORE TECHNOLOGY OVERVIEW

Arm Cortex-M0+ Core Technology Overview

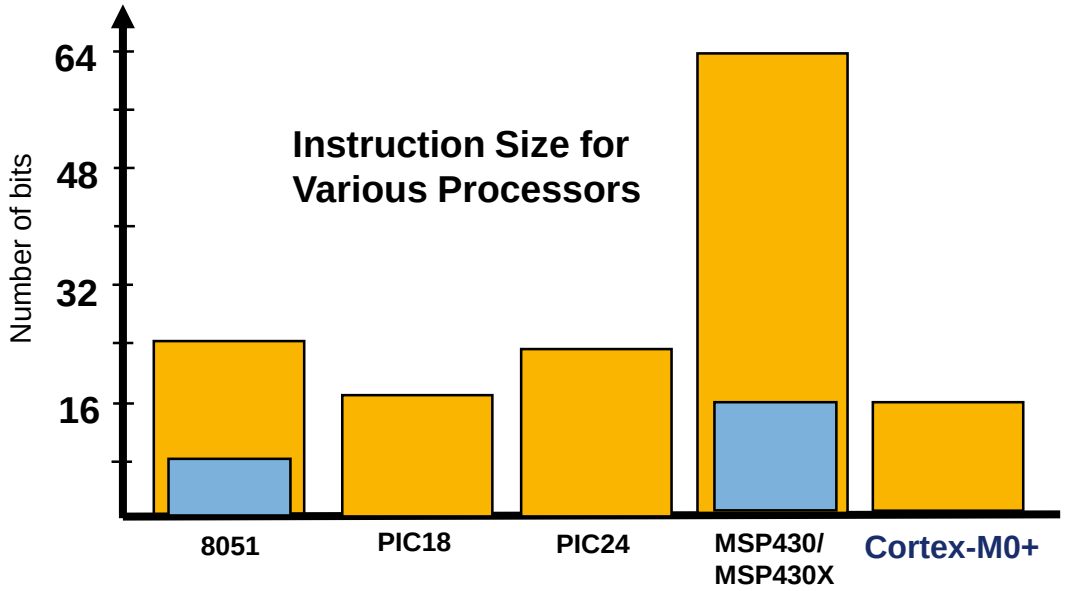
- High performance 32-bit CPU
- 2 stage pipeline
- Performance efficiency
  - 1.77 CoreMark/MHz - 0.93 DMIPS/MHz
- Deterministic operation
- Single cycle IO
- Built-in Nested Vectored Interrupt Controller (NVIC) with Wake-up Interrupt Controller (WIC)
- Debug using 2 pins with up to 4 breakpoints and 2 watchpoints
- Micro Trace Buffer (MTB)
- Vector Table relocation
- Thumb2 instructions (56 instructions)

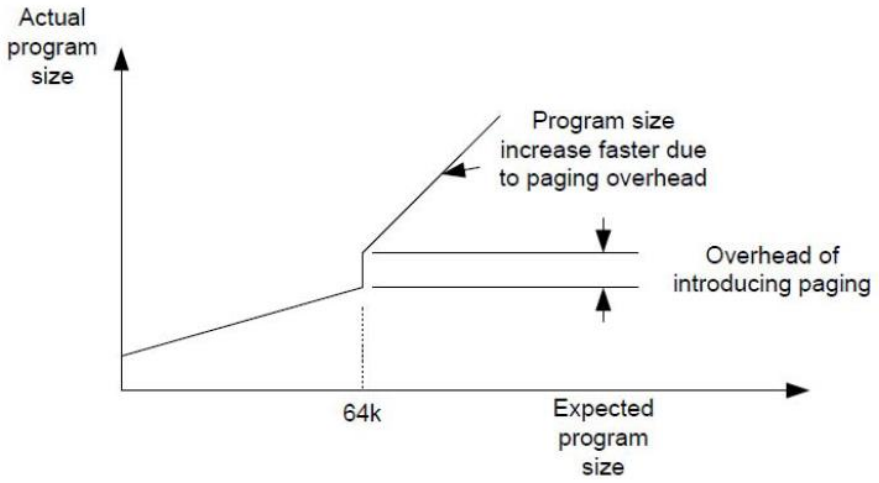


Superior Code Density



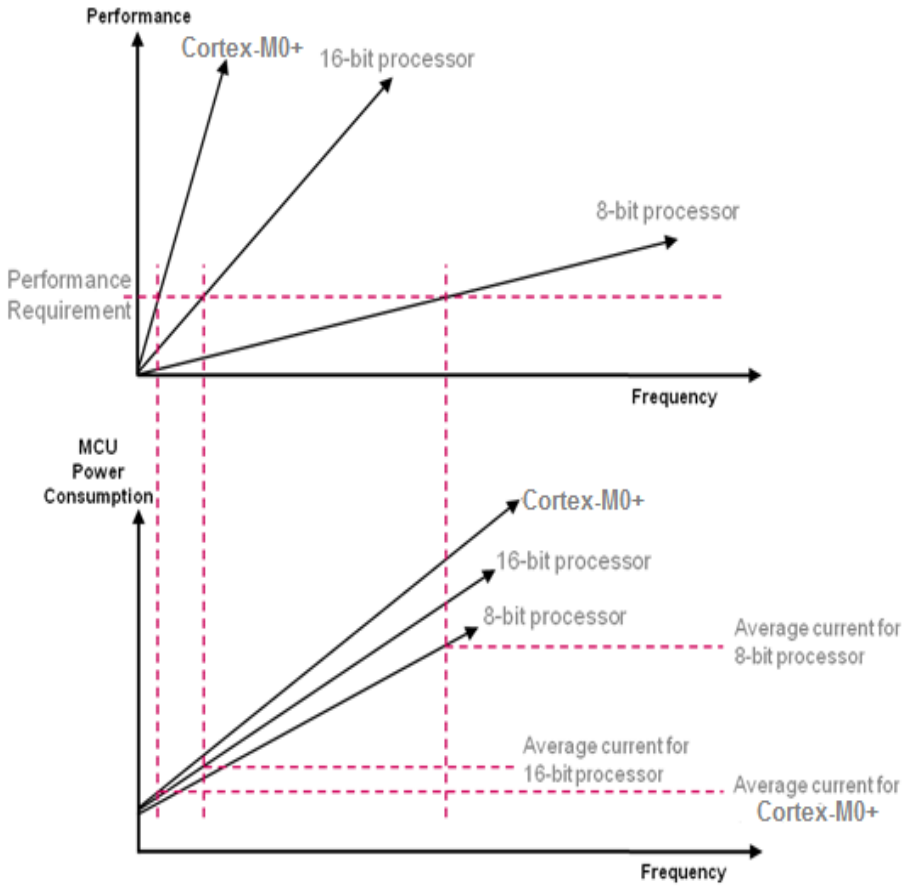
- Leading to superior code density:
  - In Cortex-M0/M0+ all instructions (except BL) are **16 bits wide** instructions
  - **Over 64kB of address space,** 8- and 16- processors have to introduce paging, leading to extra overhead in code

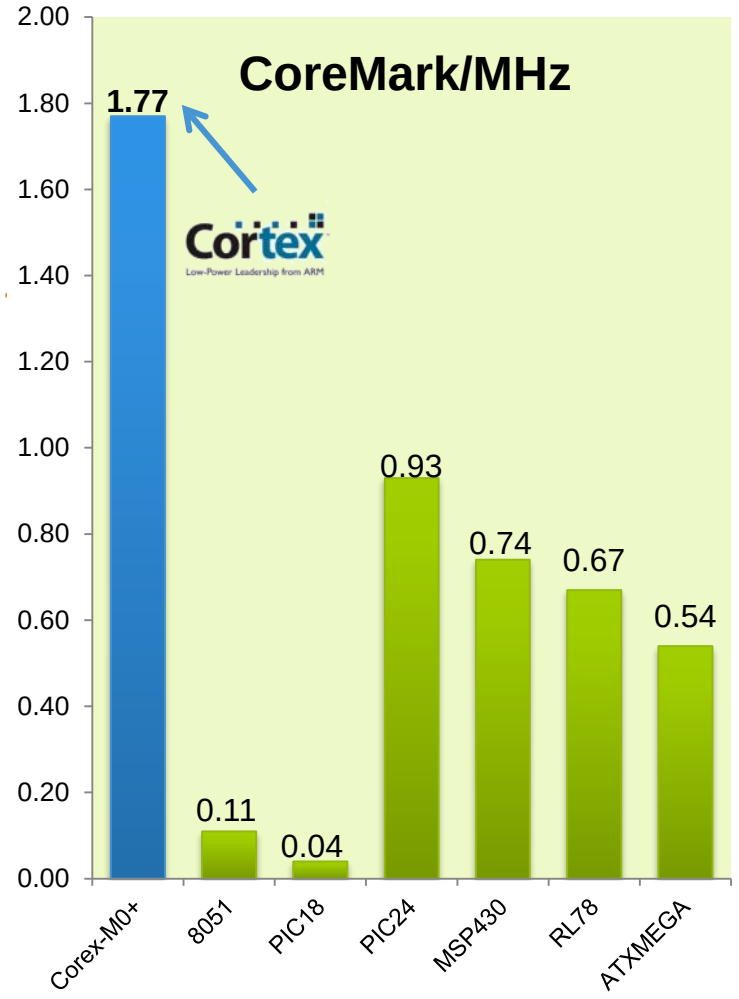




Cortex-M0+ - Energy Efficiency

- Cortex-M0+ runs at a much slower clock frequency for the same required performance
  - ✓**>2x CoreMark/mA performance** than the closest 8/16-bit competitor
- Cortex-M0+ can sleep most of the time, or it can handle additional tasks

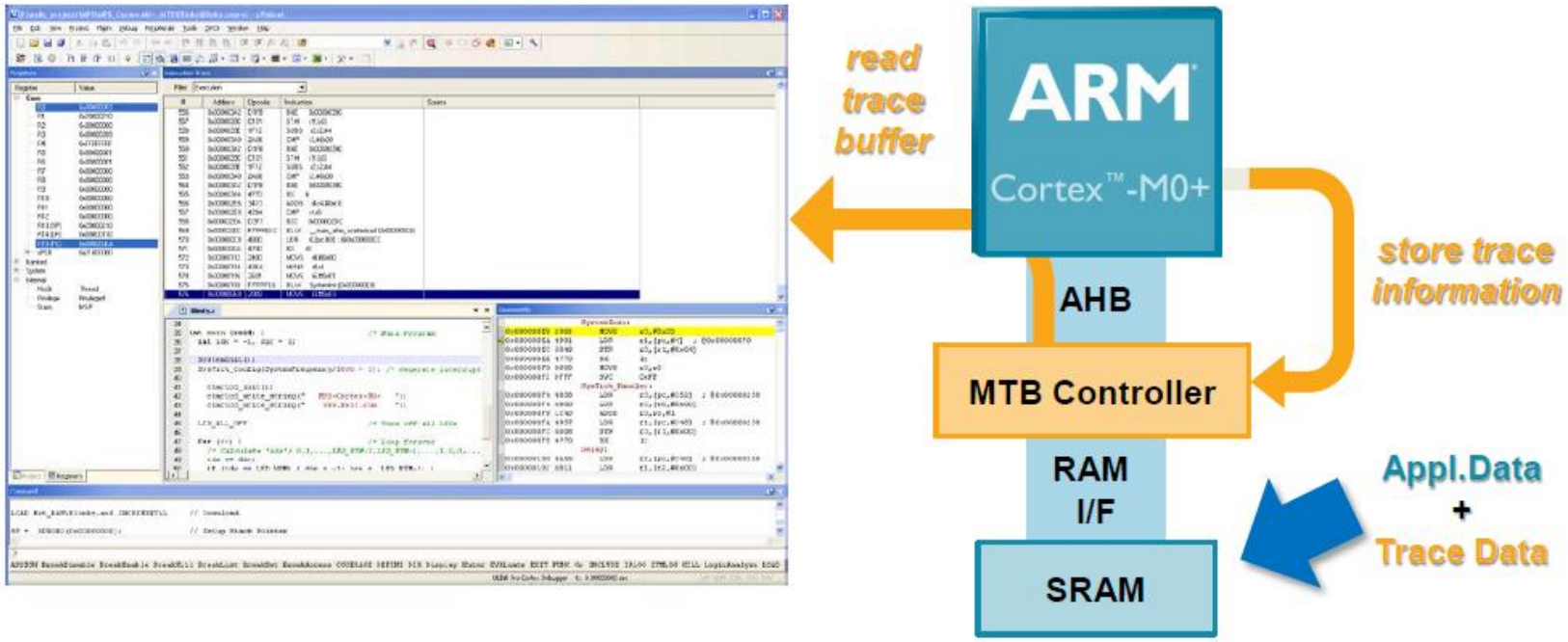




Official data: www.coremark.org

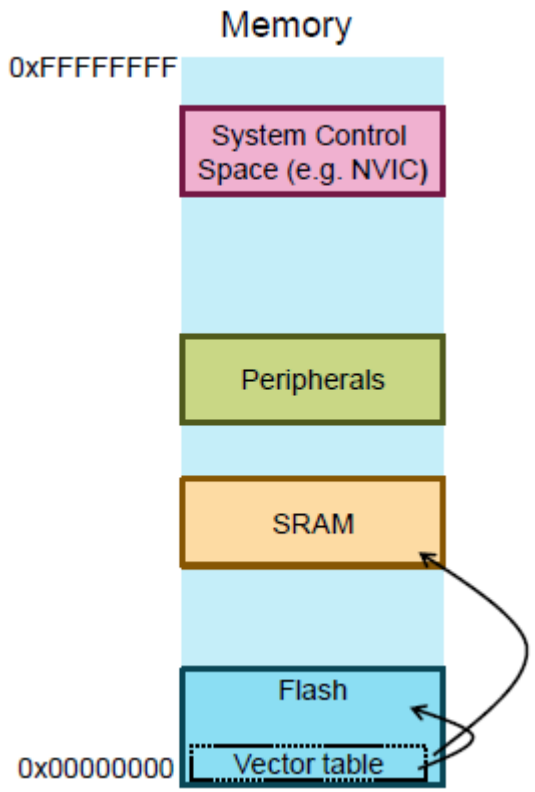
Cortex-M0+ Micro-Trace Buffer (MTB)

- Trace store in RAM (non-instructive)
- Read over Serial Wire / JTAG (CPU stopped)



Cortex-M0+ Vector Table Relocation

- Relocate vector table in other locations in flash or SRAM
- Exception vector reconfiguration at runtime



LOW POWER MODES

Low Power Modes

Low Power Mode	Impact	Wake-Up Sources	Current Consumption (LPC802)	Current Consumption (LPC804)
Sleep	System Clock to Cortex-M0+ is stopped. Peripherals and memories are active. Processor state and registers, peripheral registers, and internal SRAM are maintained, and the logic levels of the pins remain static	Any peripherals interrupts (SCT, MRT, USART, SPI, I2C, CMP) Pin interrupts & Pattern Match Engine BOD interrupt and reset WWDT interrupt and reset External Reset Self Wake-up Timer	0.6 mA @15MHz,3.3V	0.6 mA @15MHz,3.3V
Deep Sleep	Peripherals receive no internal clocks. Flash is in stand-by mode. Peripherals and memories are active. Processor state/registers, peripheral registers, and internal SRAM contents are maintained, and the logic levels of the pins remain static	Interrupts from USART, SPI, I2C Interrupt from Capacitive Touch Pin interrupts BOD interrupt and reset WWDT interrupt and reset External Reset Self Wake-up Timer	100 µA	100 µA
Power-Down	Peripherals receive no internal clocks. The flash memory is powered down. Processor state/registers, peripheral registers, and internal SRAM contents are maintained, and the logic levels of the pins remain static	Interrupts from USART, SPI, I2C) Pin interrupts BOD interrupt and reset WWDT interrupt and reset External Reset Self Wake-up Timer	6 µA	6 µA
Deep Power-Down	The entire system is shut down except for four 32-bit general purpose registers in the PMU and the self wake-up timer. Register states and internal SRAM contents are lost	Wake up on a pulse on the WAKEUP pin, RESET pin, or when the self wake-up timer times out. On wake-up, the part reboots.	150 nA	150 nA

MEMORY

LPC802 MCU Memory Block

- Flash
  - EEPROM based, no ERASE needed
  - 1kB virtual sectors with 64-byte page program/erase
  - Organization: 16 sectors x 16 pages/sector x 64 bytes/page
  - 64 Byte page erase and write
  - Erase &Program Time
    - ~2.5ms
  - Endurance
    - 500,000 cycles (typ.)

Feature	LPC802 as I²C EEPROM	Traditional I²C EEPROM
Capacity (bit)	> 64Kbit	Typ: 64Kbit
Page Size	64B	- (Byte mode); 64B (Page mode
Endurance (E/P cycles)	Typ.: 500K , min: 200K	Typ: 1000K (Byte mode) Typ: 100K (Page mode)
Retention (years)	20	>=100
Write time (ms)	2.9/page	5
IO expander	Yes	No
Level shifter (1.8 – 3.3V)	Yes	No
PLU (AND/OR/NAND, …)	Yes	No
Sensor connection	Yes	No

Code Read Protection Levels

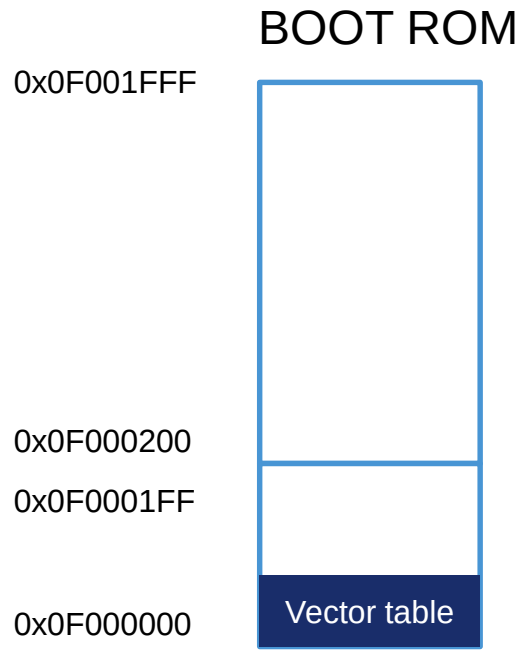
- Four levels of the Code Read Protection
- This feature allows user to enable different levels of security in the system so that access to the on-chip flash and use of the SWD and ISP can be restricted
- When needed, CRP is invoked by programming a specific pattern into a dedicated flash location
- Program CRP pattern at location @2FC

	Read Code	Full Chip Erase	Erase Sectors	Program Sectors	SWD Access
NO CRP	**Enabled**	**Enabled**	**Enabled**	**Enabled**	**Enabled**
CRP 1	Disabled	**Enabled**	**Enabled**	**Enabled**	Disabled
CRP 2	Disabled	**Enabled**	Disabled	**Enabled**	Disabled
CRP 3	Disabled	Disabled	Disabled	Disabled	Disabled
NO_ISP	No Protection (SWD can read)	Disabled	Disabled	Disabled	**Enabled**

ROM

BOOT ROM

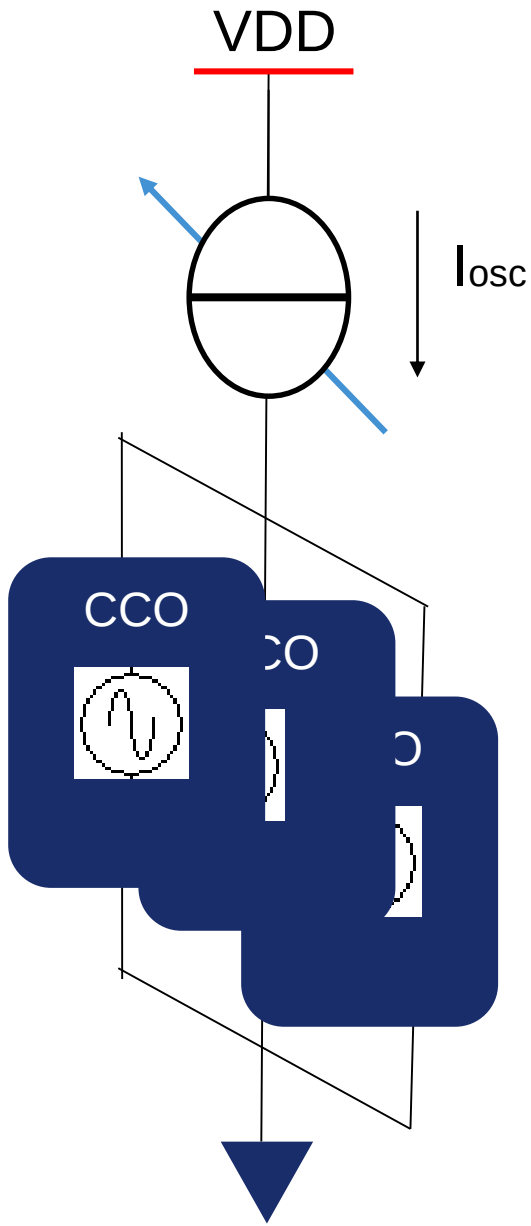
- 8 KB on-chip ROM
- Bootloader
  - In-System Programming (ISP) API calls
  - Update FLASH via USART, I2C or SPI
- ROM API
  - In-Application Programming (IAP) of flash memory
  - Integer divide routines
  - FRO API
- Memory map
  - 0x0F000000 – 0x0F001FFF



CLOCK GENERATION UNIT

Free Running Oscillator (FRO)

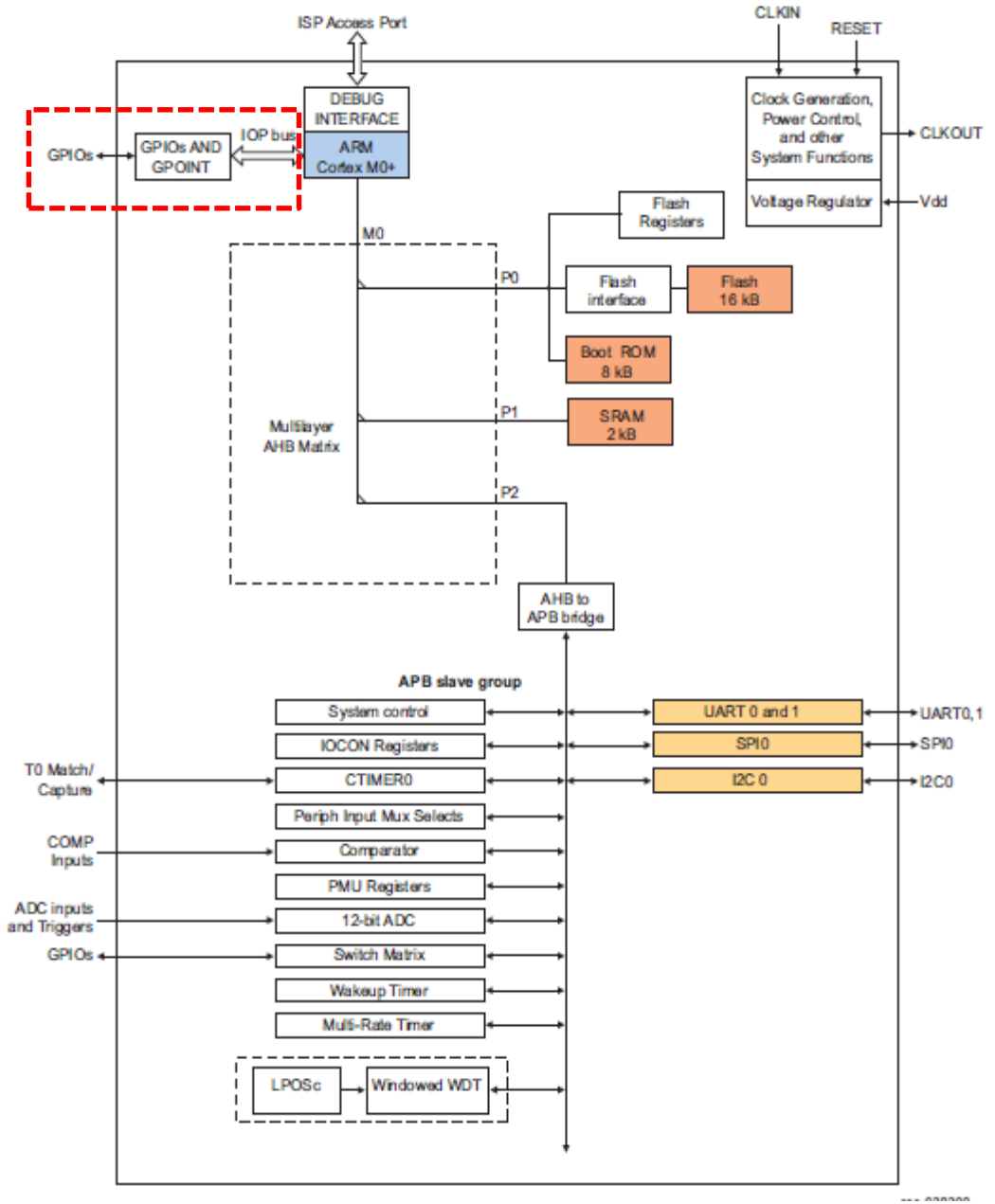
- Low power internal Free-Running Oscillator
  - ~74 uA, replaces former “IRC”
- Fast startup
  - ~50 us
- Provides selectable outputs
  - 15 MHz, 12 MHz or 9 MHz which can be divided
- Factory Trimmed 15 MHz/12 MHz/9 MHz
  - +/- 1% accuracy over 0 C to 70 C
- Some peripherals allow asynchronous operation from FRO while CPU operates from main clock
- FRO can be used as Main clock or PLL clock source
- Reduces dependency on System PLL
  - Benefit: fast restart after halting the CPU by sleep modes
  - Benefit: low power!



GPIO

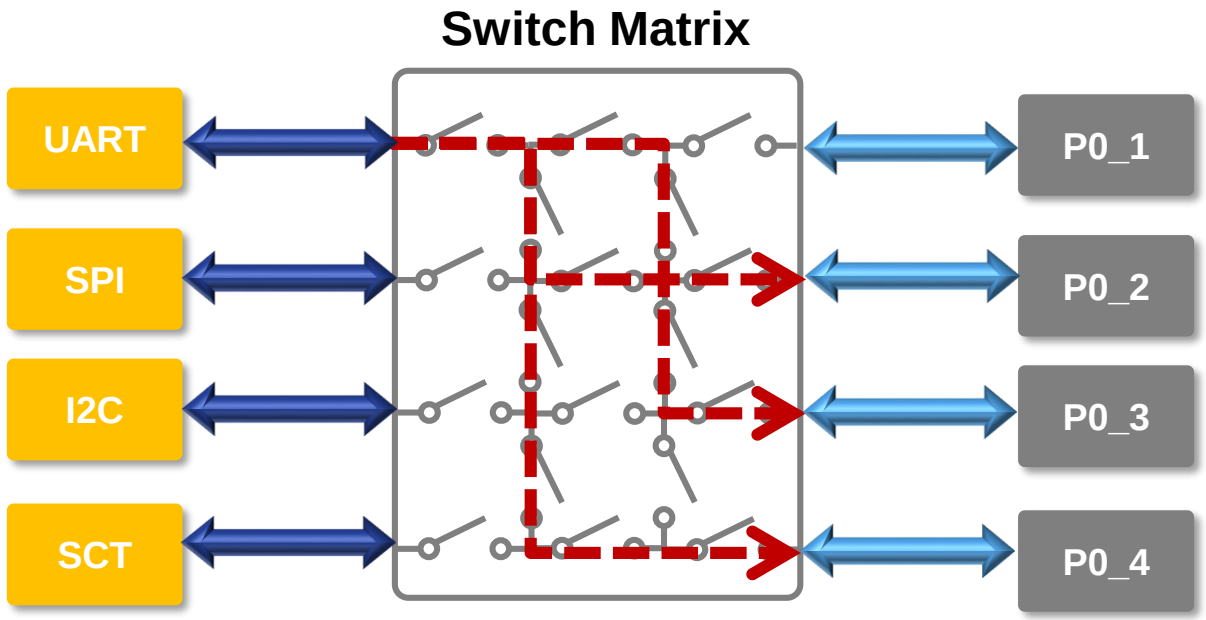
Flexible I/O Port

- **Single cycle** access to all port pins
- **Support high frequency I/O toggling**
  - As fast as CPU_Clock/2
- **Enhanced GPIO Pin Manipulation**
  - Capable of simultaneously reading Bit/Byte/Word or toggling up to all I/Os per two instructions
  - Return pin state anytime regardless of direction, masking or alternate functions for digital functions
- Up to 8 pins can be selected from all GPIO pins as edge- or level-sensitive **interrupt** requests
- **Programmable** Internal pull-up/pull-down resistor, open-drain function, input inverter, and repeater mode
- High-current source output driver/**high drive** (20 mA)



Switch Matrix

- **Movable functions**
  - Can be assigned to any external pin that is not power or ground
  - UART, SPI, I²C, SCT, comparator output, CLKOUT, pattern match output, and Ctimer
- **Fixed pin functions**
  - Oscillator pins, comparator input, GPIOs
  - Can be replaced by movable functions

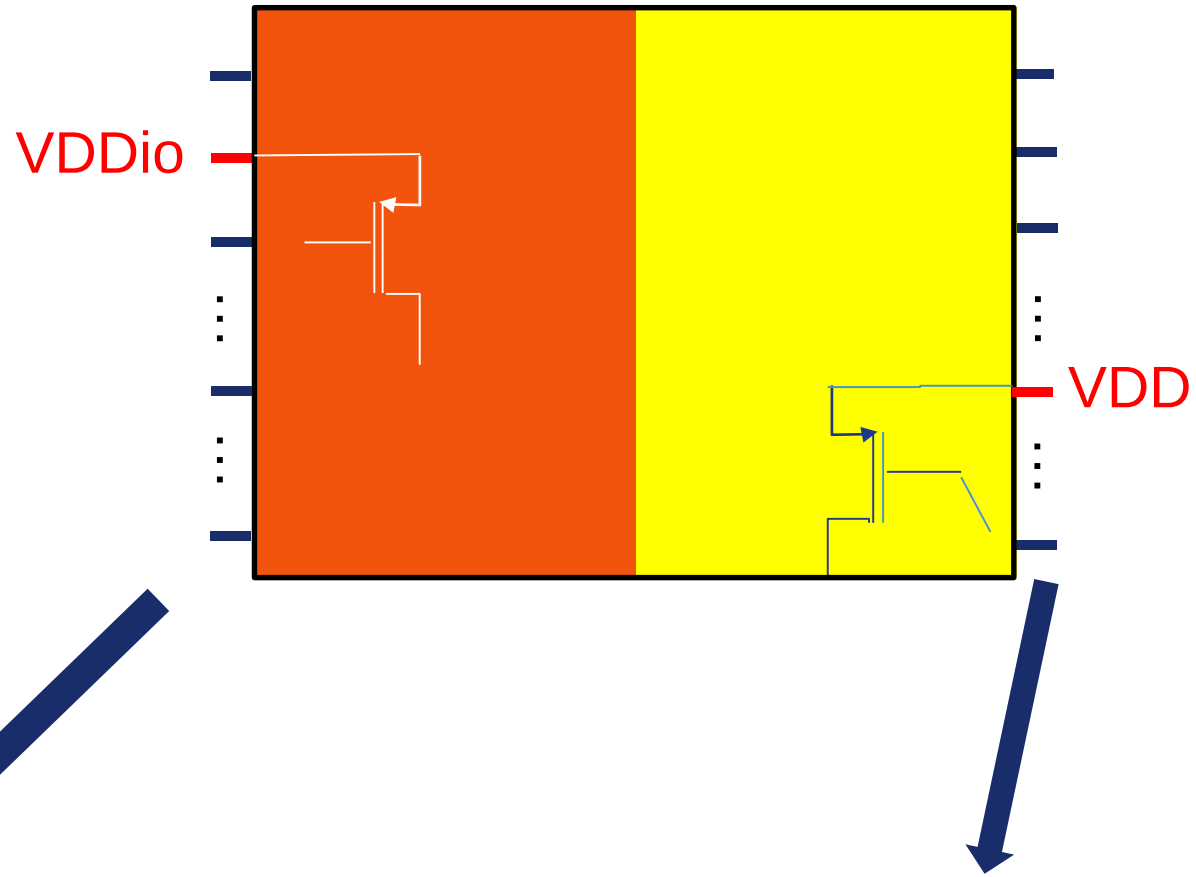


DUAL POWER SUPPLY

Dual Power Supply

- Support level shifting without external components and circuit
  - Save BOM
  - 2 different power domains: VDDio, VDD on separate package sides
    - Each package side refers to its side power supply
    - Digital: 1.71 to 3.6V
    - ADC: 2.5 to 3.6V
    - DAC: 2.7 to 3.6V
- Only applied to specific parts
  - **LPC802M011JDH20**
  - **LPC804M111JDH20**

LPC802 dual supply



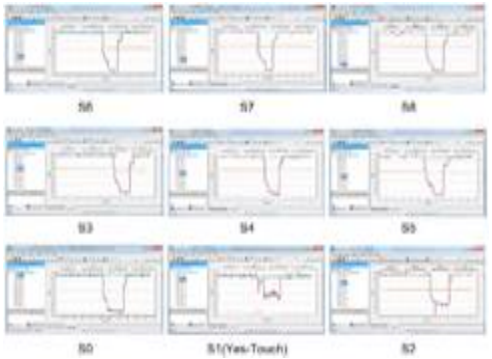
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7xVDDio		-	V
V_{IL}	LOW-level input voltage			-	-	0.3xVDDio	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		VDDio – 0.4		-	V
		I_{OH} = 3 mA; 1.71 V <= V_{DD} < 2.5 V		VDDio – 0.5		-	V

V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7xVDD		-	V
V_{IL}	LOW-level input voltage			-	-	0.3xVDD	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		VDD – 0.4		-	V
		I_{OH} = 3 mA; 1.71 V <= V_{DD} < 2.5 V		VDD – 0.5		-	V

ANALOG

Cap Touch – LPC804 MCUs

- Similar IP to LPC845 Cap Touch
- Mutual capacitive based
- Support different shapes of touch
  - up to 5 keys (pads)
  - rotary
  - slider
- Capable of gesture recognition
- FreeMaster based PC calibration tool
- Passed IEC61000-4-6 certification/current injection test



AUDIX®

AMC410-12 Injected Currents Susceptibility Test Data

Project No.: /

Immunity	Injected Currents Susceptibility	☑ IEC 61000-4-6: 2010 ☒ Others: / ☑ PASS / ☒ FAIL

*Applicant: NXP Semiconductors (China) Limited

*EUT: LPC845 CapTouch Board

*M/N: LPC845 CAPT *S/N: LPC845M301

Ambient Condition: 22 ℃ 50 %RH

Atmosphere Pressure: 101.3kPa

*Modulation Signal: ☑ 1kHz 80%AM / ☒ 200Hz 50% duty cycle

*Modulation: ☒ None / ☑ AM / ☒ Pulse

*Operation Mode: Operation *Dwell Time: 1s *Frequency Step: 1%

Frequency Range	*Injected Position	*Strength (unmodulated)	*Criterion	Result
0.15~230MHz	AC Mains	3 V (rms)	A	A/PASS
0.15~80MHz	/	/	/	/

*Operation Mode: / *Dwell Time: / s *Frequency Step: / %

Frequency Range	*Injected Position	*Strength (unmodulated)	*Criterion	Result
0.15~80MHz	/	/	/	/
0.15~80MHz	/	/	/	/

Test description: The EUT is no change during the test.

Analog Peripherals

Analog to Digital Converter

- 2-bit successive approximation
- Input multiplexing among 12 pins
- 12-bit conversion rate up to 480 Ksps

DAC

- 10-bit digital to analog converters
- Resistor string architecture
- Maximum update rate of 1 MHz

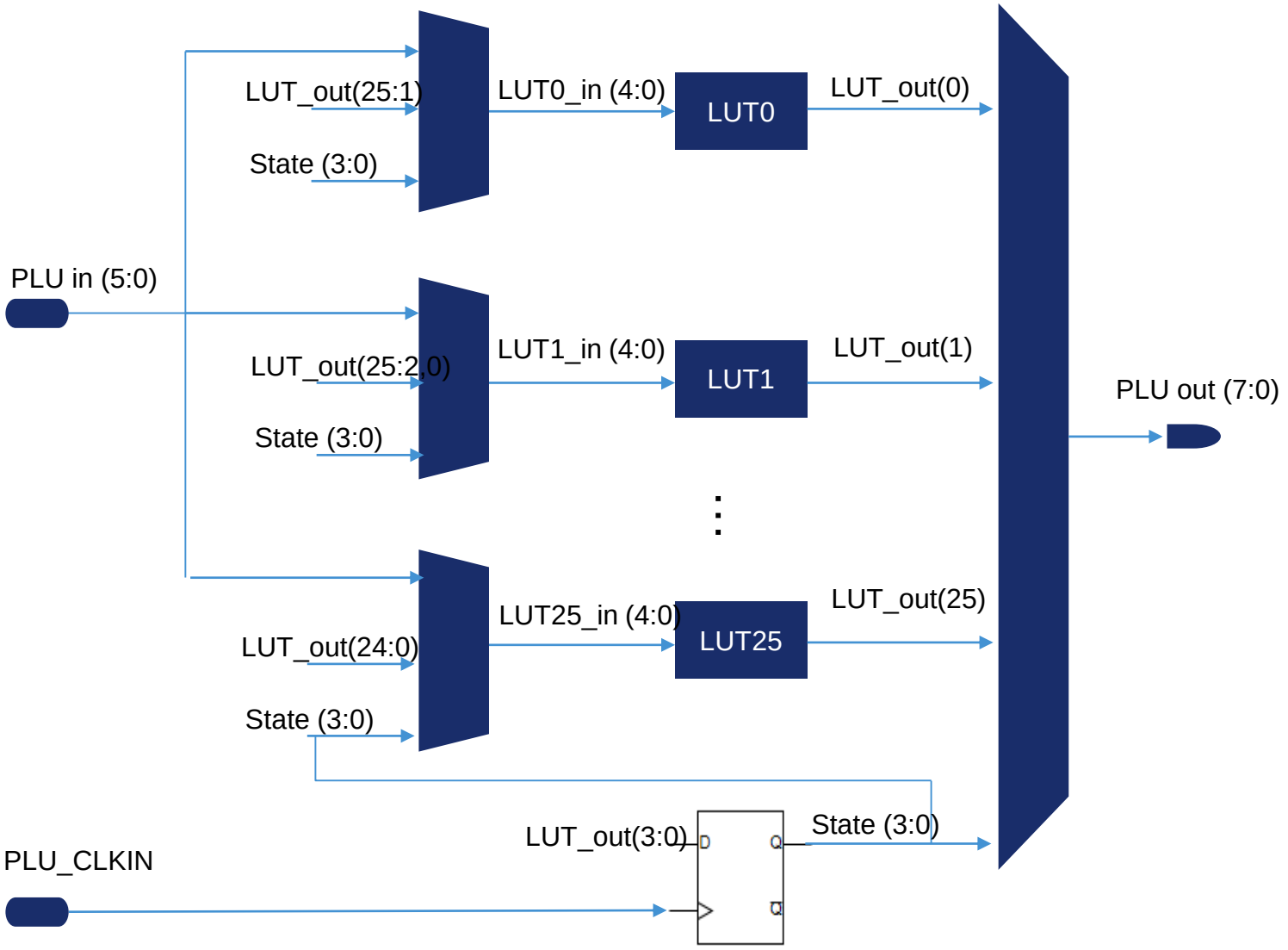
Analog Comparator

- 5 inputs are multiplexed separately to the positive voltage input and negative inputs
- The Internal voltage reference (0.9 V bandgap reference) and DACOUT can be used as either the positive or negative input of the comparator
- 32 levels of Comparator reference voltage for fine grain comparison

PROGRAMMABLE LOGIC UNIT (PLU)

PLU Features

- Create combinational and sequential logic networks
- 32-bit Truth Table - Look-up Table (LUT) based
- 4 state flip-flops
  - Clocked by external from PLU_CLKIN pad
- 6 inputs + 8 outputs to pad
  - Movable functions via SWM
- PLU bus clock can be shut off to conserve power
- Support low power mode including deep-sleep and power-down mode
- A GUI based PLU Tool available to facilitate the configuring work of PLU



OTHER PERIPHERALS

Other Peripherals

Timers

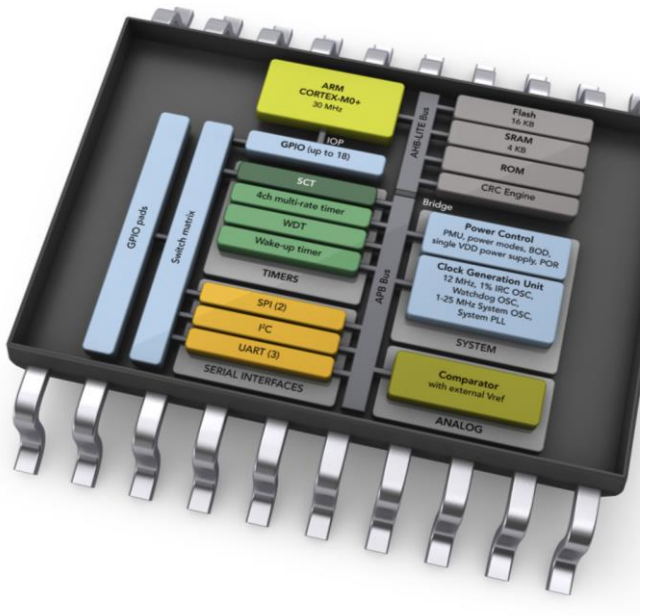
- Standard 32-bit Timer
- Multi-Rate timer (MRT)
- Self wake-up timer (WKT)
- Windowed watchdog timer (24-bit timer)
- SysTick Timer (24-bit timer)

Pattern Match Engine (PME)

- Pin Interrupt generator
- Pattern match feature

Serial Interfaces

- USART
- I²C
- SPI



Cyclic Redundancy Check (CRC) Engine

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32
- Accept any size of data width per write: 8, 16 or 32-bit

ENABLEMENT

Enablement: LPCXpresso802 Board (OM40000)

- LPC802 Arm Cortex-M0+ running at up to 15MHz
- On-board CMSIS-DAP debug interface
  - Supported by MCUXpresso IDE and popular 3rd party IDEs
  - Includes VCOM port based on LPC11U35 MCU
- Debug connector to allow debug to target LPC802 MCU using an external probe
- LPC802 ISP and User/Wake buttons
- LPC802 Reset button
- 1Mb Winbond SPI flash
- NXP LM75BDP temperature sensor
- Detachable board section with LEDs and potentiometer for prototyping and demo development
- I2C Grove connector for easy connection of sensors, or to use the LPCXpresso802 as an I/O expander peripheral

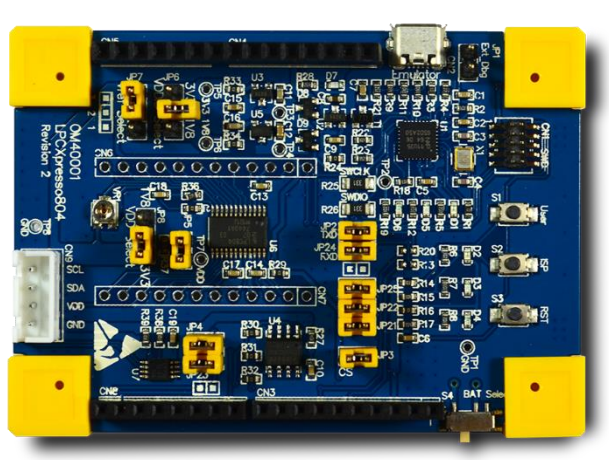
Orderable Part Number: ***OM40000UL***
http://www.nxp.com/demoboard/OM40000

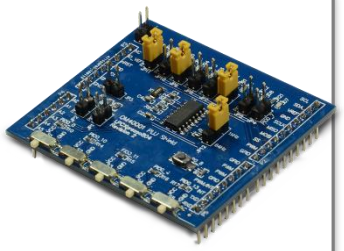
- ✓ **NXP Software Code Bundle**
- ✓ **Free MCUXpresso IDE & 3rd Party Options**

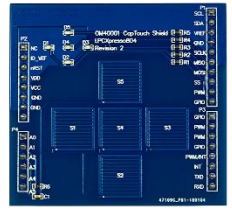
NXP IDE IAR SYSTEMS KEIL Tools by ARM

Enablement: LPCXpresso804 Board (OM40001)

- 3-board set, comprising LPCXpresso804 board with PLU and capacitive touch shields
- Compatible with MCUXpresso IDE and other popular toolchains (incl. IAR and Keil)
- LPC804 Arm Cortex-M0+ MCU in TSSOP24 package running at up to 15MHz
- On-board CMSIS-DAP (debug probe) with VCOM port, based on LPC11U35 MCU
- Debug connector to allow debug of target LPC802 MCU using an external probe
- ISP and User/Wake buttons
- 3 User LEDs
- Reset button
- 1Mb Winbond SPI flash
- NXP LM75BDP temperature sensor
- PLU shield includes LEDs, switches and oscillators for quick and easy design prototyping
- 5-button capacitive touch shield, with LED indicator for each button
- I^2C Grove connector for easy connection of sensors, or to the board as an I^2C peripheral







Orderable Part Number: ***OM40001UL***
http://www.nxp.com/demoboard/OM40001

- ✓ **NXP Software Code Bundle**
- ✓ **Free MCUXpresso IDE & 3rd Party Options**

MCUXpresso Software and Tools

for LPC & Kinetis MCUs and i.MX RT crossover processors

MCUXpresso IDE

Edit, compile, debug and optimize in an intuitive and powerful IDE

MCUXpresso SDK

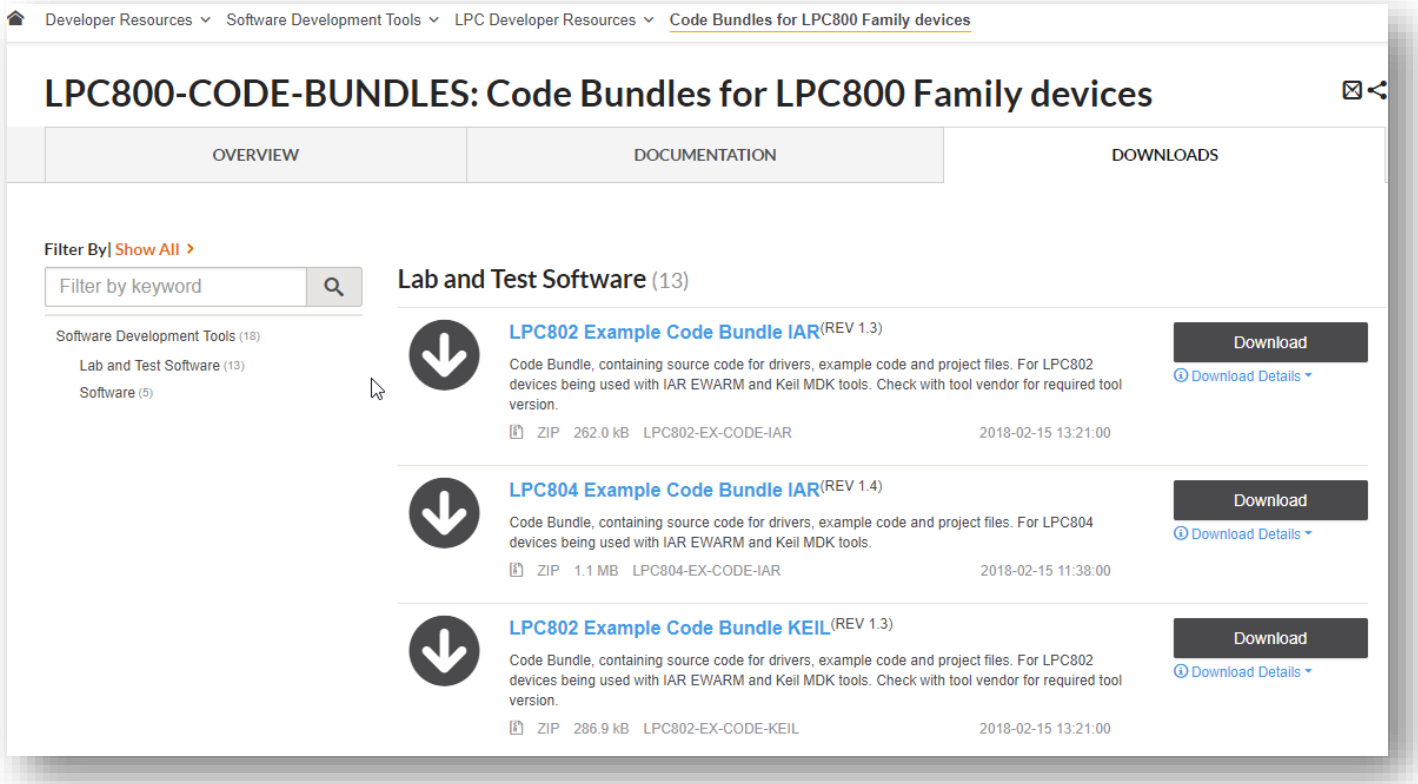
Runtime software including peripheral drivers, middleware, RTOS, demos and more

MCUXpresso Config Tools

Online and desktop tool suite for system configuration and optimization

LPC800 MCU Series Code Bundles

Learn more at: www.nxp.com/LPC80x



- The LPC800 Family of MCUs are ideal for customers who want to make the transition from 8 and 16-bit MCUs to the Cortex® M0/M0+.
- Code Bundles consist of software examples to teach users how to program the peripherals at a basic level. The examples provide register level peripheral access, and direct correspondence to the memory map in the MCU User Manual.
- Examples are concise and accurate explanations are provided within the readmes and comments in source files.

SUMMARY

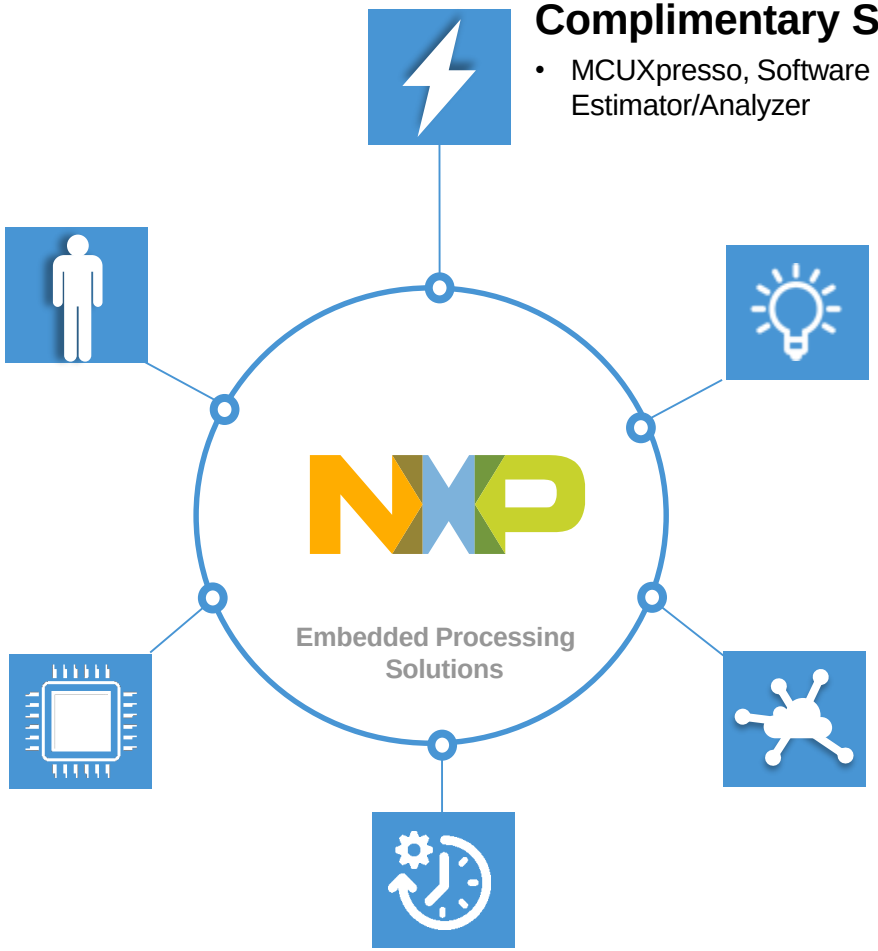
Summary

- Simplicity
- High performance at a low price point
- 2-10x higher performance than 8/16-bit MCUs
- 2-3x power saving compared to 8/16-bit MCUs
- 40-50% smaller code size than 8/16-bit MCUs
- Single cycle IO access with high drive capability and PME
- Highly integrated features to reduce system BOM cost
  - High endurance fast EEPROM
  - Simple clock generation unit with low power FRO
  - Dual power supply for direct level shifting support
  - Programmable logic unit
  - ACMP, ADC, DAC
  - Cap Touch
- Easy to use and flexible peripherals: CTimer, Multi Rate Timer, WKT, WWDT, SysTick, Switch Matrix, USART, I2C, SPI

Related Resources

- LPC80x Webpage: http://www.nxp.com/lpc80x
- LPCXpresso802 Board: http://www.nxp.com/demoboard/OM40000
- LPCXpresso804 Board: http://www.nxp.com/demoboard/OM40001
- LPC Microcontroller Community: https://community.nxp.com/community/lpc
- MCUXpresso Software and Tools: https://www.nxp.com/mcuxpresso
- Code Bundles for LPC800 Series devices: https://www.nxp.com/support/developer-resources/software-development-tools/lpc-developer-resources-/code-bundles-for-lpc800-family-devices:LPC800-CODE-BUNDLES

Software, Professional Support & Services



Complimentary Software & Tools

- MCUXpresso, Software Development Kit, Pin Config, Power Estimator/Analyzer

Professional Services

- Managing Skills Gaps & Engineering Capacity
- Global Staffing Capability
- Vested Interest in Mutual Success
- Graphic, Security, Linux/Android, Cloud, Connectivity

Complimentary Support

- NXP Boards
- Communities
- Technical Information Center
- Customer Application & Technical Support
- Distributor technical support

Hardware Services

- 1st Time Boot
- Schematics & Layout Review

Software Products / Technology

Professional Support

- Risk Reduction
- Fast Answers
- Hot Fixes

[Link to NXP Professional Services]

SECURE CONNECTIONS
FOR A SMARTER WORLD

BACK UP

ROM

FLASH programming

- In-System Programming (ISP)
  - ISP Entry Pin – PIO0_12
  - ISP Mode is entered when ISP Entry Pin is pulled LOW during RESET
  - ISP entry can be disabled using CRP

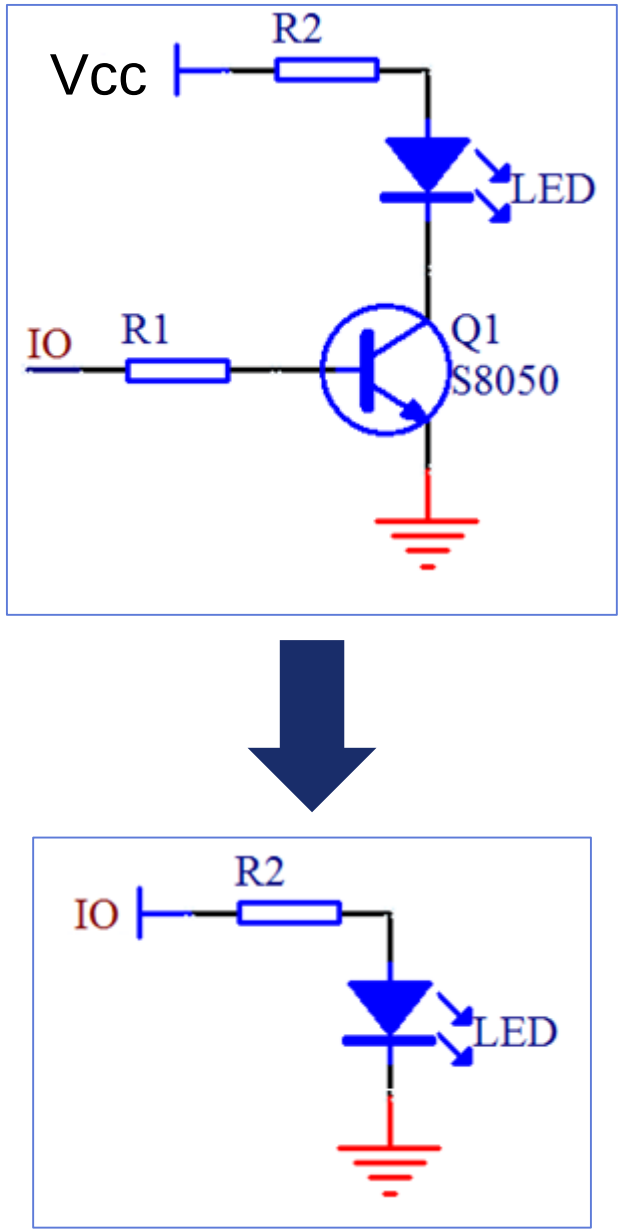
ISP Mode	Default Pin function
USART (single supply part)	PIO0_4 is UART0 TX PIO0_0 is UART0 RX
USART (Dual supply part)	PIO0_9 is UART0 TX PIO0_8 is UART0 RX

- In Application Programming (IAP)

GPIO

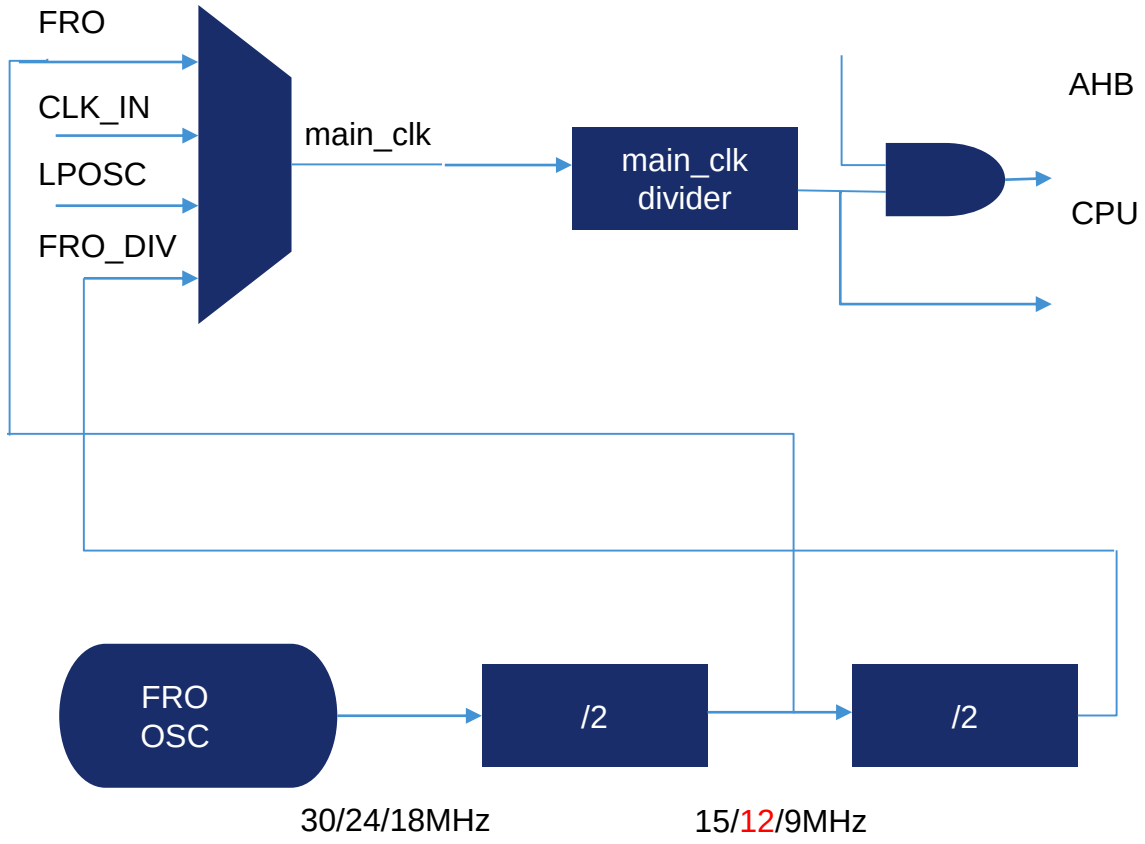
High Drive Pins

- Provide high current drive capability (20mA)
- Able to directly drive LEDs
  - ***Eliminate external drive IC***
  - ***Save BOM cost and board PCB size***
- ***High drive pins***
  - 3 pins: ***PIO0_2, PIO0_3, PIO0_12 (LPC802)***
  - 5 pins: ***PIO0_2, PIO0_3, PIO0_12, PIO0_18, and PIO0_20 (LPC804)***



CLOCK GENERATION UNIT

Clock Generation Unit



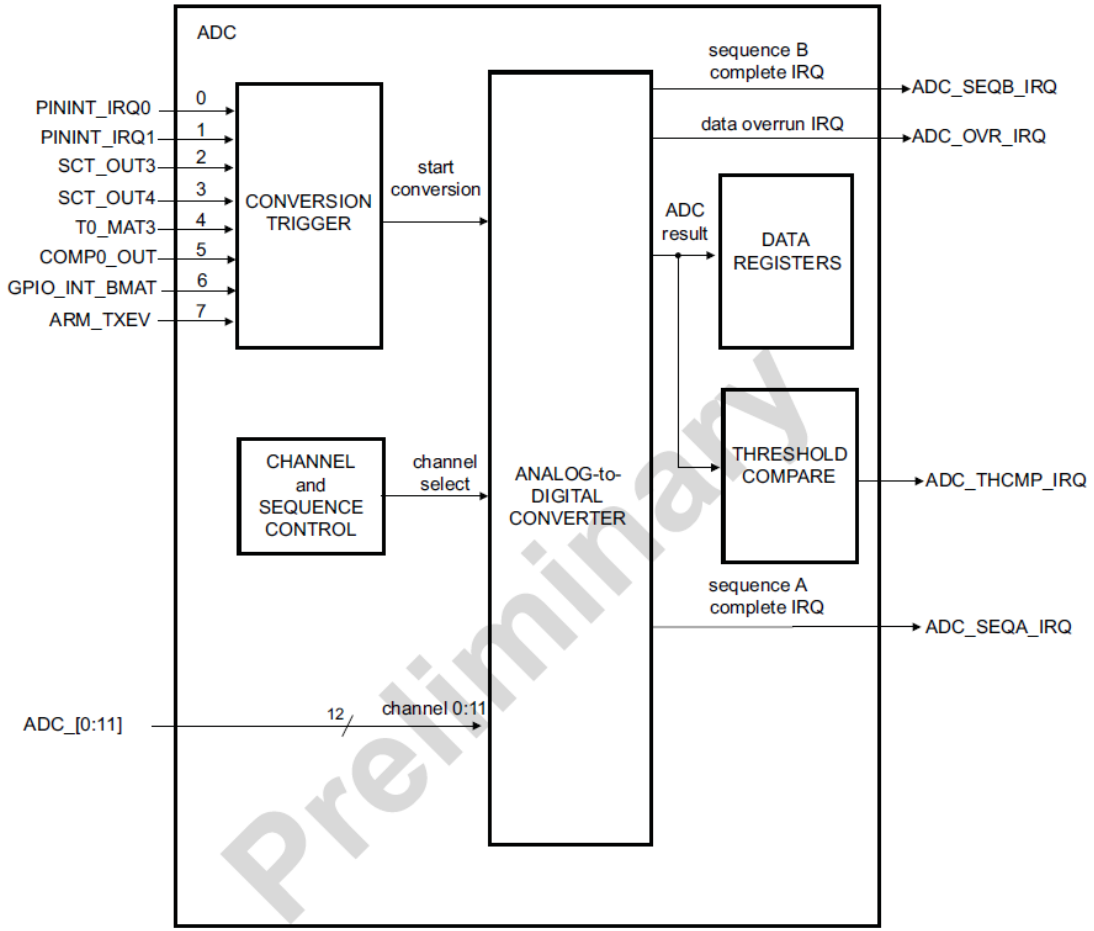
Clock Sources	Characteristics
FRO Oscillator	• System clock by default • Stable. Quick power up and power down • 30/24/18MHz (±1% over 0 C to 70 C)
CLK_IN	• 1 MHz – 15 MHz
Low Power Oscillator	• Low power operation • Low frequency oscillator • Watchdog clock source • 1 MHz (+/- 3%)

Main Clock selects the 12 MHz FRO as the clock source on power-up or after reset

ANALOG

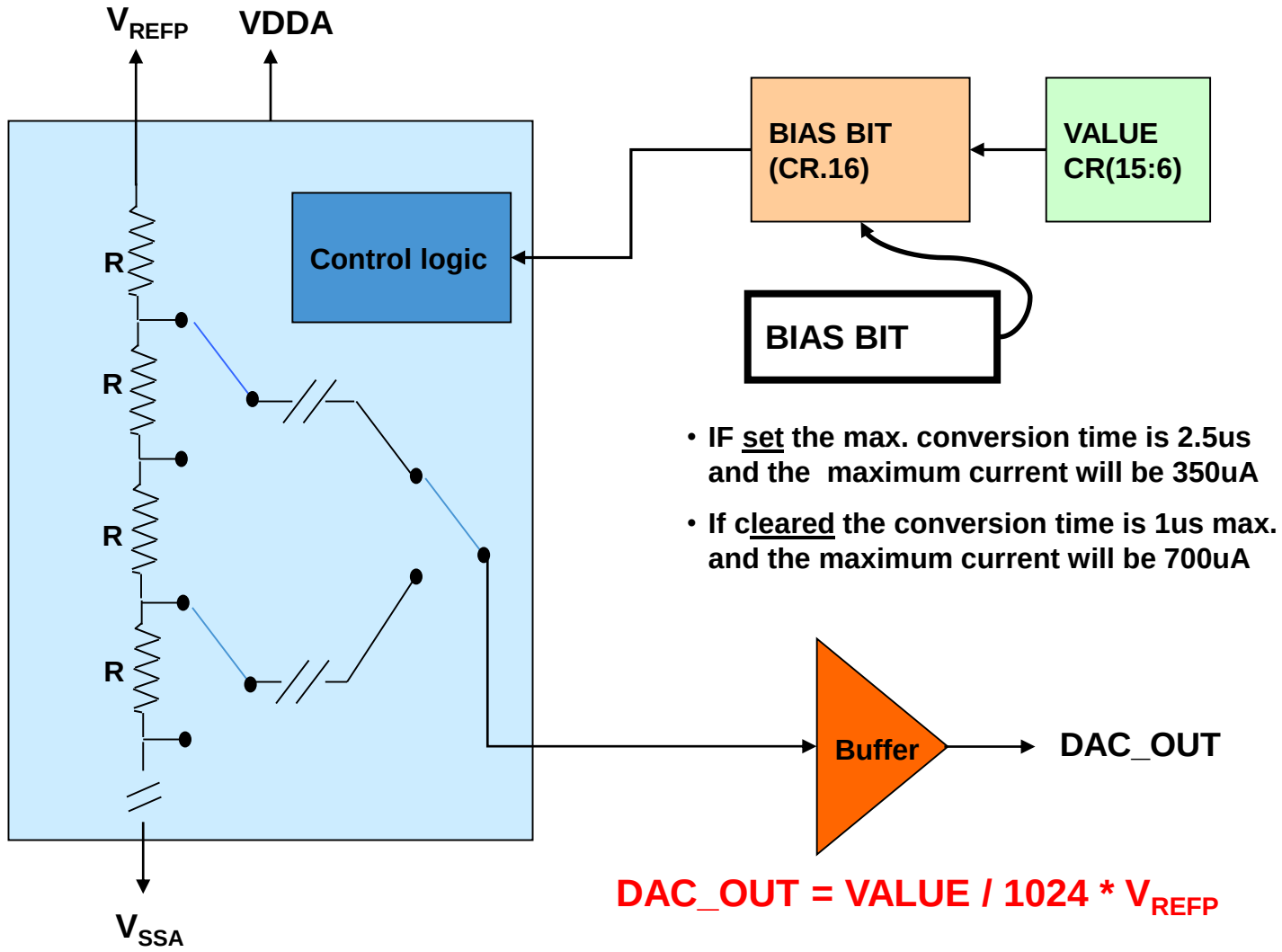
Analog to Digital Converter

- 12-bit successive approximation
- Input multiplexing among 12 pins
- 12-bit conversion rate up to 480 Ksps
- Two configurable conversion sequences with independent triggers
- Optional automatic high/low threshold comparison and “zero crossing” detection
- Power down mode and low-power operating mode
- Burst conversion mode for single and multiple inpu



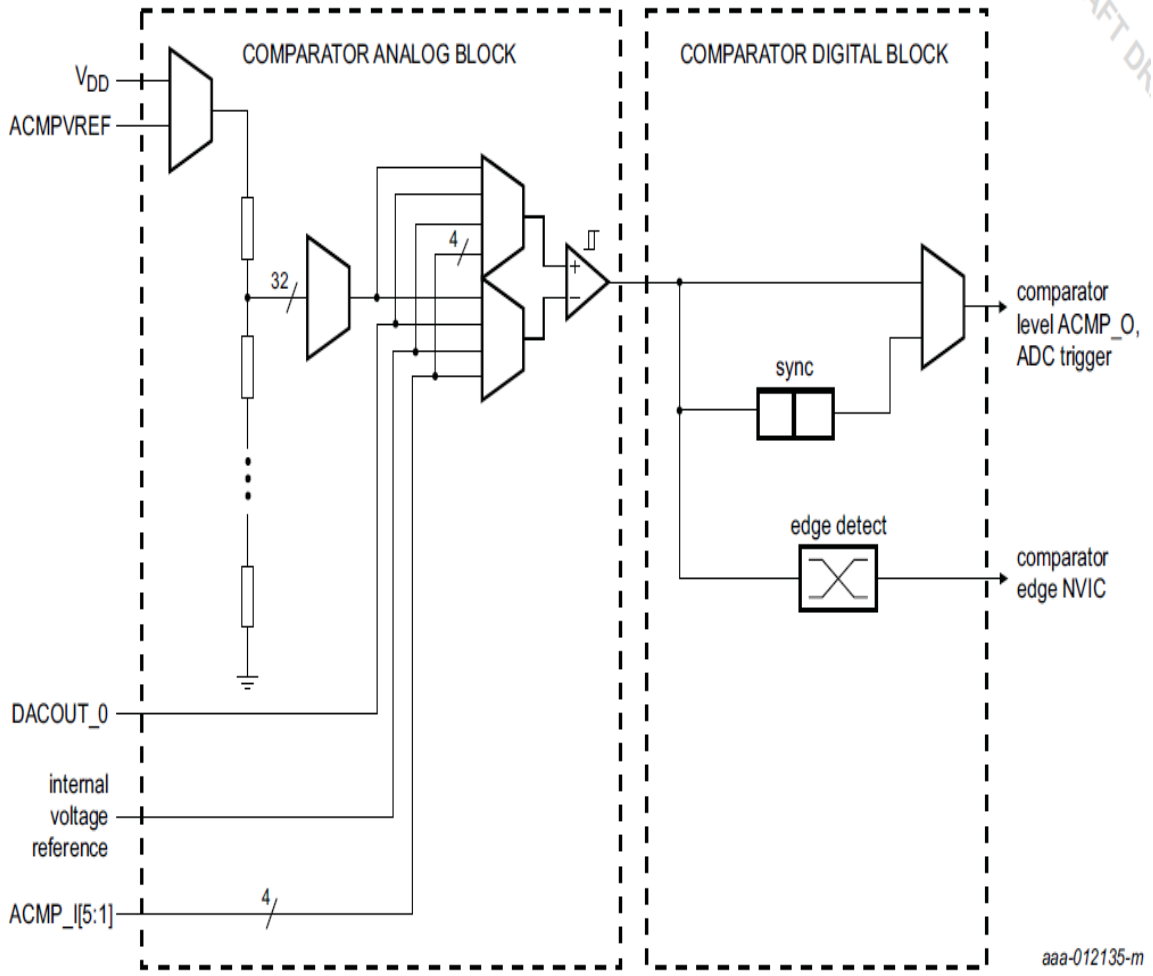
DAC Feature

- 10-bit digital to analog converters
- Resistor string architecture
- Buffered output
- Power-down mode
- Selectable speed vs. power
- Maximum update rate of 1 MHz



Analog Comparator

- Compares voltage levels on external pins and internal voltages
- 5 inputs are multiplexed separately to the positive voltage input and negative inputs
- The Internal voltage reference (0.9 V bandgap reference) and DACOUT can be used as either the positive or negative input of the comparator
- Voltage ladder source selectable between the supply pin VDD or ACMPVREF pin
- 32 levels of Comparator reference voltage for fine grain comparison
- Programmable Hysteresis for 4 levels: 0/ 5/10/20mV



DEBUG MODULE

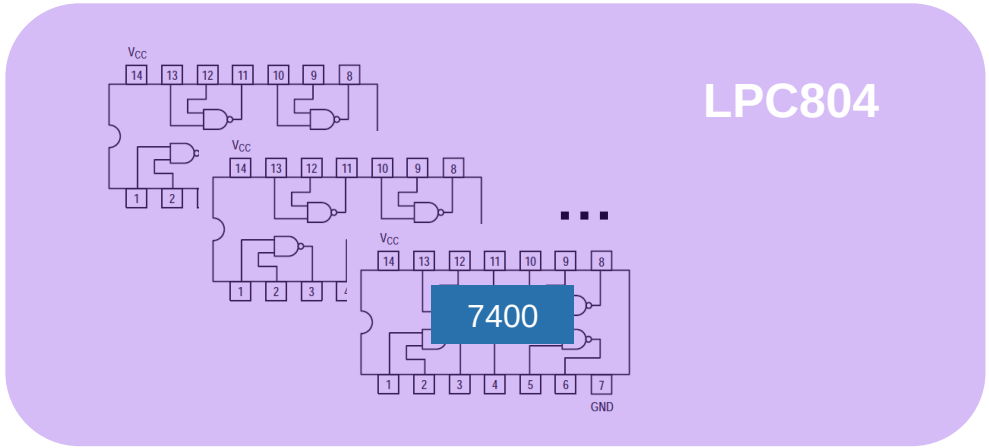
Emulation and Debugging

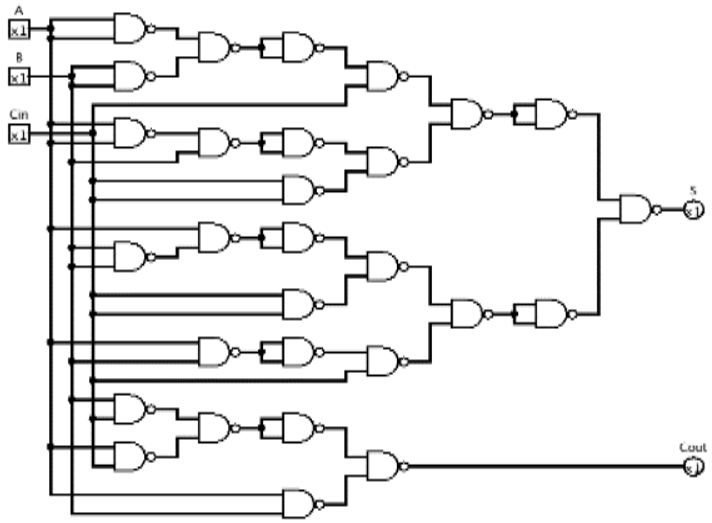
- Debug and trace functions are integrated into the ARM Cortex-M0+
- Serial wire debug (SWD: 2 pins)
- Supports up to four breakpoints and two watchpoints
- Micro Trace Buffer (MTB) supported
- Standard JTAG pins (5 pins) supports ONLY boundary scan testing

PLU

What's the advantage of PLU?

- Simple glue logic to connect MCU with external components and replace these 7400 series.
- State machine design using Flip-flop
- Address decoder
- Pattern match
- Low-power application. Many peripherals are shut off in deep-sleep and power-down mode, PLU is not.
- PLU is Programmable!!! It can be reprogrammed and reused
- Seamless connection using SWM and PLU





OTHER PERIPHERALS

Timers

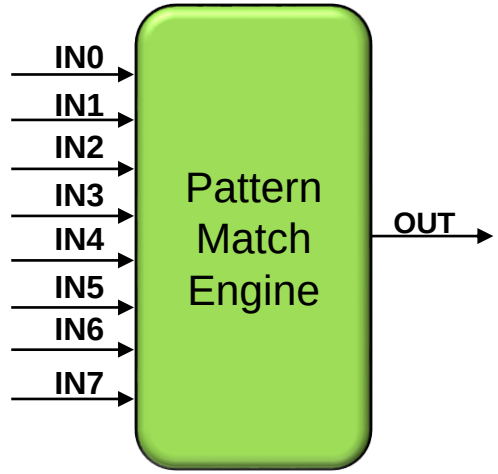
- Standard 32-bit Timer
- Multi-Rate timer (MRT)
  - Timer with four independent channels
  - Each channel can generate interrupts
    - Repeat interrupt mode
    - One-shot interrupt mode
- Self wake-up timer (WKT)
  - A non-zero value in this 32-bit timer initiates a countdown sequence. Wake-up source from low-power modes
- Windowed watchdog timer (24-bit timer)
- SysTick Timer (24-bit timer)

Pattern Match Engine (PME)

- Pin Interrupt generator
  - Up to 8 pins can be selected to generate interrupts to the core
- Pattern match feature
  - The same 8 pins (above) can be selected from all GPIO pins to contribute to a Boolean expression
- Example:

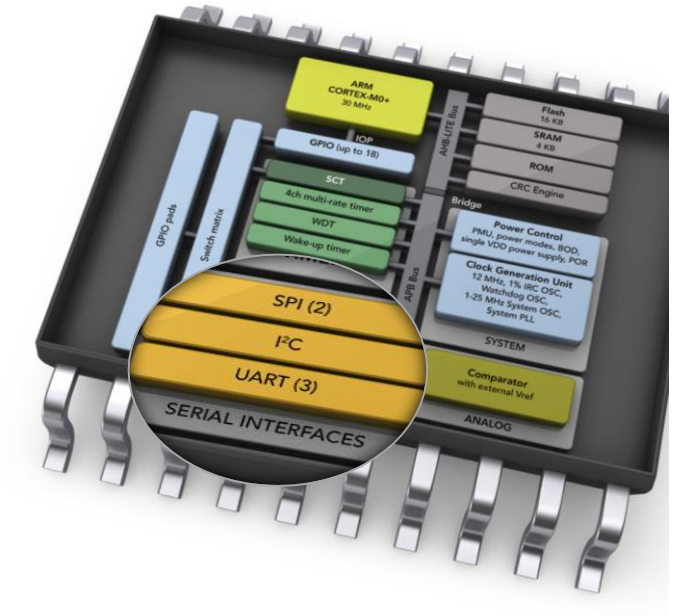
```
(IN0)~(IN1)(IN3)^+(IN4)(IN5)+(IN0)~(IN3)~(IN4)

  where: ~=low; ^=rising edge; +=OR
```

  - The PME keeps polling these pins and generates an interrupt to the core when one or more of the bit slices match
- Both the pin interrupt and pattern match blocks are mutually exclusive



USART/I²C/SPI

- USART
  - Synchronous operations on all UARTs
  - Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 10 Mbit/s in synchronous mode for USART functions
  - Fractional rate divider is shared among all USARTs
  - Built-in baud rate generator
- I²C
  - Standard-mode, Fast-mode
- SPI
  - Maximum data rate of 15 Mbit/s in master and 18 Mbit/s in slave
- Wake from sleep, deep-sleep, or power-down mode



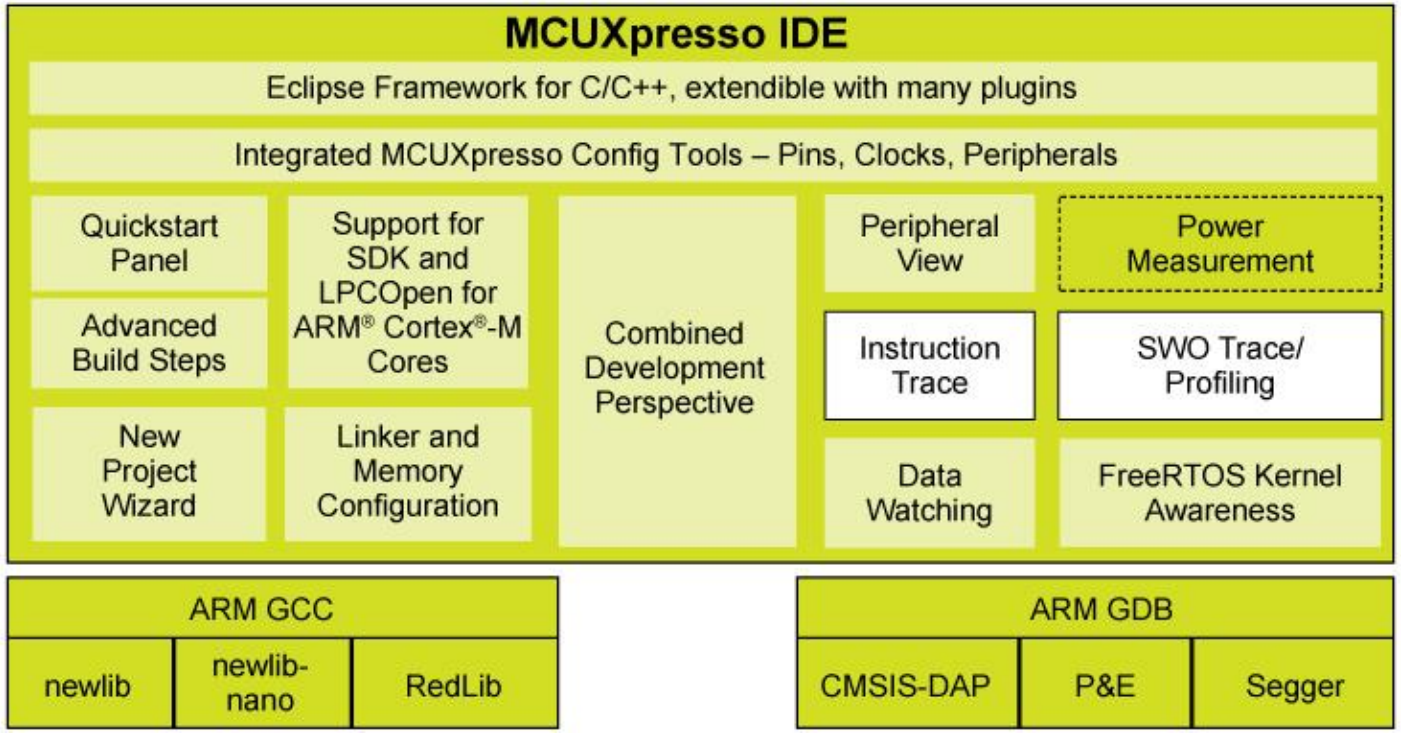
Cyclic Redundancy Check (CRC) Engine

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Accept any size of data width per write: 8, 16 or 32-bit
  - 8-bit write: 1-cycle operation
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle)
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle)

ENABLEMENT

MCUXpresso IDE

Free Eclipse and GCC-based IDE for C/C++ development on Kinetis and LPC MCUs and i.MX RT crossover processors



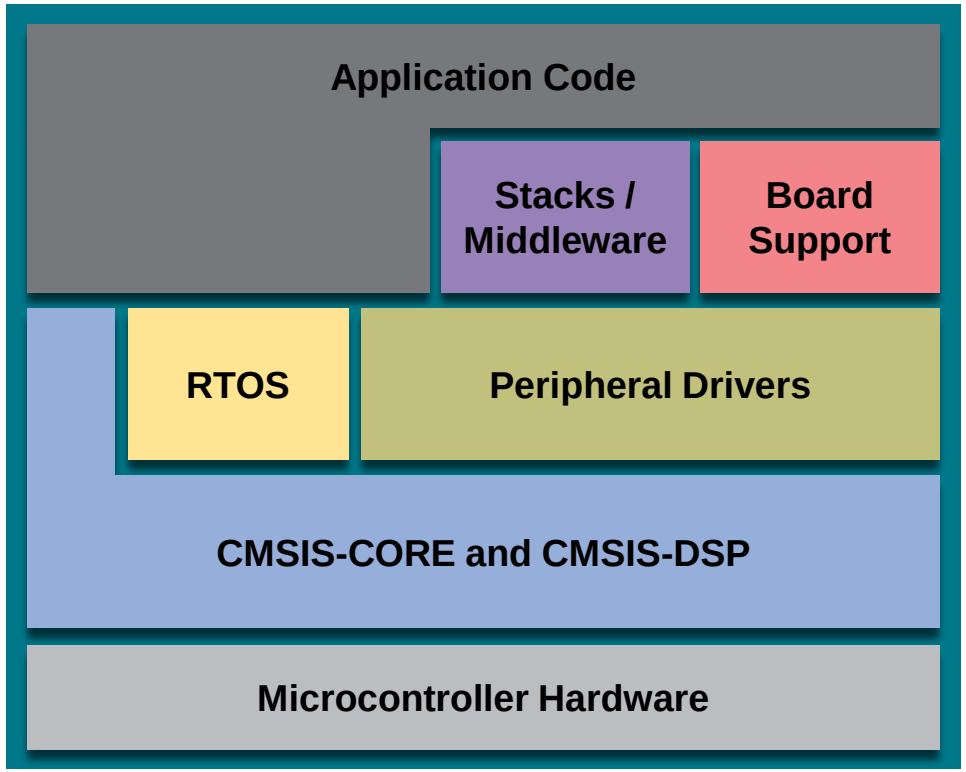
Product Features

- Feature-rich, unlimited code size, optimized for ease-of-use, based on industry standard Eclipse framework for NXP's Kinetis and LPC MCUs and i.MX RT crossover processors
- Application development with Eclipse and GCC-based IDE for advanced editing, compiling and debugging
- Supports custom development boards, Freedom, Tower and LPCXpresso boards with debug probes from NXP, P&E and Segger
- Free: Full Featured, unlimited Code Size, no special activation needed, community based support, advanced trace capabilities

Learn more at: www.nxp.com/mcuxpresso/sdk

MCUXpresso SDK

The software framework and reference for Kinetis & LPC MCU application development



Product Features

Architecture:

- CMSIS-CORE compatible
- Single driver for each peripheral
- Transactional APIs w/ optional DMA support for communication peripherals

Integrated RTOS:

- FreeRTOS v9
- RTOS-native driver wrappers

Integrated Stacks and Middleware

- USB Host, Device and OTG
- lwIP, FatFS
- Crypto acceleration plus wolfSSL & mbedTLS
- SD and eMMC card support

Reference Software:

- Peripheral driver usage examples
- Application demos
- FreeRTOS usage demos

License:

- BSD 3-clause for startup, drivers, USB stack

Toolchains:

- MCUXpresso IDE
- IAR®, ARM® Keil®, GCC w/ Cmake

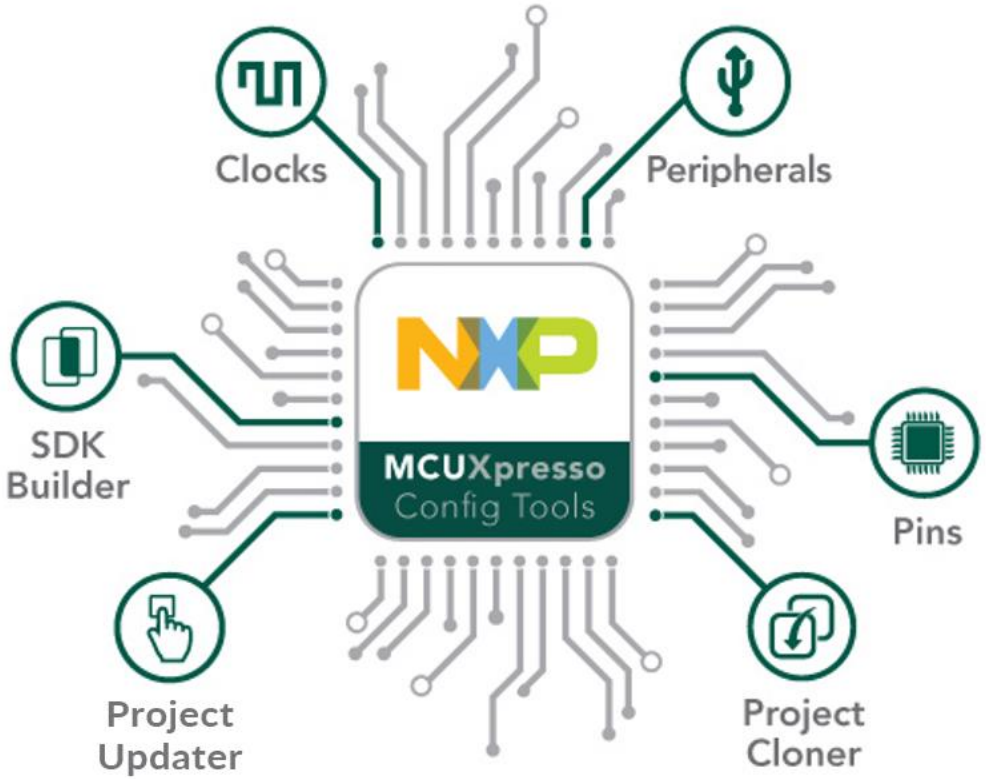
Quality

- Production-grade software
- MISRA 2004 compliance
- Checked with Coverity® static analysis tools

MCUXpresso Config Tools

Learn more at: www.nxp.com/mcuxpresso/config

Integrated configuration and development tools for LPC and Kinetis MCUs



MCUXpresso Config Tools is a suite of evaluation and configuration tools that helps guide users from first evaluation to production software development.

SDK Builder packages custom SDKs based on user selections of MCU, evaluation board, and optional software components.

Pins, **Clocks**, and **Peripheral** tools generate initialization C code for custom board support. Features validation of inputs and cross-tool conflict resolution.

Project Update works directly with existing SDK-based IDE projects with generated Pins, Clocks, and Peripheral source files.

Project Cloning creates a standalone SDK project based on a example application available within SDK release.

SECURE CONNECTIONS
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