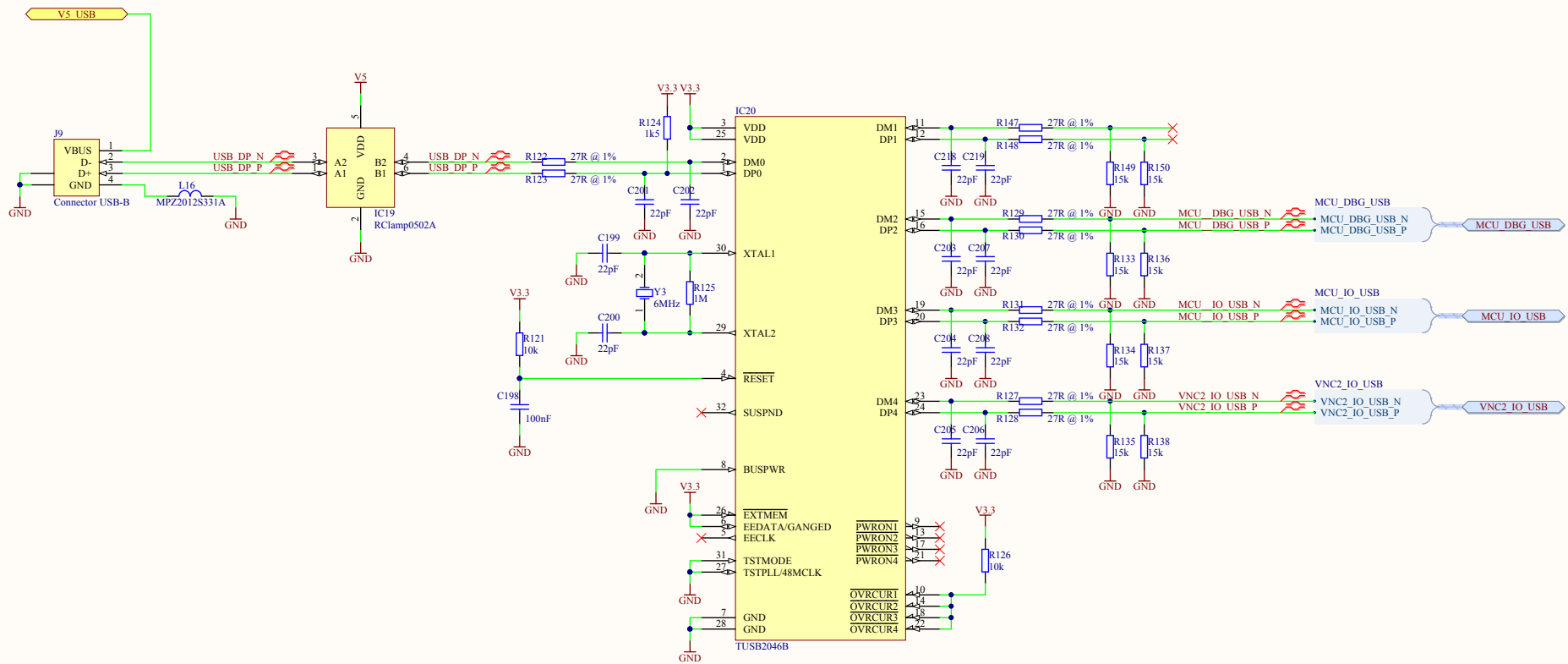
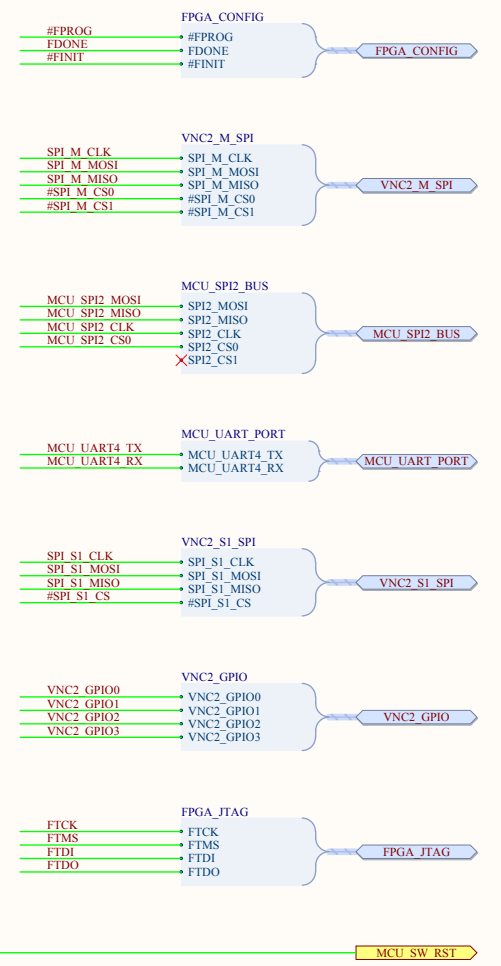
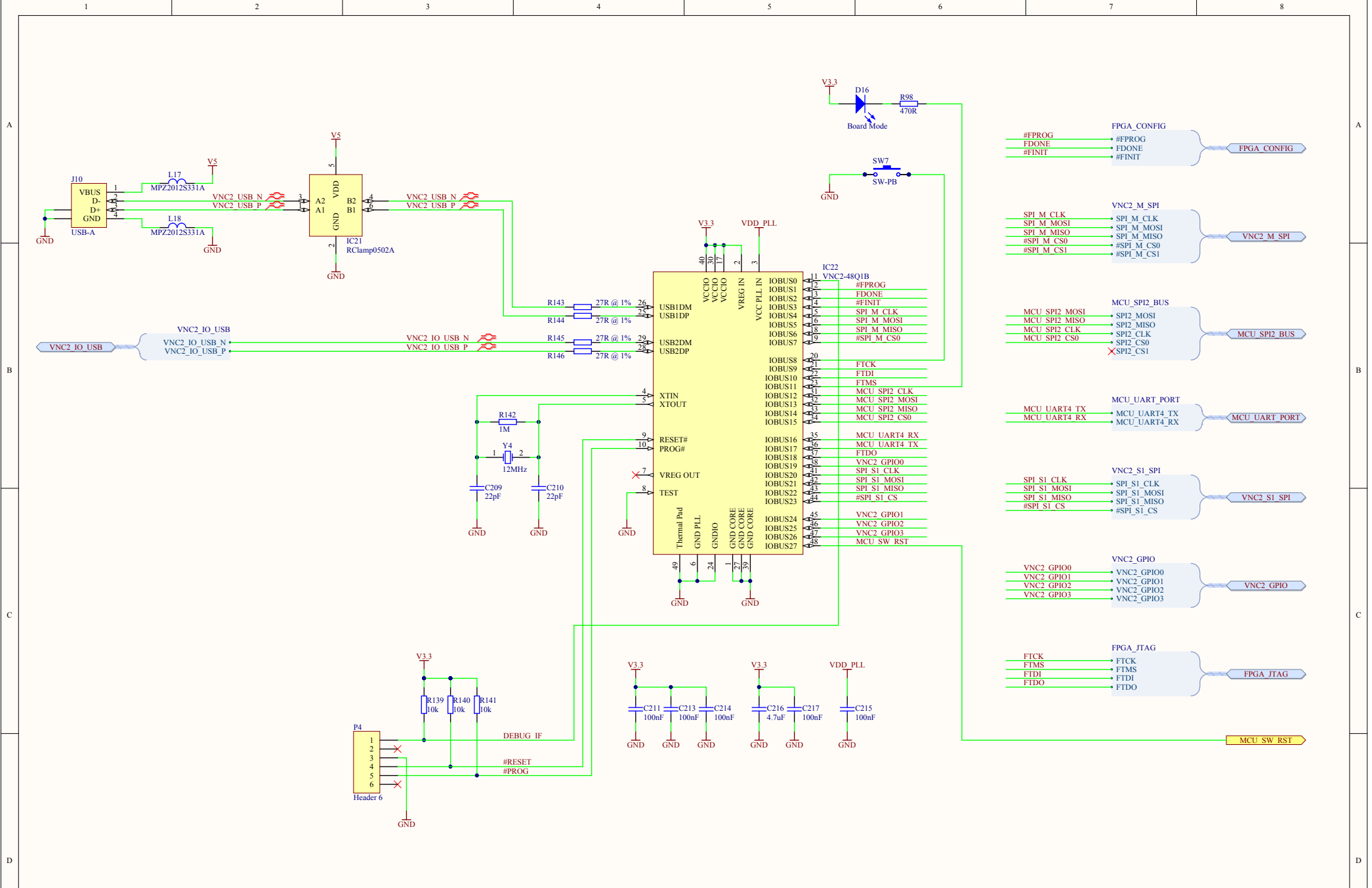


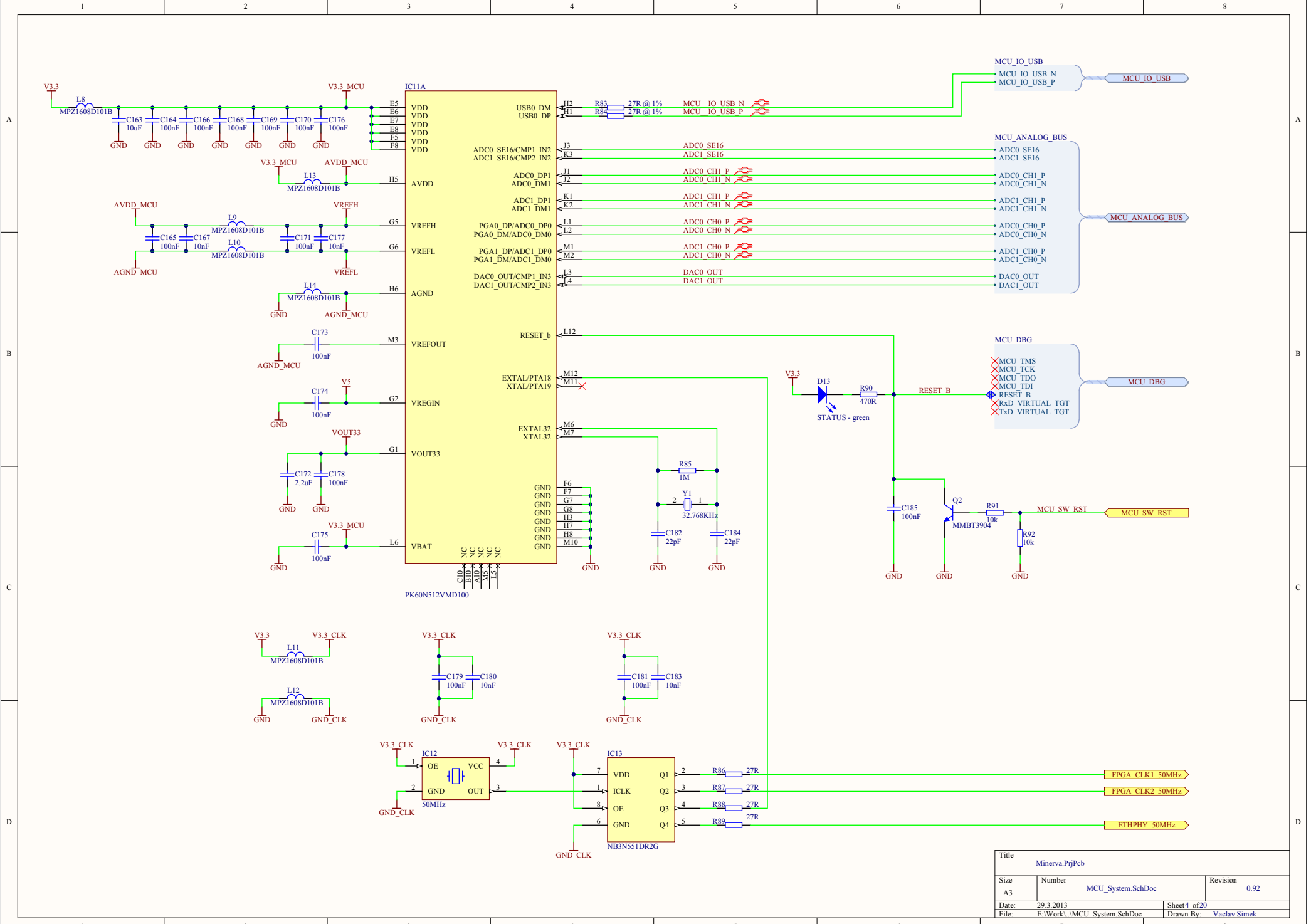
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Size	Number	Revision	
A3	Minerva.SchDoc	0.92	
Date:	29.3.2013	Sheet 1 of 20	
File:	E:\Work\Minerva.SchDoc	Drawn By:	Vaclav Simek



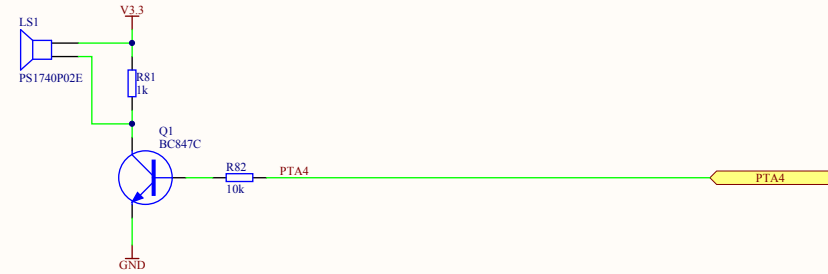
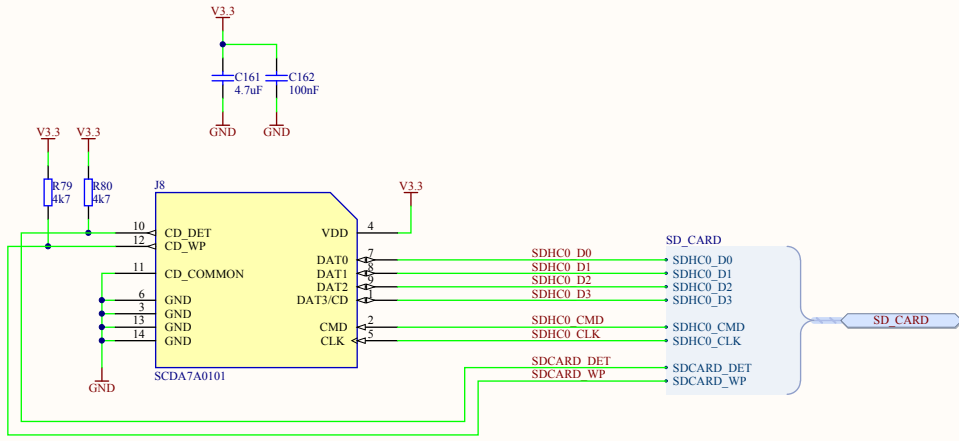
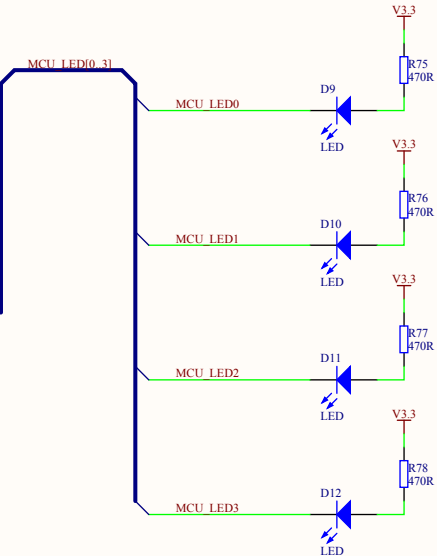
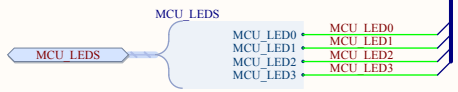
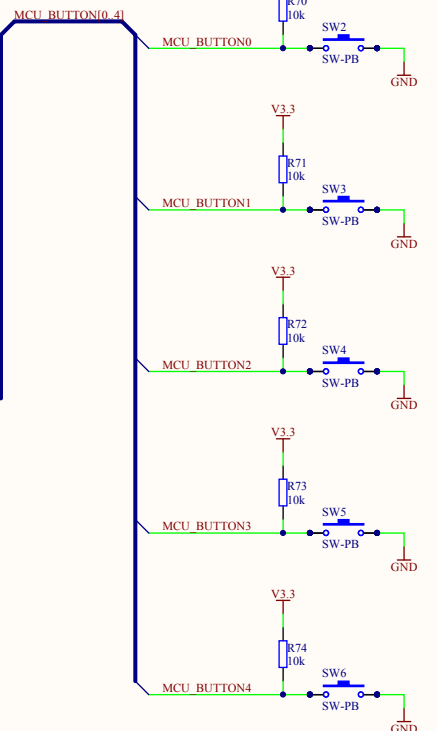
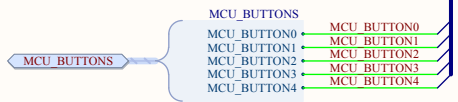
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Size	Number	Revision
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Date:	29.3.2013	Sheet of 20
File:	E:\Work\USB Hub.SchDoc	Drawn By: Vaclav Simek



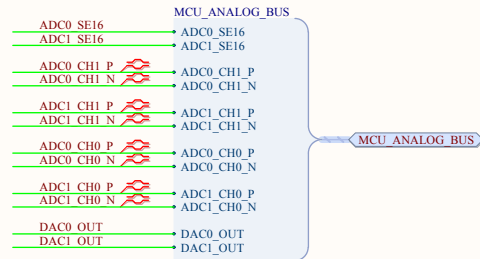
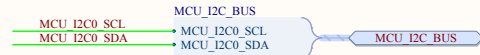
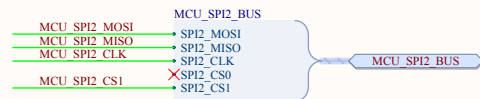
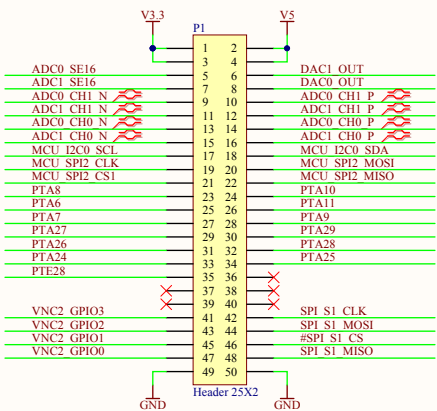
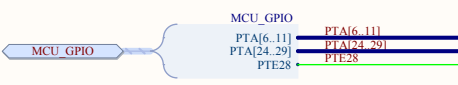
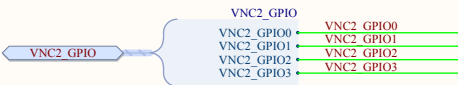
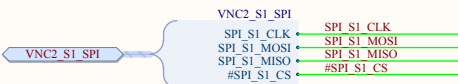
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Size	Number	Revision	
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Date:	29.3.2013	Sheet 3 of 20	
File:	E:\Work\...\VNC2 Board Control.SchDoc	Drawn By:	Vaclav Simek



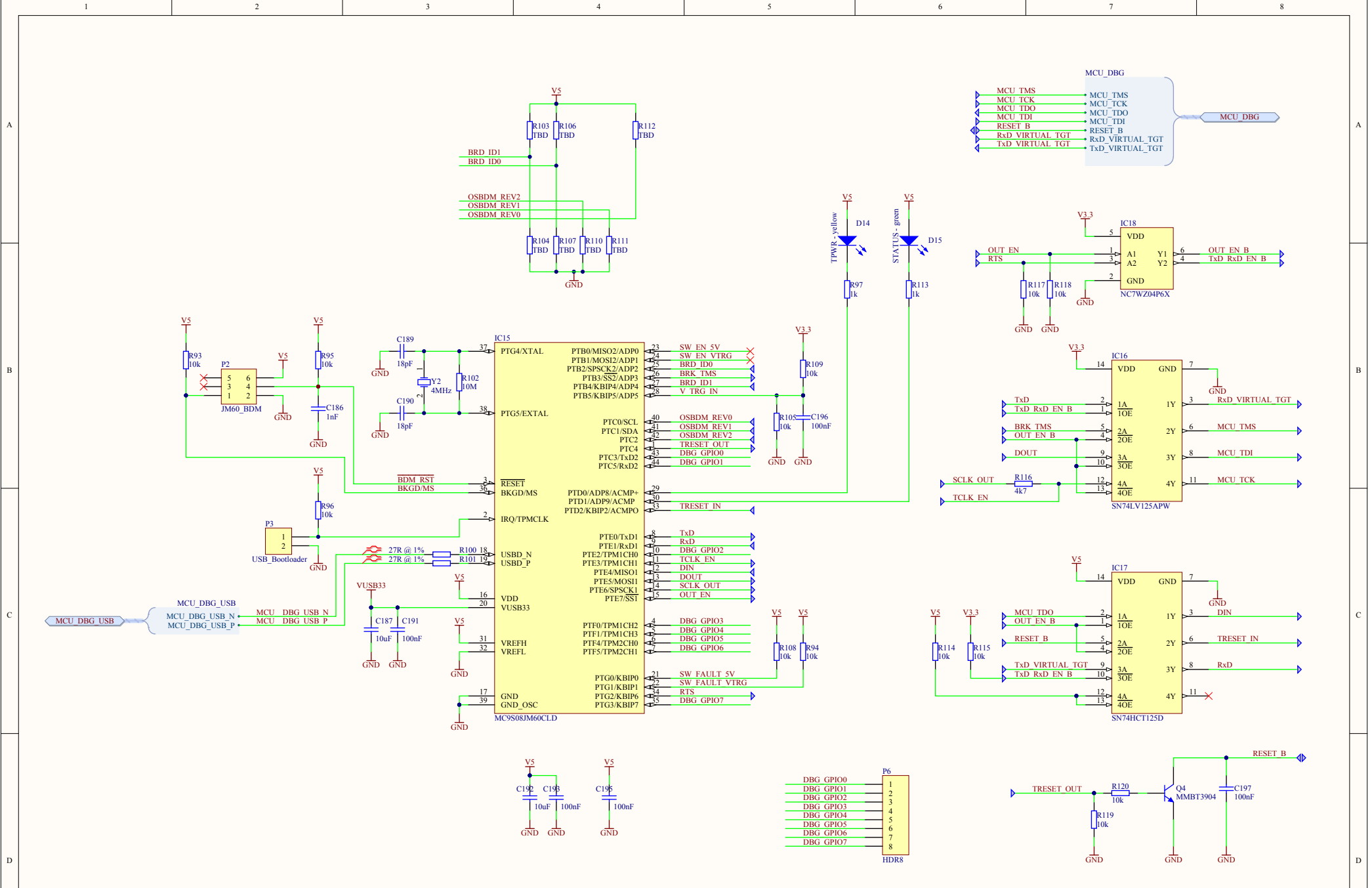
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Size	Number	Revision	
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Date:	29.3.2013	Sheet4 of20	
File:	E:\Work\MCU_System.SchDoc	Drawn By:	Vaclav Simek



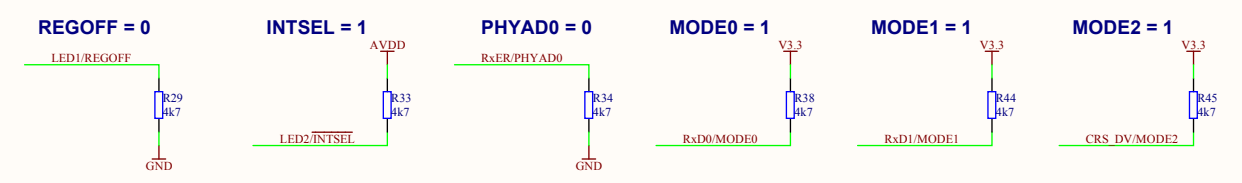
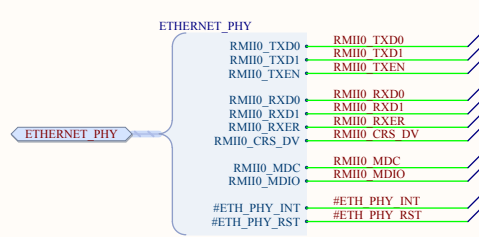
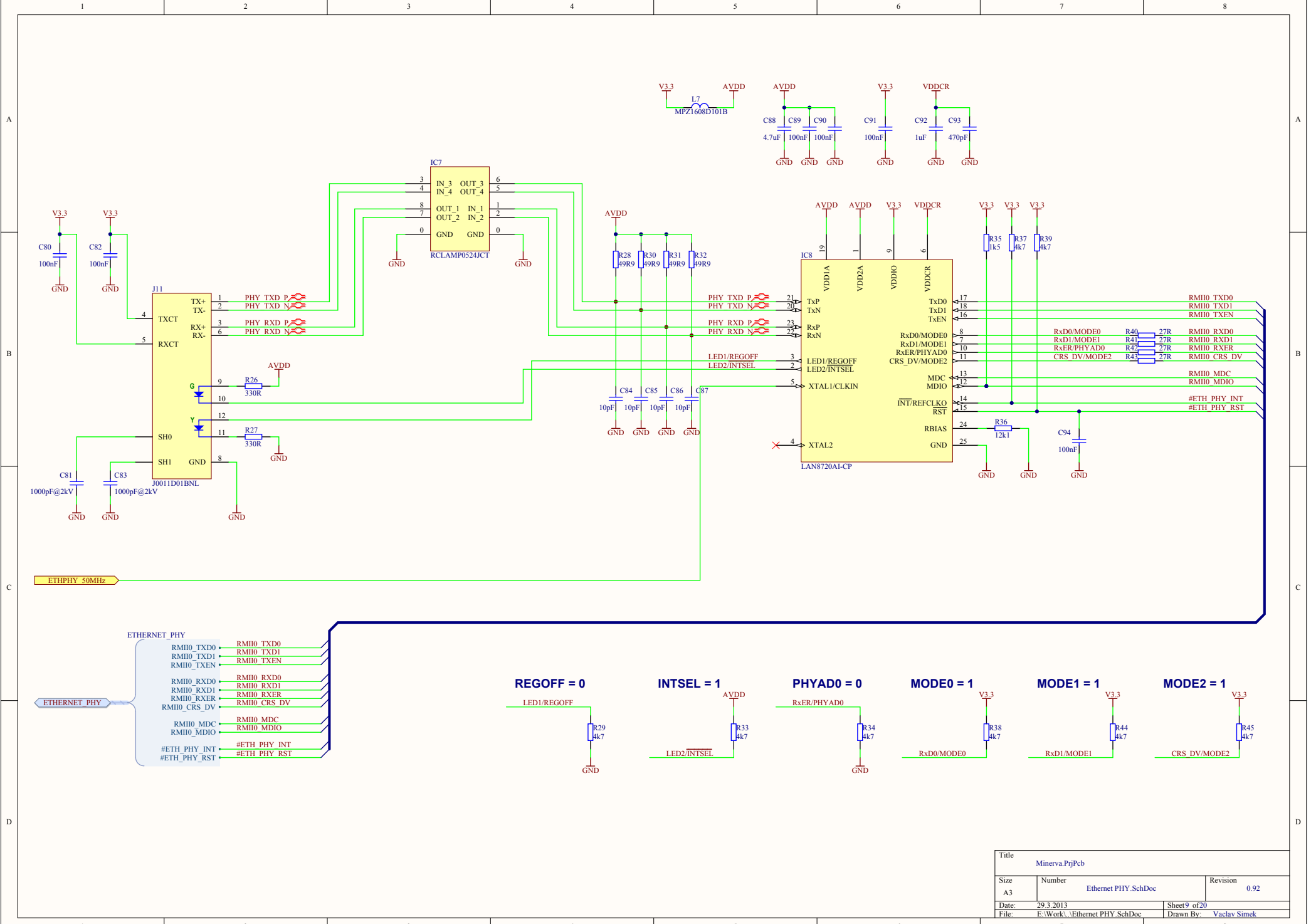
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Size	Number	MCU_Peripherals.SchDoc		Revision	0.92
Date:	29.3.2013	Sheet 6 of 20			
File:	E:\Work\MCU_Peripherals.SchDoc	Drawn By:		Vaclav Simek	



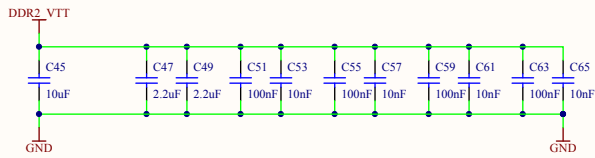
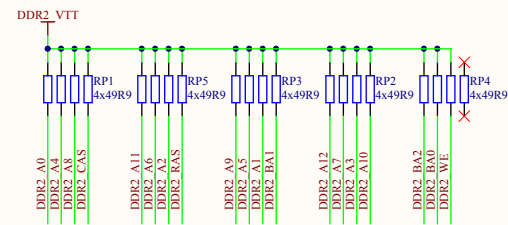
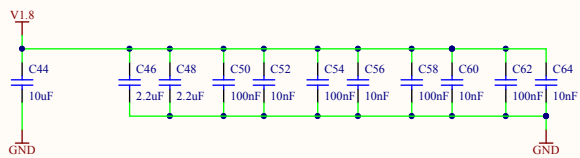
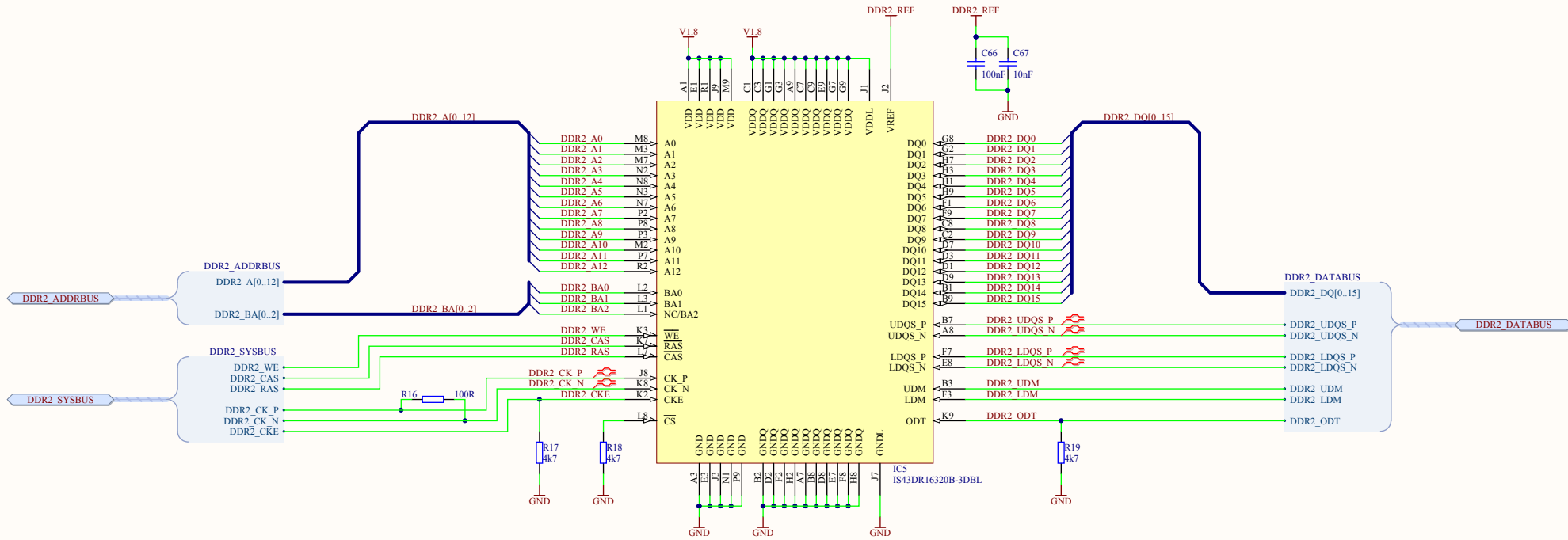
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Size	Number	Revision	
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File:	E:\Work\MCU_Expansion.SchDoc	Drawn By:	Vaclav Simek



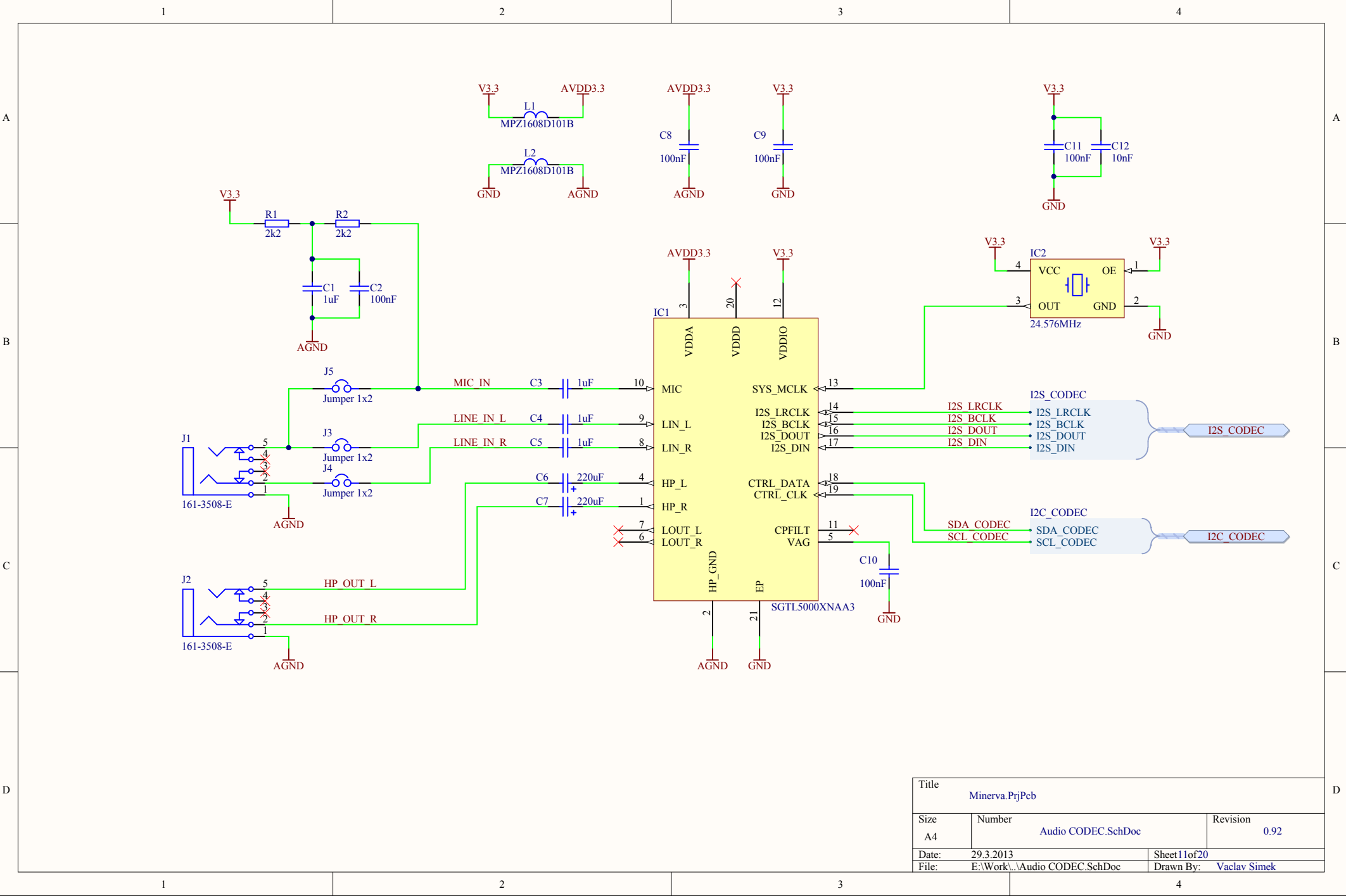
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Size	Number	Revision	0.92
A3	MCU Debug.SchDoc		
Date:	29.3.2013	Sheet 8 of 20	
File:	E:\Work\MCU Debug.SchDoc	Drawn By:	Vaclav Simek



Title			
Minerva.PjPcb			
Size	Number	Revision	
A3	Ethernet PHY.SchDoc	0.92	
Date:	29.3.2013	Sheet 9 of 20	
File:	E:\Work\...\Ethernet PHY.SchDoc	Drawn By:	Vaclav Simek



Title Minerva.PjPeb		
Size A3	Number DDR2 Memory.SchDoc	Revision 0.92
Date: 29.3.2013	Sheet 10of20	
File: E:\Work\...DDR2 Memory.SchDoc	Drawn By: Vaclav Simek	



Title			
Minerva.PrxPcb			
Size	Number	Revision	
A4	Audio CODEC.SchDoc	0.92	
Date:	29.3.2013	Sheet 1 of 20	
File:	E:\Work\Audio CODEC.SchDoc	Drawn By:	Vaclav Simek

A

B

C

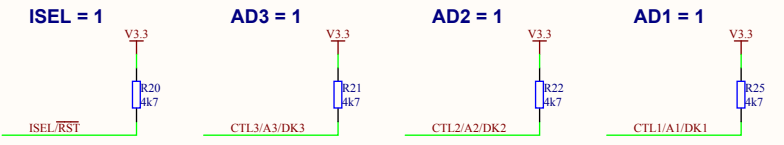
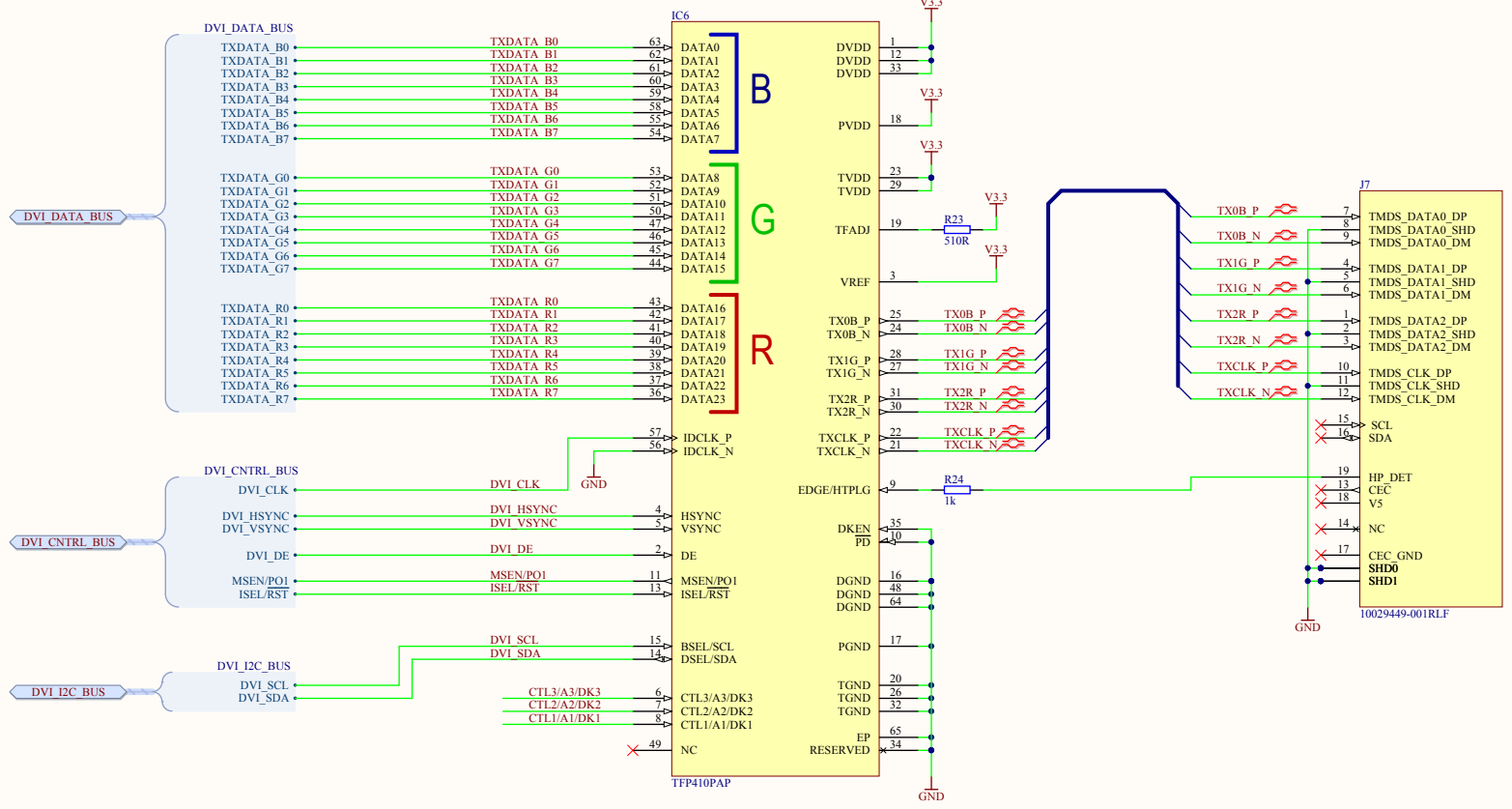
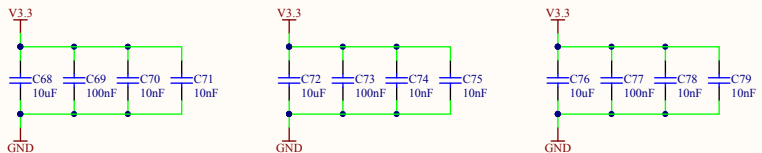
D

A

B

C

D



Title			Minerva.PjPeb		
Size	Number	Revision		0.92	
A3	DVI Controller.SchDoc				
Date:	29.3.2013	Sheet	12of20		
File:	E:\Work\...DVI Controller.SchDoc	Drawn By:	Vaclav Simek		

IC9A

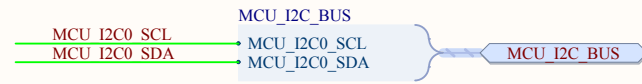
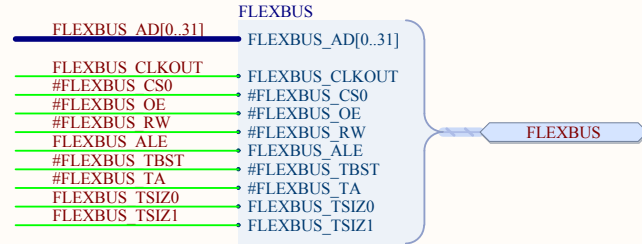
BANK 0

IO_L1P_HSWAPEN_0	D4	FLEXBUS_AD17
IO_L1N_VREF_0	C4	FLEXBUS_AD22
IO_L2P_0	B2	FLEXBUS_AD23
IO_L2N_0	A2	FLEXBUS_AD29
IO_L3P_0	D6	FLEXBUS_AD30
IO_L3N_0	C6	FLEXBUS_AD20
IO_L4P_0	B3	FLEXBUS_AD21
IO_L4N_0	A3	FLEXBUS_AD18
IO_L5P_0	B4	FLEXBUS_AD19
IO_L5N_0	A4	FLEXBUS_AD15
IO_L6P_0	C5	FLEXBUS_AD16
IO_L6N_0	A5	FLEXBUS_AD31
IO_L8P_0	B6	#FLEXBUS_OE
IO_L8N_VREF_0	A6	FLEXBUS_AD28
IO_L10P_0	C7	FLEXBUS_AD14
IO_L10N_0	A7	MCU_I2C0_SDA
IO_L11P_0	D8	FLEXBUS_AD13
IO_L11N_0	C8	FLEXBUS_AD12
IO_L33P_0	B8	FLEXBUS_AD10
IO_L33N_0	A8	FLEXBUS_AD10
IO_L34P_GCLK19_0	D9	FLEXBUS_CLKOUT
IO_L34N_GCLK18_0	C9	MCU_I2C0_SCL
IO_L35P_GCLK17_0	B9	FLEXBUS_AD9
IO_L35N_GCLK16_0	A9	FLEXBUS_AD6
IO_L36P_GCLK15_0	D11	FLEXBUS_AD27
IO_L36N_GCLK14_0	C11	FLEXBUS_AD24
IO_L37P_GCLK13_0	C10	FLEXBUS_AD26
IO_L37N_GCLK12_0	A10	FLEXBUS_AD5
IO_L38P_0	D9	FLEXBUS_AD11
IO_L38N_VREF_0	F9	FLEXBUS_AD8
IO_L39P_0	B11	FLEXBUS_AD25
IO_L39N_0	A11	FLEXBUS_TSIZ0
IO_L41P_0	B12	FLEXBUS_AD7
IO_L41N_0	A12	#FLEXBUS_RW
IO_L62P_0	B14	#FLEXBUS_CS0
IO_L62N_VREF_0	A14	#FLEXBUS_TBST
IO_L63P_SCP7_0	F13	FLEXBUS_ALE
IO_L63N_SCP6_0	E13	FLEXBUS_TSIZ1
IO_L64P_SCP5_0	C15	FLEXBUS_AD1
IO_L64N_SCP4_0	A15	FLEXBUS_AD4
IO_L65P_SCP3_0	D14	FLEXBUS_AD3
IO_L65N_SCP2_0	C14	#FLEXBUS_TA
IO_L66P_SCP1_0	B16	FLEXBUS_AD0
IO_L66N_SCP0_0	A16	FLEXBUS_AD2

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V3.3

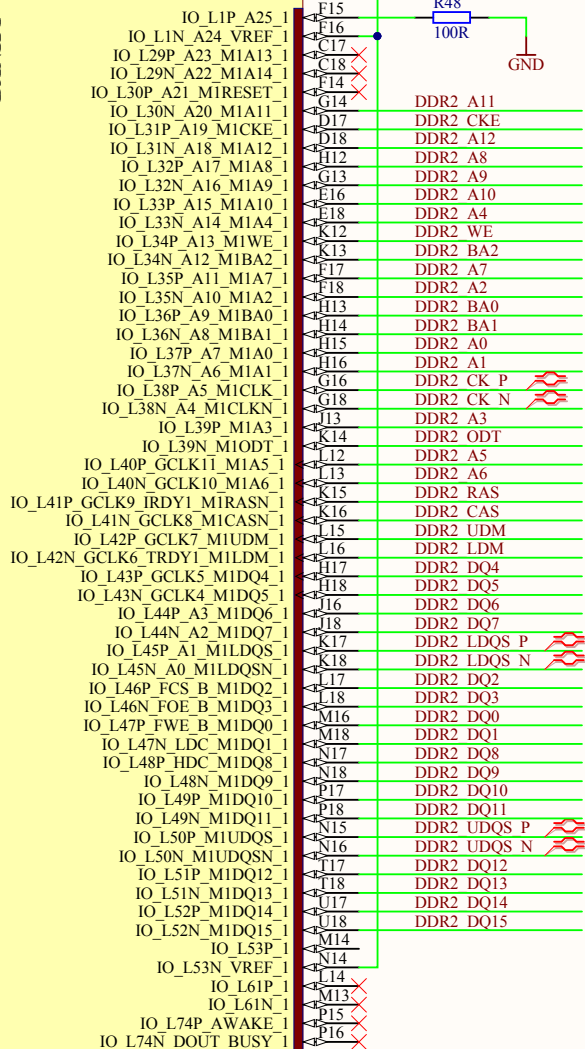
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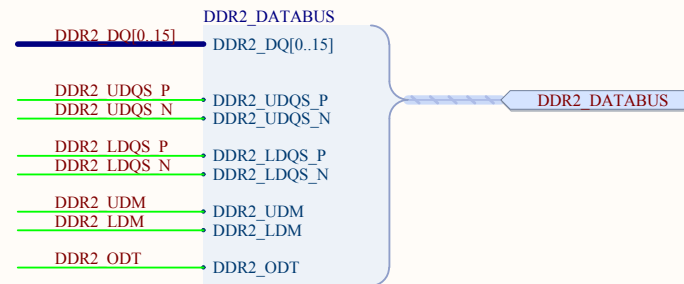
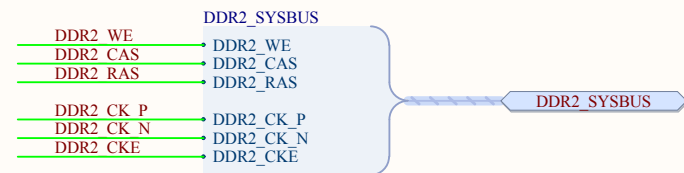
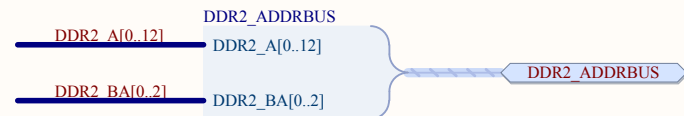
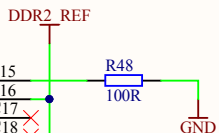
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Size	Number	Revision	
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Date:	29.3.2013	Sheet	13of20
File:	E:\Work\..FPGA Bank 0.SchDoc	Drawn By:	Vaclav Simek

IC9B

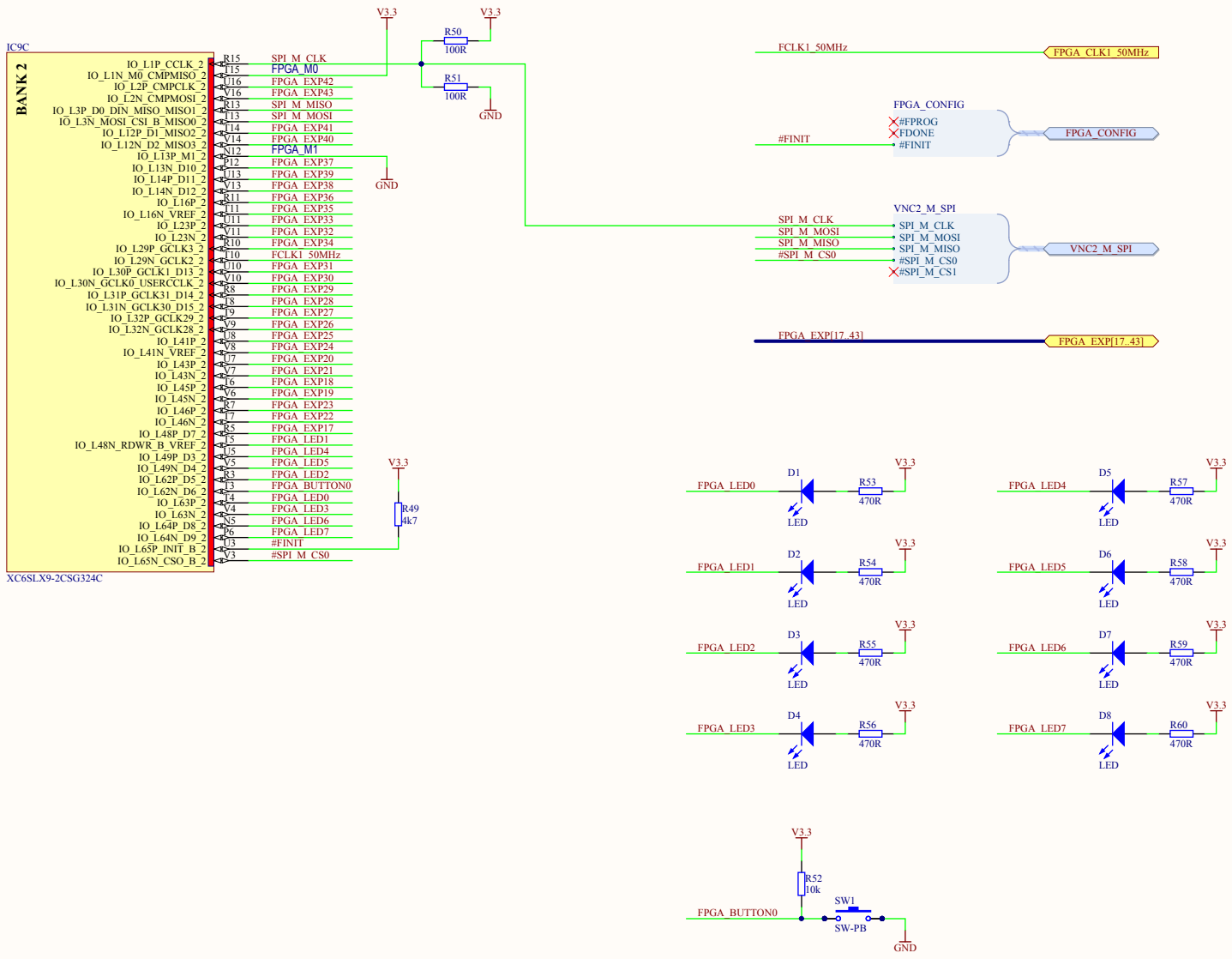
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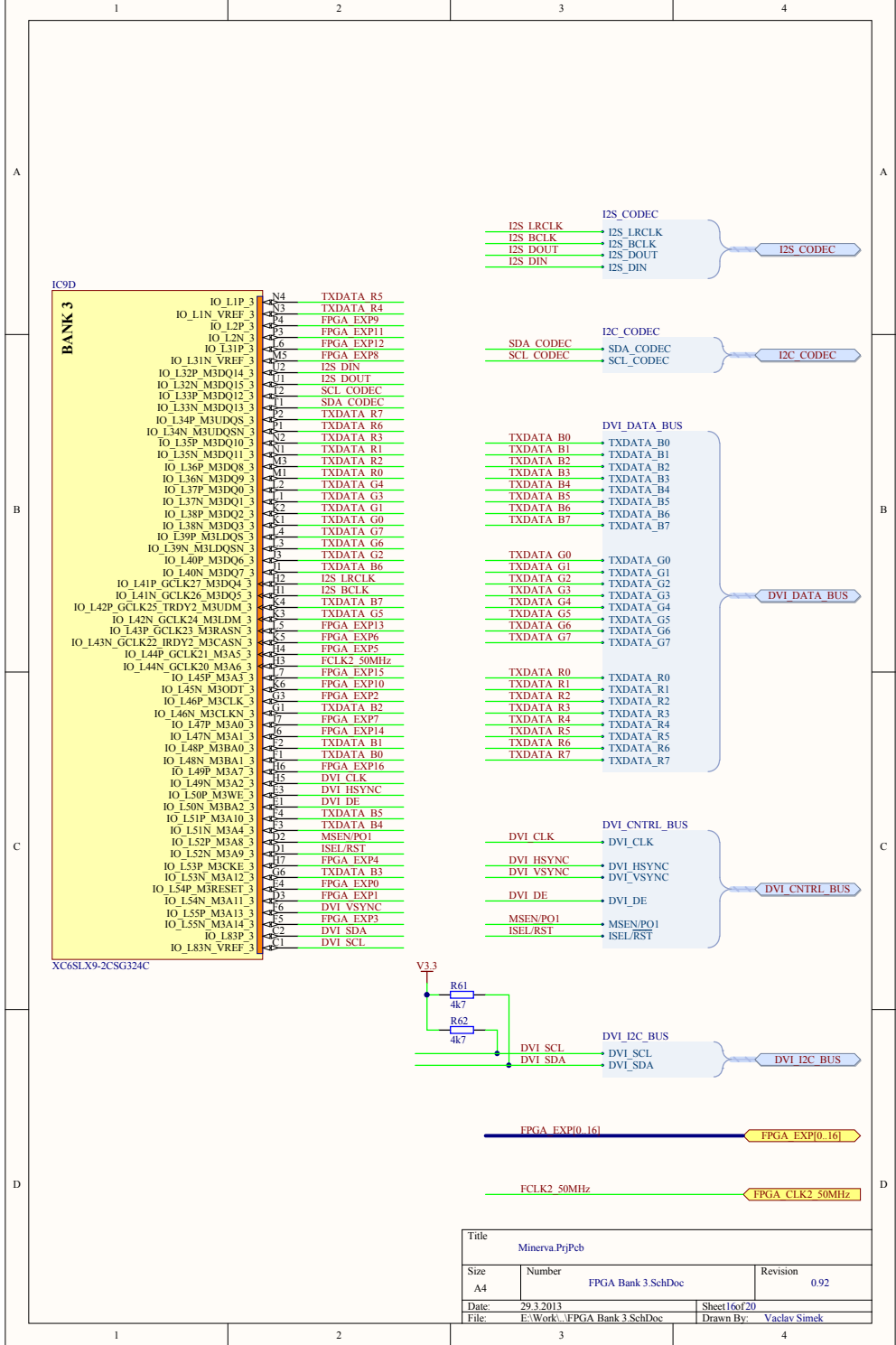
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Title			
Minerva.PrfPcb			
Size	Number	Revision	
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Date:	29.3.2013	Sheet	14of20
File:	E:\Work\..FPGA Bank 1.SchDoc	Drawn By:	Vaclav Simek



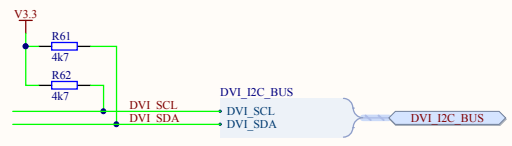
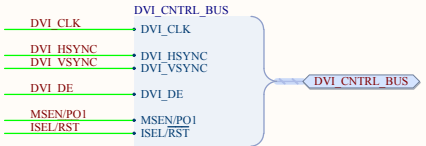
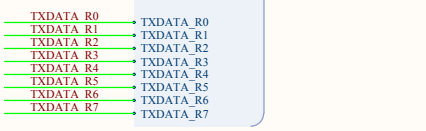
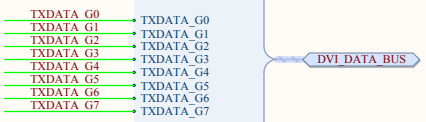
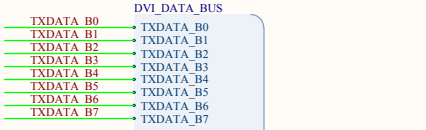
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Size	Number	Revision			
A3	FPGA Bank 2.SchDoc	0.92			
Date:	29.3.2013	Sheet 15 of 20			
File:	E:\Work\...FPGA Bank 2.SchDoc	Drawn By:		Vaclav Simek	



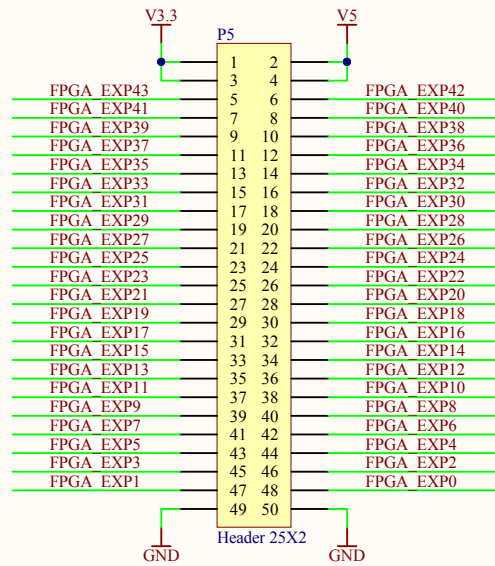
BANK 3

IO_L1P_3	N4	TXDATA R5
IO_L1N_VREF_3	N3	TXDATA R4
IO_L2P_3	N4	FPGA EXP9
IO_L2N_3	N3	FPGA EXP11
IO_L31P_3	N6	FPGA EXP12
IO_L31N_VREF_3	N5	FPGA EXP8
IO_L32P_M3DDQ14_3	N2	I2S_DIN
IO_L32N_M3DDQ15_3	N1	I2S_DOUT
IO_L33P_M3DDQ12_3	N2	SCL_CODEC
IO_L33N_M3DDQ13_3	N1	SDA_CODEC
IO_L34P_M3UDQS_3	N2	TXDATA R7
IO_L34N_M3UDQSN_3	N1	TXDATA R6
IO_L35P_M3DDQ10_3	N2	TXDATA R3
IO_L35N_M3DDQ11_3	N1	TXDATA R1
IO_L36P_M3DDQ8_3	N3	TXDATA R2
IO_L36N_M3DDQ9_3	N1	TXDATA R0
IO_L37P_M3DDQ0_3	N2	TXDATA G4
IO_L37N_M3DDQ1_3	N1	TXDATA G3
IO_L38P_M3DDQ2_3	N2	TXDATA G1
IO_L38N_M3DDQ3_3	N1	TXDATA G0
IO_L39P_M3LDS_3	N4	TXDATA G7
IO_L39N_M3LDS_3	N3	TXDATA G6
IO_L40P_M3DDQ6_3	N1	TXDATA B6
IO_L40N_M3DDQ7_3	N2	TXDATA G2
IO_L41P_GCLK27_M3DD4_3	N1	I2S_BCLK
IO_L41N_GCLK26_M3DOS_3	N4	TXDATA B7
IO_L42P_GCLK25_TRDY2_M3DDM_3	N3	TXDATA G5
IO_L42N_GCLK24_M3DDM_3	N5	TXDATA G5
IO_L43P_GCLK23_M3RASN_3	N5	FPGA EXP13
IO_L43N_GCLK22_IRDY2_M3RASN_3	N5	FPGA EXP6
IO_L44P_GCLK21_M3A5_3	N4	FPGA EXP5
IO_L44N_GCLK20_M3A6_3	N3	FCLK2 50MHz
IO_L45P_M3A3_3	N7	FPGA EXP15
IO_L45N_M3DDT_3	N3	FPGA EXP2
IO_L46P_M3CLK_3	N1	TXDATA B2
IO_L46N_M3CLKN_3	N7	FPGA EXP7
IO_L47P_M3A0_3	N6	FPGA EXP14
IO_L47N_M3A1_3	N2	TXDATA B1
IO_L48P_M3BA0_3	N1	TXDATA B0
IO_L48N_M3BA1_3	N6	FPGA EXP16
IO_L49P_M3A7_3	N5	DVI_CLK
IO_L49N_M3A2_3	N1	DVI_HSYNC
IO_L50P_M3WE_3	N1	DVI_DE
IO_L50N_M3BA2_3	N4	TXDATA B5
IO_L51P_M3A10_3	N3	TXDATA B4
IO_L51N_M3A4_3	N2	MSEN/PO1
IO_L52P_M3A8_3	N7	ISEL/RST
IO_L52N_M3A9_3	N7	FPGA EXP4
IO_L53P_M3CKE_3	N6	TXDATA B3
IO_L53N_M3A12_3	N6	DVI_VSYNC
IO_L54P_M3RESET_3	N4	FPGA EXP0
IO_L54N_M3A11_3	N3	FPGA EXP1
IO_L55P_M3A13_3	N5	DVI_VSYNC
IO_L55N_M3A14_3	N5	FPGA EXP3
IO_L83P_3	N2	DVI_SDA
IO_L83N_VREF_3	N1	DVI_SCL

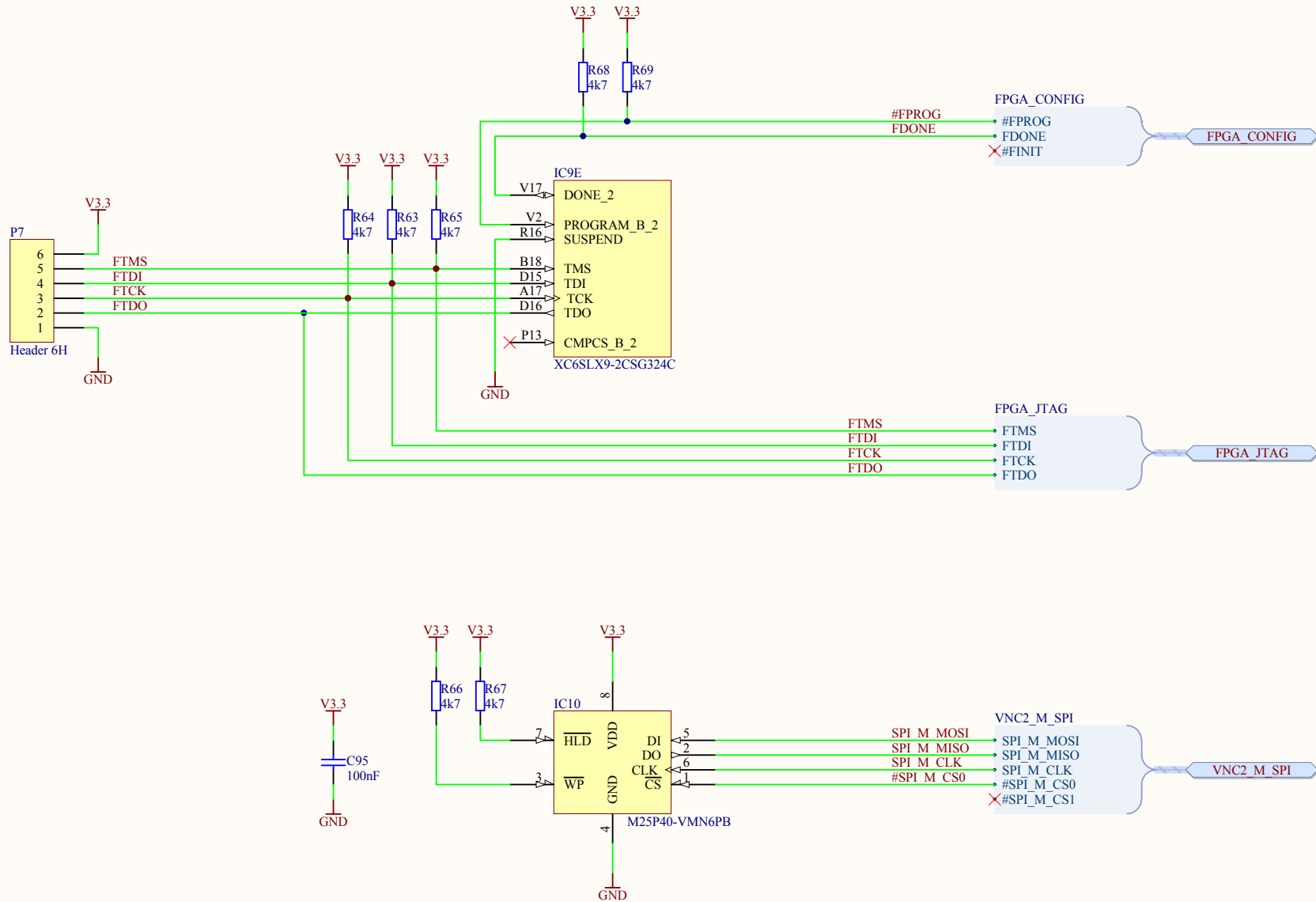
XC6SLX9-2CSG324C



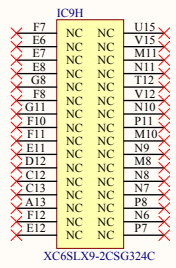
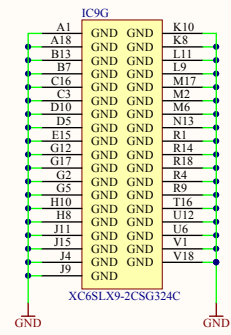
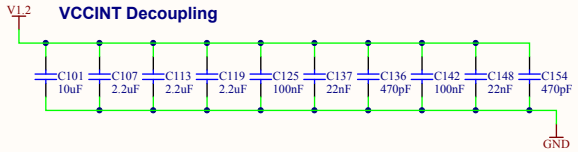
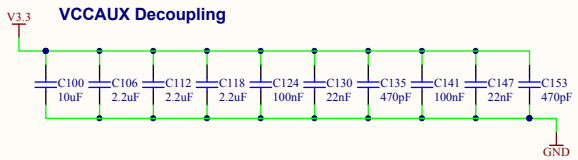
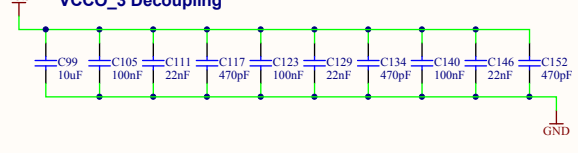
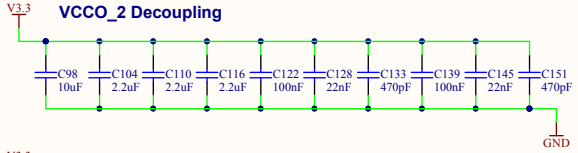
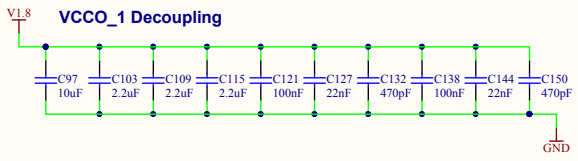
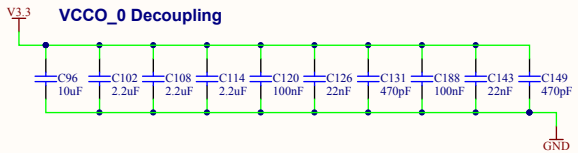
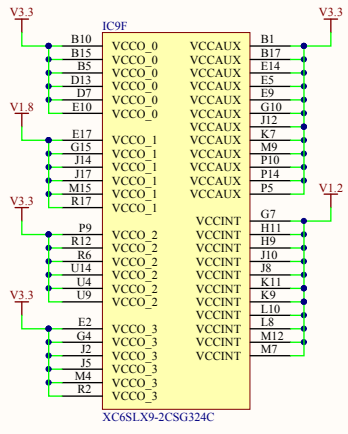
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Size	Number	Revision	
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Date:	29.3.2013	Sheet 16 of 20	
File:	E:\Work\...FPGA Bank 3 SchDoe	Drawn By:	Vaclav Simek



Title			
Minerva.PrjPcb			
Size	Number	Revision	
A4	FPGA_Expansion.SchDoc	0.92	
Date:	29.3.2013	Sheet 17 of 20	
File:	E:\Work\...\FPGA_Expansion.SchDoc	Drawn By:	Vaclav Simek



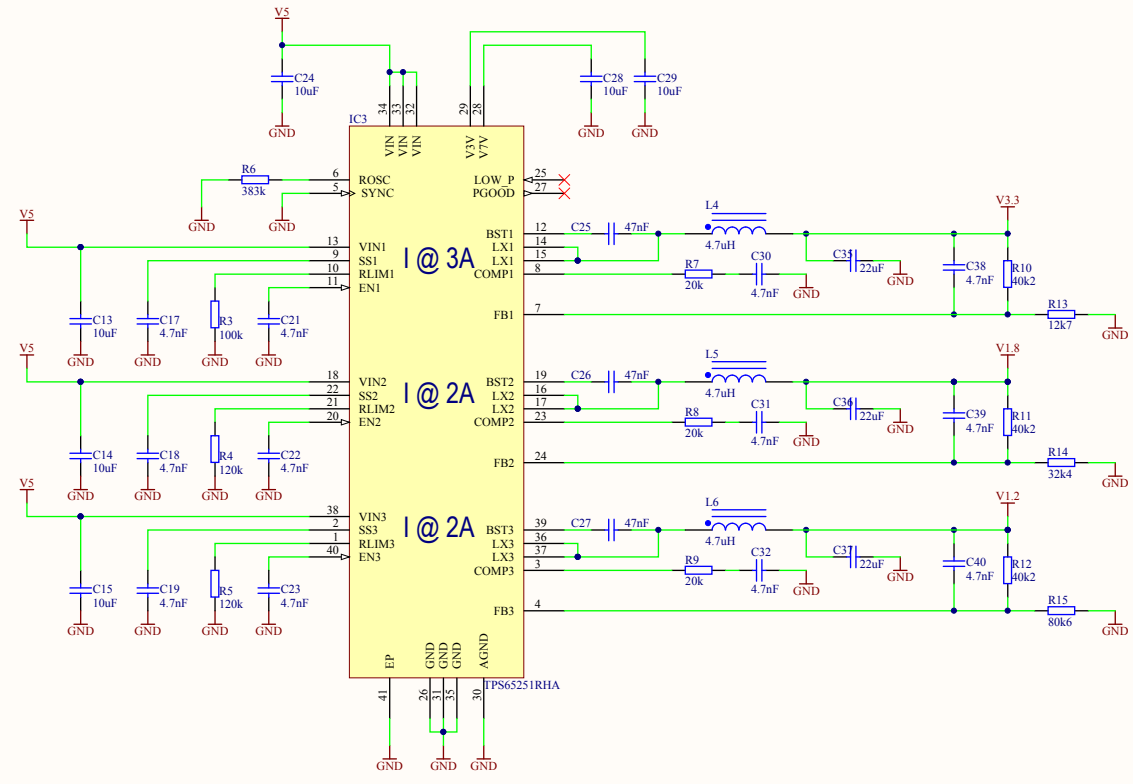
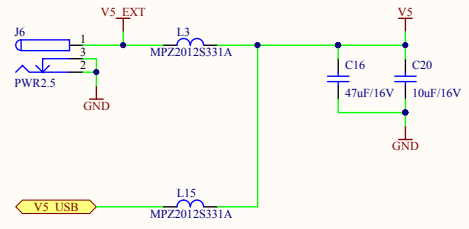
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Size	Number	Revision	
A4	FPGA Config.SchDoc	0.92	
Date:	29.3.2013	Sheet 18of20	
File:	E:\Work\..FPGA Config.SchDoc	Drawn By:	Vaclav Simek



Title			
Minerva.PjPeb			
Size	Number	Revision	
A3	FPGA Power.SchDoc	0.92	
Date:	29.3.2013	Sheet19of20	
File:	E:\Work\...FPGA Power.SchDoc	Drawn By:	Vaclav Simek

A

A

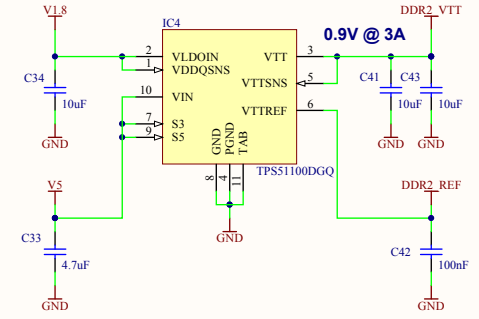


B

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C

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D

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Title			Minerva.PjPcb		
Size	Number	Revision			
A3	Board Power.SchDoc	0.92			
Date:	29.3.2013	Sheet20of20			
File:	E:\Work\Board Power.SchDoc	Drawn By:		Vaclav Simek	