Chapter 10
Pinouts and Packaging

10.1 Package Types

KM family of devices shall support the following packages options:

- 100-pin LQFP (14 x 14 mm^2)
- 64-pin LQFP (10 x 10 mm^2)
- 44-pin LGA (5 x 5 mm^2)

NOTE

Pin muxing selection between TAMPER0 and WKUP is done using control bit in RTC registers.

NOTE

All pin muxing configurations reset to default value on any reset assertion (reset asserts on VLLSx mode exit).

When RESET pin is used as GPIO and pulled low; an internal reset (e.g. VLLSx mode exit or WDOG reset, etc) will make this pin function as RESET (default function) and since it is pulled low, it will appear as if pin reset is asserted and will cause full chip reset.

NOTE

- For devices other than MKMx4, the SDADP3 and SDADM3 functions on the corresponding pins are disabled.
- All input pins including TAMPER pins must be pulled up or down to avoid extra power consumption.

10.2 Photon Signal Multiplexing and Pin Assignments

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	–	Disabled	LCD23	PTA0						

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
2	2	—	Disabled	LCD24	PTA1						
3	3	—	Disabled	LCD25	PTA2						
4	—	—	Disabled	LCD26	PTA3						
5	4	1	NMI_B	LCD27	PTA4	LLWU_P15					NMI_B
6	5	2	Disabled	LCD28	PTA5	CMP0OUT					
7	6	3	Disabled	LCD29	PTA6	PXBAR_IN0	LLWU_P14				
8	7	4	Disabled	LCD30	PTA7	PXBAR_OUT0					
9	—	—	Disabled	LCD31	PTB0						
10	8	5	VDD	VDD							
11	9	6	VSS	VSS							
12	—	—	Disabled	LCD32	PTB1						
13	—	—	Disabled	LCD33	PTB2						
14	—	—	Disabled	LCD34	PTB3						
15	—	—	Disabled	LCD35	PTB4						
16	—	—	Disabled	LCD36	PTB5						
17	—	—	Disabled	LCD37/ CMP1P0	PTB6						
18	10	—	Disabled	LCD38	PTB7	AFE_CLK					
19	11	—	Disabled	LCD39	PTC0	SCI3_RTS	PXBAR_IN1				
20	12	—	Disabled	LCD40/ CMP1P1	PTC1	SCI3_CTS					
21	13	—	Disabled	LCD41	PTC2	SCI3_TxD	PXBAR_OUT1				
22	14	—	Disabled	LCD42/ CMP0P3	PTC3	SCI3_RxD	LLWU_P13				
23	—	—	Disabled	LCD43	PTC4						
24	15	7	VBAT	VBAT							
25	16	8	XTAL32K	XTAL32K							
26	17	9	EXTAL32K	EXTAL32K							
27	18	10	VSS	VSS							
28	18	10	TAMPER2	TAMPER2							
29	18	10	TAMPER1	TAMPER1							
30	19	11	WKUP	TAMPER0							
31	20	12	VDDA	VDDA							
32	21	13	VSSA	VSSA							
33	22	14	SDADP0	SDADP0							
34	23	15	SDADM0	SDADM0							
35	24	16	SDADP1	SDADP1							
36	25	17	SDADM1	SDADM1							
37	26	18	VREFH	VREFH							
38	27	19	VREFL	VREFL							
39	28	20	SDADP2/ CMP1P2	SDADP2/ CMP1P2							

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
40	29	21	SDADM2/ CMP1P3	SDADM2/ CMP1P3							
41	30	22	VREF	VREF							
42	—	24	SDADP3/ CMP1P4	SDADP3/ CMP1P4							
43	—	23	SDADM3/ CMP1P5	SDADM3/ CMP1P5							
44	—	—	Disabled	AD0	PTC5	SCI0_RTS	LLWU_P12				
45	—	—	Disabled	AD1	PTC6	SCI0_CTS	QT1				
46	—	—	Disabled	AD2	PTC7	SCI0_TxD	PXBAR_OUT2				
47	—	—	Disabled	CMP0P0	PTD0	SCI0_RxD	PXBAR_IN2	LLWU_P11			
48	31	—	Disabled		PTD1	SCI1_TxD	SPI0_SS_B	PXBAR_OUT3	QT3		
49	32	—	Disabled	CMP0P1	PTD2	SCI1_RxD	SPI0_SCK	PXBAR_IN3	LLWU_P10		
50	33	—	Disabled		PTD3	SCI1_CTS	SPI0_MOSI				
51	34	—	Disabled	AD3	PTD4	SCI1_RTS	SPI0_MISO	LLWU_P9			
52	—	—	Disabled	AD4	PTD5	LPTIM2	QT0	SCI3_CTS			
53	—	—	Disabled	AD5	PTD6	LPTIM1	CMP1OUT	SCI3_RTS	LLWU_P8		
54	—	—	Disabled	CMP0P4	PTD7	I2C0_SCL	PXBAR_IN4	SCI3_RxD	LLWU_P7		
55	—	—	Disabled		PTE0	I2C0_SDA	PXBAR_OUT4	SCI3_TxD	CLKOUT		
56	35	25	RESET_B		PTE1						RESET_B
57	—	26	EXTAL1	EXTAL1	PTE2	EWM_IN	PXBAR_IN6	I2C1_SDA			
58	—	27	XTAL1	XTAL1	PTE3	EWM_OUT	AFE_CLK	I2C1_SCL			
59	36	28	VSS	VSS							
60	36	29	SAR_VSSA	SAR_VSSA							
61	37	30	SAR_VDDA	SAR_VDDA							
62	37	31	VDD	VDD							
63	—	—	Disabled		PTE4	LPTIM0	SCI2_CTS	EWM_IN			
64	—	—	Disabled		PTE5	QT3	SCI2_RTS	EWM_OUT	LLWU_P6		
65	38	32	SWD_IO	CMP0P2	PTE6	PXBAR_IN5	SCI2_RxD	LLWU_P5	I2C0_SCL		SWD_IO
66	39	33	SWD_CLK	AD6	PTE7	PXBAR_OUT5	SCI2_TxD		I2C0_SDA		SWD_CLK
67	40	—	Disabled	AD7	PTF0	RTCCLKOUT	QT2	CMP0OUT	LLWU_P4		
68	41	34	Disabled	LCD0/ AD8	PTF1	QT0	PXBAR_OUT6				
69	42	35	Disabled	LCD1/ AD9	PTF2	CMP1OUT	RTCCLKOUT				
70	43	—	Disabled	LCD2	PTF3	SPI1_SS_B	LPTIM1	SCI0_RxD			
71	44	—	Disabled	LCD3	PTF4	SPI1_SCK	LPTIM0	SCI0_TxD			
72	45	—	Disabled	LCD4	PTF5	SPI1_MISO	I2C1_SCL				
73	46	—	Disabled	LCD5	PTF6	SPI1_MOSI	I2C1_SDA	LLWU_P3			
74	47	—	Disabled	LCD6	PTF7	QT2	CLKOUT				
75	48	—	Disabled	LCD7	PTG0	QT1	LPTIM2				
76	49	36	Disabled	LCD8/ AD10	PTG1	LLWU_P2	LPTIM0				

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
77	50	37	Disabled	LCD9/ AD11	PTG2	SPI0_SS_B	LLWU_P1				
78	51	38	Disabled	LCD10	PTG3	SPI0_SCK	I2C0_SCL				
79	52	39	Disabled	LCD11	PTG4	SPI0_MOSI	I2C0_SDA				
80	53	40	Disabled	LCD12	PTG5	SPI0_MISO	LPTIM1				
81	54	—	Disabled	LCD13	PTG6	LLWU_P0	LPTIM2				
82	—	—	Disabled	LCD14	PTG7						
83	—	—	Disabled	LCD15	PTH0						
84	—	—	Disabled	LCD16	PTH1						
85	—	—	Disabled	LCD17	PTH2						
86	—	—	Disabled	LCD18	PTH3						
87	—	—	Disabled	LCD19	PTH4						
88	—	—	Disabled	LCD20	PTH5						
89	—	41	Disabled		PTH6	SCI1_CTS	SPI1_SS_B	PXBAR_IN7			
90	—	42	Disabled		PTH7	SCI1_RTS	SPI1_SCK	PXBAR_OUT7			
91	55	43	Disabled	CMP0P5	PTI0	SCI1_RxD	PXBAR_IN8	SPI1_MISO	SPI1_MOSI		
92	56	44	Disabled		PTI1	SCI1_TxD	PXBAR_OUT8	SPI1_MOSI	SPI1_MISO		
93	57	—	Disabled	LCD21	PTI2						
94	58	—	Disabled	LCD22	PTI3						
95	59	—	VSS	VSS							
96	60	—	VLL3	VLL3							
97	61	—	VLL2	VLL2							
98	62	—	VLL1	VLL1							
99	63	—	VCAP2	VCAP2							
100	64	—	VCAP1	VCAP1							

10.3 KM Family Pinouts

10.3.1 100-pin LQFP

Figure below shows the KM 100 LQFP pinouts.

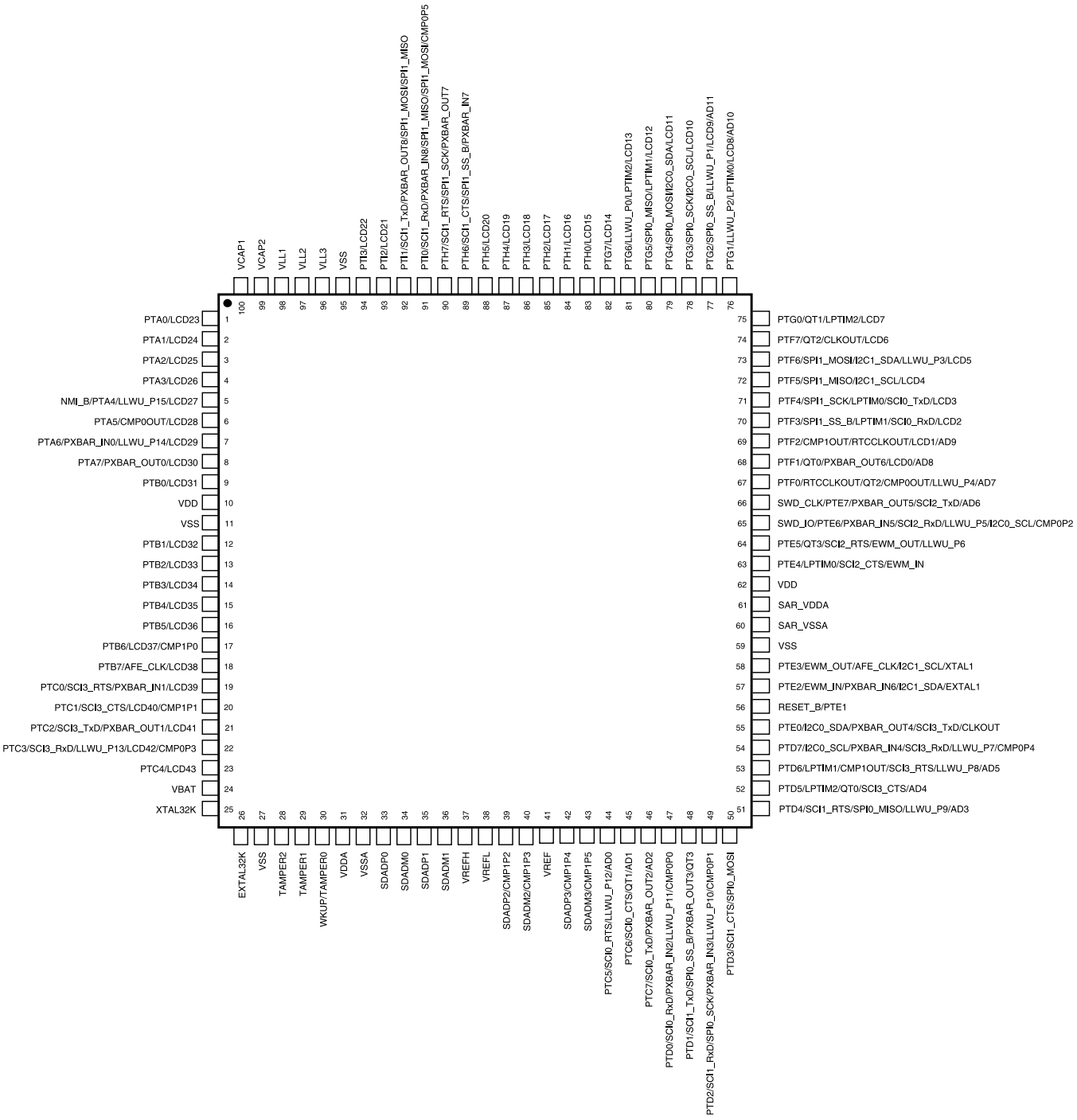

Figure 10-1. 100-pin LQFP Pinout Diagram

10.3.2 64-pin LQFP

Figure below shows the 64-pin LQFP pinouts.

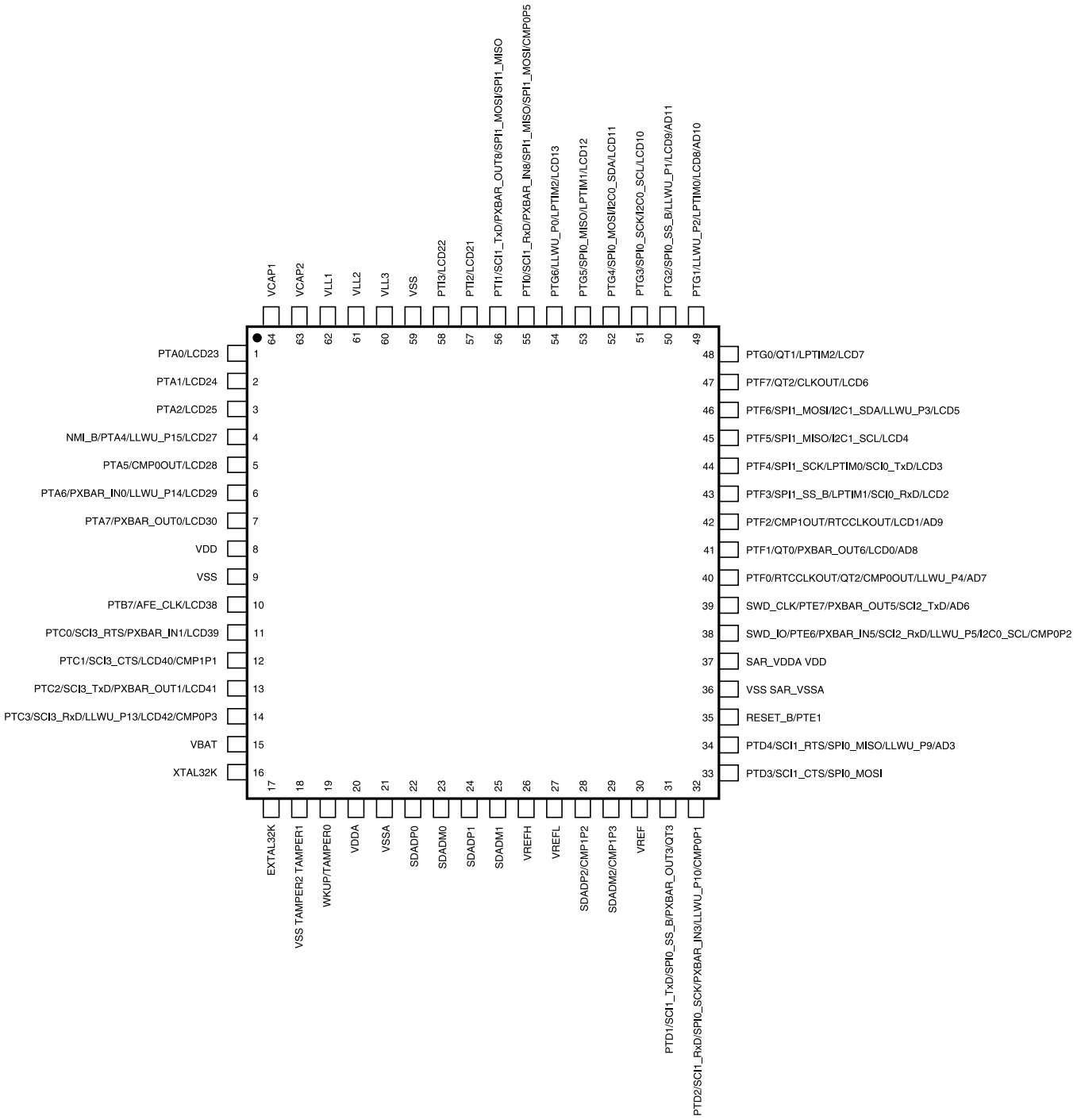

Figure 10-2. 64-pin LQFP Pinout Diagram

10.3.3 44-pin LGA

Figure below shows the 44-pin LGA pinouts.

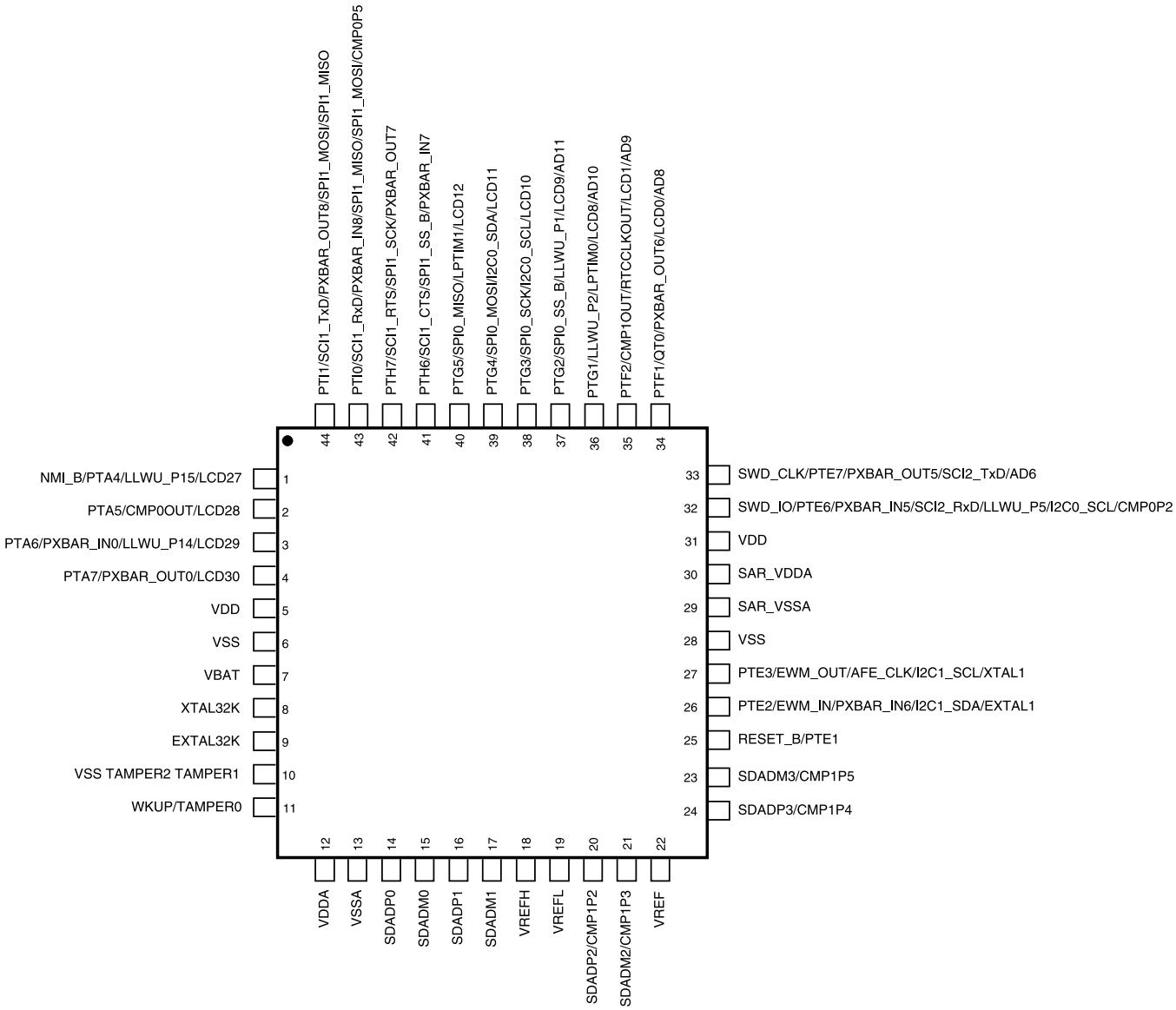

Figure 10-3. 44-pin LGA Pinout Diagram

NOTE

VSS also connects to flag on 44 LGA.