


1. Unless Otherwise Specified:
 All resistors are in ohms
 All capacitors are in uF
 All voltages are DC
 All polarized capacitors are aluminum electrolytic
2. Interrupted lines coded with the same letter or letter combinations are electrically connected.
3. Device type number is for reference only. The number varies with the manufacturer.
4. Special signal usage:
 _B Denotes - Active-Low Signal
 <> or [] Denotes - Vectored Signals
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Power & Ground Nets

NET	VOLTAGE	DESCRIPTION
P5V_USB	5V	Primary input power. Filtered from USB connector. Input to USB power switch.
P5V_SW	5V	Output of USB power switch controlled by the 5V_EN signal from the JM60 MCU. Used by OSBDM voltage translation circuits.
P5V_TRG_USB	5V	Output of USB power switch controlled by the VTRG_EN signal from the JM60 MCU. Provides input to regulator.
P3V3	3.3V	Output of regulator using USB power input (P5V_TRG_USB).
SYS_PWR	3.3V/1.8V	MCU digital power. Can Default 3.3V, Opetional 1.8V
CORE_MCU	3.3V/1.8V	MCU digital power. Can Default 3.3V Derived from SYS_PWR, Opetional 1.8V
P1V8	1.8V	Opetional Poqwer rail to power the power by 1.8V.
VDDA	3.3V	VDDA power for MCU and analog circuits. Filtered from P3V3_MCU.
VREFH	3.3V	Upper reference voltage for ADC on the MCU. Filtered from VDDA.
VREFL	0V	Lower reference voltage for ADC on the MCU. Filtered from VSSA.
VSSA	0V	VSSA power for MCU and analog circuits. Filtered from GND.
GND	0V	Digital Ground.

		
ICAP Classification: FCP: _____ FIUO: X PUBI: _____		
Drawing Title: TWR-K53N512		
Page Title: NOTE		
Size C	Document Number SCH-26994 PDF: SPF-26994	Rev BX2
Date: Friday, May 13, 2011	Sheet 2 of 8	

Sheet 8

ELEVATOR CONNECTORS

Sheet 5

OSJTAG/USB Bridge Circuit
USB Mini B Connector
MC9S08JM60
Voltage Translation
OSJTAG/JTAG Header
SCI Source Selectors
Power Supply Circuits

Sheet 4

PK53N512CMD100
50MHz XTAL
32.768 KHz XTAL
VSSA/VDDA filter
VREFH/VREFL filter
VREF_OUT
VREGIN, VOUT33
VBAT

Sheet 7

INFRARED PORT

Sheet 7

PUSH BUTTONS

Sheet 6

CAPACITIVE TOUCH PADS
WITH LEDs

Sheet 7

MEDICAL CONNECTOR

Sheet 7

SD CARD SOCKET

Sheet 6


TOWER PLUG-IN (TWRPI)
SENSOR HEADERS

Sheet 6

ANALOG INPUTS
MMA7660 ACCELEROMETER
POTENTIOMETER

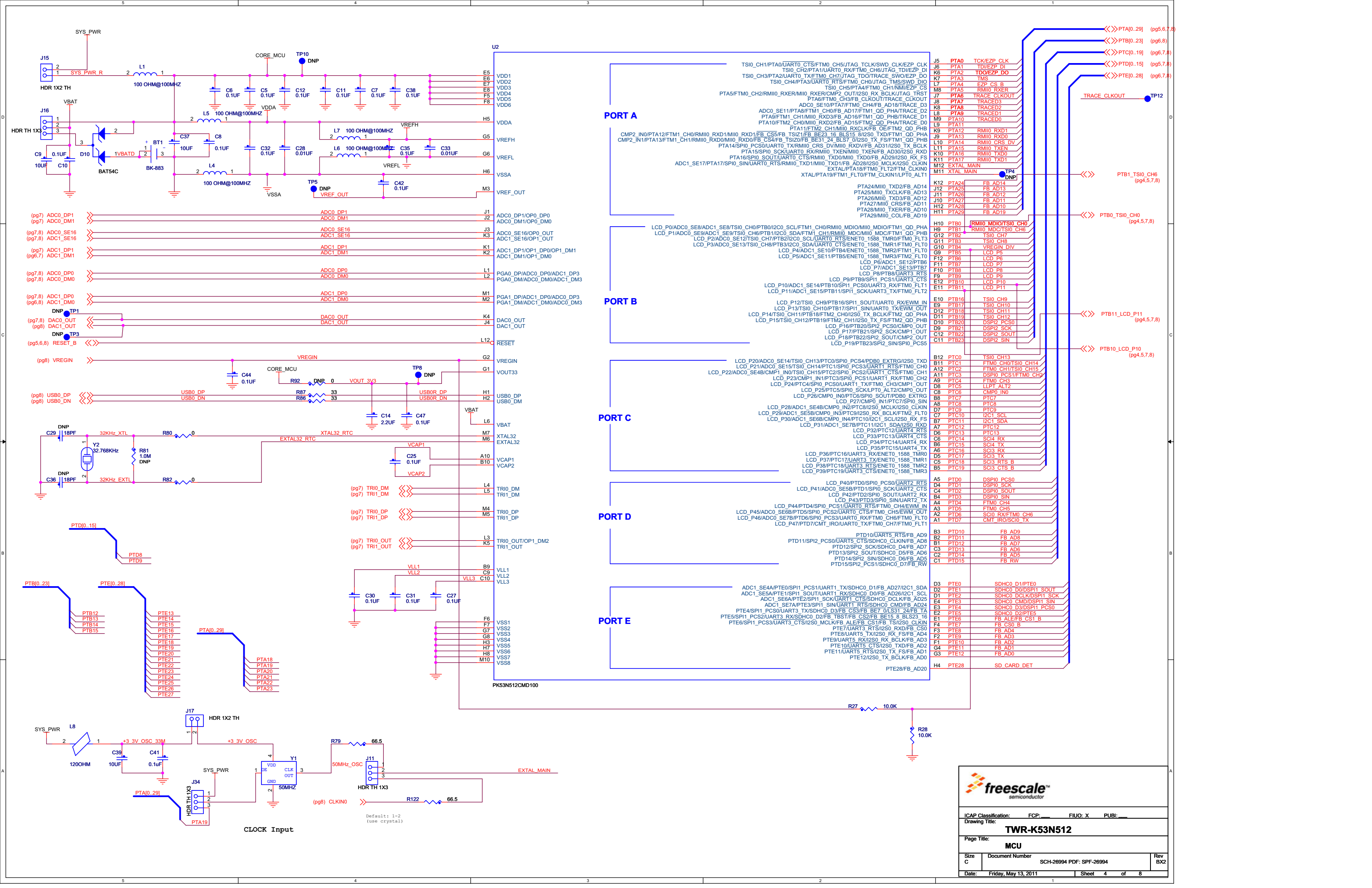
Sheet 6

TOWER PLUG-IN (TWRPI)
TOUCH HEADER



ICAP Classification: FCP: FIUO: X PUBI:
Drawing Title: **TWR-K53N512**
Page Title: **Block Diagram**

Size C	Document Number SCH-26994 PDF: SPF-26994	Rev BX2
Date: Friday, May 13, 2011	Sheet 3 of 8	



PORT A

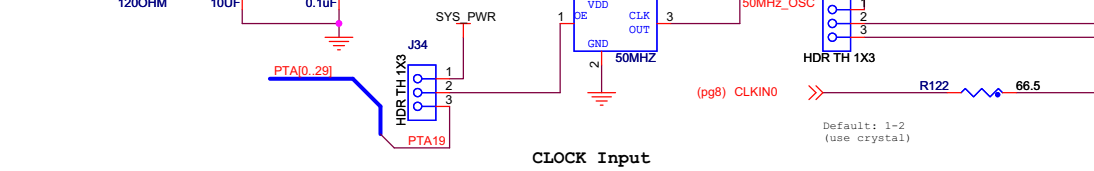
PORT B

PORT C

PORT D

PORT E

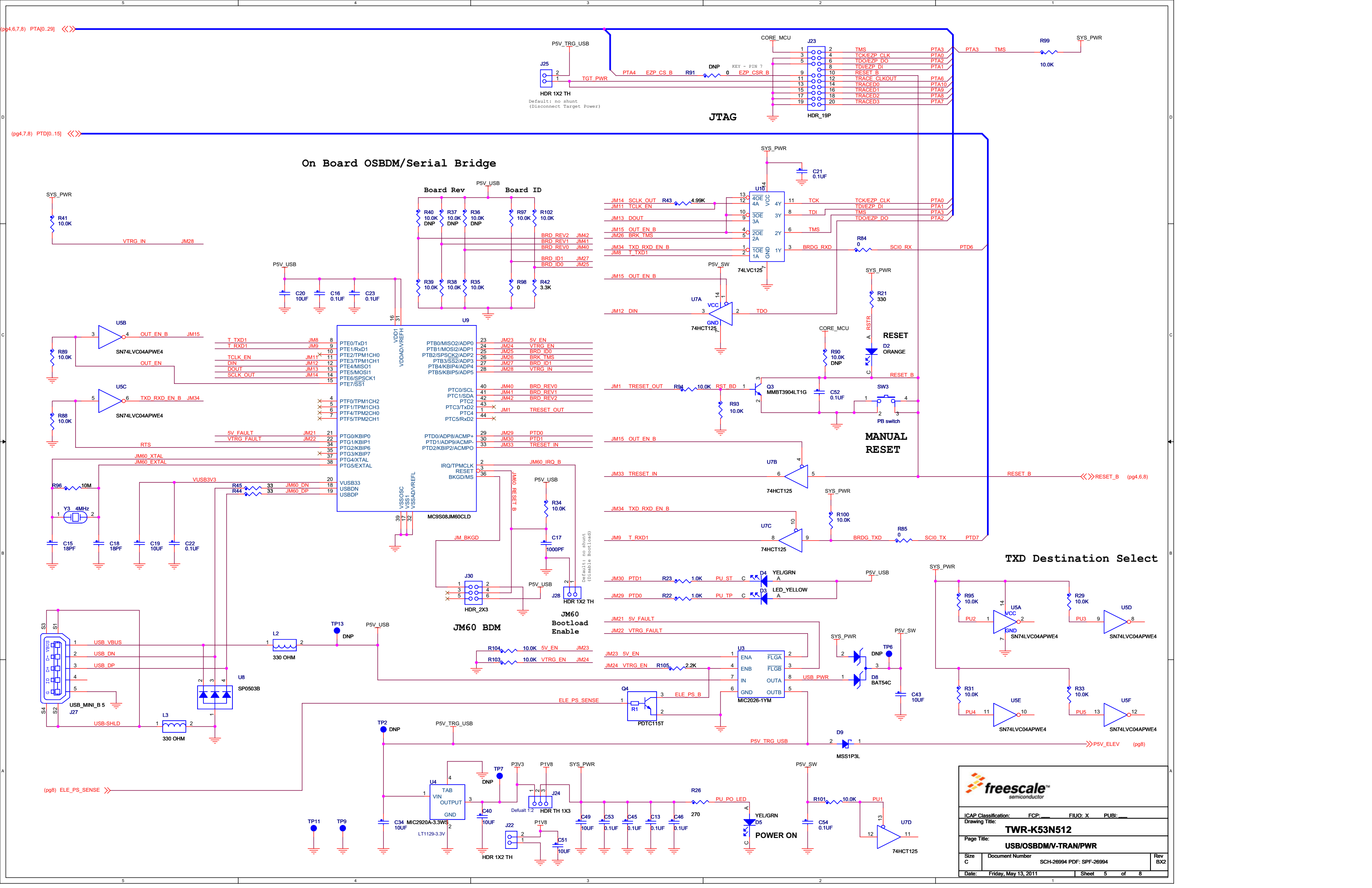
E5	VDD1	TSIO_CH1/PTA0/UART0_CTS/FTM0_CH5/JTAG_TCLK/SWD_CLK/EZP_CLK
E6	VDD2	TSIO_CH2/PTA1/UART0_RX/FTM0_CH6/JTAG_TDI/EZP_DI
E7	VDD3	TSIO_CH3/PTA2/UART0_TX/FTM0_CH7/JTAG_TDO/EZP_DO
E8	VDD4	PTA6/FTM0_CH3/FB_BLS23_16_BLS15_8/I2S0_TX_FS/FTM1_QD_PHA
F5	VDD5	TSIO_CH4/PTA3/UART0_RTS/FTM0_CH0/JTAG_TMS/SWD_DIO
F8	VDD6	TSIO_CH5/PTA4/FTM0_CH1/NMI/EZP_CS
H5	VDDA	PTA5/FTM0_CH2/RMII0_RXER/MII0_RXER/CMP2_OUT/I2S0_RX_BCLK/JTAG_TRST
G5	VREFH	PTA6/FTM0_CH3/FB_BLS23_16_BLS15_8/I2S0_TX_FS/FTM1_QD_PHA
G6	VREFL	ADC0_SE10/PTA7/FTM0_CH4/FB_AD18/TRACE_D3
H6	VSSA	PTA10/FTM2_CH0/MII0_RXD2/FB_AD15/FTM2_QD_PHA/TRACE_D0
M3	VREF_OUT	PTA11/FTM2_CH1/MII0_RXCLK/FB_OE/FTM2_QD_PHB
J1	ADC0_DP1	CMP2_IN0/PTA12/FTM1_CH0/RMII0_RXD1/MII0_RXD0/FB_CS5/FB_TS20/FB_BLS23_16_BLS15_8/I2S0_TX_FS/FTM1_QD_PHA
J2	ADC0_DM1	CMP2_IN1/PTA13/FTM1_CH1/RMII0_RXD0/MII0_RXD0/FB_CS4/FB_TS20/FB_BLS23_16_BLS15_8/I2S0_TX_FS/FTM1_QD_PHB
K3	ADC0_SE16	PTA14/SPI0_PCS0/UART0_TX/RMII0_CRS_DV/MII0_RXD0/FB_AD31/I2S0_TX_BCLK
K4	DAC0_OUT	PTA15/SPI0_SCK/UART0_RX/RMII0_TXEN/MII0_TXEN/FB_AD30/I2S0_RXD
K5	DAC1_OUT	PTA16/SPI0_SOUT/UART0_CTS/RMII0_TXD0/MII0_TXD0/FB_AD29/I2S0_RX_FS
L1	PGA0_DP	ADC1_SE17/PTA17/SPI0_SIN/UART0_RTS/RMII0_TXD1/MII0_TXD1/FB_AD28/I2S0_MCLK/I2S0_CLKIN
L2	PGA0_DM	XTAL/PTA18/FTM0_FLT2/FTM_CLKIN0
M1	PGA1_DP	XTAL/PTA19/FTM1_FLT0/FTM_CLKIN1/LPT0_ALT1
M2	PGA1_DM	PTA24/MII0_TXD2/FB_AD14
K1	ADC1_DP1	PTA25/MII0_TXCLK/FB_AD13
K2	ADC1_DM1	PTA26/MII0_TXD3/FB_AD12
L3	RESET	PTA27/MII0_CRS/FB_AD11
H1	USB0_DP	PTA28/MII0_TXER/FB_AD10
H2	USB0_DM	PTA29/MII0_COL/FB_AD9
M7	EXTAL32	
M6	EXTAL32	
A10	VCAP1	
B10	VCAP2	
L4	TRI0_DM	LCD_P0/ADC0_SE8/ADC1_SE8/TSIO_CH0/PTB0/I2C0_SCL/FTM1_CH0/RMII0_MDI0/MII0_MDI0/FTM1_QD_PHA
L5	TRI1_DM	LCD_P1/ADC0_SE9/ADC1_SE9/TSIO_CH1/PTB1/I2C0_SDA/FTM1_CH1/RMII0_MDC0/MII0_MDC0/FTM1_QD_PHB
M4	TRI0_DP	LCD_P2/ADC0_SE12/TSIO_CH1/PTB2/I2C0_SCL/UART0_RTS/ENET0_1588_TMR0/FTM0_FLT3
M5	TRI1_DP	LCD_P3/ADC0_SE13/TSIO_CH1/PTB3/I2C0_SDA/UART0_CTS/ENET0_1588_TMR1/FTM0_FLT0
L3	TRI0_OUT/OP1_DM2	LCD_P4/ADC1_SE10/PTB4/ENET0_1588_TMR2/FTM1_FLT0
K5	TRI1_OUT	LCD_P5/ADC1_SE11/PTB5/ENET0_1588_TMR3/FTM2_FLT0
B9	VLL1	LCD_P6/ADC1_SE12/PTB6
C9	VLL2	LCD_P7/ADC1_SE13/PTB7
C10	VLL3	LCD_P8/PTB8/UART3_RTS
F6	VSS1	LCD_P9/PTB9/SPI1_PCS1/UART3_CTS
G7	VSS2	LCD_P10/ADC1_SE14/PTB10/SPI1_PCS0/UART3_RX/FTM0_FLT1
G8	VSS3	LCD_P11/ADC1_SE15/PTB11/SPI1_SCK/UART3_TX/FTM0_FLT2
H3	VSS4	LCD_P12/TSIO_CH0/PTB16/SPI1_SOUT/UART0_RX/EWM_IN
H7	VSS5	LCD_P13/TSIO_CH10/PTB17/SPI1_SIN/UART0_TX/EWM_OUT
H8	VSS6	LCD_P14/TSIO_CH11/PTB18/FTM2_CH0/I2S0_TX_BCLK/FTM2_QD_PHA
H8	VSS6	LCD_P15/TSIO_CH12/PTB19/FTM2_CH1/I2S0_TX_FS/FTM2_QD_PHB
M10	VSS7	LCD_P16/PTB20/SPI2_PCS0/CMP0_OUT
G7	VSS2	LCD_P17/PTB21/SPI2_SCK/CMP1_OUT
G7	VSS2	LCD_P18/PTB22/SPI2_SOUT/CMP2_OUT
G7	VSS2	LCD_P19/PTB23/SPI2_SIN/SPI0_PCS5
F6	VSS1	LCD_P20/ADC0_SE14/TSIO_CH13/PTC0/SPI0_PCS4/PDB0_EXTRG/I2S0_TXD
G7	VSS2	LCD_P21/ADC0_SE15/TSIO_CH14/PTC1/SPI0_PCS3/UART1_RTS/FTM0_CH0
G7	VSS2	LCD_P22/ADC0_SE4B/CMP1_IN0/TSIO_CH15/PTC2/SPI0_PCS2/UART1_CTS/FTM0_CH1
G7	VSS2	LCD_P23/CMP1_IN1/PTC3/SPI0_PCS1/UART1_RX/FTM0_CH2
G7	VSS2	LCD_P24/PTC4/SPI0_PCS0/UART1_TX/FTM0_CH3/CMP1_OUT
G7	VSS2	LCD_P25/PTC5/SPI0_SCK/LPT0_ALT2/CMP0_OUT
G7	VSS2	LCD_P26/CMP0_IN0/PTC6/SPI0_SOUT/PDB0_EXTRG
G7	VSS2	LCD_P27/CMP0_IN/PTC7/SPI0_SIN
G7	VSS2	LCD_P28/ADC1_SE4B/CMP0_IN2/PTC8/I2S0_MCLK/I2S0_CLKIN
G7	VSS2	LCD_P29/ADC1_SE5B/CMP0_IN3/PTC9/I2S0_RX_BCLK/FTM2_FLT0
G7	VSS2	LCD_P30/ADC1_SE6B/CMP0_IN4/PTC10/I2C1_SCL/I2S0_RX_FS
G7	VSS2	LCD_P31/ADC1_SE7B/PTC11/I2C1_SDA/I2S0_RXD
G7	VSS2	LCD_P32/PTC12/UART4_RTS
G7	VSS2	LCD_P33/PTC13/UART4_CTS
G7	VSS2	LCD_P34/PTC14/UART4_RX
G7	VSS2	LCD_P35/PTC15/UART4_TX
G7	VSS2	LCD_P36/PTC16/UART3_RX/ENET0_1588_TMR0
G7	VSS2	LCD_P37/PTC17/UART3_TX/ENET0_1588_TMR1
G7	VSS2	LCD_P38/PTC18/UART3_RTS/ENET0_1588_TMR2
G7	VSS2	LCD_P39/PTC19/UART3_CTS/ENET0_1588_TMR3
L4	TRI0_DM	LCD_P40/PTD0/SPI0_PCS0/UART2_RTS
L5	TRI1_DM	LCD_P41/ADC0_SE5B/PTD1/SPI0_SCK/UART2_CTS
M4	TRI0_DP	LCD_P42/PTD2/SPI0_SOUT/UART2_RX
M5	TRI1_DP	LCD_P43/PTD3/SPI0_SIN/UART2_TX
L3	TRI0_OUT/OP1_DM2	LCD_P44/PTD4/SPI0_PCS1/UART0_RTS/FTM0_CH4/EWM_IN
K5	TRI1_OUT	LCD_P45/ADC0_SE6B/PTD5/SPI0_PCS2/UART0_CTS/FTM0_CH5/EWM_OUT
B3	PTD10	LCD_P46/ADC0_SE7B/PTD6/SPI0_PCS3/UART0_RX/FTM0_CH6/FTM0_FLT0
B2	PTD11	LCD_P47/PTD7/CMT_IRO/UART0_TX/FTM0_CH7/FTM0_FLT1
B1	PTD12	PTD10/UART5_RTS/FB_AD9
C3	PTD13	PTD11/SPI2_PCS0/UART5_CTS/SDHC0_CLKIN/FB_AD8
C2	PTD14	PTD12/SPI2_SCK/SDHC0_D4/FB_AD7
C1	PTD15	PTD13/SPI2_SOUT/SDHC0_D5/FB_AD6
D3	PTD0	PTD14/SPI2_SIN/SDHC0_D6/FB_AD5
D2	PTD1	PTD15/SPI2_PCS1/SDHC0_D7/FB_RW
D1	PTD2	
E4	PTD3	
E3	PTD4	
E2	PTD5	
E1	PTD6	
F4	PTD7	
F3	PTD8	
F2	PTD9	
F1	PTD10	
G4	PTD11	
G3	PTD12	
H4	PTD13	
D3	PTD0	SDHC0_D1/PTD0
D2	PTD1	SDHC0_D0/DSPI1_SOUT
D1	PTD2	SDHC0_DCLK/DSPI1_SCK
E4	PTD3	SDHC0_CMD/DSPI1_SIN
E3	PTD4	SDHC0_D3/DSPI1_PCS0
E2	PTD5	SDHC0_D2/PTD5
E1	PTD6	FB_ALE/FB_CS1_B
F4	PTD7	FB_CS0_B
F3	PTD8	FB_AD4
F2	PTD9	FB_AD3
F1	PTD10	FB_AD2
G4	PTD11	FB_AD1
G3	PTD12	FB_AD0
H4	PTD13	SD_CARD_DET



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Drawing Title: **TWR-K53N512**
Page Title: **MCU**

Size C	Document Number SCH-26994 PDF: SPF-26994	Rev BX2
Date: Friday, May 13, 2011	Sheet 4 of 8	



On Board OSBDM/Serial Bridge

JTAG

RESET

MANUAL RESET

TXD Destination Select

POWER ON

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semiconductor

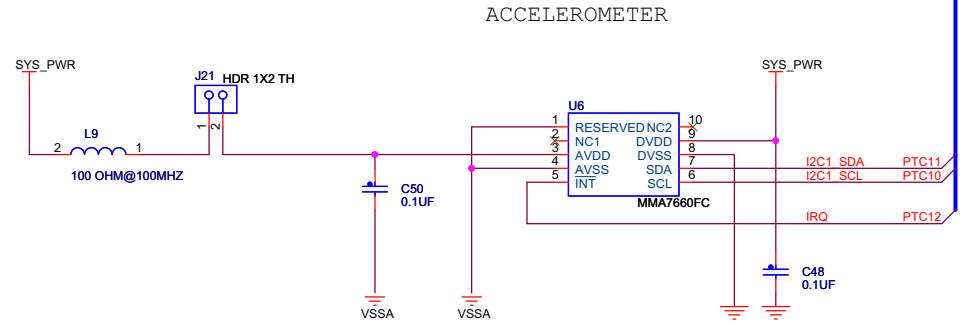
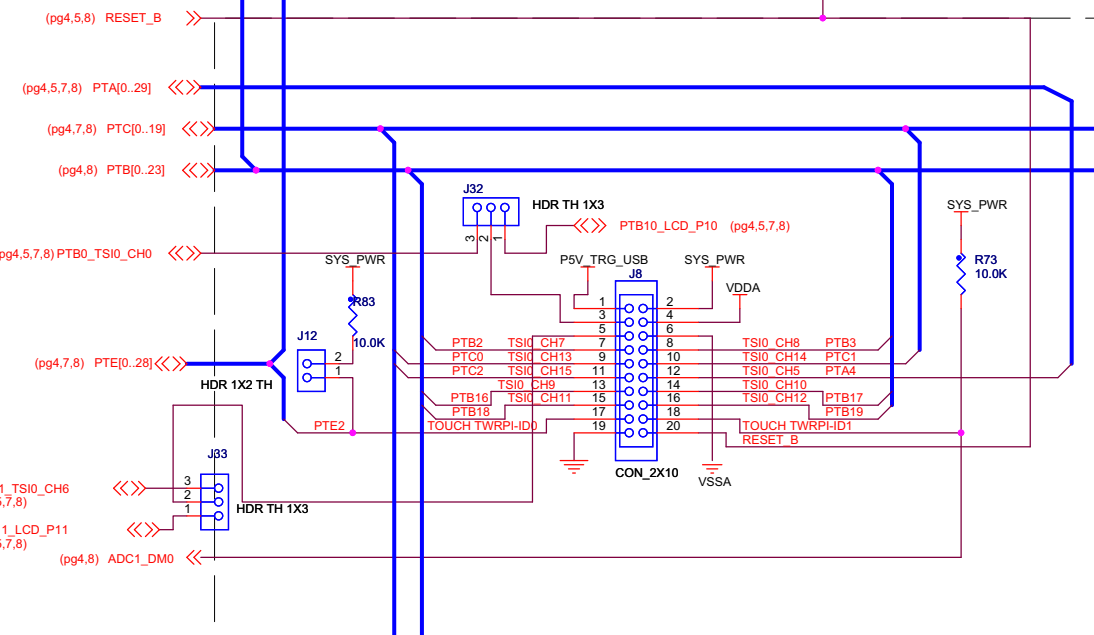
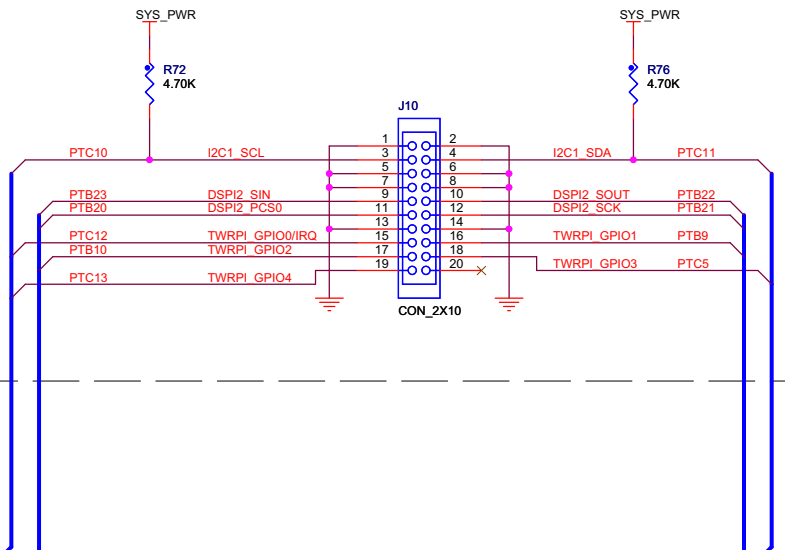
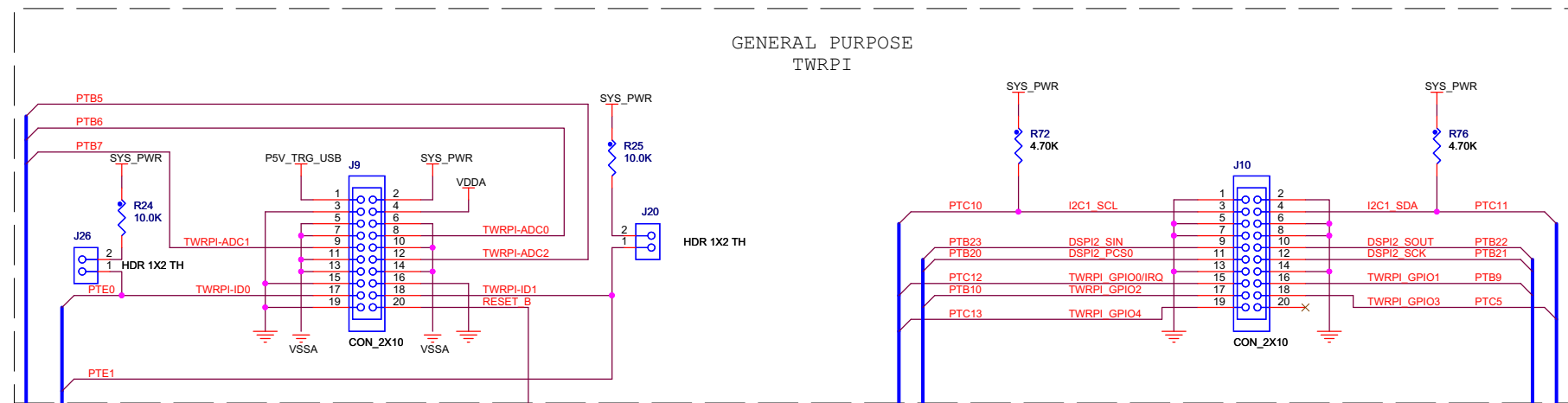
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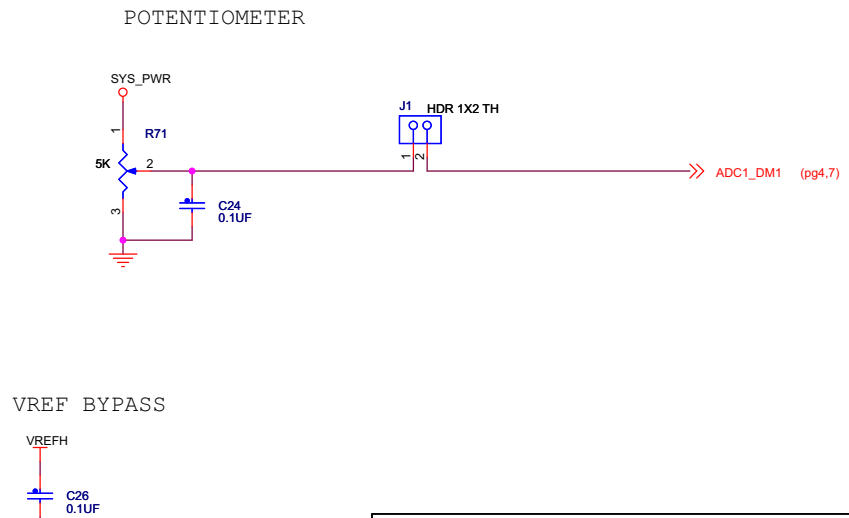
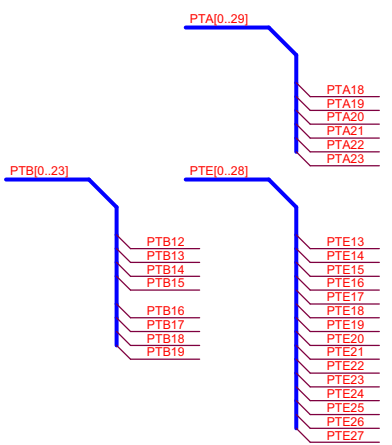
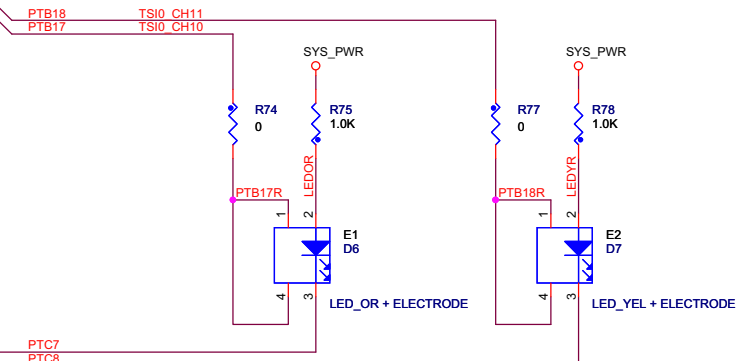
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Size C	Document Number SCH-26994 PDF: SPF-26994	Rev BX2
Date: Friday, May 13, 2011	Sheet 5 of 8	

GENERAL PURPOSE
TWRPI



NOTE:-TWRPI modules draw current from VDDA. So avoid plug in a TWRPI module if K53 current consumption need to be measured at J1.
TOUCH PAD/SLCD
TWRPI

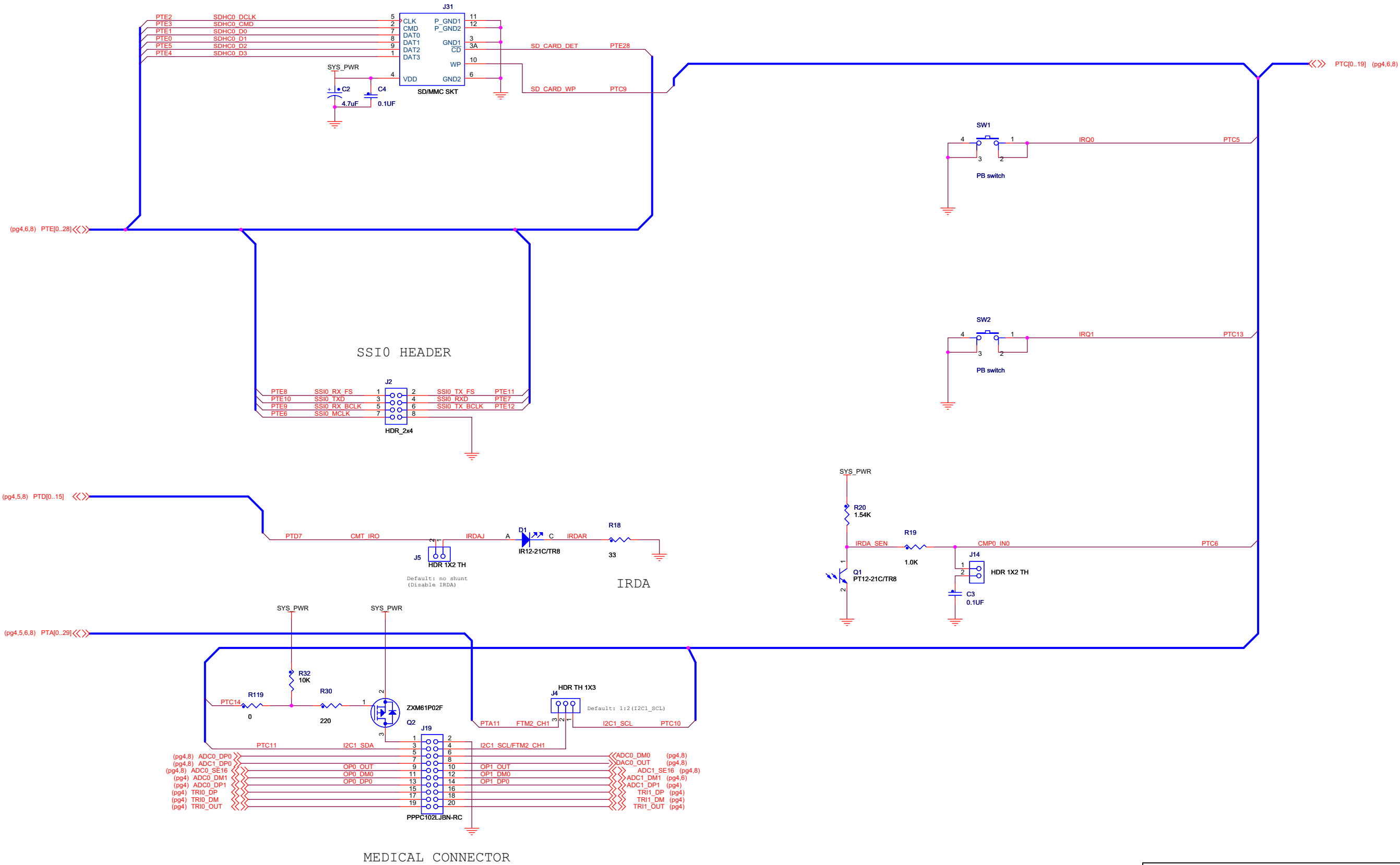


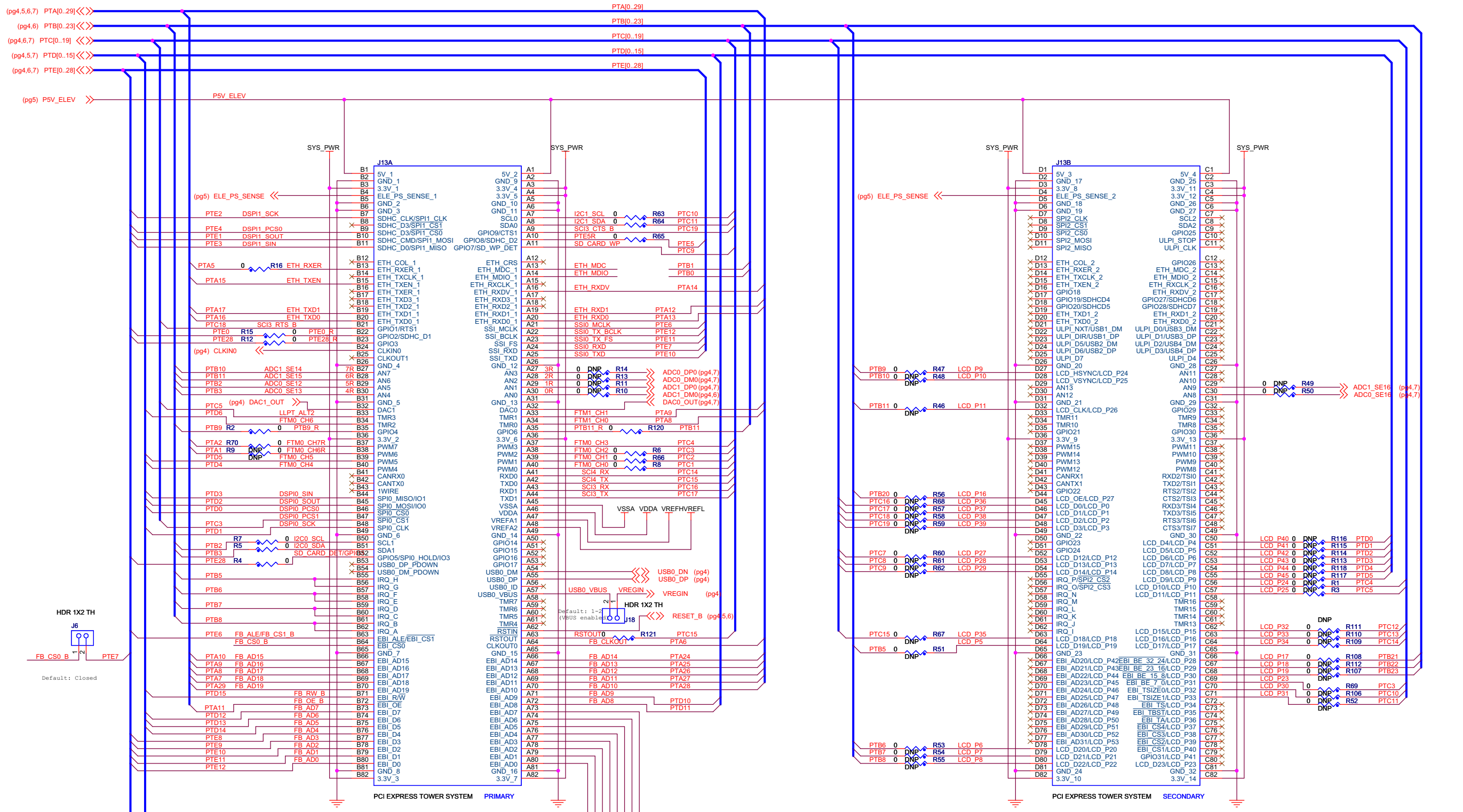
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Page Title: **Sensors**

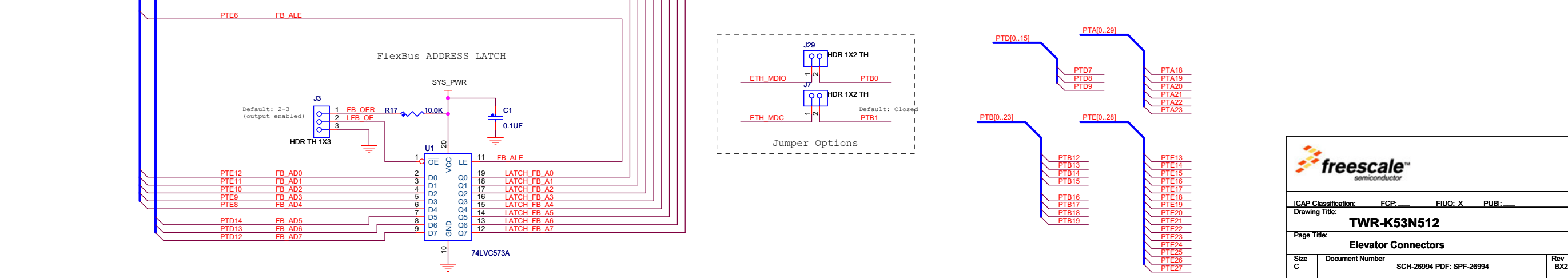
Size	Document Number	Rev
C	SCH-26994 PDF: SPF-26994	BX2

Date: Friday, May 13, 2011 | Sheet 6 of 8





(pg4,5,6,7) PTA[0..29] <<>>
 (pg4,6) PTB[0..23] <<>>
 (pg4,6,7) PTC[0..19] <<>>
 (pg4,5,7) PTD[0..15] <<>>
 (pg4,6,7) PTE[0..28] <<>>
 (pg5) P5V_ELEV >>



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 Drawing Title: **TWR-K53N512**
 Page Title: **Elevator Connectors**

Size C	Document Number SCH-26994 PDF: SPF-26994	Rev BX2
Date: Friday, May 13, 2011	Sheet 8 of 8	