```
#include "drivers.h"

#define SIM_MODULE_IRTC_RTCCLKSEL_ON_CONFIG                                      \
(tSIM){                                                                          \
/* SOPT1     */ SET(SIM_SOPT1_OSC32KSEL(0)),                                    \
/* SOPT1_CFG*/ CLR(SIM_SOPT1_CFG_RAMBPEN_MASK)|CLR(SIM_SOPT1_CFG_RAMSBDIS_MASK)|\
/* .........*/ SET(SIM_SOPT1_CFG_LPTMR3SEL(0))|SET(SIM_SOPT1_CFG_LPTMR2SEL(0))| \
/* .........*/ SET(SIM_SOPT1_CFG_LPTMR1SEL(0))|SET(SIM_SOPT1_CFG_LPTMR0SEL(0)), \
/* CTRL_REG */ CLR(SIM_CTRL_REG_TMRFREEZE_MASK)|SET(SIM_CTRL_REG_LPUARTSRC(1))| \
/* ........ */ CLR(SIM_CTRL_REG_AFEOUTCLKSEL_MASK)|                             \
/* ........ */ SET(SIM_CTRL_REG_XBARCLKOUT(0))|SET(SIM_CTRL_REG_PLLFLLSEL(2))|  \
/* ........ */ CLR(SIM_CTRL_REG_SPI1_INV3_MASK)|                                \
/* ........ */ CLR(SIM_CTRL_REG_SPI1_INV2_MASK)|                                \
/* ........ */ CLR(SIM_CTRL_REG_SPI1_INV1_MASK)|                                \
/* ........ */ CLR(SIM_CTRL_REG_SPI1_INV0_MASK)|                                \
/* ........ */ CLR(SIM_CTRL_REG_SPI0_INV3_MASK)|                                \
/* ........ */ CLR(SIM_CTRL_REG_SPI0_INV2_MASK)|                                \
/* ........ */ CLR(SIM_CTRL_REG_SPI0_INV1_MASK)|                                \
/* ........ */ CLR(SIM_CTRL_REG_SPI0_INV0_MASK)|                                \
/* ........ */ SET(SIM_CTRL_REG_CLKOUT(0))|                                     \
/* ........ */ SET(SIM_CTRL_REG_ADCTRGSEL(0))|                                  \
/* ........ */ CLR(SIM_CTRL_REG_PLLVLPEN_MASK)|SET(SIM_CTRL_REG_NMIDIS_MASK),   \
/* SCGC4     */ CLR(SIM_SCGC4_SPI1_MASK)|CLR(SIM_SCGC4_SPI0_MASK)|               \
/* ........ */ CLR(SIM_SCGC4_CMP_MASK)|CLR(SIM_SCGC4_VREF_MASK)|               \
/* ........ */ CLR(SIM_SCGC4_UART3_MASK)|CLR(SIM_SCGC4_UART2_MASK)|            \
/* ........ */ CLR(SIM_SCGC4_UART1_MASK)|CLR(SIM_SCGC4_UART0_MASK)|            \
/* ........ */ CLR(SIM_SCGC4_I2C1_MASK)|CLR(SIM_SCGC4_I2C0_MASK)|              \
/* ........ */ CLR(SIM_SCGC4_EWM_MASK),                                         \
/* SCGC5     */ CLR(SIM_SCGC5_TMR3_MASK)|CLR(SIM_SCGC5_TMR2_MASK)|              \
/* ........ */ CLR(SIM_SCGC5_TMR1_MASK)|CLR(SIM_SCGC5_TMR0_MASK)|              \
/* ........ */ CLR(SIM_SCGC5_XBAR_MASK)|SET(SIM_SCGC5_RTCREG_MASK)|            \
/* ........ */ SET(SIM_SCGC5_RTC_MASK)|                                         \
/* ........ */ CLR(SIM_SCGC5_PORTI_MASK)|CLR(SIM_SCGC5_PORTH_MASK)|            \
/* ........ */ CLR(SIM_SCGC5_PORTG_MASK)|CLR(SIM_SCGC5_PORTF_MASK)|            \
/* ........ */ CLR(SIM_SCGC5_PORTE_MASK)|CLR(SIM_SCGC5_PORTD_MASK)|            \
/* ........ */ CLR(SIM_SCGC5_PORTC_MASK)|CLR(SIM_SCGC5_PORTB_MASK)|            \
/* ........ */ CLR(SIM_SCGC5_PORTA_MASK)|CLR(SIM_SCGC5_SLCD_MASK),             \
/* SCGC6     */ CLR(SIM_SCGC6_LPTMR_MASK)|CLR(SIM_SCGC6_PORTM_MASK)|            \
/* ........ */ CLR(SIM_SCGC6_PORTL_MASK)|CLR(SIM_SCGC6_PORTK_MASK)|            \
/* ........ */ CLR(SIM_SCGC6_PORTJ_MASK)|CLR(SIM_SCGC6_PDB_MASK)|             \
/* ........ */ CLR(SIM_SCGC6_CRC_MASK)|CLR(SIM_SCGC6_AFE_MASK)|               \
/* ........ */ CLR(SIM_SCGC6_PIT1_MASK)|CLR(SIM_SCGC6_PIT0_MASK)|             \
/* ........ */ CLR(SIM_SCGC6_ADC_MASK)|CLR(SIM_SCGC6_LPUART_MASK)|            \
/* ........ */ CLR(SIM_SCGC6_RNGA_MASK)|CLR(SIM_SCGC6_DMACHMUX_MASK)|         \
/* ........ */ SET(SIM_SCGC6_FTFA_MASK),                                        \
/* SCGC7     */ CLR(SIM_SCGC7_CAU_MASK)|CLR(SIM_SCGC7_DMA_MASK)|               \
/* ........ */ CLR(SIM_SCGC7_MPU_MASK),                                         \
/* CLKDIV1   */ SET(SIM_CLKDIV1_CLKDIVSYS(0))|SET(SIM_CLKDIV1_CLKDIVBUS(1))|    \
/* ........ */ CLR(SIM_CLKDIV1_FLASHCLKMODE_MASK),                              \
/* FCFG1     */ CLR(SIM_FCFG1_FLASHDOZE_MASK)|CLR(SIM_FCFG1_FLASHDIS_MASK),     \
/* MISC_CTL */ SET(SIM_MISC_CTL_VREFBUFPD_MASK)|                                \
/* ........ */ CLR(SIM_MISC_CTL_VREFBUFINSEL_MASK)|                            \
/* ........ */ CLR(SIM_MISC_CTL_VREFBUFOUTEN_MASK)|                            \
/* ........ */ SET(SIM_MISC_CTL_RTCCLKSEL_MASK)|                               \
/* ........ */ SET(SIM_MISC_CTL_TMR3PCSSEL(0))|SET(SIM_MISC_CTL_TMR2PCSSEL(0))| \
/* ........ */ SET(SIM_MISC_CTL_TMR1PCSSEL(0))|SET(SIM_MISC_CTL_TMR0PCSSEL(0))| \
/* ........ */ CLR(SIM_MISC_CTL_TMR3SCSEL_MASK)|                               \
/* ........ */ CLR(SIM_MISC_CTL_TMR2SCSEL_MASK)|                               \
/* ........ */ CLR(SIM_MISC_CTL_TMR1SCSEL_MASK)|                               \
/* ........ */ CLR(SIM_MISC_CTL_TMR0SCSEL_MASK)|                               \
/* ........ */ CLR(SIM_MISC_CTL_TMR0PLLSEL_MASK)|                              \
/* ........ */ CLR(SIM_MISC_CTL_EWMINSEL_MASK)|                                \
/* ........ */ CLR(SIM_MISC_CTL_UART3IRSEL_MASK)|                              \
/* ........ */ CLR(SIM_MISC_CTL_UART2IRSEL_MASK)|                              \
/* ........ */ CLR(SIM_MISC_CTL_UART1IRSEL_MASK)|                              \
/* ........ */ CLR(SIM_MISC_CTL_UART0IRSEL_MASK)|                              \
/* ........ */ CLR(SIM_MISC_CTL_UARTMODTYPE_MASK)|                             \
/* ........ */ CLR(SIM_MISC_CTL_AFECLKPADDIR_MASK)|                            \
/* ........ */ SET(SIM_MISC_CTL_AFECLKSEL(0))|SET(SIM_MISC_CTL_DMADONESEL(0))|  \
/* ........ */ CLR(SIM_MISC_CTL_PDBADCTRG_MASK)                                 \
```

```
}

#define FLL_MODULE_FEI_20_25MHZ_IRCLKEN_ON_CONFIG                                \
(tFLL){                                                                          \
/* C1 */ SET(MCG_C1_CLKS(0x00))|SET(MCG_C1_FRDIV(0x00))|                         \
/* .. */ SET(MCG_C1_IREFS_MASK)|SET(MCG_C1_IRCLKEN_MASK)|                        \
/* .. */ CLR(MCG_C1_IREFSTEN_MASK),                                             \
/* C2 */ SET(MCG_C2_LOCRE0_MASK)|SET(MCG_C2_RANGE0(0x00))|CLR(MCG_C2_HGO0_MASK)|\
/* .. */ CLR(MCG_C2_EREFS0_MASK)|CLR(MCG_C2_LP_MASK)|CLR(MCG_C2_IRCS_MASK),     \
/* C4 */ CLR(MCG_C4_DMX32_MASK)|SET(MCG_C4_DRST_DRS(0x00)),                     \
/* C6 */ CLR(MCG_C6_LOLIE0_MASK)|CLR(MCG_C6_PLLS_MASK)|CLR(MCG_C6_CME0_MASK)|  \
/* .. */ SET(MCG_C6_CHGPMP_BIAS(0x08)),                                         \
/* SC */ CLR(MCG_SC_ATME_MASK)|CLR(MCG_SC_ATMS_MASK)|                           \
/* .. */ CLR(MCG_SC_FLTPRSRV_MASK)|SET(MCG_SC_FCRDIV(0x01)),                    \
/* C7 */ SET(MCG_C7_PLL32KREFSEL(0))|CLR(MCG_C7_OSCSEL_MASK),                   \
/* C8 */ SET(MCG_C8_LOCRE1_MASK)|CLR(MCG_C8_LOLRE_MASK)|CLR(MCG_C8_CME1_MASK)|\
/* .. */ CLR(MCG_C8_COARSE_LOLIE_MASK)                                          \
}

static int seconds_wr, seconds_rd;

static void irtc_callback (IRTC_CALLBACK_TYPE type, void *data)
{
  if(type == IRTC_1HZ_CALLBACK)
  {
    seconds_wr++;
    IRTC_WrRam (&seconds_wr, sizeof(seconds_wr));
  }
}

void main (void)
{
  /* clock mode 2:1:1 (core:bus:flash)                                          */
  SIM_Init (SIM_MODULE_IRTC_RTCCLKSEL_ON_CONFIG);

  /* FLL settings, 32kHz IRC used                                               */
  FLL_Init (FLL_MODULE_FEI_20_25MHZ_IRCLKEN_ON_CONFIG);

  /* enable IRTC clocked by internal IRC & insteall callback function           */
  /* called every second                                                        */
  IRTC_Init (IRTC_MODULE_COMP_OFF_CONFIG,
             IRTC_TAMPER_PIN_DI_CONFIG,
             IRTC_TAMPER_PIN_DI_CONFIG,
             IRTC_TAMPER_PIN_DI_CONFIG,
             IRTC_1HZ_MASK);
  IRTC_InstallCallback (PRI_LVL3,irtc_callback);

  /* enable interrupts on global level                                          */
  EnableInterrupts();

  while(1){
    IRTC_RdRam (&seconds_rd, sizeof(seconds_rd));
    arch_delay(1000000);
  }
}
```