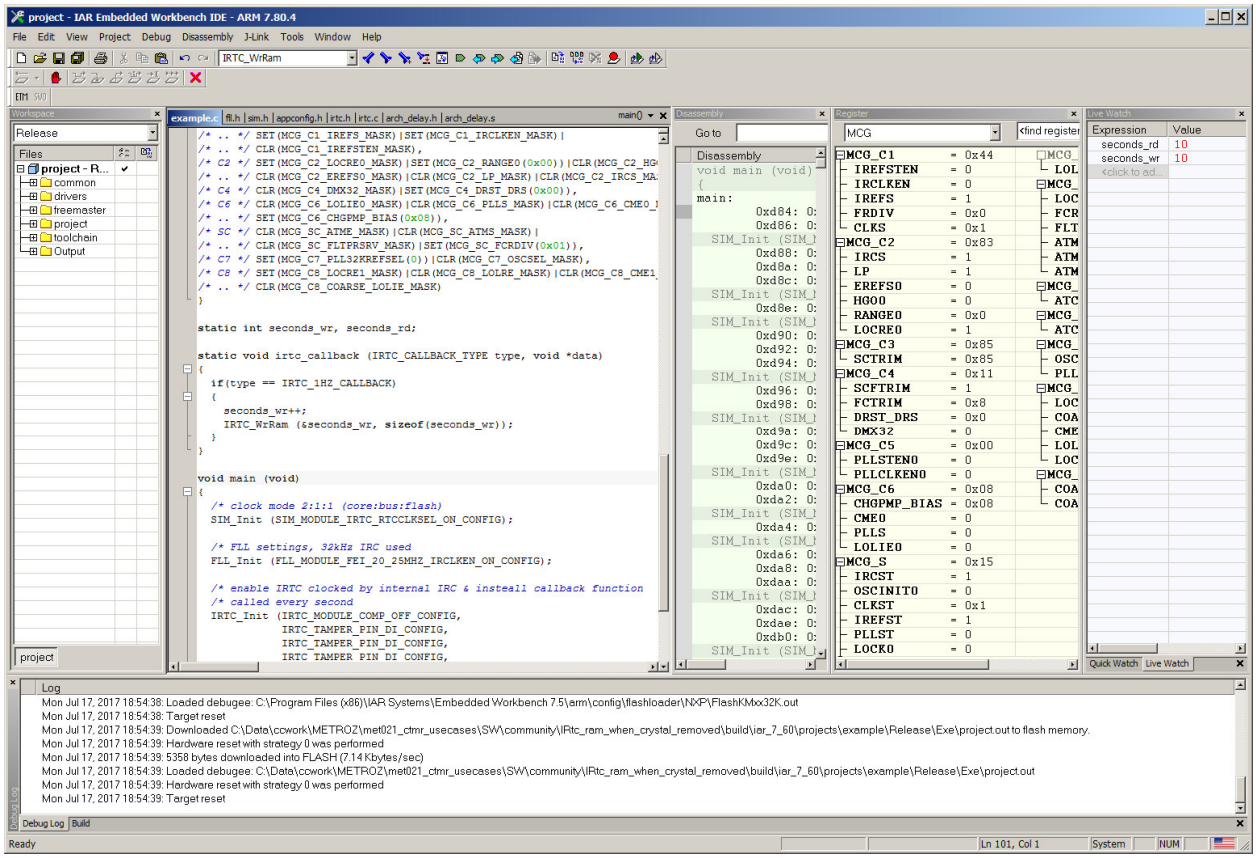
project - IAR Embedded Workbench IDE - ARM 7.80.4
File Edit View Project Debug Disassembly J-Link Tools Window Help
IRTC_WrRam
Workspace
Release
Files
project - R...
common
drivers
freemaster
project
toolchain
Output
project
example.c
fli.h | sim.h | appconfig.h | irtc.h | irtc.c | arch_delay.h | arch_delay.s
main()
/* .. */ SET(MCG_C1_IREFS_MASK)|SET(MCG_C1_IRCLKEN_MASK)|
/* .. */ CLR(MCG_C1_IREFSTEN_MASK),
/* C2 */ SET(MCG_C2_LOCRE0_MASK)|SET(MCG_C2_RANGE0(0x00))|CLR(MCG_C2_HG
/* .. */ CLR(MCG_C2_EREFS0_MASK)|CLR(MCG_C2_LP_MASK)|CLR(MCG_C2_IRCS_MA
/* C4 */ CLR(MCG_C4_DMX32_MASK)|SET(MCG_C4_DRST_DRS(0x00)),
/* C6 */ CLR(MCG_C6_LOLIE0_MASK)|CLR(MCG_C6_PLLS_MASK)|CLR(MCG_C6_CME0_
/* .. */ SET(MCG_C6_CHGPMP_BIAS(0x08)),
/* SC */ CLR(MCG_SC_ATME_MASK)|CLR(MCG_SC_ATMS_MASK)|
/* .. */ CLR(MCG_SC_FLTPRSRV_MASK)|SET(MCG_SC_FCRDIV(0x01)),
/* C7 */ SET(MCG_C7_PLL32KREFSEL(0))|CLR(MCG_C7_OSCSEL_MASK),
/* C8 */ SET(MCG_C8_LOCRE1_MASK)|CLR(MCG_C8_LOLRE_MASK)|CLR(MCG_C8_CME1_
/* .. */ CLR(MCG_C8_COARSE_LOLIE_MASK)
}
static int seconds_wr, seconds_rd;
static void irtc_callback (IRTC_CALLBACK_TYPE type, void *data)
{
if(type == IRTC_1HZ_CALLBACK)
{
seconds_wr++;
IRTC_WrRam (&seconds_wr, sizeof(seconds_wr));
}
}
void main (void)
{
/* clock mode 2:1:1 (core:bus:flash)
SIM_Init (SIM_MODULE_IRTC_RTCCLKSEL_ON_CONFIG);
/* FLL settings, 32kHz IRC used
FLL_Init (FLL_MODULE_FEI_20_25MHZ_IRCLKEN_ON_CONFIG);
/* enable IRTC clocked by internal IRC & insteall callback function
/* called every second
IRTC_Init (IRTC_MODULE_COMP_OFF_CONFIG,
IRTC_TAMPER_PIN_DI_CONFIG,
IRTC_TAMPER_PIN_DI_CONFIG,
IRTC TAMPER PIN DI CONFIG,
Disassembly
Go to
Disassembly
void main (void)
{
main:
0xd84: 0:
0xd86: 0:
SIM_Init (SIM_
0xd88: 0:
0xd8a: 0:
0xd8c: 0:
SIM_Init (SIM_
0xd8e: 0:
SIM_Init (SIM_
0xd90: 0:
0xd92: 0:
0xd94: 0:
SIM_Init (SIM_
0xd96: 0:
0xd98: 0:
SIM_Init (SIM_
0xd9a: 0:
0xd9c: 0:
0xd9e: 0:
SIM_Init (SIM_
0xda0: 0:
0xda2: 0:
SIM_Init (SIM_
0xda4: 0:
SIM_Init (SIM_
0xda6: 0:
0xda8: 0:
0xdaa: 0:
SIM_Init (SIM_
0xdac: 0:
0xdae: 0:
0xdb0: 0:
SIM_Init (SIM_
Register
MCG
<find register
MCG_C1 = 0x44
IREFSTEN = 0
IRCLKEN = 0
IREFS = 1
FRDIV = 0x0
CLKS = 0x1
MCG_C2 = 0x83
IRCS = 1
LP = 1
EREFS0 = 0
HGO0 = 0
RANGE0 = 0x0
LOCRE0 = 1
MCG_C3 = 0x85
SCTRIM = 0x85
MCG_C4 = 0x11
SCFTRIM = 1
FCTRIM = 0x8
DRST_DRS = 0x0
DMX32 = 0
MCG_C5 = 0x00
PLLSTEN0 = 0
PLLCLKEN0 = 0
MCG_C6 = 0x08
CHGPMP_BIAS = 0x08
CME0 = 0
PLLS = 0
LOLIE0 = 0
MCG_S = 0x15
IRCST = 1
OSCINIT0 = 0
CLKST = 0x1
IREFST = 1
PLLST = 0
LOCK0 = 0
MCG_
LOL
MCG_
LOC
FCR
FLT
ATM
ATM
ATM
MCG_
ATC
MCG_
ATC
MCG_
OSC
PLL
MCG_
LOC
COA
CME
LOL
LOC
MCG_
COA
COA
Live Watch
Expression
Value
seconds_rd
10
seconds_wr
10
<click to ad...
Quick Watch
Live Watch
Log
Mon Jul 17, 2017 18:54:38: Loaded debugee: C:\Program Files (x86)\IAR Systems\Embedded Workbench 7.5\arm\config\flashloader\NXP\FlashKMxx32K.out
Mon Jul 17, 2017 18:54:38: Target reset
Mon Jul 17, 2017 18:54:39: Downloaded C:\Data\ccwork\METROZ\met021_ctmr_usecases\SW\community\IRtc_ram_when_crystal_removed\build\iar_7_60\projects\example\Release\Exe\project.out to flash memory.
Mon Jul 17, 2017 18:54:39: Hardware reset with strategy 0 was performed
Mon Jul 17, 2017 18:54:39: 5358 bytes downloaded into FLASH (7.14 Kbytes/sec)
Mon Jul 17, 2017 18:54:39: Loaded debugee: C:\Data\ccwork\METROZ\met021_ctmr_usecases\SW\community\IRtc_ram_when_crystal_removed\build\iar_7_60\projects\example\Release\Exe\project.out
Mon Jul 17, 2017 18:54:39: Hardware reset with strategy 0 was performed
Mon Jul 17, 2017 18:54:39: Target reset
Debug Log
Build
Ready
Ln 101, Col 1
System
NUM