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OF120M MCU	
OSB, OSBDM/V-TRAN/PWR	
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Revisions			
Rev	Description	Date	Approved
X1	Initial Release	02 Aug 11	M.H
X2	1. L9 replaced with DNF 0 ohm resistor. 2.Note updated for R172 & R173 Placement 3.C77, C78, R91, R92 & R93 removed 4.Jumper added on Y1 power 5.PTB4 to PTB7 used for Analog inputs on Primary elevator 6.IRQ signals removed from Secondary Elevator	03 Aug 11	M.H
X3	1. Jumper added between potentiometer and ADC1_DM1 2. I2S signals added on the elevator connector (A58-A61) 3.accelerometer part chnaged to MMA8451QT 4.0 ohms added to PTC16 to isolate Nand Flash & R118 5.UART connections swapped on Elevator	08 Aug 11	M.H
X4	Net names changed for PTDD & PTD1 on OSBDM circuit	16 Aug 11	M.H
A	Proto Release	22 Aug 11	M.H
A1	Re-run ECO for A085 to correct BOM import.	16 Sept 11	E.T
AX1	1. PTE8 , PTE9 used instead of PTC16 & PTC17 on Primary elevator UART connections 2. Similarly RTS & CTS connections changed to PTE10 & PTE11 3. I2S signals extracted from PTA series through Jumpers 4. Board ID pull down resistor changed to 1.3K	14 Nov 11	M.H
AX2	1. I2S0 Header connections sourced from either PTC or PTA through Jumper 2. 0 ohm resistor added for Trace clock out(PTA6) 3. 0 ohm resistor added between elevator and MCU for Ethernet signals on PTA pins 4. IRQ signals added to secondary elevator 5. 0 ohms resistor added between Nand Flash and MCU on PTC signals which is shared with I2S0	15 Nov 11	M.H
B	Prototype Release	17 Nov 11	M.H
BX1	CLK OSC Circuitry for FCC: Removed J18 3 Pin Jumper Added 2 Pin Jumper to ON / OFF OSC	10 Feb 12	Peter, Kevin
C	Production Release	14 Feb 12	Peter, Kevin

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ICAP Classification:		FCP:	FIUC: X PUBI:
Designer: io:DSN	Drawing Title: TWR-K60F120M		
Drawn by: io:DSN	Page Title: Table of Contents/Revisions		
Approved: Melissa Hunter	Size C	Document Number SCH-27167 PDF: SPF-27167	Rev C
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otherwise Specified:

Resistors are in ohms
Capacitors are in uF

Power supplies are DC

All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:

—B Denotes - Active-Low Signal

<> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Power & Ground Nets

NET	VOLTAGE	DESCRIPTION
P5V_USB	5V	Primary input power. Filtered from USB connector. Input to USB power switch.
P5V_SW	5V	Output of USB power switch controlled by the 5V_EN signal from the JM60 MCU. Used by OSBDM voltage translation circuits.
P5V_TRG_USB	5V	Output of USB power switch controlled by the VTRG_EN signal from the JM60 MCU. Provides input to regulator.
P3V3	3.3V	Output of regulator using USB power input (P5V_TRG_USB).
P3V3_MCU	3.3V	MCU digital power. Filtered from P3V3.
VDDA	3.3V	VDDA power for MCU and analog circuits. Filtered from P3V3_MCU.
VREFH	3.3V	Upper reference voltage for ADC on the MCU. Filtered from VDDA.
VREFL	0V	Lower reference voltage for ADC on the MCU. Filtered from VSSA.
VSSA	0V	VSSA power for MCU and analog circuits. Filtered from GND.
GND	0V	Digital Ground.

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ELEVATOR CONNECTORS

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Sheet 5

OSJTAG/USB Bridge Circuit
 USB Mini B Connector
 MC9S08JM60
 Voltage Translation
 OSJTAG/JTAG Header
 SCI Source Selectors
 Power Supply Circuits

Sheet 4

K60NF1M MCU
 50 MHz XTAL
 12 MHz XTAL
 32.768 KHz XTAL
 VSSA/VDDA filter
 VREFH/VREFL filter
 VREF_OUT
 VREGIN, VOUT33
 VBAT

Sheet 6

INFRARED PORT

Sheet 6

PUSH BUTTONS

Sheet 6

SD CARD SOCKET

Sheet 7

ANALOG INPUTS
 MMA7660 ACCELEROMETER
 POTENTIOMETER

Sheet 8

NAND Flash

Sheet 7

TOWER PLUG-IN (TWRPI)
 SENSOR HEADERS

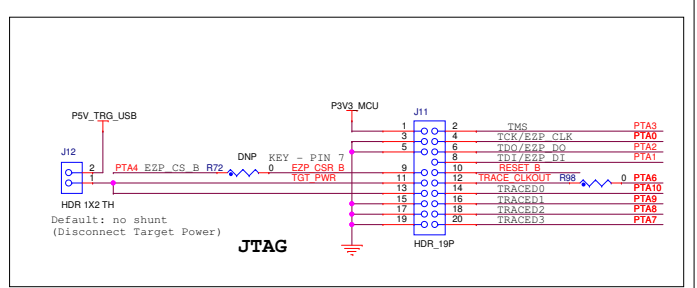
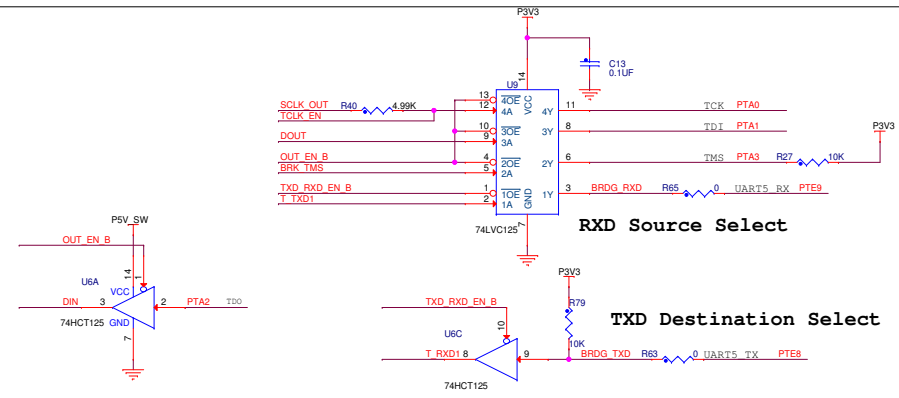
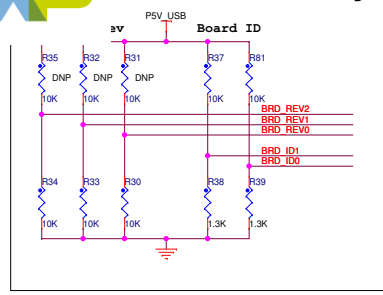
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TOWER PLUG-IN (TWRPI)
 TOUCH HEADER

ICAP Classification: FCP: _____ FIUC: X PUBL: _____			
Drawing Title: TWR-K60F120M			
Page Title: Block Diagram			
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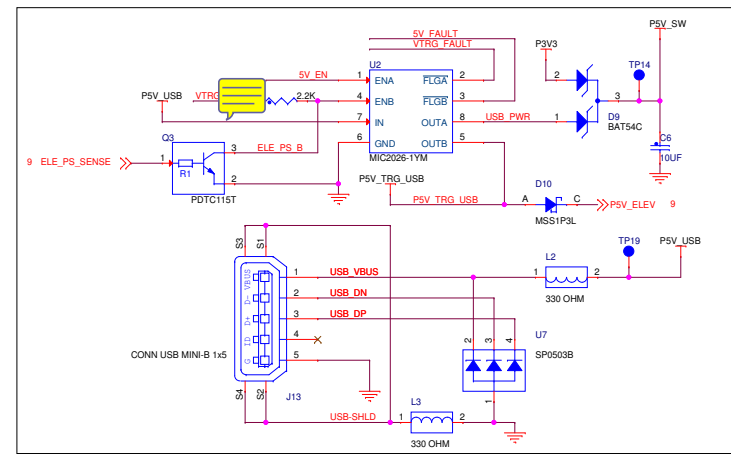
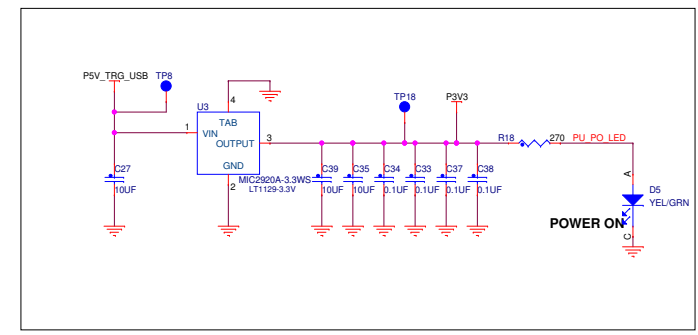
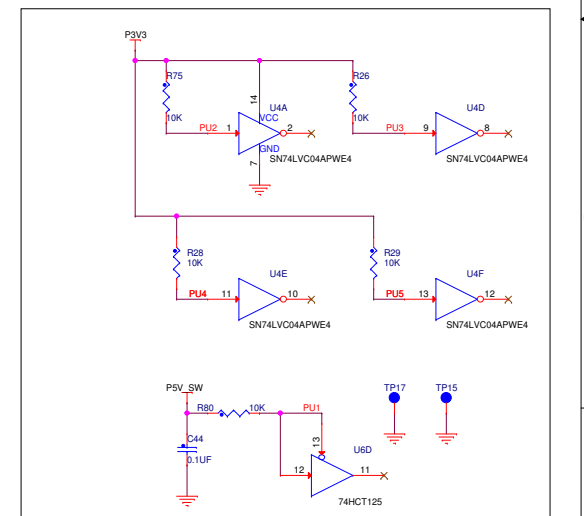
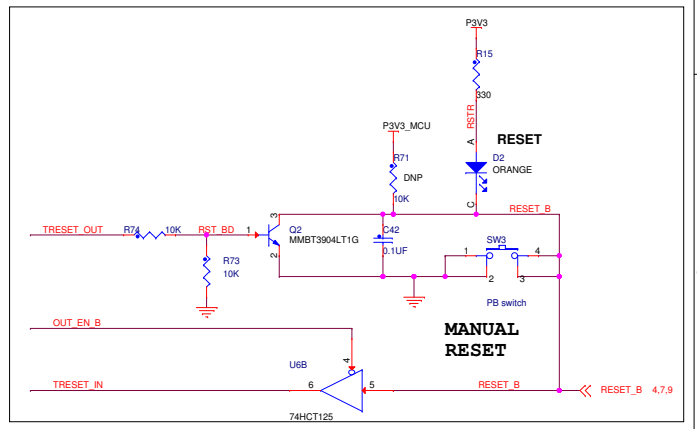
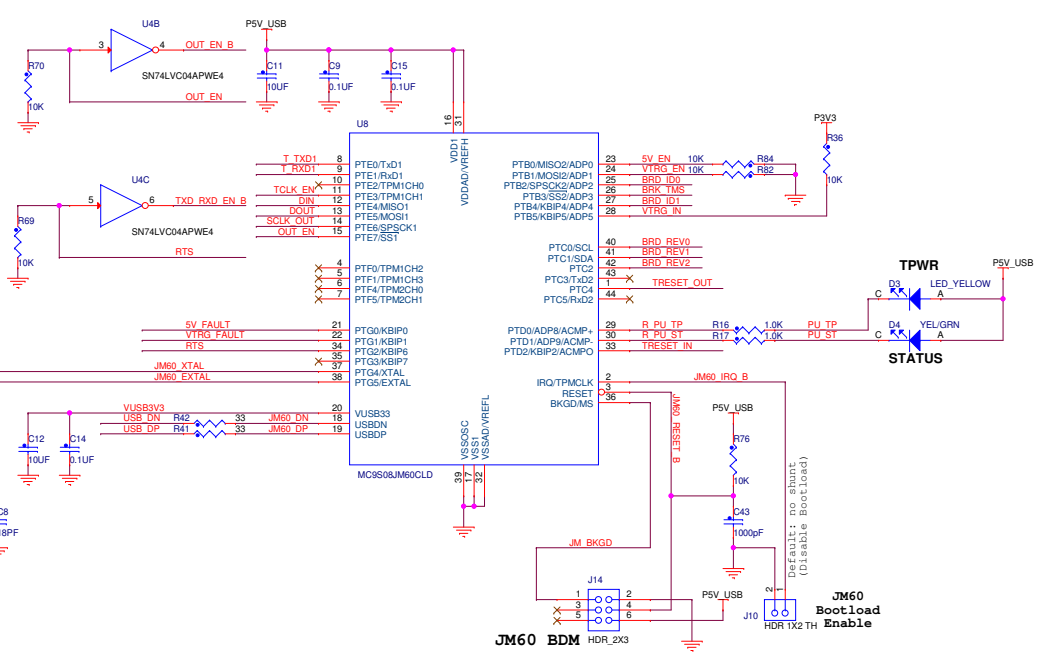


PTA0	TCK	50	PTA0/TS10_CH1/UART0_CTS/UART0_C0D/FTM0_CH5/JTAG_TCLK/SWD_CLK/EZP_CLK
PTA1	TDI/FTM0_CH6/UART0_RX	51	PTA1/TS10_CH2/UART0_RX/FTM0_CH4/JTAG_TDI/EZP_DI
PTA2	TDO/FTM0_CH7/UART0_TX	52	PTA2/TS10_CH3/UART0_TX/FTM0_CH7/JTAG_TDO/TRACE_SWO/EZP_DO
PTA3	TRST	53	PTA3/TS10_CH4/UART0_TRST/FTM0_CH6/JTAG_TRST/SWD_SWO/EZP_D0
PTA4	EZP_CS_N/TS10_CH5	54	PTA4/TS10_CH5/FTM0_CH1/MI0/EZP_CS
PTA5	IRF2/IRF10_RXER/M10_RXER	55	PTA5/USB_CLKIN/FTM0_CH2/RM10_RXER/MI0_RXER/JTAG_TRST/CMP2_OUT/IS20_TX_BCLK
PTA6	UPL1_CLK/TRACE_D3/FTM0_CH3	56	PTA6/ADC3_SE4A/ULP1_CLK/FTM0_CH2/IS11_RXD0/TRACE_CLKOUT
PTA7	UPL1_DIR/TRACE_D3/FTM0_CH4	58	PTA7/ADC0_SE15/ULP1_CLK/FTM0_CH4/IS11_RX_BCLK/TRACE_D3
PTA8	UPL1_NXT/TRACE_D2/FTM0_CH0	59	PTA8/ADC0_SE15/ULP1_NXT/FTM0_CH0/IS11_RX_FS/FTM0_OD_PHA/TRACE_D0
PTA9	UPL1_SIP/FTM0_CH1/TRACE_D1	61	PTA9/ADC3_SE4A/ULP1_STP/FTM0_CH1/MI0_RX/FTM0_OD_PHA/TRACE_D0
PTA10	UPL1_DATA0	62	PTA10/ADC3_SE4A/ULP1_DATA0/FTM2_CH0/MI0_RXD2/FTM2_OD_PHA/TRACE_D0
PTA11	UPL1_DATA1	63	PTA11/ADC3_SE4A/ULP1_DATA1/FTM2_CH1/MI0_RXCLK/FTM2_OD_PHB
PTA12	RM10_RXD1/MI10_RXD1/CAN_TX0	64	PTA12/CAN0_TX/FTM1_CH0/RM10_RXD1/RXD1/FTM0_OD_PHA/CMP2_IN0/IS20_TXD0
PTA13	RM10_RXD0/MI10_RXD0/CAN_RX0	65	PTA13/CAN0_RX/FTM1_CH1/RM10_RXD0/RXD0/FTM0_OD_PHB/CMP2_IN1/IS20_TXF5
PTA14	RM10_TXEN/MI10_TXEN	66	PTA14/CMP3_IN0/SPI0_PCS0/UART0_TX/RM10_CRS_DV/MI0_RXD0/IS20_RX_BCLK/IS20_TXD1
PTA15	RM10_TXD0/MI10_TXD0	67	PTA15/CMP3_IN1/SPI0_SCK/UART0_RX/RM10_TXEN/MI0_TXEN/IS20_RXD0
PTA16	RM10_TXD1/MI10_TXD1	68	PTA16/CMP3_IN2/SPI0_SOUT/UART0_CTS/UART0_C0L/RM10_TXD0/MI0_TXD1/IS20_MCLK
PTA17	EXTAL	72	PTA17/ADC1_SE17/SPI0_SIN/UART0_RTS/RM10_TXD1/MI0_TXD1/IS20_MCLK
PTA18	TRWP1_GP103/pushbutton1	73	PTA18/EXTAL_FTM0_FLT2/FTM0_CLKIN0
PTA19	TRWP1_GP103/pushbutton1	73	PTA19/XTAL_FTM1_FLT0/FTM0_CLKIN1/LTPMR0_ALT1
PTA24	UPL1_DATA2	75	PTA24/CMP3_IN4/ULP1_DATA2/MI0_TXD2/FB_A29
PTA25	UPL1_DATA3	76	PTA25/CMP3_IN5/ULP1_DATA3/MI0_TXCLK/FB_A28
PTA26	UPL1_DATA4	77	PTA26/ADC2_SE15/ULP1_DATA4/MI0_TXD3/FB_A27
PTA27	UPL1_DATA5	78	PTA27/ADC2_SE14/ULP1_DATA5/MI0_CRS/FB_A26
PTA28	UPL1_DATA6	80	PTA28/ADC2_SE13/ULP1_DATA6/MI0_TXER/FB_A25
PTA29	UPL1_DATA7	80	PTA29/ADC2_SE12/ULP1_DATA7/MI0_C0L/FB_A24
PTB0	RM10_MDIO/MI10_MDIO/TS10_CH0	81	PTB0/ADC0_SE14/TS10_SEB/TS10_WU/IS20_SCL/FTM1_CH0/RM10_MDIO/MI0_MDIO/FTM1_OD_PHA
PTB1	RM10_MDC/MI10_MDC/TS10_CH6	82	PTB1/ADC0_SE14/TS10_SEB/TS10_WU/IS20_SCL/FTM1_CH0/RM10_MDIO/MI0_MDIO/FTM1_OD_PHA
PTB2	TS_TCH_I2C_SCL/TS10_CH7	83	PTB2/ADC0_SE14/TS10_SEB/TS10_WU/IS20_SCL/FTM1_CH0/RM10_MDIO/MI0_MDIO/FTM1_OD_PHA
PTB3	TS_TCH_I2C_SDA/TS10_CH8	84	PTB3/ADC0_SE14/TS10_SEB/TS10_WU/IS20_SCL/FTM1_CH0/RM10_MDIO/MI0_MDIO/FTM1_OD_PHA
PTB4	IR0E/IR0F/ADC1_SE11	86	PTB4/ADC0_SE14/TS10_SEB/TS10_WU/IS20_SCL/FTM1_CH0/RM10_MDIO/MI0_MDIO/FTM1_OD_PHA
PTB5	IR0E/IR0F/ADC1_SE11	86	PTB5/ADC1_SE11/ENET0_1588_TMR3/FTM2_FLT0
PTB6	AD22/IR0A/IR0B/ADC1_SE12	87	PTB6/ADC1_SE12/FB_A23
PTB7	AD22/IR0A/IR0B/ADC1_SE12	87	PTB7/ADC1_SE12/FB_A22
PTB8	AD27/TRWP1_GP101	89	PTB8/UART3_RTS/FB_A21
PTB9	FB_A20/TRWP1_GP102	91	PTB9/SPI_PCS1/UART3_CTS/FB_A20
PTB10	FB_A19	91	PTB10/ADC1_SE14/SPI1_RX/IS21_TX_BCLK/FB_A19/FTM0_FLT1
PTB11	FB_A18	92	PTB11/ADC1_SE15/SCK/UART3_TX/IS21_TX_FS/FB_A18/FTM0_FLT2
PTB12	FB_A17/DSP1_D0U7/TS1_CH9	95	PTB12/SPI0_CS/SPI1_SOUT/UART0_RX/IS21_TXD0/FB_A17/EWM_IN
PTB13	FB_A16/DSP1_D1N/TS10_CH10	96	PTB13/TS10_CH9/SPI1_SIN/UART0_TX/IS21_TXD0/FB_A16/EWM_OUT
PTB14	FB_A15/TS10_CH11	97	PTB14/TS10_CH11/CAN0_TX/FTM2_CH0/FB_A15/FTM2_OD_PHA/IS20_TX_BCLK
PTB15	FB_A14/TS10_CH12	98	PTB15/TS10_CH12/CAN0_RX/FTM2_CH1/FB_OE/FTM2_OD_PHB/IS20_TX_FS
PTB16	FB_A13-NF_I014/SP12_PCS0	99	PTB16/ADC2_SE4A/SP2_C0S/FB_A13/NFC_DATA3/FTM2_OD_PHB/IS20_TX_FS
PTB17	FB_A13-NF_I014/SP12_SCK	100	PTB17/ADC2_SE4A/SP2_SCK/FB_A13/NFC_DATA1/4CMP1_OUT
PTB18	FB_A13-NF_I014/SP12_SOUT	101	PTB18/ADC2_SE4A/SP2_SOUT/FB_A13/NFC_DATA3/4CMP2_OUT
PTB19	FB_A13-NF_I014/SP12_SIN	102	PTB19/ADC2_SE4A/SP2_SIN/SP2_C0S/FB_A13/NFC_DATA1/4CMP3_OUT
PTC0	FB_A14-NF_I011/TS10_CH13	103	PTC0/ADC0_SE14/TS10_CH13/SPI0_PCS4/PD03_EXT/IRF2_FB_A14/NFC_DATA1/1/IS20_TXD1
PTC1	FB_A13-NF_I011/TS10_CH14/FTM0_CH0	104	PTC1/ADC0_SE14/TS10_CH13/SPI0_PCS4/UART1_RTS/FTM0_CH0/FB_A13/NFC_DATA1/0/IS20_TXD0
PTC2	FB_A12-NF_I09/FTM0_CH1/TS10_CH15	105	PTC2/ADC0_SE4B/TS10_CH15/SPI0_PCS2/UART1_CTS/FTM0_CH1/FB_A12/NFC_DATA1/IS20_TX_FS/CMP1_IN0
PTC3	FB_A11-NF_I08/DSP1_CS_N	106	PTC3/SPI0_PCS1/UART1_RX/FTM0_CH2/FB_A11/NFC_DATA1/0/IS20_TX_BCLK/CMP1_IN1
PTC4	FB_A11-NF_I08/DSP1_CS_N	109	PTC4/SPI0_PCS1/UART1_TX/FTM0_CH2/FB_A11/NFC_DATA1/IS21_TX_BCLK/CMP1_OUT
PTC5	FB_A10-NF_I07/DSP1_CS_N	110	PTC5/SPI0_SCK/LTPMR0_ALT2/FB_A10/NFC_DATA7/CMP1_OUT/IS21_TX_FS/IS20_RXD0
PTC6	FB_A10-NF_I06/USB_AB_FD	111	PTC6/CMP0_IN0/SPI0_SOUT/IRF0A/FB_A10/NFC_DATA7/IS20_MCLK/IS20_RX_BCLK
PTC7	FB_A10-NF_I06/USB_AB_FD	112	PTC7/CMP0_IN1/SPI0_SIN/USB_SOF_OUT/FB_A10/NFC_DATA7/IS20_RX_BCLK
PTC8	FB_A10-NF_I06/USB_AB_FD	113	PTC8/ADC1_SE4B/CMP0_IN2/FTM3_CH4/FB_A10/NFC_DATA1/IS20_MCLK
PTC9	FB_A10-NF_I06/USB_AB_FD	114	PTC9/ADC1_SE4B/CMP0_IN3/FTM3_CH5/FB_A10/NFC_DATA3/FTM2_FLT0/IS20_RX_BCLK
PTC10	FB_A10-NF_I06/USB_AB_FD	115	PTC10/ADC1_SE4B/CMP0_IN4/FTM3_CH6/FB_A10/NFC_DATA2/IS11_MCLK/IS20_RX_FS
PTC11	FB_A10-NF_I06/USB_AB_FD	116	PTC11/ADC1_SE7B/C01_S0A/FTM3_CH7/FB_A10/NFC_DATA1/IS20_RXD1
PTC12	FB_A10-NF_I06/USB_AB_FD	117	PTC12/UART3_RTS/FB_A10/FTM3_FLT0
PTC13	FB_A10-NF_I06/USB_AB_FD	118	PTC13/UART4_CTS/FB_A25
PTC14	FB_A10-NF_I06/USB_AB_FD	119	PTC14/UART4_RX/FB_A25
PTC15	FB_A10-NF_I06/USB_AB_FD	120	PTC15/UART4_TX/FB_A24
PTC16	CAN_RX1_NFC_RnB/UART3_RXD	123	PTC16/CAN1_RX/UART3_RX/ENET0_1588_TMR0/FB_C55/FB_TSI21/FB_BE23_16_BLS15_NFC_FB
PTC17	CAN_TX1_NFC_Cp_R/UART3_TXD	124	PTC17/CAN1_TX/UART3_TX/ENET0_1588_TMR0/FB_C54/FB_TSI20/FB_BE31_24_BLS7_NFC_CEO
PTD0	FB_CS1_B/USB_AB_VBUS_EN	127	PTD0/SPI0_PCS0/UART2_RTS/FTM3_CH0/FB_ALE/FB_CS1/FB_TSI61/RXD1
PTD1	FB_CS0	128	PTD1/ADC0_SE5B/SPI0_SCK/UART2_CTS/FTM3_CH1/FB_C58/IS21_RXD0
PTD2	FB_A14/UART2_RX	129	PTD2/SPI0_SOUT/UART2_RX/FTM3_CH2/FB_A14/IS21_RX_FS
PTD3	FB_A13/IRDA_TXD	130	PTD3/SPI0_SIN/UART2_TX/FTM3_CH3/FB_A13/NFC_DATA1/IS21_TX_BCLK
PTD4	FB_A12-NF_I01	131	PTD4/SPI0_PCS1/UART0_RTS/FTM0_CH4/FB_A12/NFC_DATA1/EWM_IN
PTD5	FB_A11-NF_I00/FTM0_CH5	132	PTD5/ADC0_SE5B/SPI0_PCS2/UART0_CTS/UART0_C0D/FTM0_CH5/FB_A11/NFC_DATA0/EWM_OUT
PTD6	FB_A10/TRACE/UART0_RX	133	PTD6/ADC0_SE7B/SPI0_PCS3/UART0_TX/FTM0_CH6/FB_A10/FTM0_FLT0
PTD7	CMT_IRO/UART0_TX	136	PTD7/CMT_IRO/UART0_TX/FTM0_CH7/FTM0_FLT1
PTD8	NEC_ALE/I2C0_SCL	137	PTD8/I2C0_SCL/UART3_RX/FB_A16/NFC_RE
PTD9	NEC_ALE/I2C0_SDA	138	PTD9/I2C0_SDA/UART3_TX/FB_A17/NFC_ALE
PTD10	SP12_S0	139	PTD10/UART3_RTS/FB_A18/NFC_RE
PTD11	SP12_S0	140	PTD11/SPI2_PCS0/UART5_CTS/SDH00_CLKIN/FB_A19
PTD12	SP12_S0	141	PTD12/SPI2_SCK/FTM3_FLT0/SDH00_D0/FB_A20
PTD13	SP12_S0	142	PTD13/SPI2_SOUT/SDH00_D5/FB_A21
PTD14	SP12_S0	143	PTD14/SPI2_SIN/SDH00_D6/FB_A22
PTD15	SP12_S1	144	PTD15/SPI2_PCS1/SDH00_D7/FB_A23
PTE0	SDH00_D1	1	PTE0/ADC1_SE4A/SPI1_PCS1/UART1_TX/SDH00_D1/IC1_S0A/RTC_CLKOUT
PTE1	SDH00_D0/SP11_SIN	2	PTE1/ADC1_SE4A/SPI1_SCK/UART1_RX/SDH00_D0/IC2_S0A/RTC_CLKOUT
PTE2	SDH00_D0/SP11_SOUT	3	PTE2/ADC1_SE4A/SPI1_SCK/UART1_CTS/SDH00_D0/CLK
PTE3	SDH00_CMD/SP11_SOUT	4	PTE3/ADC1_SE4A/SPI1_SIN/UART1_RTS/SDH00_CMD/SPI1_SOUT
PTE4	SDH00_D3/SP11_EC50	7	PTE4/SPI1_PCS0/UART3_TX/SDH00_D3
PTE5	SDH00_D2/GPIO_B	8	PTE5/SPI1_PCS0/UART3_TX/SDH00_D3
PTE6	GPIO_B6/I2S0_MCLK	9	PTE6/SPI1_PCS0/UART3_TX/SDH00_D2/FTM3_CH0
PTE7	AUD_SDA1X/GPIO_B7	10	PTE7/SPI1_PCS0/UART3_TX/SDH00_D2/FTM3_CH0
PTE8	I2S0_RX_FS/UART5_TXD	11	PTE8/SPI1_PCS0/UART3_TX/SDH00_D1/IS20_RX_BCLK
PTE9	I2S0_RX_BCLK/UART5_RXD	12	PTE9/UART3_CTS/FTM3_CH2/IS20_RXD0
PTE10	AUD_SDA0A/UART5_CTS_B	13	PTE10/ADC2_SE16/UART5_TX/FTM3_CH3/IS20_RXD1/IS20_RX_FS
PTE11	I2S0_RX_FS/UART5_RTS_B	14	PTE11/ADC2_SE16/UART5_TX/FTM3_CH4/IS20_TXD1/IS20_RX_BCLK
PTE12	I2S0_TX_BCLK/GPIO_B12	15	PTE12/UART5_CTS/FTM3_CH5/IS20_TXD0
PTE13	I2S0_TX_BCLK/GPIO_B12	15	PTE13/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
PTE14	I2S0_TX_BCLK/GPIO_B12	15	PTE14/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
PTE15	I2S0_TX_BCLK/GPIO_B12	15	PTE15/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
PTE16	I2S0_TX_BCLK/GPIO_B12	15	PTE16/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
PTE17	I2S0_TX_BCLK/GPIO_B12	15	PTE17/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
PTE18	I2S0_TX_BCLK/GPIO_B12	15	PTE18/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
PTE19	I2S0_TX_BCLK/GPIO_B12	15	PTE19/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
PTE20	I2S0_TX_BCLK/GPIO_B12	15	PTE20/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
PTE21	I2S0_TX_BCLK/GPIO_B12	15	PTE21/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
PTE22	I2S0_TX_BCLK/GPIO_B12	15	PTE22/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
PTE23	I2S0_TX_BCLK/GPIO_B12	15	PTE23/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
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PTE26	I2S0_TX_BCLK/GPIO_B12	15	PTE26/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
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PTE96	I2S0_TX_BCLK/GPIO_B12	15	PTE96/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
PTE97	I2S0_TX_BCLK/GPIO_B12	15	PTE97/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
PTE98	I2S0_TX_BCLK/GPIO_B12	15	PTE98/ADC3_SE17/FTM3_CH7/IS20_TX_BCLK
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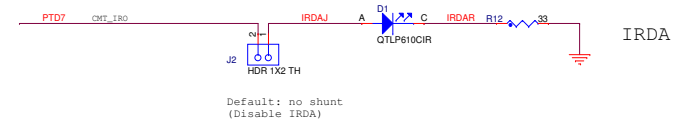
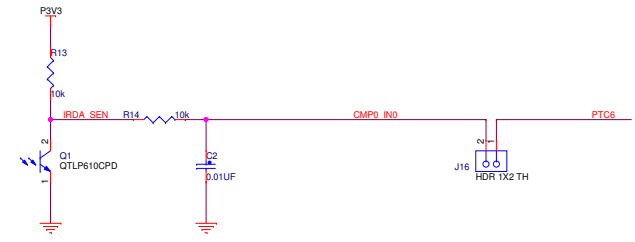
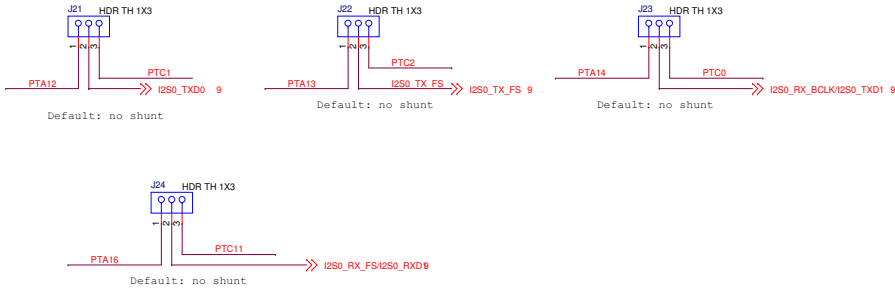
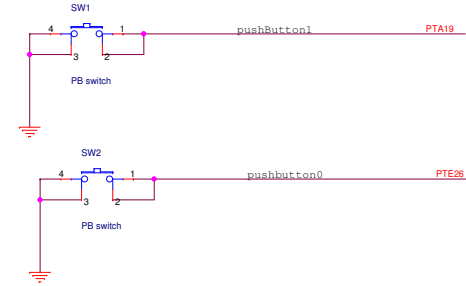
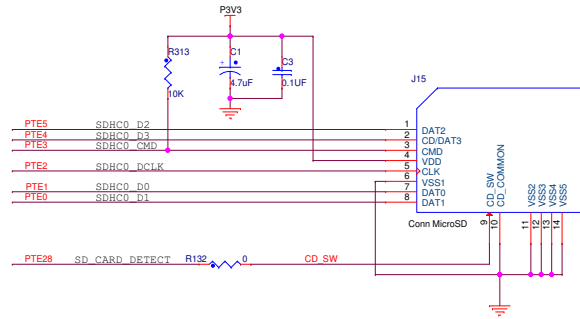


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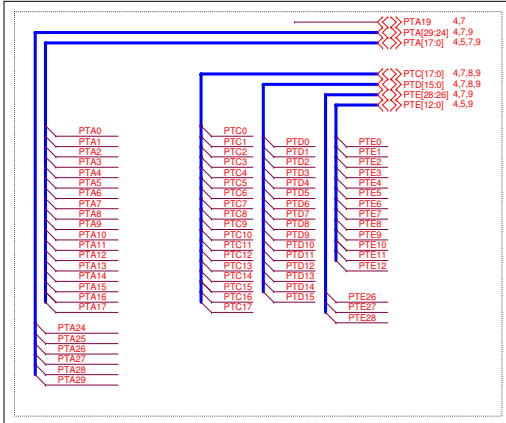
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MICRO SD INTERFACE



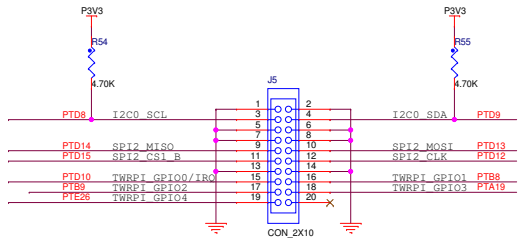
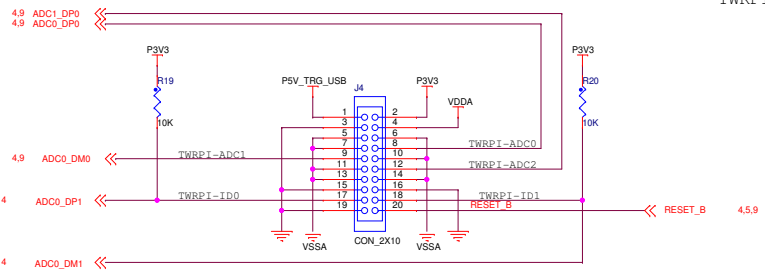
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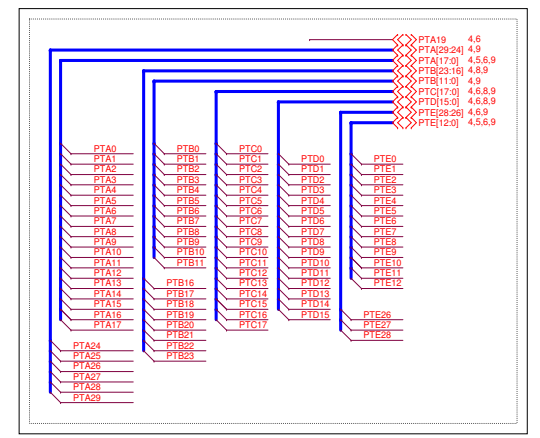
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Date: Tuesday, February 14, 2012	Sheet 6 of 9



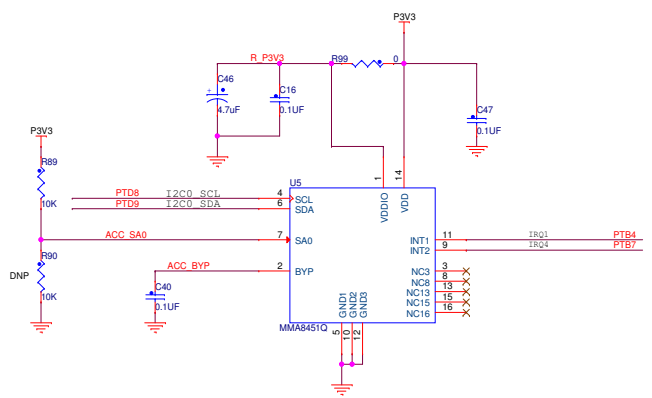
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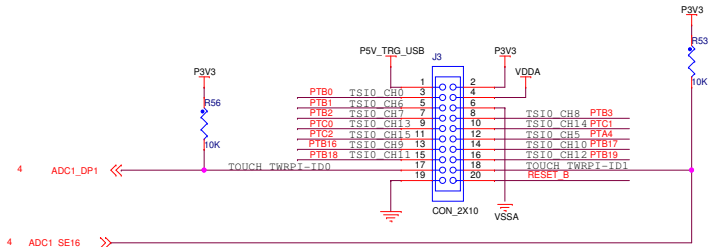
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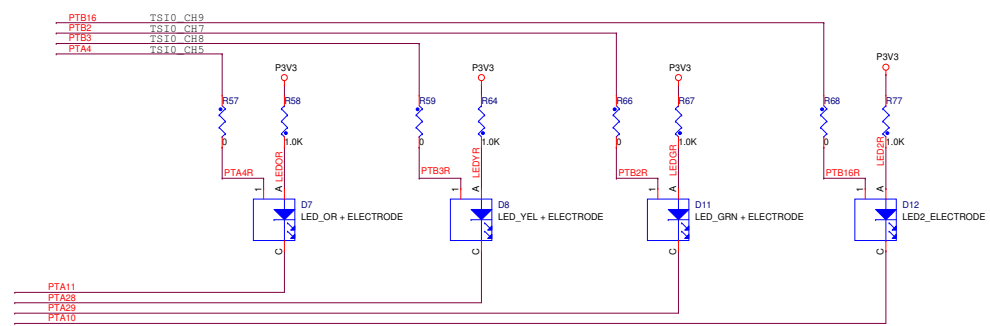
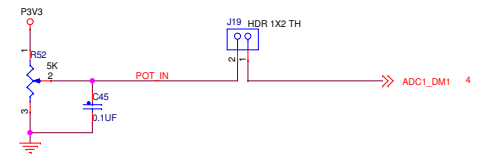
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TOUCH PAD
TWRPI



POTENTIOMETER



freescale
semiconductor

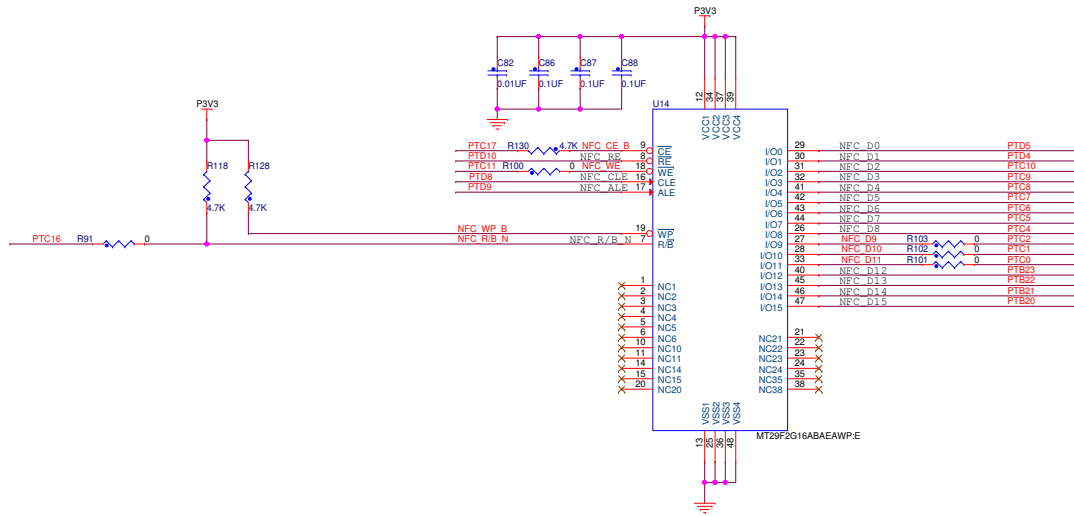
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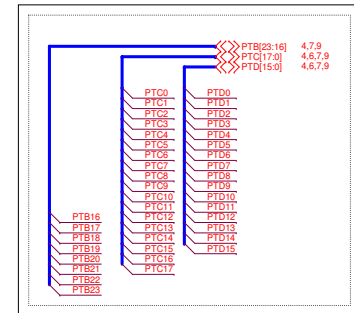
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NAND FLASH



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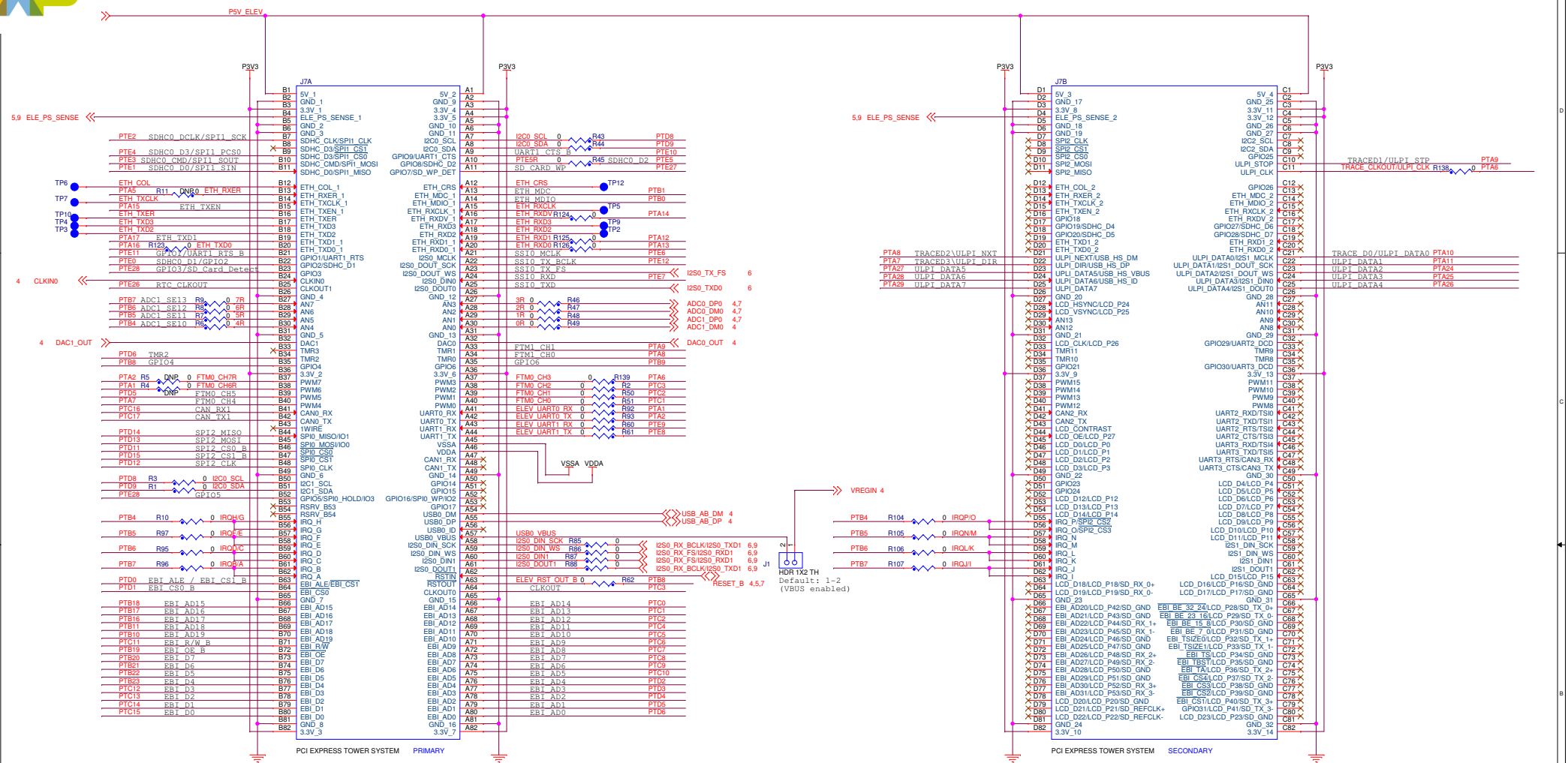
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