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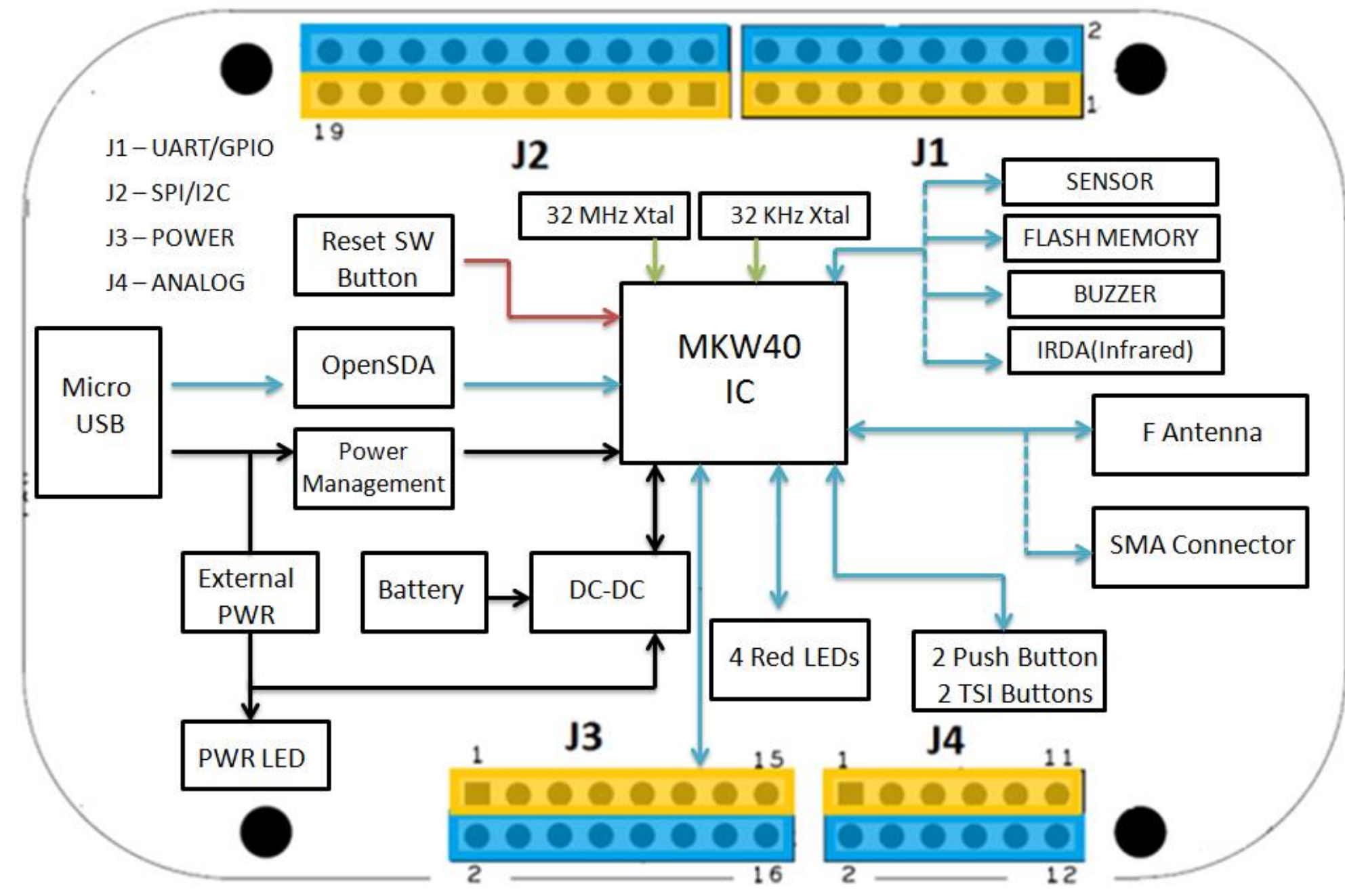
**Revisions & Change Log**

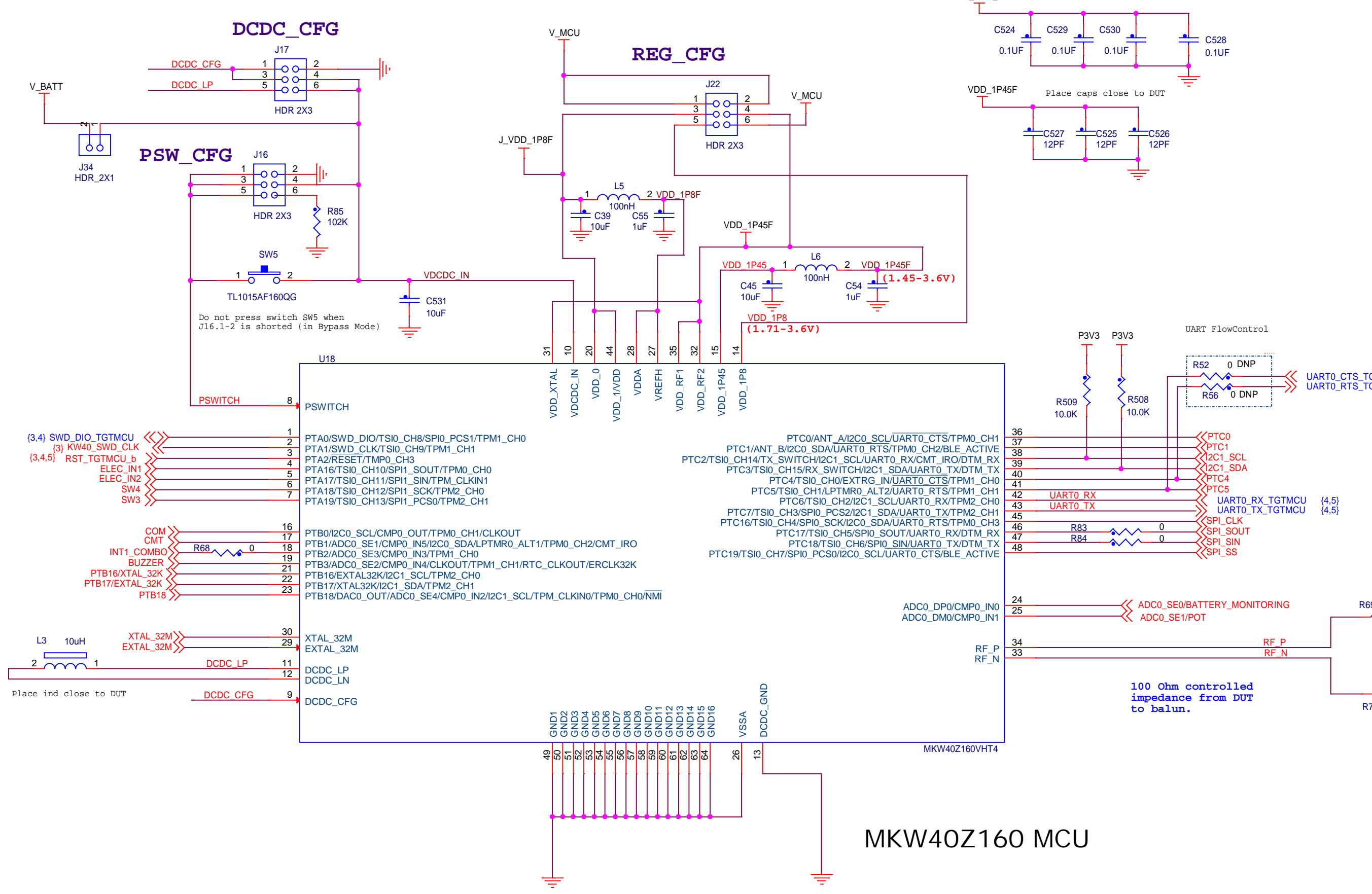
Rev	Description	Date	Approved
X1	Initial Draft	05/9/14	A. QUIROZ
X2	DCDC Jumper Sets FXOS8700CQ Accel RF Balun matching	05/19/14	A. QUIROZ
	BOM Optimization, Adding TP for Testing	05/23/14	A. QUIROZ
A	Prototype Release	07/08/14	A. QUIROZ
B	Update BOM, SPI Flash Memory	11/18/14	A. QUIROZ
B3	Update RF BOM, Adding DCDC capacitor	04/06/15	A. QUIROZ
C	Update headers and PokaYokes	8/05/15	A. QUIROZ
C1	Power supply updates, added headers	10/09/15	A. QUIROZ
C2	RF optimization	12/14/15	A. QUIROZ

# FREEDOM KW40Z BLE/Zigbee

		<b>Wireless Connectivity Operation</b> 6501 William Cannon Drive West Austin, TX 78735-8598	
This document contains information proprietary to Freescale Semiconductor and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of Freescale Semiconductor.			
Designer: A. QUIROZ		ICAP Classification: FCP: FIUO: PUBI: X	
Drawing Title: A. QUIROZ		<b>FRDM-KW40Z</b>	
Drawn by: A. QUIROZ		<b>TITLE PAGE</b>	
Approved: L. KELVIN	Size C	Document Number <b>SCH-28379   PDF: SPF-28379</b>	Rev C2
Date: Monday, December 14, 2015		Sheet 1 of 5	

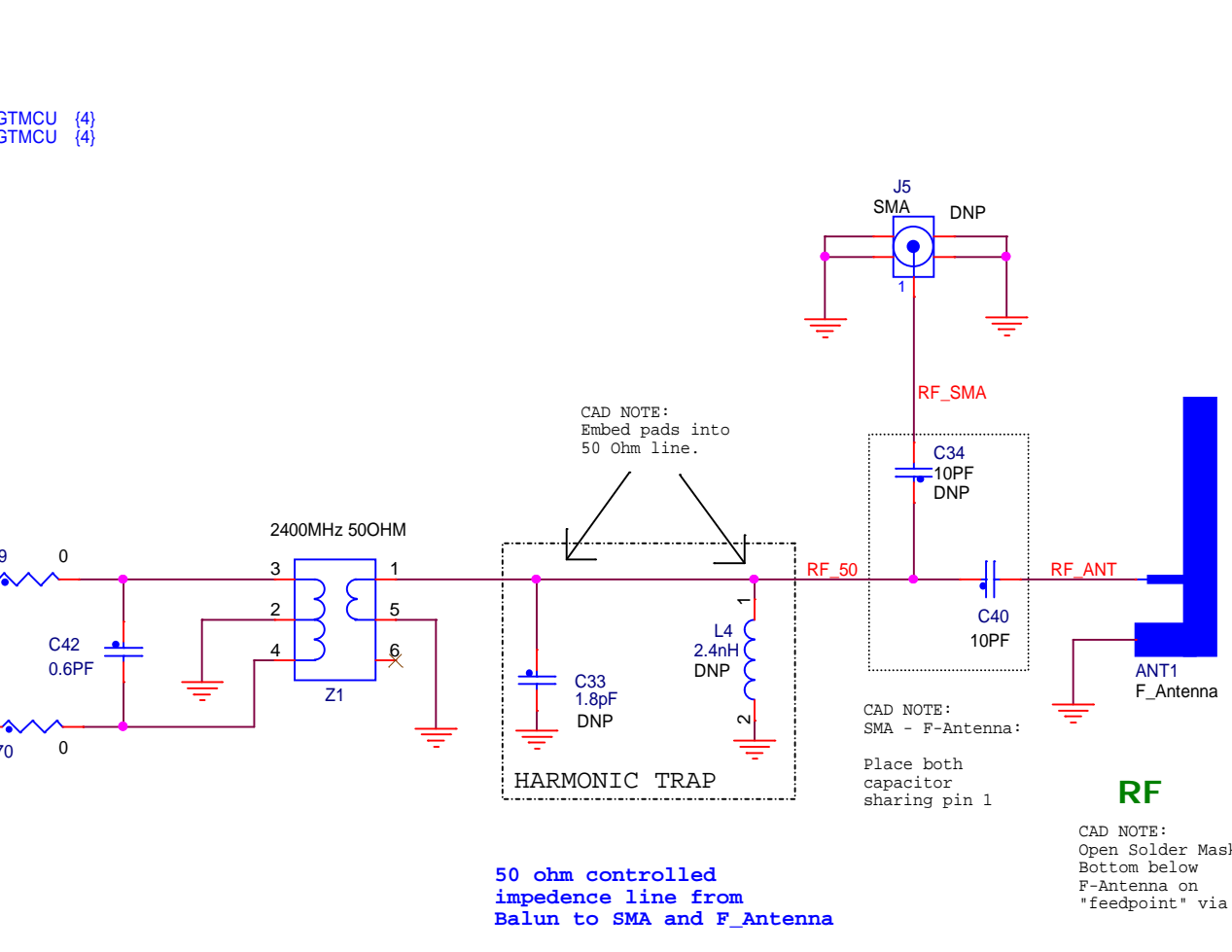
- Unless Otherwise Specified:  
 All resistors are in ohms, 5%, 1/8 Watt  
 All capacitors are in uF, 20%, 50V  
 All voltages are DC  
 All polarized capacitors are aluminum electrolytic
- Interrupted lines coded with the same letter or letter combinations are electrically connected.
- Device type number is for reference only. The number varies with the manufacturer.
- Special signal usage:  
 \_B Denotes - Active-Low Signal  
 <> or [] Denotes - Vectored Signals
- Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.





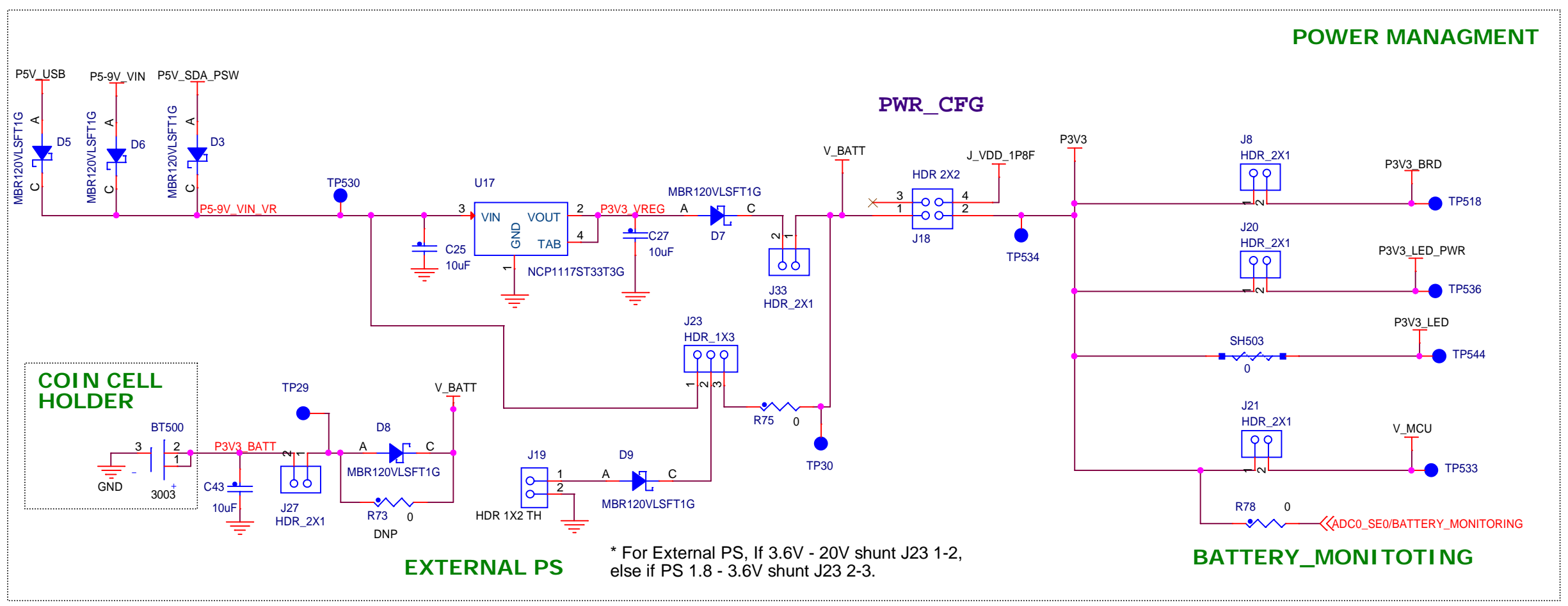
### Power Configuration

	PWR_CFG J18	PSW_CFG J16	DCDC_CFG J17	REG_CFG J22
<b>Bypass (1.8V - 3.6V)</b>	1-2	1-2	3-4	1-3 2-4 5-6
<b>Buck (1.8V - 4.2V) - Coin Cell</b>	2-4	5-6	3-4	3-5
<b>Buck Auto Mode (1.8V - 4.2V)</b>	2-4	3-4	3-4	3-5
<b>Boost (0.9V - 1.8V) - Single battery</b>	2-4	3-4	1-2 5-6	3-5

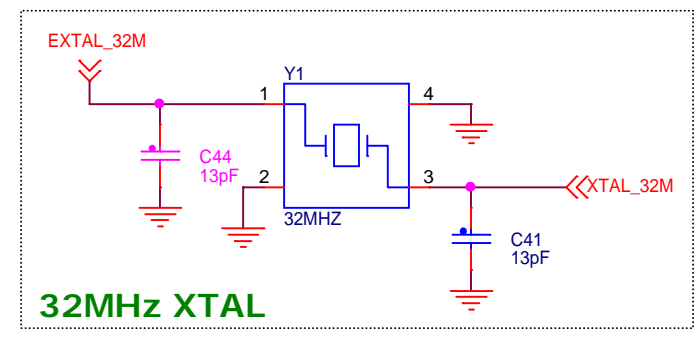
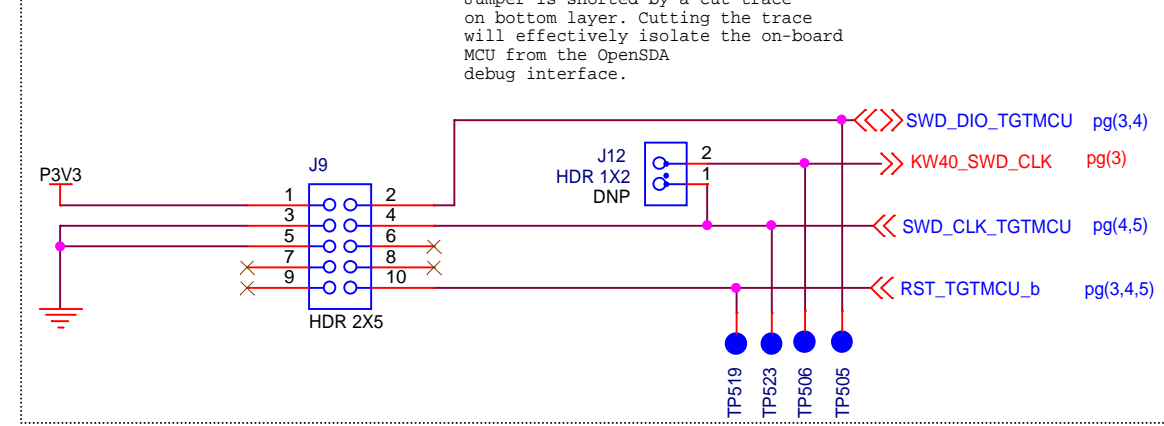


MKW40Z160 MCU

### POWER MANAGEMENT



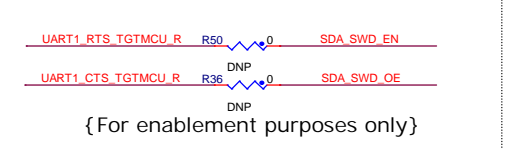
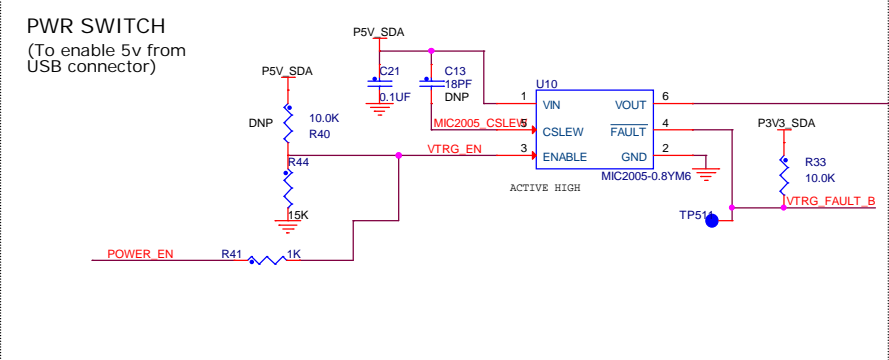
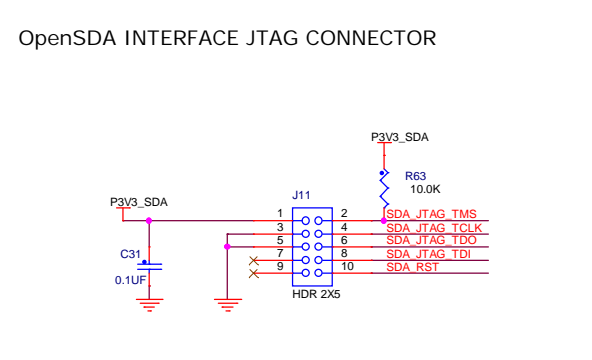
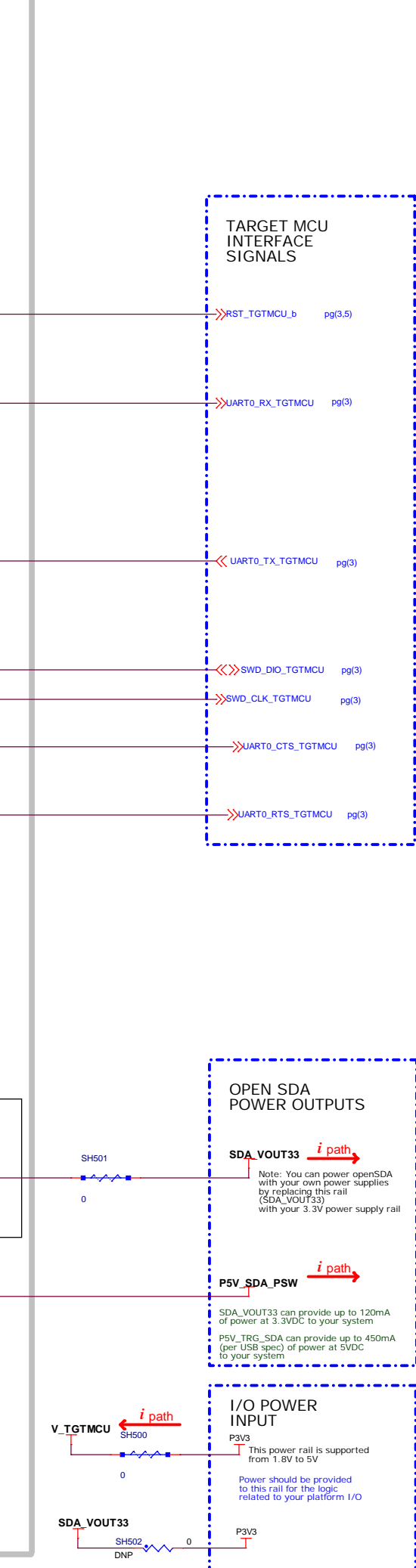
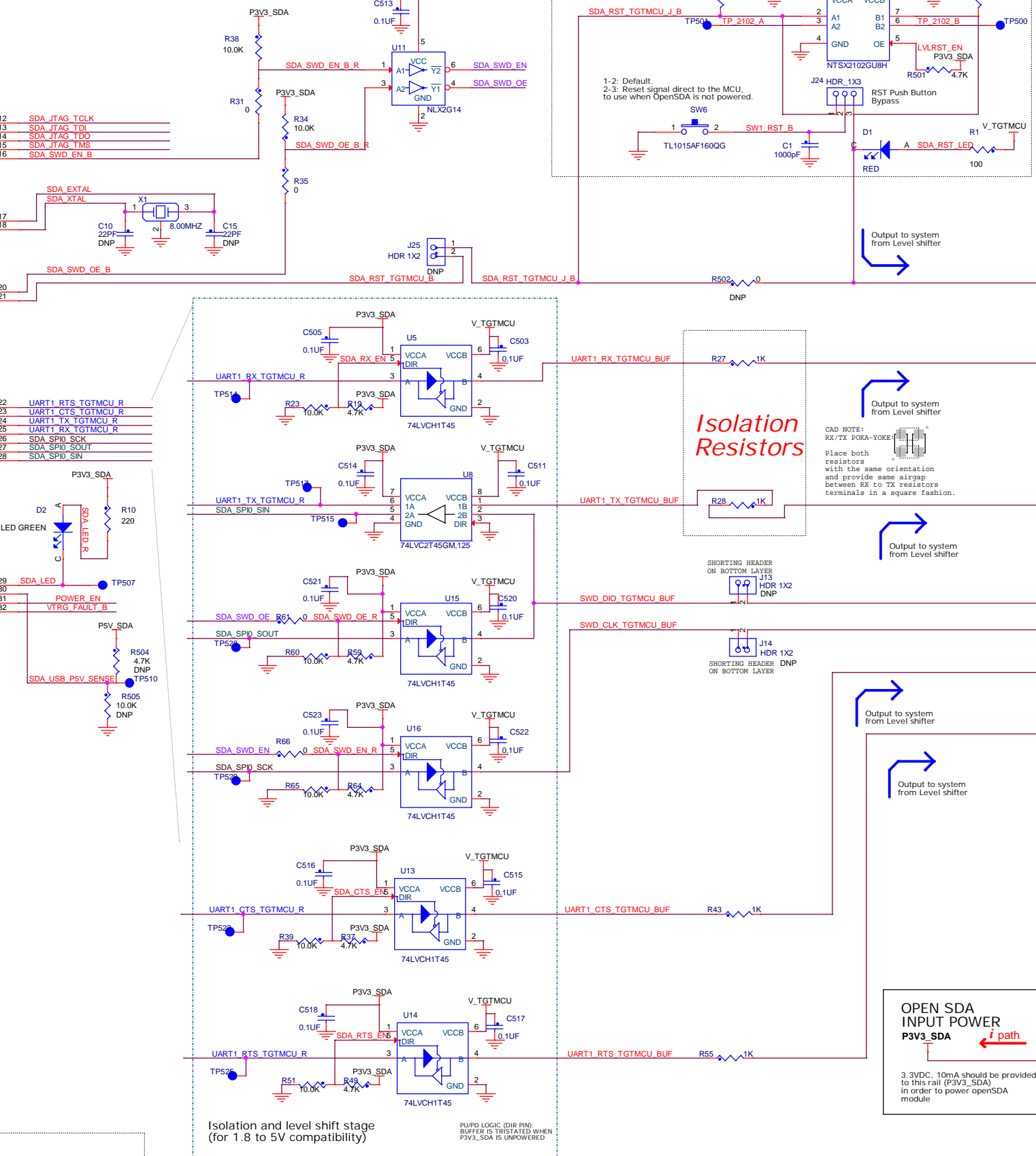
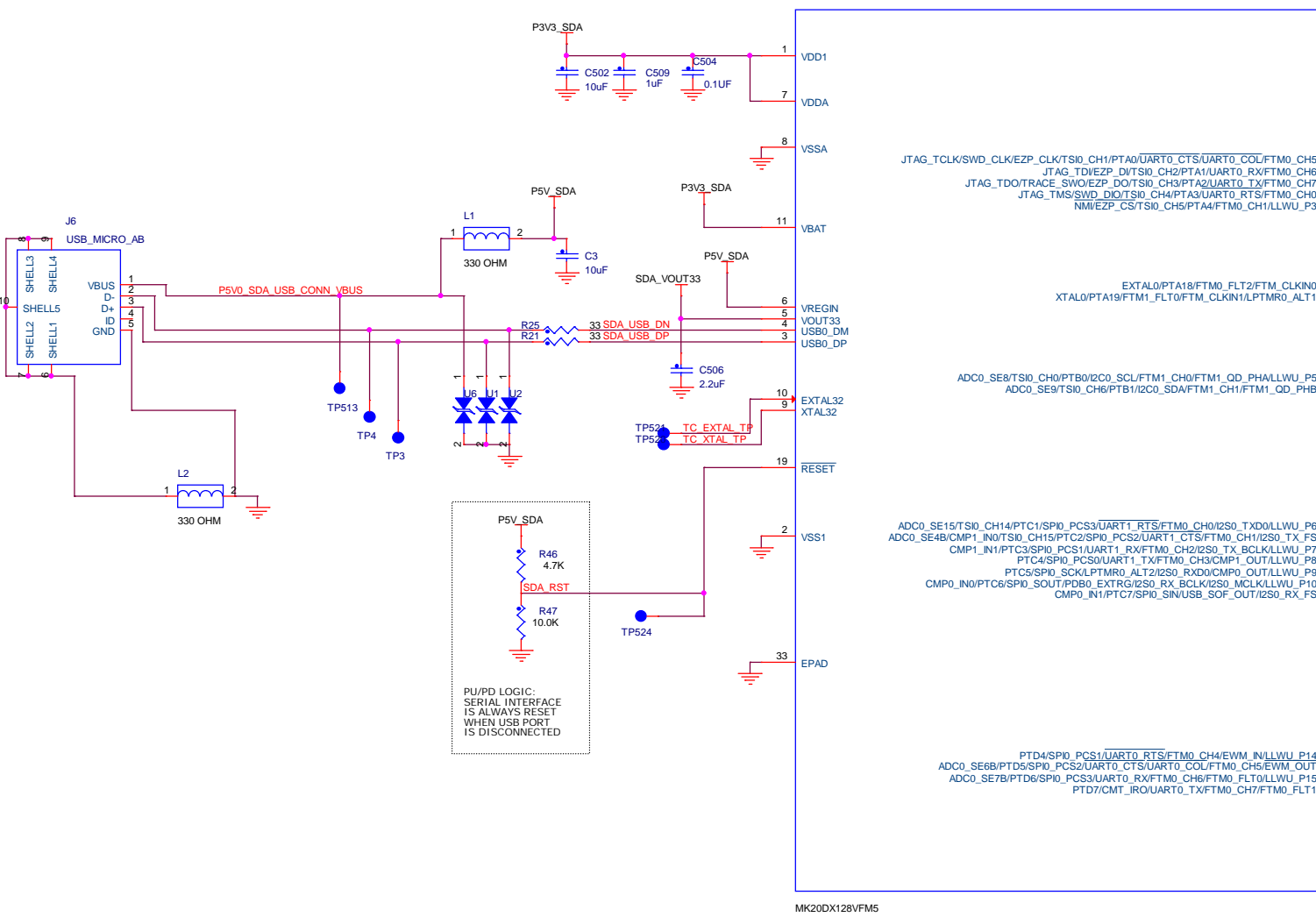
### SWD CONNECTOR

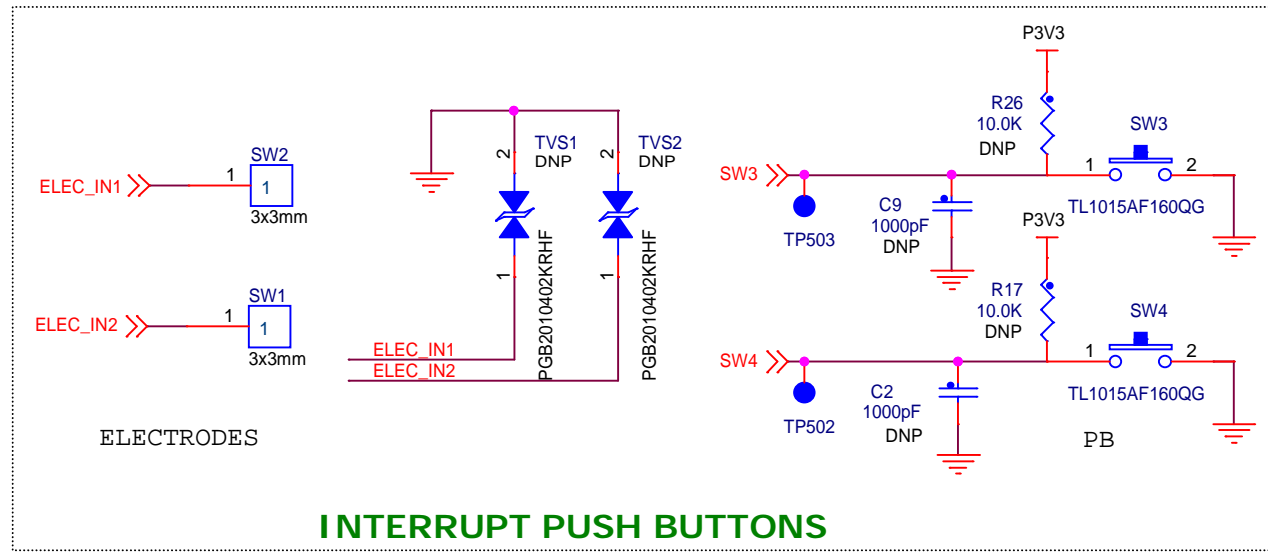


**freescale**

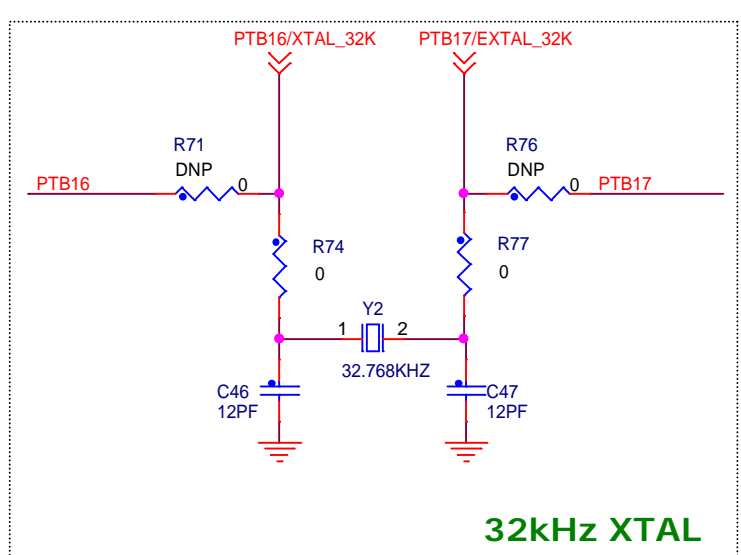
ICAP Classification: FCP: \_\_\_ FIUO: \_\_\_ PUBI: X  
 Drawing Title: **FRDM-KW40Z**  
 Page Title: **KW40x MCU**  
 Size C Document Number SCH-28379 | PDF: SPF-28379 Rev C2  
 Date: Monday, December 14, 2015 Sheet 3 of 5

# OpenSDA Interface

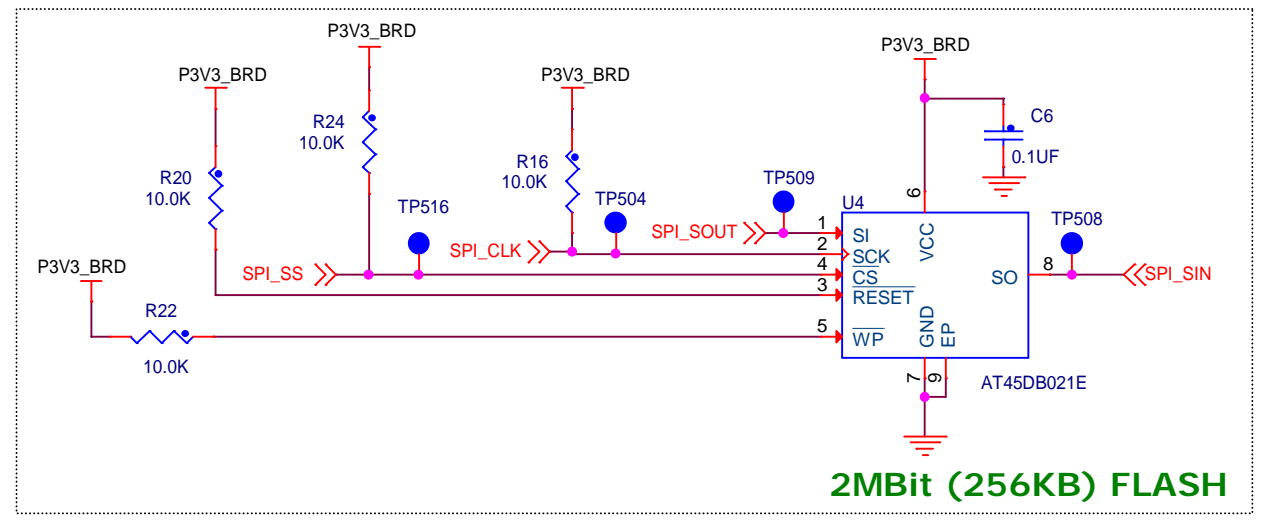




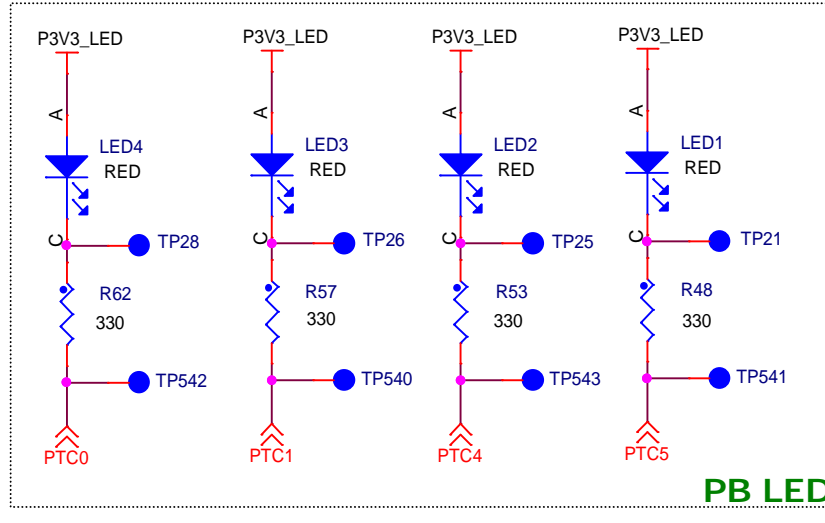
**INTERRUPT PUSH BUTTONS**



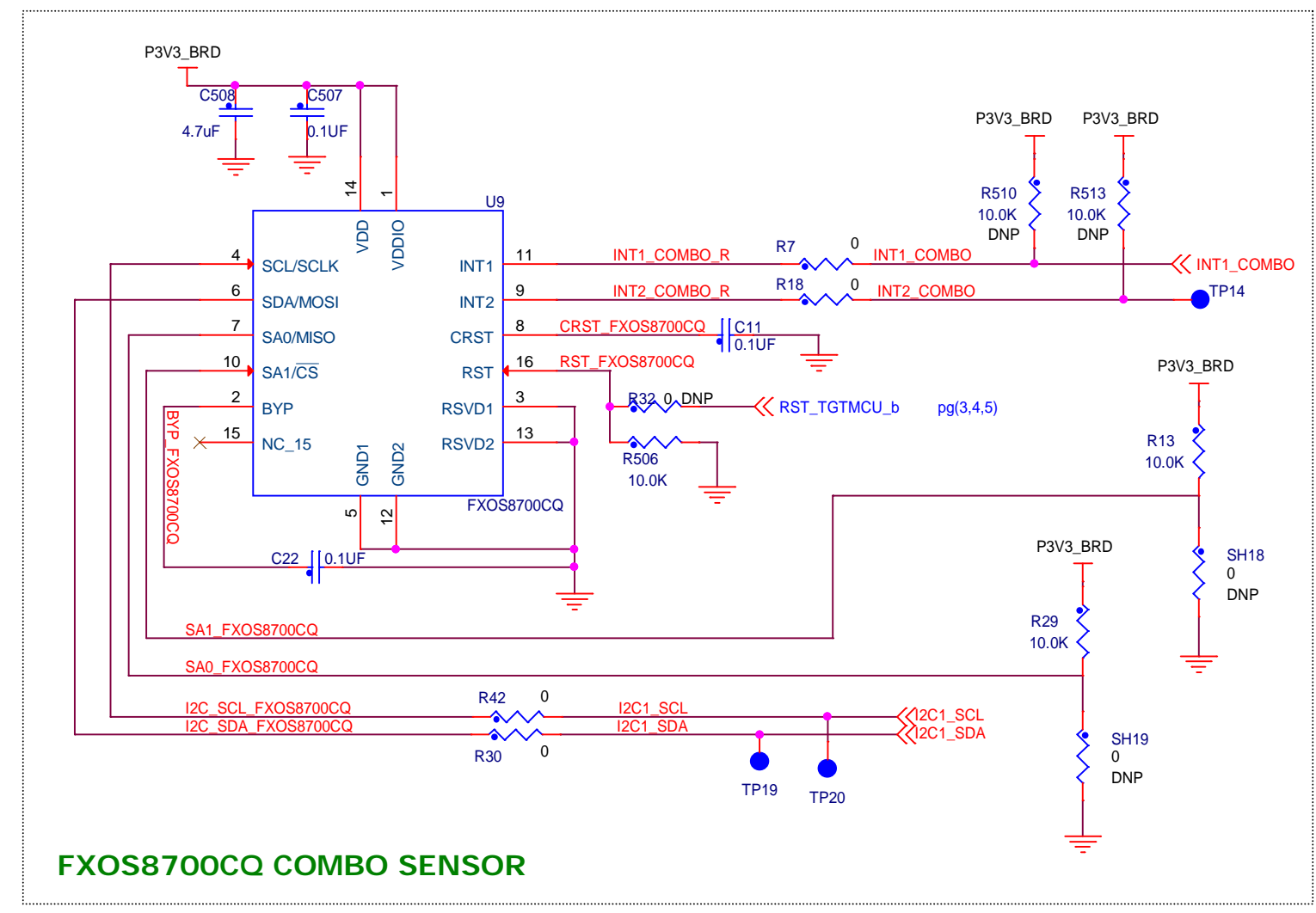
**32kHz XTAL**



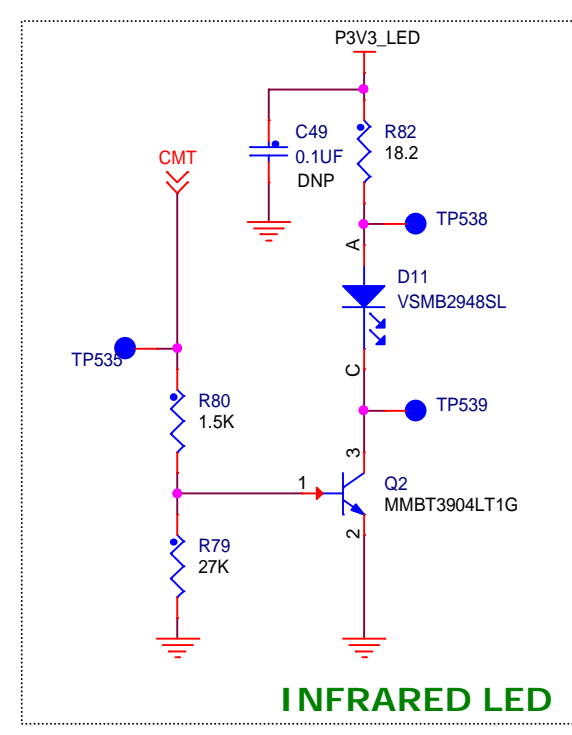
**2MBit (256KB) FLASH**



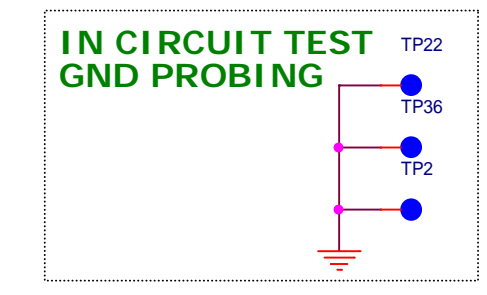
**PB LED**



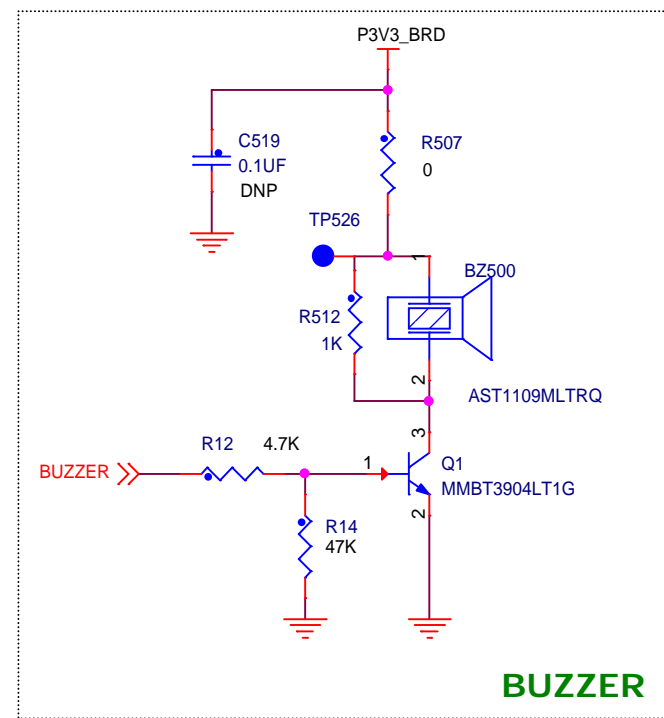
**FXOS8700CQ COMBO SENSOR**



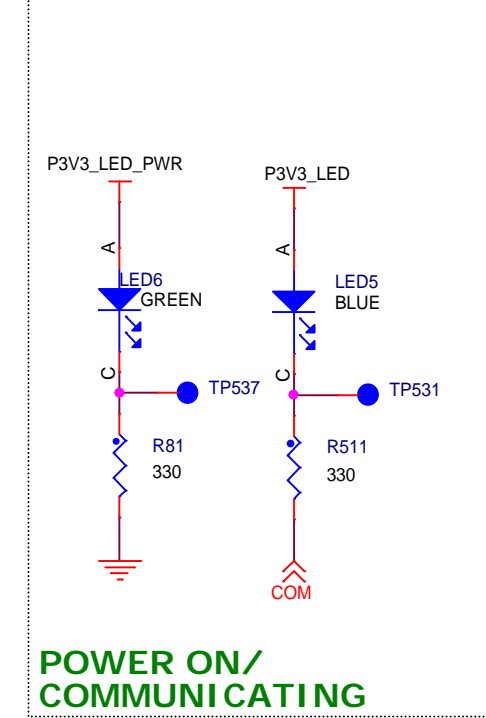
**INFRARED LED**



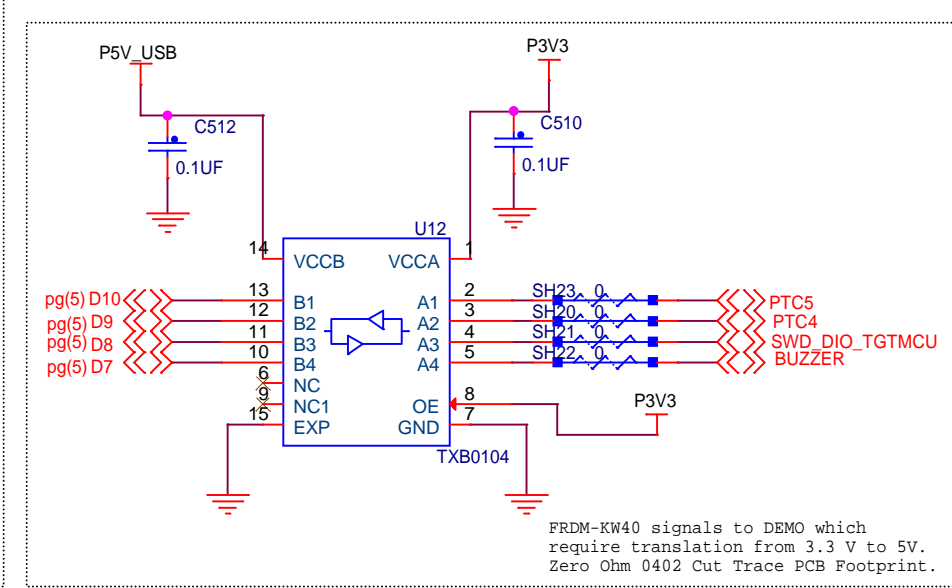
**IN CIRCUIT TEST GND PROBING**



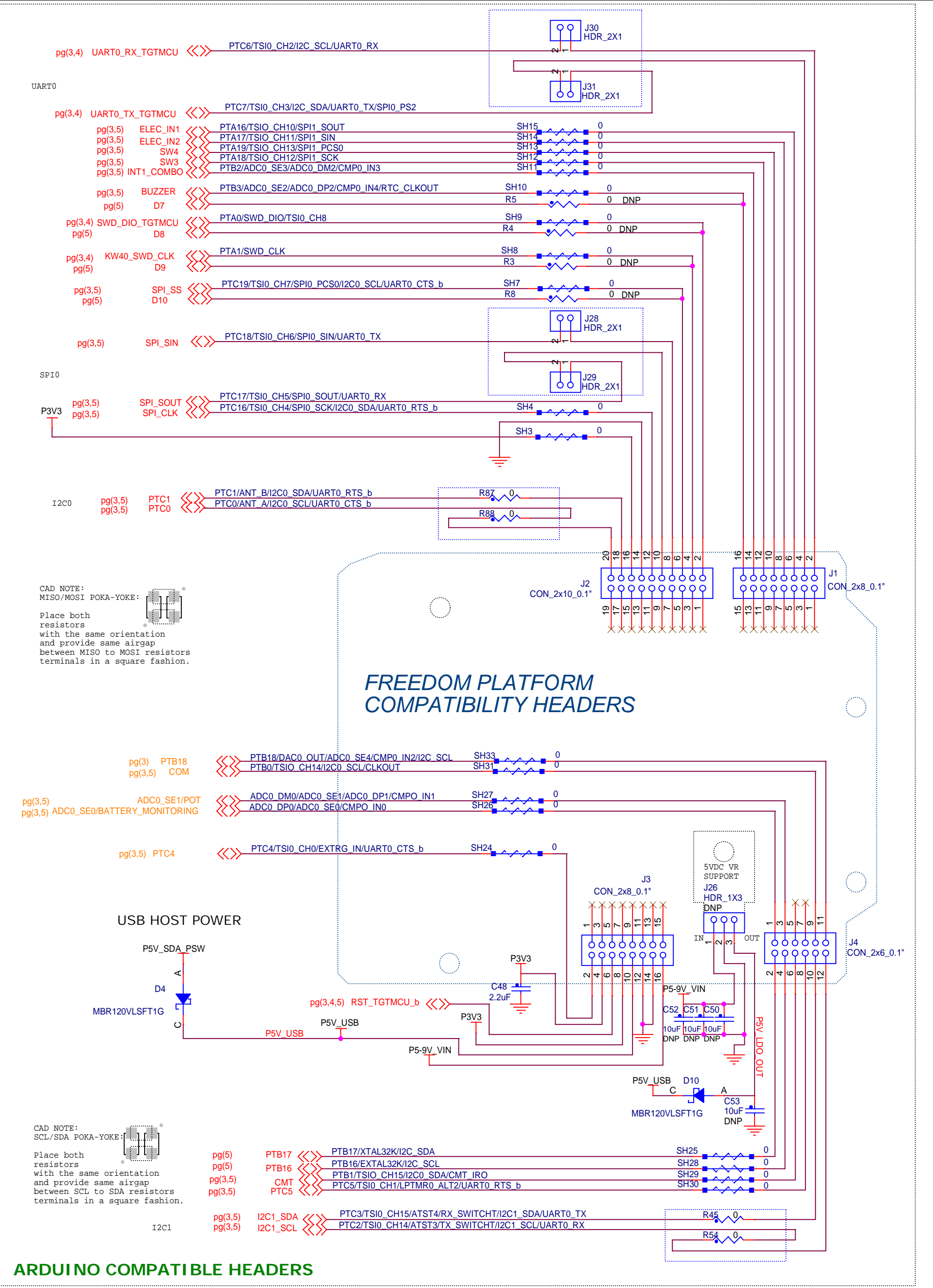
**BUZZER**



**POWER ON/ COMMUNICATING**



**POT**



**FREEDOM PLATFORM COMPATIBILITY HEADERS**

**ARDUINO COMPATIBLE HEADERS**

**DEBUG GROUND HOOK**

CAD NOTE:  
MISO/MOSI POKA-YOKE:  
Place both resistors with the same orientation and provide same airgap between MISO to MOSI resistors terminals in a square fashion.

CAD NOTE:  
SCL/SDA POKA-YOKE:  
Place both resistors with the same orientation and provide same airgap between SCL to SDA resistors terminals in a square fashion.

ICAP Classification:	FCP: FIUC: PUBI: X
Drawing Title:	<b>FRDM-KW40Z</b>
Page Title:	<b>ARDUINO SHIELDS &amp; PERIPHERALS</b>
Size C	Document Number SCH-28379   PDF: SPF-28379
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