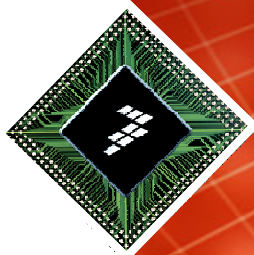




# Graphical LCD Controller Configuration Steps



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# LCDC Configuration

- Enable clock for all the LCDC PORT pins: PTF, PTE, PTD, PTB  
[SIM\_SCGC5]
- Set clock source for LCDC PLL0/PLL1/..  
[MCG\_S, MCG\_C2, etc..]
- Configure and enable DDR memory  
[SIM\_MCR, DDR\_RCR, DDR\_CR00, etc..]
- Enable LCDC Module  
[SIM\_SCGC3]
- Disable MPU or configure for LCDC Master access to DDR slave  
[MPU\_CESR]

# LCDC Configuration

- Configure LCDC pins Multiplexing for LCDC function  
[PORTF\_PCR4, PORTF\_PCR5, etc..]
- Set background plane DMA to burst mode (Recommended)  
[LCDC\_LDCR&=~LCDC\_LDCR\_BURST\_MASK;]
- Set graphic window DMA to burst mode (Recommended)  
[LCDC\_LGWDCR&=~LCDC\_LGWDCR\_GWBT\_MASK;]
- Set Frame buffer base address  
[LCDC\_LSSAR = FRAME\_START\_ADDRESS]
- Set LCD size  
[LCDC\_LSR= LCDC\_LSR\_XMAX() | LCDC\_LSR\_YMAX()]

# LCDC Configuration

- Set Fractional divisor if needed  
[SIM\_CLKDIV3]
- Set LCD Virtual Page  
[LCDC\_LVPWR]
- Set LCD cursor position and settings  
[LCDC\_LCPR, LCDC\_LCWHB]
- Set LCD panel configuration  
[LCDC\_LPCR]

TFT/CSTN Screen, Color/B&W, Pixel Polarity, bpp, first line marker active low/high, line pulse active low/high, Clock Polarity, Enable LSCLK when Vsync is idle, Always enable clock, LCD Divisor for Source clock

# LCDC Configuration

- Set LCD horizontal configuration bas

**LCDC\_LHCR =**

```
LCDC_LHCR_H_WIDTH(71) | //(71+1)=72 SCLK period for H
LCDC_LHCR_H_WAIT_1(23) | //(23+1)=24SCLK period betw
LCDC_LHCR_H_WAIT_2(125); //(125+3)=128 SCLK periods
```

- Set LCD vertical configuration based

**LCDC\_LVCR =**

```
LCDC_LVCR_V_WIDTH(1) | //1 SCLK period for VSYNC at
LCDC_LVCR_V_WAIT_1(2) | //2 SCLK period between end
LCDC_LVCR_V_WAIT_2(22); //22 SCLK periods between en
```

- Set [LCDC]

- Set L [LCDC]

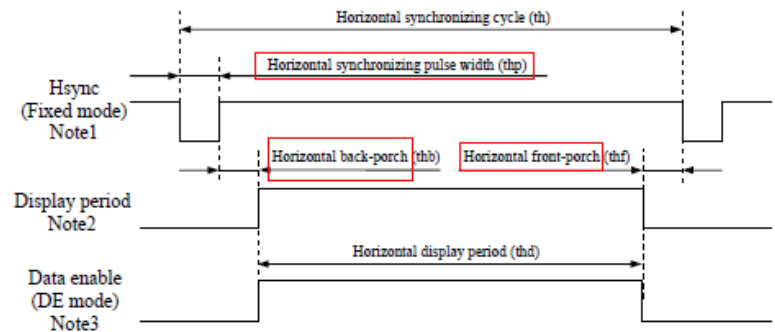


	Parameter	Symbol	min.	typ.	max.	Unit	Remarks	
Hsync	Cycle	th	24.0	26.7	30.1	μs	37.5 kHz (typ.)	
	Display period	thd		800		CLK	Note1	
	Front-porch	thf		24		CLK		
	Pulse width	thp	12	72	-	CLK		
	Back-porch	thb	-	128	198	CLK		
	Total of pulse width and back-porch	thp + thb		200		CLK		
	CLK- Hsync	Setup time	ths	8	-	-	ns	-
		Hold time	thh	10	-	-	ns	
		Rise time, Fall time	thrf	-	-	10	ns	
	Vsync	Cycle	tv	16.0	16.7	18.8	ms	59.9 Hz (typ.)
Display period		tvd		600		H	Note1	
Front-porch		tvf		1		H		
Pulse width		tvp	1	-	2	H		
Back-porch		tvb	22	-	23	H		
Total of pulse width and back-porch		tvp + tvb		24		H		
Vsync-Hsync		Setup time	tvhs	15	-	-	ns	Note1
		Hold time	tvhh	1	-	-	CLK	
	Rise time, Fall time	tvrf	-	-	10	ns		

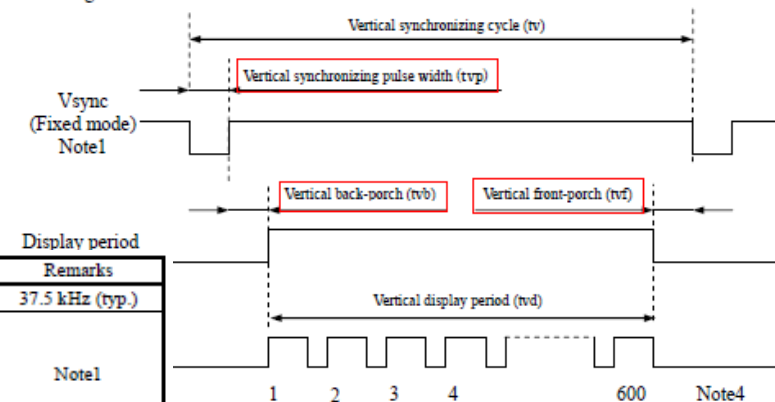
## 4.9 INPUT SIGNAL TIMINGS

### 4.9.1 Outline of input signal timings

- Horizontal signal



- Vertical signal



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# LCDC Configuration

- Set LCD interrupt enable if needed  
[\[LCDC\\_LIER\]](#)
- Set LCD graphic window start address  
[\[LCDC\\_LGWSAR\]](#)
- Set LCD graphic window size  
[\[LCDC\\_LGWSR\]](#)
- Set LCD graphic window virtual page width  
[\[LCDC\\_LGWVPWR\]](#)
- Set LCD graphic window panning offset  
[\[LCDC\\_LGWPOR\]](#)

# LCDC Configuration

- Set LCD graphic window position  
[LCDC\_LGWPR ]
- Set LCD graphic window control  
[LCDC\_LGWCR ]
- Enable LCD  
[SIM\_MCR]