2.5.3 Debug interface

The Kinetis MCUs use the Cortex Debug interfaces for debugging and programming. The 19-pin Cortex Debug+ETM interface provides connections for JTAG and Serial Wire debugging, as well as target power. The 9-pin Cortex Debug interface provides connections for JTAG and Serial Wire debugging. Figure 2-7 shows the 20-pin header implementation (19 pins populated) as used on the TWR system boards. Figure 2-8 shows the 10-pin header implementation (9 pins populated).

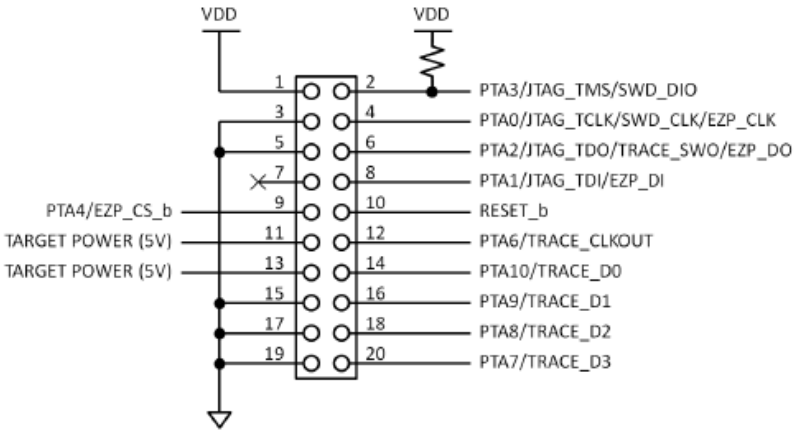

Figure 2-7. 20-pin debug interface

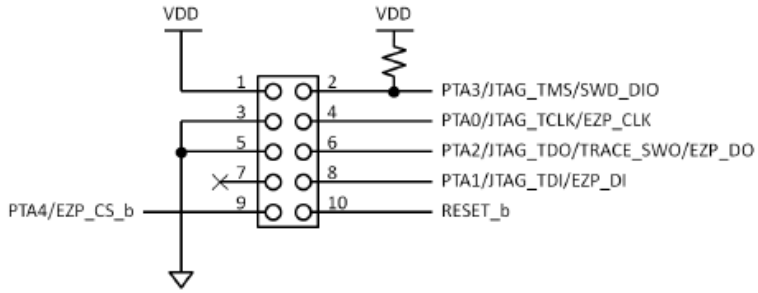

Figure 2-8. 10-pin debug interface

The debug signals are multiplexed with general purpose I/O pins, so some signals will require proper biasing to select the operating mode. The JTAG_TMS signal on PTA3 requires a strong pullup resistor for mode selection. The Cortex Debug specification recommends that the JTAG_TCLK and JTAG_TDI pins (on PTA0 and PTA1) have pull resistors (high or low) to force a known state on these debug input pins. Note that the RESET_b signal in the debug interface is the MCU's reset pin and not the JTAG_TRST signal. The connectors for this interface are keyed dual row 0.050" centered headers. When implementing either of these headers on a target system, pin 7 must be depopulated to use the 19-pin or 9-pin adapters from the debug tool. The Samtec part numbers for these connectors are:

- FTSH-110-01-L-DV-K – 20-pin keyed connector
- FTSH-105-01-L-DV-K – 10-pin keyed connector

- FTSH-110-01-L-DV – 20-pin connector, no key
- FTSH-105-01-L-DV – 10-pin connector, no key

This interface is useful during the development phase of a project. The header may not need to be populated in the production phase of the project, but the PCB pads should be kept available for future debugging purposes.