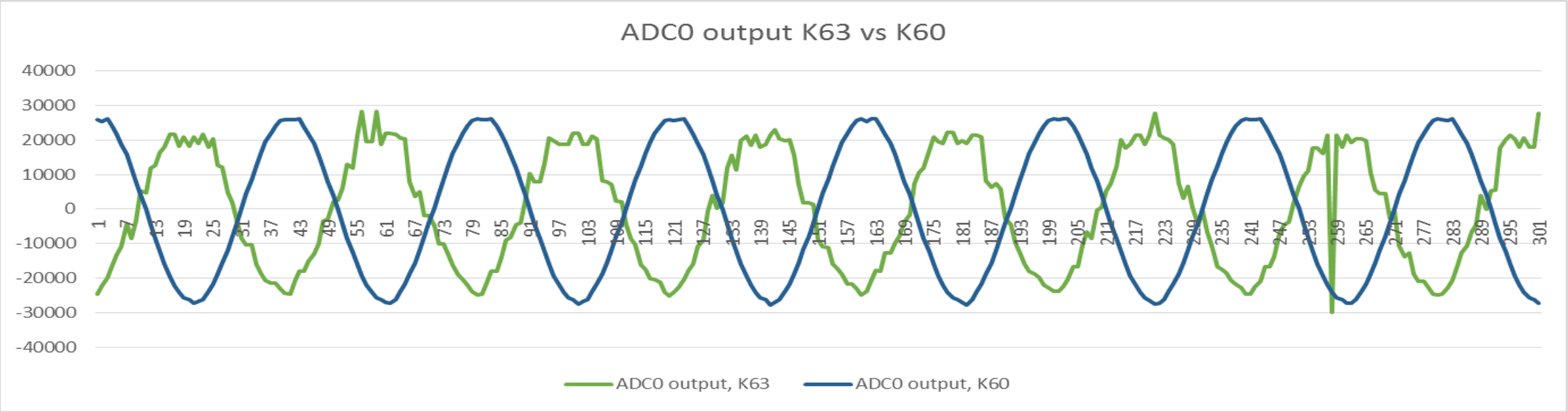
K63 ADC output is bad vs K60



When switching the K60 with the K63 it looks like ADC positive values saturate below the expected dynamic range and are noisy.
Input signal on ADC pins is 50Hz sine wave with range between 0,8V and 1,6V

ADC register settings

- Busclk = 50 MHz (K60), Busclk = 60Mhz(K63)
- ADC0_CFG1
  - Clock Input = Busclk2 (ADICLK = 0x1)
  - Clock divider = 8 (ADIV = 0x3)
  - Mode Single ended 16 bits (MODE = 0x3)
  - Long Sample (ADLSMP = 0x1)
  - No low power (ADLPC = 0x0)
- ADC0_CFG2
  - 24 cycle time (ADLSTS = 0x0)
  - High speed conversion (ADHSC =0x1)
  - ADACKEN = 0x0
  - MuxSel = 0x0
- ADC0_SC1A
  - DADP1 input (ADCH = 0x1)
  - Single Ended (DIFF = 0x0)
  - AIEN =0x0
  - COCO = 0x0
- ADC0_SC1B
  - Disabled (ADCH = 0x1F)
  - DIFF = 0x0
  - AIEN =0x0
  - COCO = 0x0
- ADC0_SC2 = 0x00000005
  - REFSel = 0x1
  - DMA interupt enabled (DMAEN = 0x1)
  - SW trigger (ADTRG = 0x0)
- External VREF is not used, internal is used.

Test conditions

- Issue is not board dependent: it is observed on several board samples, several tests have been made to shorten the root cause to the chip family only.
- Same freescale SW, MQX rev411.
- Input signal on ADC pins is 50Hz sine wave with range between 0,8V and 1,6V (offset is 1,2V)
- K60 runs BusClk at 48MHz, K63 runs BusClk at 60MHz (as per reference manual)
  - Aligning K63 clocks with K60 clock values does not solve the problem
  - Modifying ADIV value to any higher value makes the signal even more noisy on K63,
  - Modifying ADIV value to 3, 2 or1 has no impact on ADC output (ADIV=0 is out of spec on K60)
  - Using ADICLK = BusClk (0), ADIV=2 instead of BusClk/2 (1), ADIV=1 on the K60 makes the ADC output to be degraded in a similar way, however it may be a different root cause than the one we are facing with K63.
- No difference ADC0 or ADC1 is used.