FRDM_KL27Z cyclone max error 0x000000007, cant program / debug.

I have done some testing over the last few days, I believe I have done my job and checked everything, this should be very simple, but has proven to be complex for some reason. Mostly due to PE Micro wanting to force you to use their own adaptors (making us pay another $100 on top of the already $900 programmer).

I am running Windows 7, KDS (Kinetis Design Studio), the OpenSDA and the FRDM-KL27Z dev board works fine for debugging.

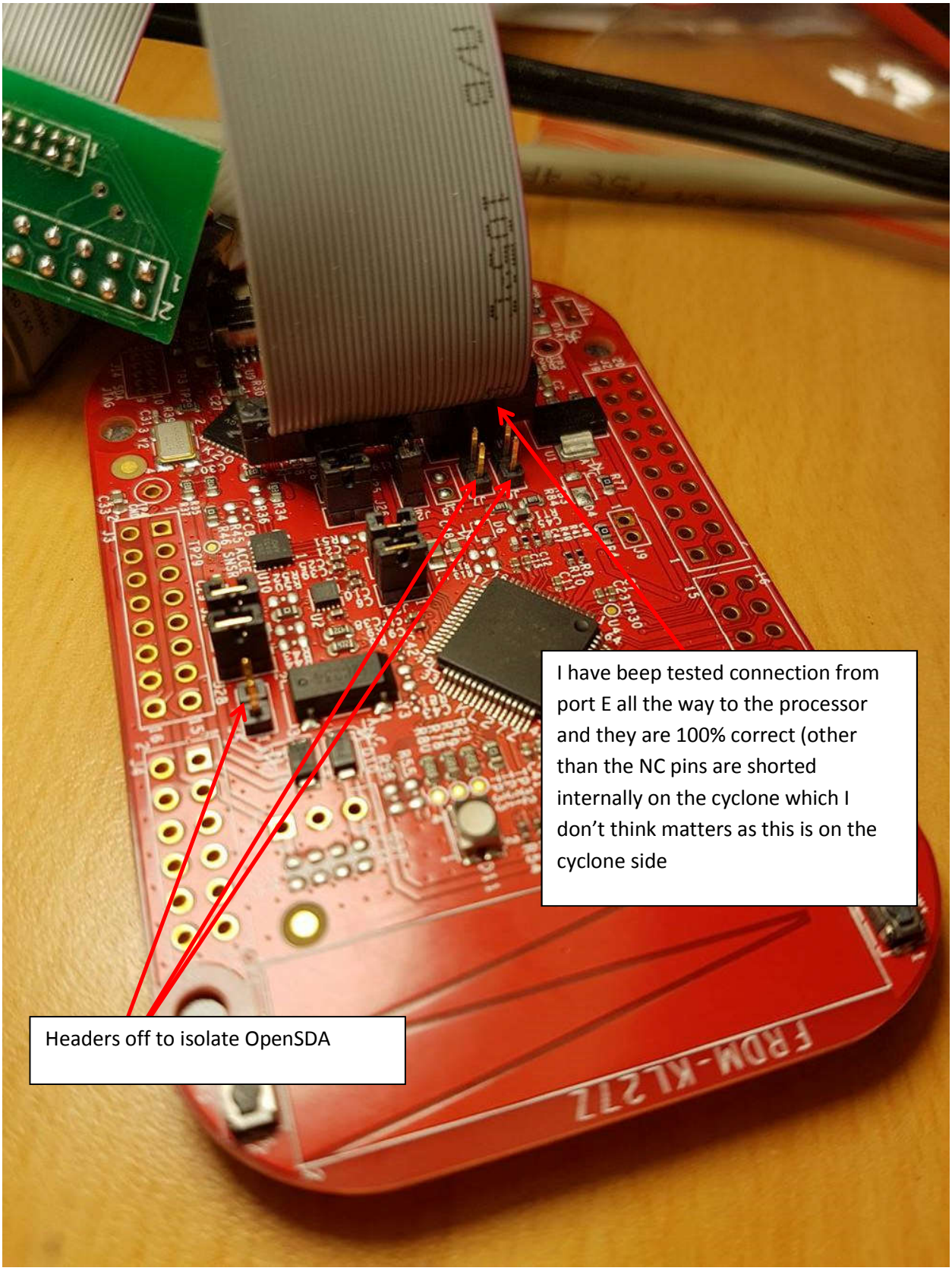
The cyclone is running version V7.93-6.2. I have tried both KDS (Kinetis Design Studio) and the cyclone image creation tool to use to program and both do the same thing… nothing…

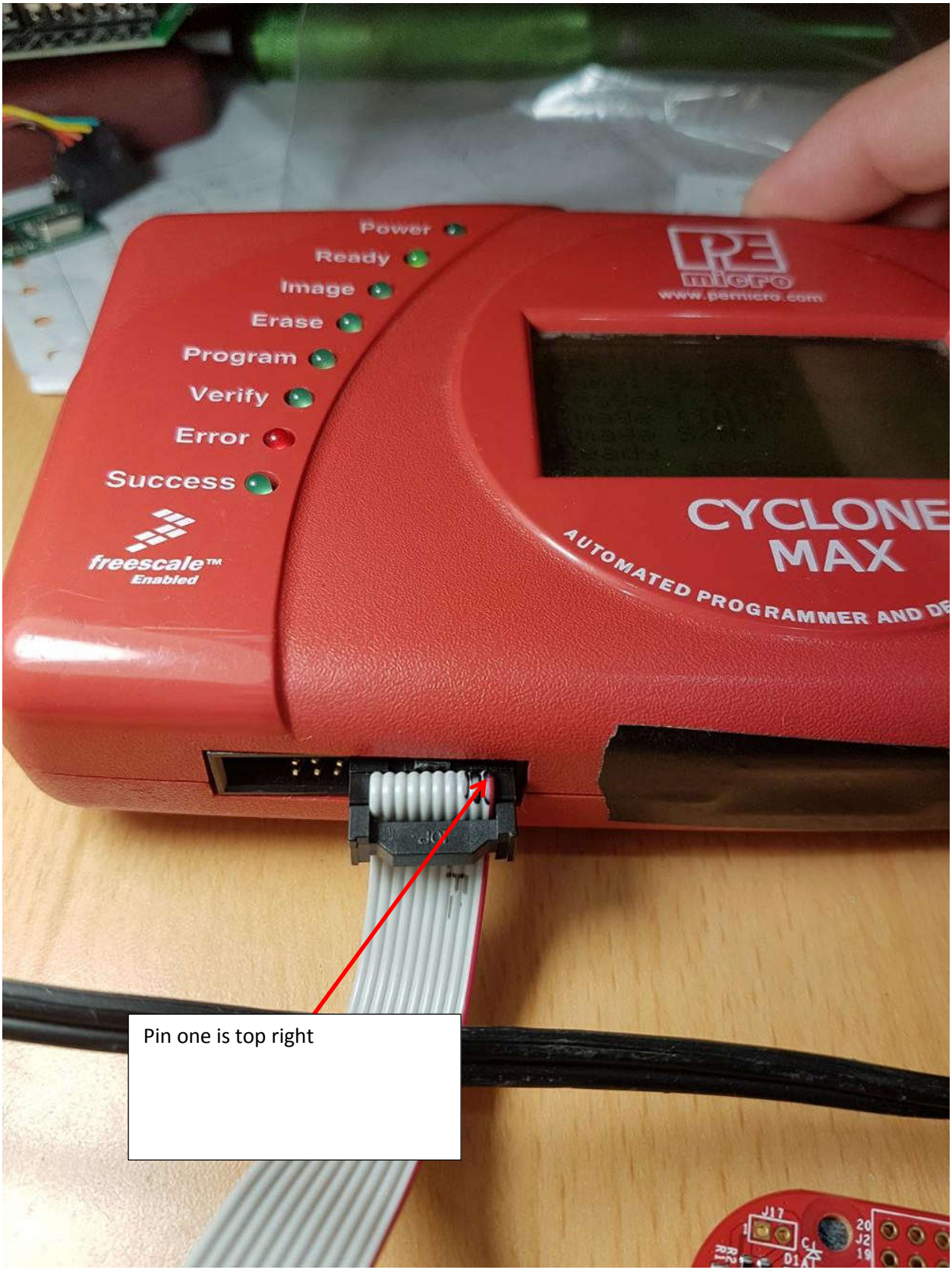
As we have our own tool chain coming, I have connected my own test 10 pin IDE cable to an adaptor to go from 2.54mm to 1.27mm connected to Port E on the cyclone MAX, I have tested the connections 1 to 10 and are all perfect. I have found a post saying you must short pins 3 and 10 on cyclone max port B to "enable" SWD to work, so this has been done, still not luck (apparently this shorts out pins 7 and 15 on PORTE which is all the adaptor does to enable SWD debug/programming).

On the FRDM board I take off the three jumpers that connect the OpenSDA programmer (J5, J7, J6), J18 remains shorted for CLK.

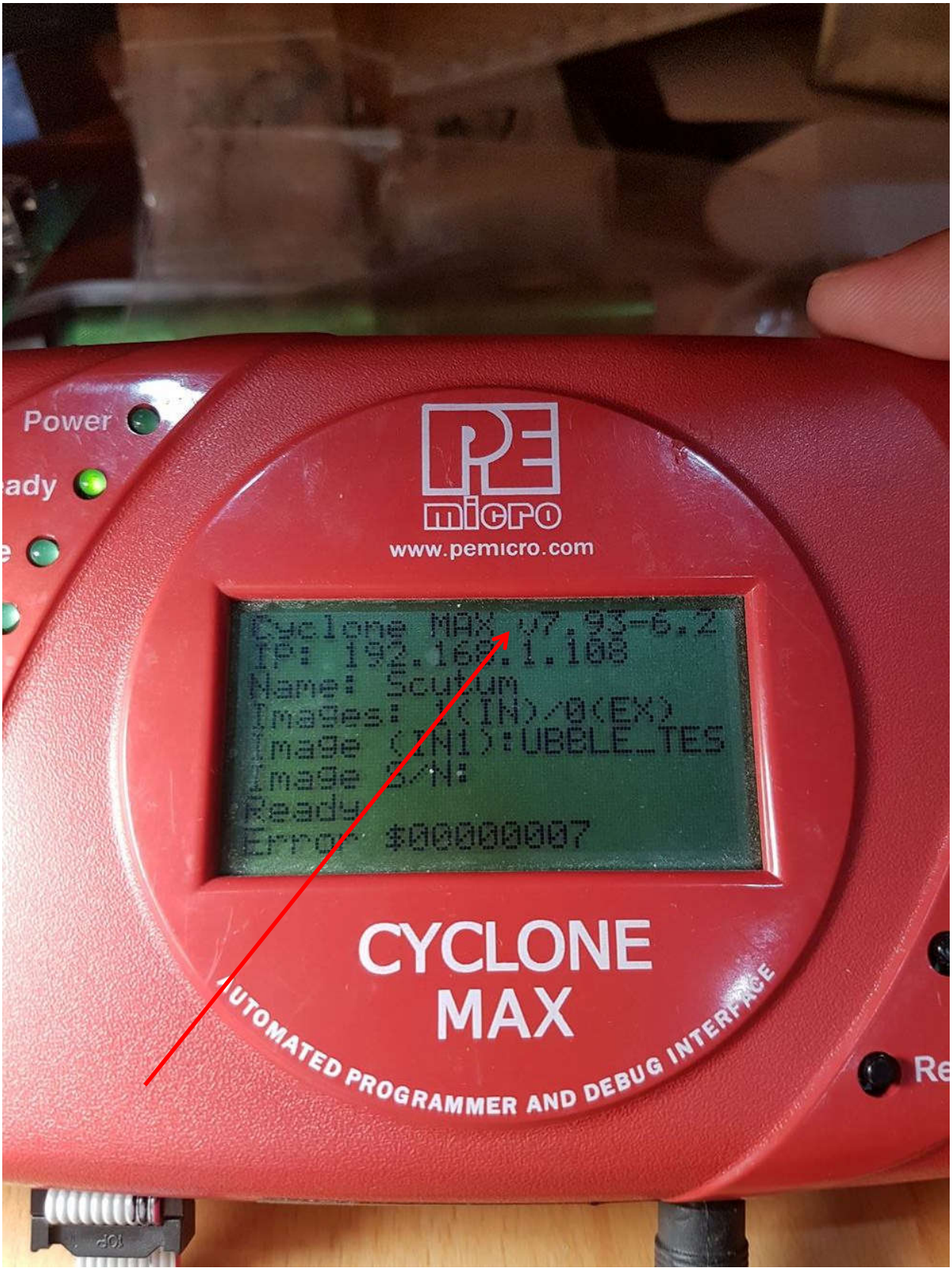
This is all straight forward, I have beep tested each connection from processor back to cyclone MAX and they are right. I have checked VCC, operation, everything is fine. I have my oscilloscope on and reset does literally nothing, I would expect to see it pull low, SWD pins also do literally nothing.

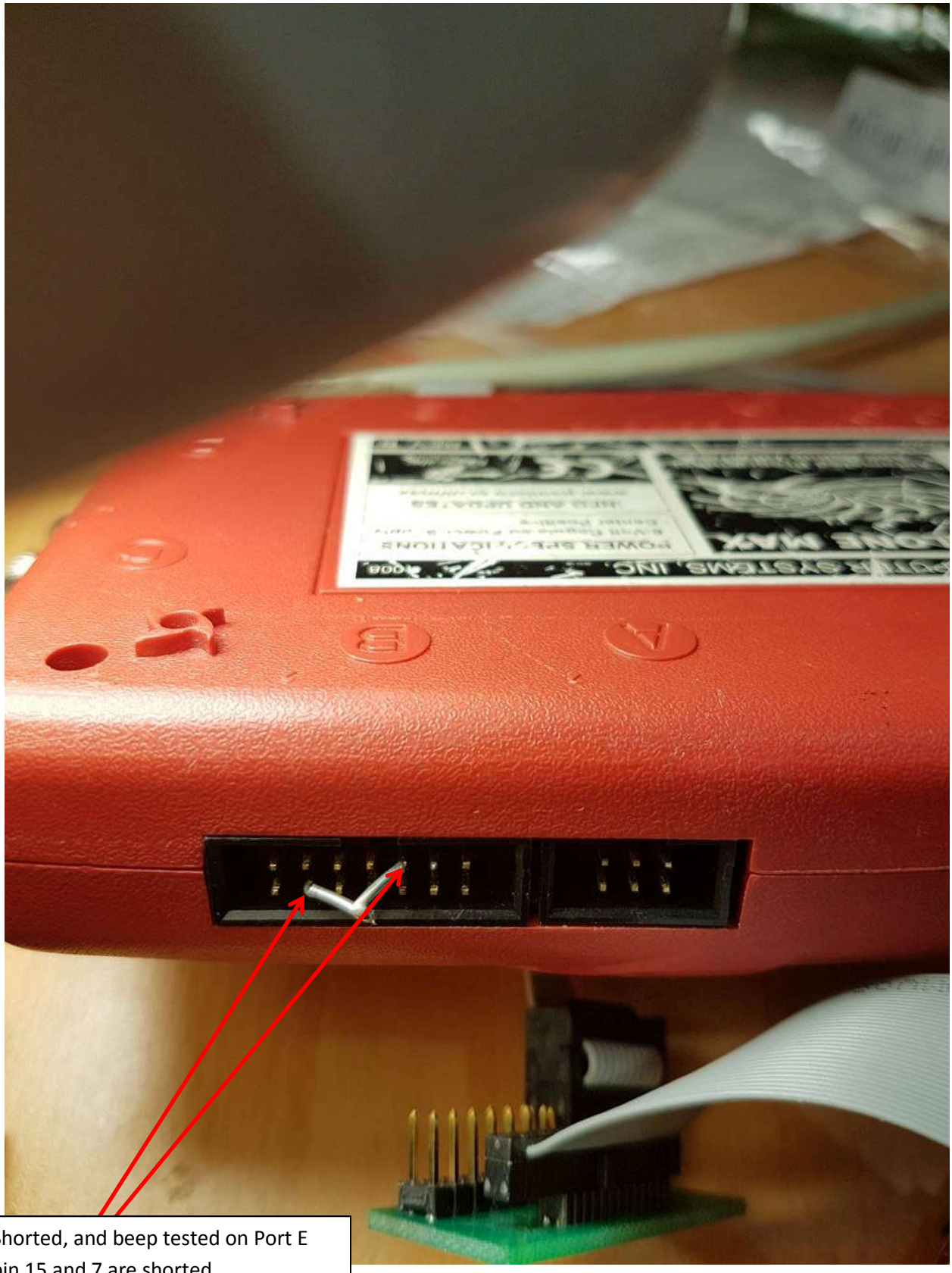
I also have my own prototypes board with a standard 2.54mm header so I can just go Cyclone max to my board, and I get exactly the same result. The cyclone is doing nothing, the pins don't change state at all, no reset, no nothing.


I have beep tested connection from port E all the way to the processor and they are 100% correct (other than the NC pins are shorted internally on the cyclone which I don't think matters as this is on the cyclone side
Headers off to isolate OpenSDA

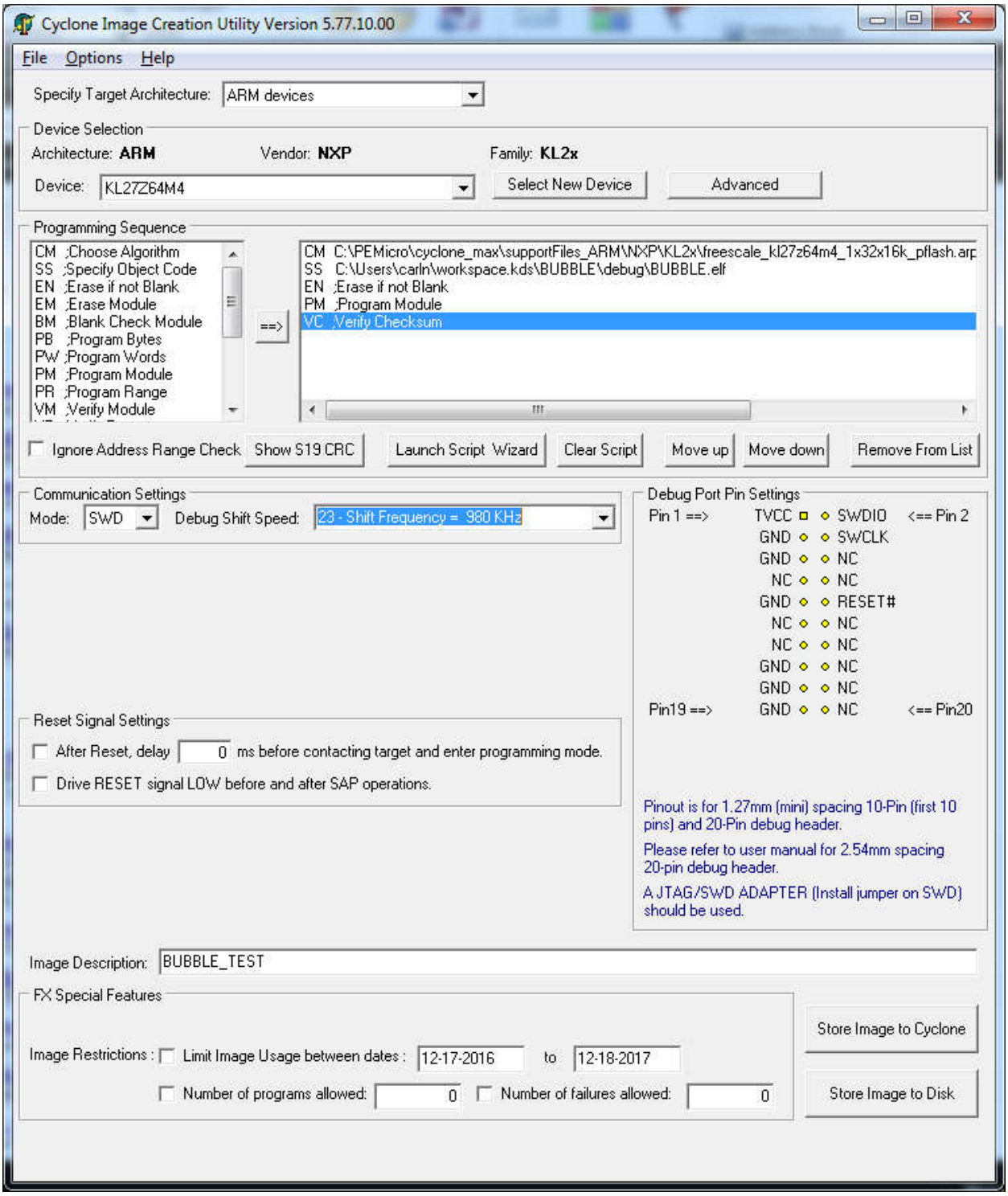

Power
Ready
Image
Erase
Program
Verify
Error
Success
freescale™
Enabled
www.pemicro.com
CYCLONE
MAX
AUTOMATED PROGRAMMER AND
Pin one is top right


MOSI
SCLK
CS


Power
www.pemicro.com
Cyclone MAX v7.93-6.2
IP: 192.168.1.108
Name: Scutum
Images: 1(IN)/0(EX)
Image (IN1):UBBLE_TES
Image 2/N:
Ready
Error $00000007
CYCLONE
MAX
AUTOMATED PROGRAMMER AND DEBUG INTERFACE



Shorted, and beep tested on Port E
pin 15 and 7 are shorted


Cyclone Image Creation Utility Version 5.77.10.00
File Options Help
Specify Target Architecture: ARM devices
Device Selection
Architecture: ARM
Vendor: NXP
Family: KL2x
Device: KL27Z64M4
Select New Device
Advanced
Programming Sequence
CM ;Choose Algorithm
SS ;Specify Object Code
EN ;Erase if not Blank
EM ;Erase Module
BM ;Blank Check Module
PB ;Program Bytes
PW ;Program Words
PM ;Program Module
PR ;Program Range
VM ;Verify Module
==>
CM C:\PEMicro\cyclone_max\supportFiles_ARM\NXP\KL2x\freescale_kl27z64m4_1x32x16k_pflash.arp
SS C:\Users\carln\workspace.kds\BUBBLE\debug\BUBBLE.elf
EN ;Erase if not Blank
PM ;Program Module
VC ;Verify Checksum
Ignore Address Range Check
Show S19 CRC
Launch Script Wizard
Clear Script
Move up
Move down
Remove From List
Communication Settings
Mode: SWD
Debug Shift Speed: 23 - Shift Frequency = 980 KHz
Debug Port Pin Settings
Pin 1 ==> TVCC SWDIO <== Pin 2
GND SWCLK
GND NC
NC NC
GND RESET#
NC NC
NC NC
GND NC
GND NC
Pin19 ==> GND NC <== Pin20
Reset Signal Settings
After Reset, delay 0 ms before contacting target and enter programming mode.
Drive RESET signal LOW before and after SAP operations.
Pinout is for 1.27mm (mini) spacing 10-Pin (first 10 pins) and 20-Pin debug header.
Please refer to user manual for 2.54mm spacing 20-pin debug header.
A JTAG/SWD ADAPTER (Install jumper on SWD) should be used.
Image Description: BUBBLE_TEST
FX Special Features
Image Restrictions : Limit Image Usage between dates : 12-17-2016 to 12-18-2017
Number of programs allowed: 0
Number of failures allowed: 0
Store Image to Cyclone
Store Image to Disk