RTC Module with internal clock source

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Requirement Description :

The PCB size is limated of some kind of application , so external crystal can't be used . For example , space restricted on magnetic head of smart car reader . The PCB size smaller than 10x10mm . The RTC function is required , but external crystal can't be used . However , Freescale Kinetis RTC not support internal reference clock (IRC) .

Below image copy from K65 datasheet .

The time counter within the RTC is clocked by a 32.768 kHz clock and can supply this clock to other peripherals. The 32.768 kHz clock can only be sourced from an external crystal using the oscillator that is part of the RTC module.

Table 6-2. Module clocks (continued)

Module	Bus interface clock	Internal clocks	I/O interface clocks
RNGA	Bus clock	—	—
Analog			
ADC	Bus clock	OSCERCLK	—
CMP	Bus clock	—	—
VREF	Flash clock	—	—
Timers			
TPM	Bus clock	TPM clock	TPM_CLKIN0, TPM_CLKIN1
PDB	Bus clock	—	—
FlexTimers	Bus clock	MCGFFCLK	FTM_CLKINx
PIT	Bus clock	—	—
LPTMR	Flash clock	LPO,OSCERCLK_UNDIV, MCGIRCLK, ERCLK32K	—
CMT	Bus clock	—	—
RTC	Flash clock	EXTAL32	—

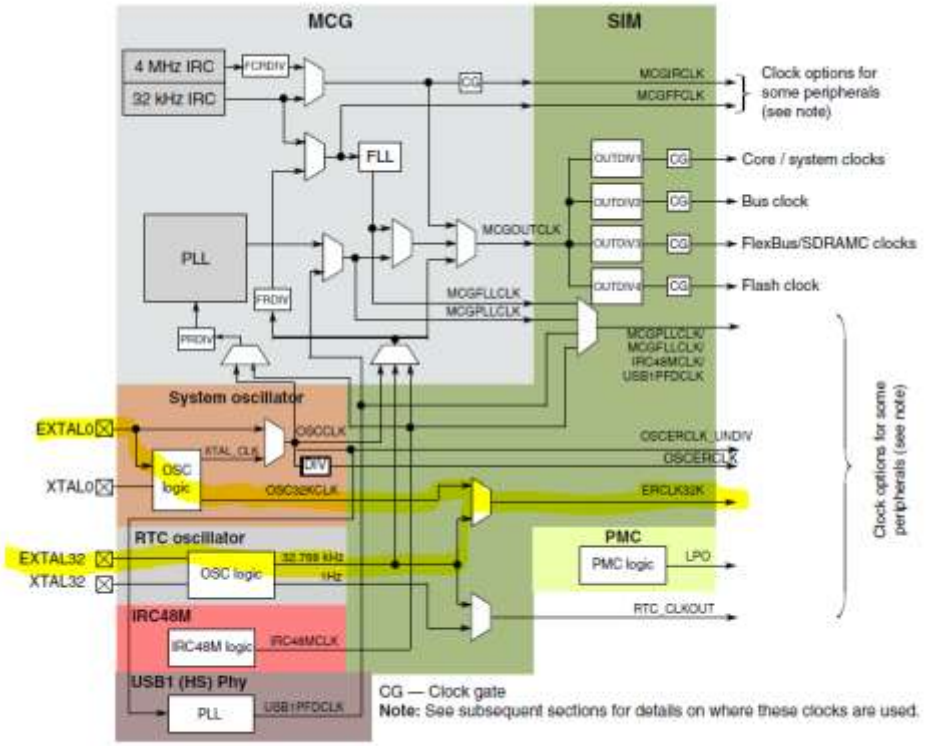


Figure 6-1. Clocking diagram

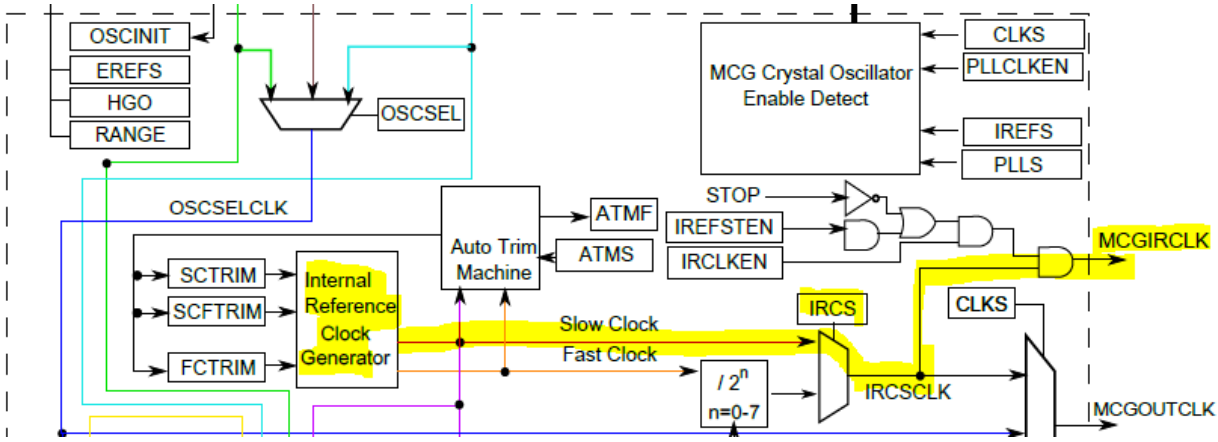
Solution description :

1. *Internal Clock Source:*

a. There is a MCG output clock MCGIRCLK can be configured as slow speed internal reference clock (32.768KHz) . Another word , internal reference clock 32.768KHz can be selected as MCGIRCLK clock source .

i. MCG_C2[IRCS] = 0 //slow internal reference clock selected
ii. MCG_C1[IRCLKEN] = 1 // MCGIRCLK active
iii. MCG_C1[IREFSTEN] = 1 //IRC enabled in STOP mode

- MCG Internal Reference Clock (MCGIRCLK) is provided as a clock source for other on-chip peripherals



27.5.3.1 MCG Internal Reference Clock

The MCG Internal Reference Clock (MCGIRCLK) provides a clock source for other on-chip peripherals and is enabled when C1[IRCLKEN]=1. When enabled, MCGIRCLK is driven by either the fast internal reference clock (4 MHz IRC which can be divided down by the FRDIV factors) or the slow internal reference clock (32 kHz IRC). The IRCS

Clock name	High Speed Run mode clock frequency	Run mode clock frequency	VLPR mode clock frequency	Clock source	Clock is disabled when...
Internal reference (MCGIRCLK)	30-40 kHz or 4 MHz	30-40 kHz or 4 MHz	4 MHz only	MCG	MCG_C1[IRCLKEN] cleared, Stop or VLPS mode and MCG_C1[IREFSTEN] cleared, or LLS/VLLS mode

MCG_C2 field descriptions (continued)

Field	Description
1 LP	Low Power Select Controls whether the FLL or PLL is disabled in BLPI and BLPE modes. In FBE or PBE modes, setting this bit to 1 will transition the MCG into BLPE mode; in FBI mode, setting this bit to 1 will transition the MCG into BLPI mode. In any other MCG mode, LP bit has no affect. 0 FLL or PLL is not disabled in bypass modes. 1 FLL or PLL is disabled in bypass modes (lower power)
0 IRCS	Internal Reference Clock Select Selects between the fast or slow internal reference clock source. 0 Slow internal reference clock selected. 1 Fast internal reference clock selected.

MCG_C1 field descriptions

Field	Description
1 IRCLKEN	Internal Reference Clock Enable Enables the internal reference clock for use as MCGIRCLK. 0 MCGIRCLK inactive. 1 MCGIRCLK active.

MCG_C1 field descriptions (continued)

Field	Description
0 IREFSTEN	Internal Reference Stop Enable Controls whether or not the internal reference clock remains enabled when the MCG enters Stop mode.
	0 Internal reference clock is disabled in Stop mode. 1 Internal reference clock is enabled in Stop mode if IRCLKEN is set or if MCG is in FEI, FBI, or BLPI modes before entering Stop mode.

2. Clock output pin :

a. There is a CLKOUT pin on Kinetis and its clock source can be configured from MCGIRCLK .

i. SIM_SCGC5[PORTx] = 1 // enable PORTx clock gate

ii. PORTx_PCRn[MUX] = b101 // configure pin muxing slot as alternative 5 as CKLOUT

iii. SIM_-SOPT2[CLKOUTSEL] = b100 // MCGIRCLK output on CLKOUT pin

SIM_SOPT2 field descriptions (continued)

Field	Description
	0 MCGOUTCLK, divided by the TRACECLK fractional divider as configured by SIM_CLKDIV4[TRACEFRAC, TRACEDIV] 1 Core/system clock
11 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
10 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
9–8 FBSL	FlexBus security level If flash security is enabled, then this field affects what CPU operations can access off-chip via the FlexBus or SDRAMinterface. This field has no effect if flash security is not enabled. 00 All off-chip accesses (instruction and data) via the FlexBus or SDRAM are disallowed. 01 All off-chip accesses (instruction and data) via the FlexBus or SDRAM are disallowed. 10 Off-chip instruction accesses are disallowed. Data accesses are allowed. 11 Off-chip instruction accesses and data accesses are allowed.
7–5 CLKOUTSEL	CLKOUT select Selects the clock to output on the CLKOUT pin. 000 FlexBus CLKOUT 001 Reserved 010 Flash clock 011 LPO clock (1 kHz) 100 MCGIRCLK 101 RTC 32.768kHz clock 110 OSCERCLK0 111 IRC 48 MHz clock

SIM_SCGC5 field descriptions

Field	Description
13 PORTE	Port E Clock Gate Control This bit controls the clock gate to the Port E module. 0 Clock disabled 1 Clock enabled
12 PORTD	Port D Clock Gate Control This bit controls the clock gate to the Port D module. 0 Clock disabled 1 Clock enabled
11 PORTC	Port C Clock Gate Control This bit controls the clock gate to the Port C module.

Pinout

169 WLCSP	169 MAPBGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
N5	M10	PTA6	DISABLED		PTA6		FTM0_CH3		CLKOUT		TRACE_CLKOUT	
B1	A12	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK		

3. *Reference Source code :*

```
    /*Enable I/O port clock gate */
SIM_HAL_EnableClock(SIM,kSimClockGatePortC);
    /*Configure I/O as clock output pin */
PORT_HAL_SetMuxMode(PORTC,3UL,kPortMuxAlt5);
    /*Select MCGIRCLK as CLKOUT pin output source */
CLOCK_HAL_SetClkOutSel(SIM , kClockClkoutSelMcgIrClk);
```

4. *Hardware :*

Connect CLKOUT pin to EXTAL32 for RTC clock source .

Note :

1. The internal 32kHz OSC deviation is around ±2% .

3.3.1 MCG specifications

Table 16. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
I_{ints}	Internal reference (slow clock) current	—	20	—	μA	
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 0.5	± 2	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	1.5	$\%f_{dco}$	1