FUSE MAP

	EVK Pull Down: 0	EVK Pull Down: 0	EVK Pull Down: 0	EVK Pull Down: 0	EVK Switch	EVK Pull Down: 0	EVK Pull Down: 0	EVK Pull Down: 0	EVK Pull Down: 0	EVK Switch
	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
TYPE	**BOOT_CFG[9]**	**BOOT_CFG[8]**	**BOOT_CFG[7]**	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
FlexSPI1 - Serial NOR	*HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms*		*0*	*0*	*0*	*0*	*FLASH_TYPE: 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR 101 - Micron Octal DDR 111 - QSPI device supports 3B read by default (on secondary pinmux option) (3B Read Means: QSPI 1 Byte command + 3 Byte Address.)*			*EncryptedXIP 0 - Disabled 1- Enabled*
SD	*SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104*		*0*	*0*	*1*	*Bus Width: 0 - 1-bit 1 - 4-bit*	*SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad*	*SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct*	*Port Select: 0 - eSDHC1 1 - eSDHC2*	*Fast Boot: 0 - Regular 1 - Fast Boot*
FlexSPI1 - Serial NAND	*"CS_INTERVAL: CS de-asserted interval between two commands 0 ~C 100ns 1 ~C 200ns 2 ~C 400ns 3 ~C 50ns"*		*1*	*1*	*BOOT_SEARCH_COUNT: 0 - 1 1 - 2*	*COL_ADDRESS_WIDTH: 0 ~C 12bits 1 ~C 13bits*	*SPI NAND HOLD TIME 00 - 0 us 01 - 500us 10 - 1ms 11 - 3ms*		*BOOT_SEARCH_STRIDE: Search Stride for FCB and DBBT (in terms of pages) 0 - 64 1 - 128 2 - 256 3 - 32*